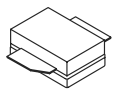
TriQuint SEMICONDUCTOR

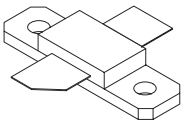
AGR09030E
30 W, 865 MHz—895 MHz, N-Channel E-Mode, Lateral MOSFET

Introduction

The AGR09030E is a high-voltage, gold-metalized, laterally diffused metal oxide semiconductor (LDMOS) RF power transistor suitable for cellular band, code-division multiple access (CDMA), global system for mobile communication (GSM), enhanced data for global evolution (EDGE), and time-division multiple access (TDMA) single and multicarrier class AB wireless base station amplifier applications. This device is manufactured on an advanced LDMOS technology, offering state-of-the-art performance, reliability, and thermal resistance. Packaged in an industry-standard CuW package capable of delivering a minimum output power of 30 W, it is ideally suited for today's RF power amplifier applications.



AGR09030EU (unflanged)



AGR09030EF (flanged)

Figure 1. Available Packages

Features

Typical performance ratings are for IS-95 CDMA, pilot, sync, paging, traffic codes 8—13:
- Output power (P_{OUT}): 7 W.
- Power gain: 21 dB.
- Efficiency: 27%.
- Adjacent channel power ratio (ACPR) for 30 kHz bandwidth (BW):
  (750 kHz offset: –45 dBc)
  (1.98 MHz offset: –60 dBc).
- Input return loss: 10 dB.

High-reliability, gold-metalization process.

High gain, efficiency, and linearity.

Integrated ESD protection.

Si LDMOS.

Industry-standard packages.

30 W minimum output power.

Table 1. Thermal Characteristics

Parameter	Sym	Value	Unit
Thermal Resistance, Junction to Case:			
AGR09030EU	$R_{\theta JC}$	1.85	°C/W
AGR09030EF	$R_{\theta JC}$	2.2	°C/W

Table 2. Absolute Maximum Ratings*

Parameter	Sym	Value	Unit
Drain-source Voltage	V_{DSS}	65	Vdc
Gate-source Voltage	V_{GS}	–0.5, +15	Vdc
Drain Current—Continuous	I_D	4.25	Adc
Total Dissipation at T_C = 25 °C:			
AGR09030EU	P_D	95	W
AGR09030EF	P_D	80	W
Derate Above 25 °C:			
AGR09030EU	—	0.54	W/°C
AGR09030EF	—	0.45	W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	–65, +150	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. ESD Rating*

AGR09030E	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1500	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. PEAK Devices employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

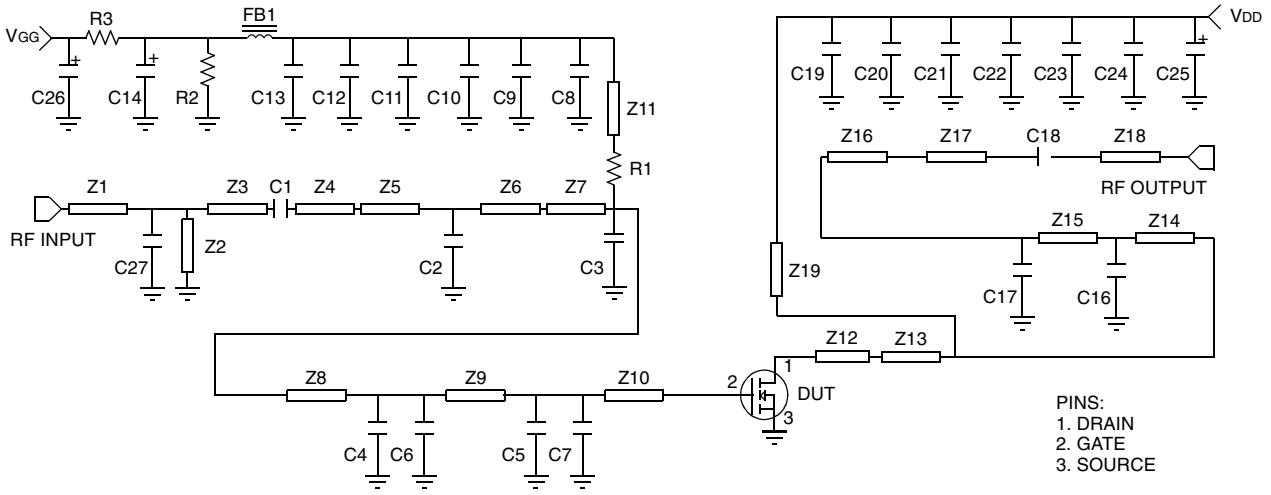
Table 4. dc Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage (V_{GS} = 0, I_D = 150 µA)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current (V_{GS} = 5 V, V_{DS} = 0 V)	I_{GSS}	—	—	0.95	µAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	50	µAdc
On Characteristics					
Forward Transconductance (V_{DS} = 10 V, I_D = 1.0 A)	G_{FS}	—	2.2	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 400 µA)	$V_{GS(TH)}$	—	—	5.0	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_{DQ} = 330 mA)	$V_{GS(Q)}$	—	3.8	—	Vdc
Drain-source On-voltage (V_{GS} = 10 V, I_D = 1.0 A)	$V_{DS(ON)}$	—	0.35	—	Vdc

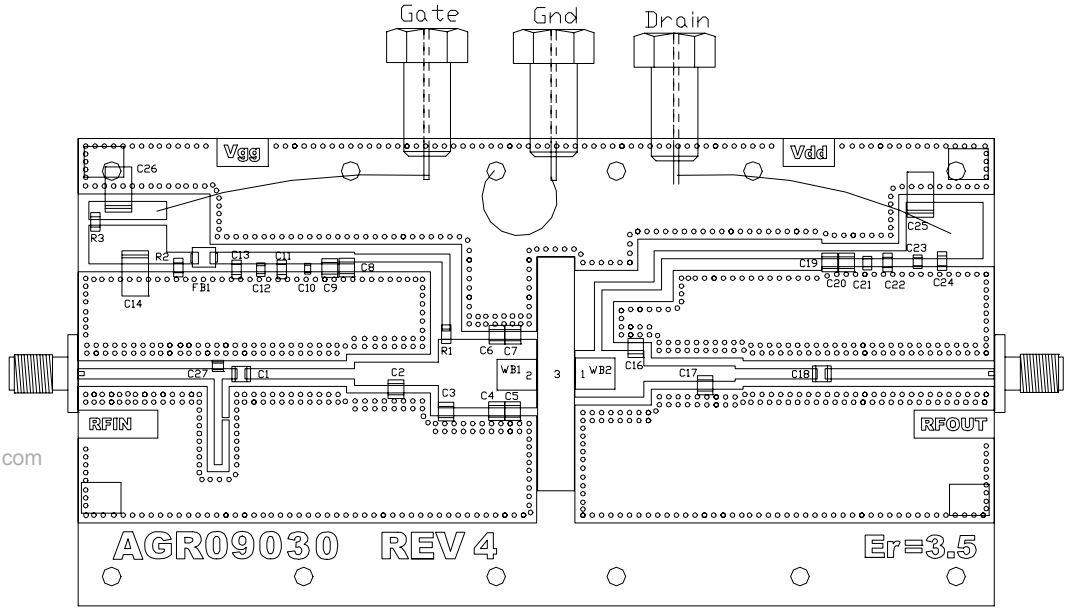
Table 5. RF Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{ISS}	—	56	—	pF
Output Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{OSS}	—	15.7	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{RSS}	—	0.73	—	pF
Functional Tests (in Supplied Test Fixture) (Test frequencies (f) = 865 MHz, 880 MHz, 895 MHz)					
Linear Power Gain (V_{DS} = 28 V, P_{OUT} = 5 W, I_{DQ} = 330 mA)	G_L	19	21	—	dB
Output Power (V_{DS} = 28 V, 1 dB compression, I_{DQ} = 330 mA)	P1dB	30	40	—	W
Drain Efficiency (V_{DS} = 28 V, P_{OUT} = P1dB, I_{DQ} = 330 mA)		—	57	—	%
Third-order Intermodulation Distortion (100 kHz spacing, V_{DS} = 28 V, P_{OUT} = 30 WPEP, I_{DQ} = 330 mA)	IMD	—	–31	—	dBc
Input Return Loss	I_{RL}	—	10	—	dB
Ruggedness (V_{DS} = 28 V, P_{OUT} = 30 W, I_{DQ} = 330 mA, f = 880 MHz, VSWR = 10:1, all angles)	—	No degradation in output power.			

Test Circuit Illustrations for AGR09030E



A. Schematic



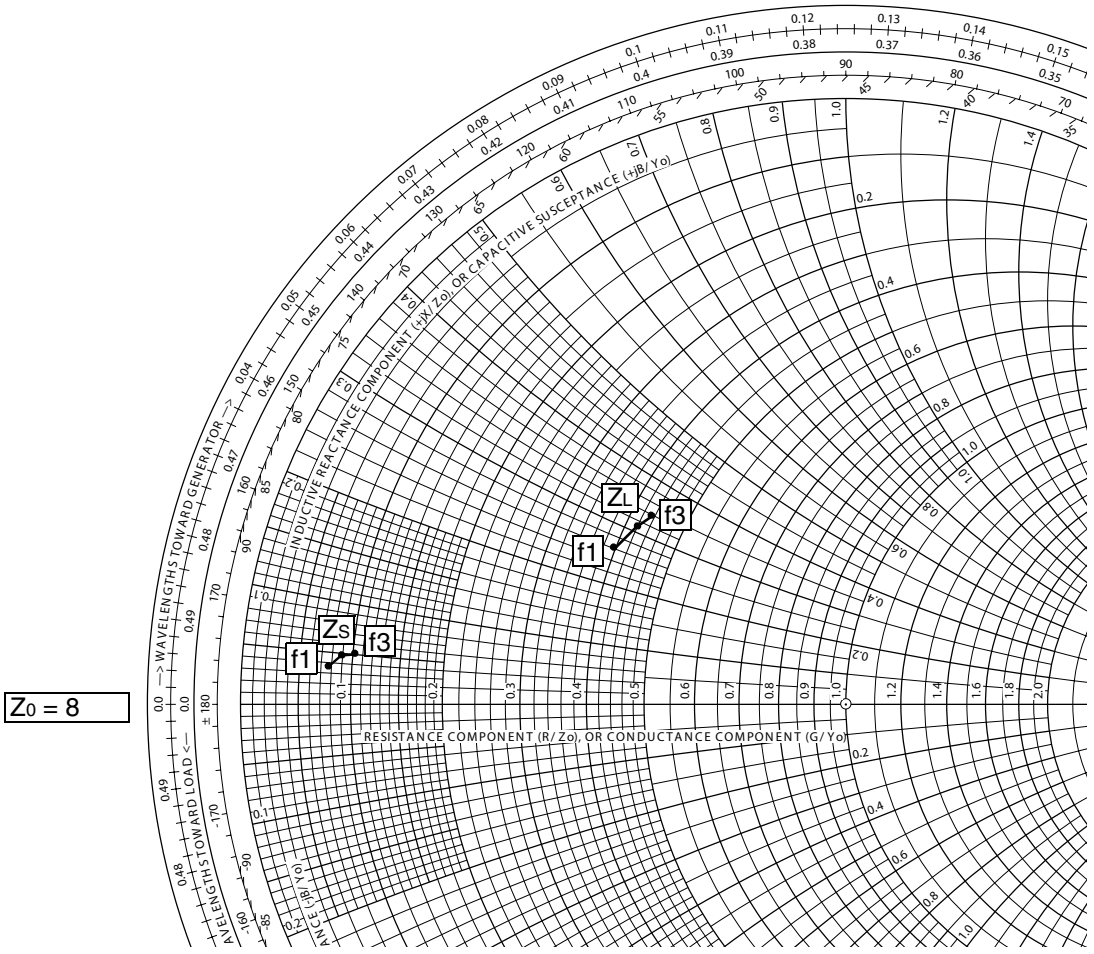
Parts List:

Microstrip line: Z1 0.900 in. x 0.066 in.; Z2 0.294 in. x 0.050 in.; Z3 0.123 in. x 0.066 in.; Z4 0.703 in. x 0.066 in.; Z5 0.267 in. x 0.150 in.; Z6 0.270 in. x 0.150 in.; Z7 0.050 in. x 0.440 in.; Z8 0.324 in. x 0.440 in.; Z9 0.100 in. x 0.440 in.; Z10 0.155 in. x 0.440 in.; Z11 1.024 in. x 0.050 in.; Z12 0.123 in. x 0.300 in.; Z13 0.050 in. x 0.300 in.; Z14 0.213 in. x 0.300 in.; Z15 0.393 in. x 0.100 in.; Z16 0.194 in. x 0.100 in.; Z17 0.523 in. x 0.066 in.; Z18 1.085 in. x 0.066 in.; Z19 2.048 x 0.050.
ATC® chip capacitor: C1, C8, C18, C19: 47 pF, 100B470JW; C27: 8.2 pF, 100A8R2BW; C4, C5, C6, C7: 12 pF, 100B120JW; C3: 1.0 pF, 100B1R0BW; C9, C16, C20: 10 pF, 100B100JW; C2, C17: 8.2 pF, 100B8R2BW.
Murata® chip capacitor: C12, C23: 0.01 µF GRM40X7R103K100AL.
0603 chip capacitor: C10, C21: 220 pF.
Sprague® tantalum chip capacitor: C14, C25, C26: 22 µF, 35 V.
Kreger® ferrite bead: FB1: 2743D19447.
Kemet® chip capacitor: C13, C24: 0.10 µF C1206C104KRAC7800.
Vitramon® chip capacitor: C11, C22: 2200 pF, VJ1206Y222KXA.
1206 size 0.25 W, fixed film, chip resistors: R1: 51 , RM73B2B510J; R2: 47 k , RM73B2B473J; R3: 1 k , RM73B2B102J.
Taconic® ORCER RF-35: board material, 1 oz. copper, 30 mil thickness, r = 3.5.

B. Component Layout

Figure 2. AGR09030E Test Circuit

Typical Performance Characteristics



MHz (f)	ZS (Complex Source Impedance)	ZL (Complex Optimum Load Impedance)
865 (f1)	0.618 + j0.290	3.26 + j2.10
880 (f2)	0.711 + j0.364	3.39 + j2.47
895 (f3)	0.788 + j0.380	3.55 + j2.83

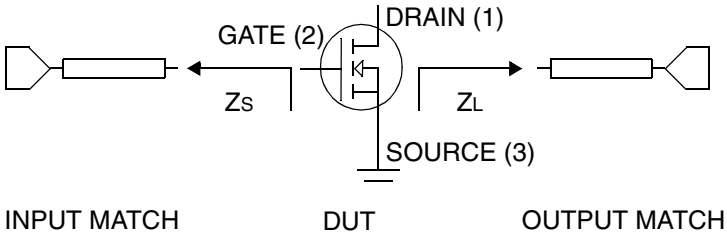
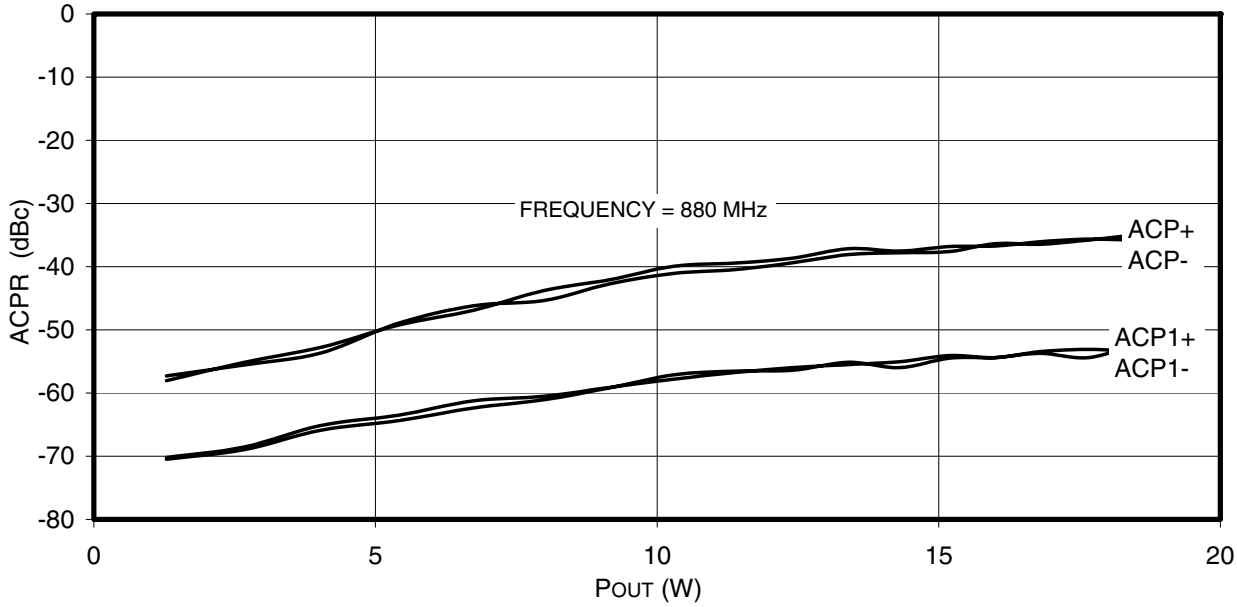


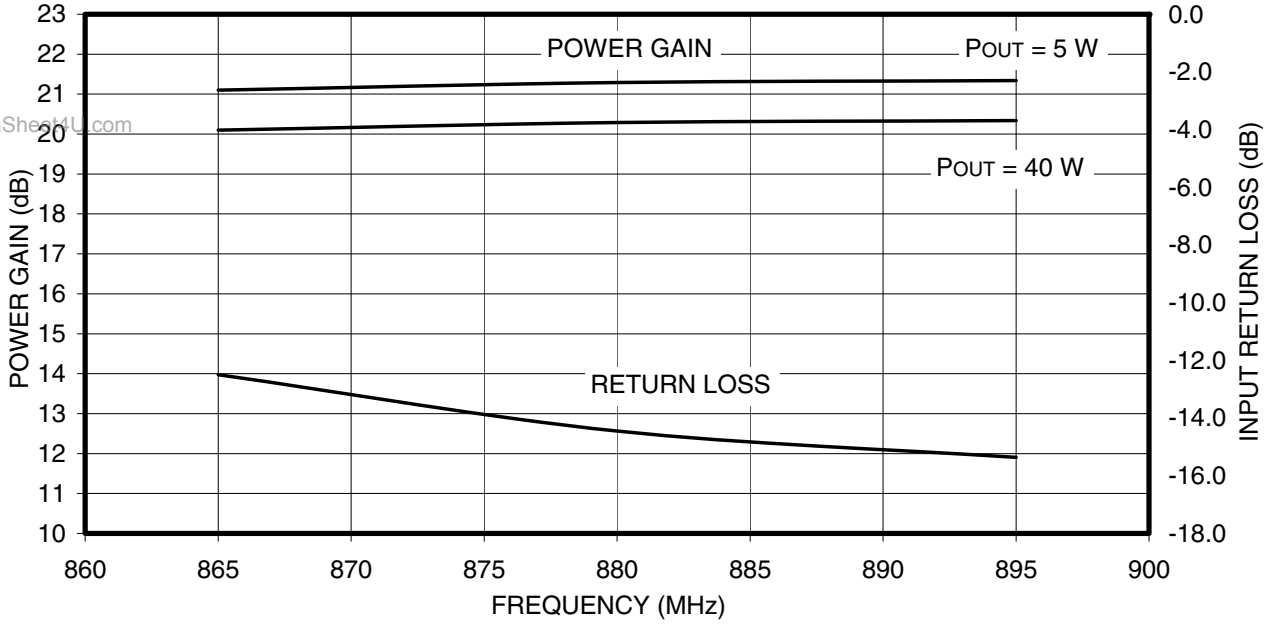
Figure 3. Series Equivalent Input and Output Impedances

Typical Performance Characteristics (continued)



TEST CONDITIONS:
V_{DD} = 28 Vdc, I_{DQ} = 0.33 A, T_C = 30 °C.
IS-95 CDMA PILOT, PAGING, SYNC, TRAFFIC CODES 8—13. OFFSET 1 = 750 kHz, 30 kHz BW. OFFSET 2 = 1.98 MHz, 30 kHz BW.

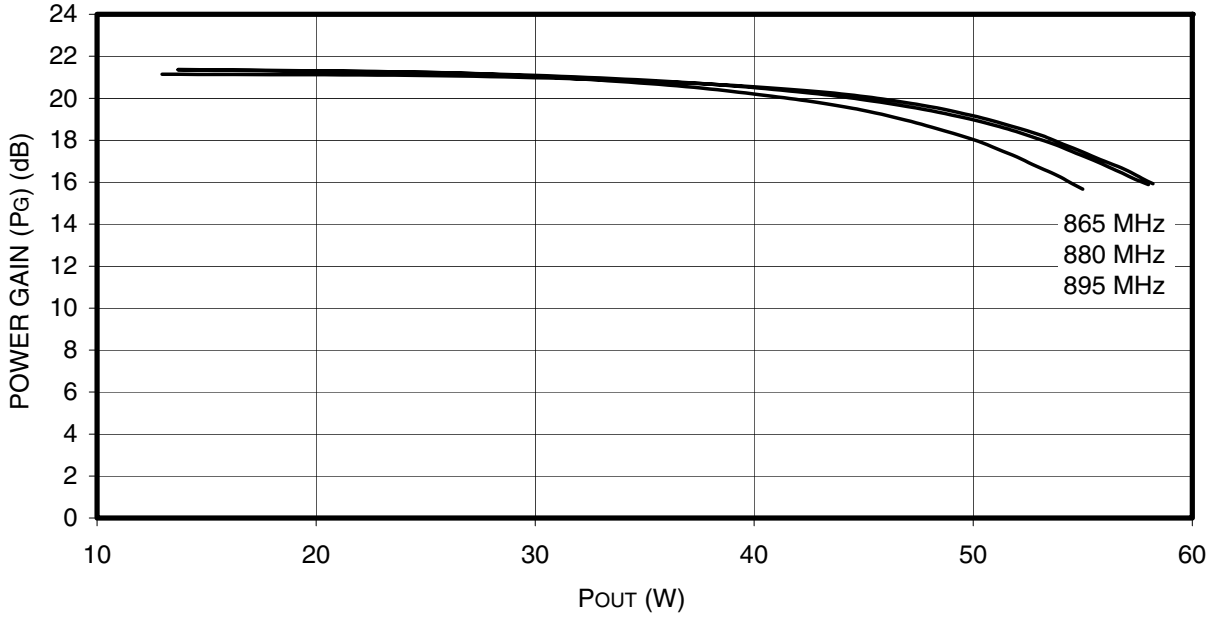
Figure 4. ACPR vs. POUT



TEST CONDITIONS:
V_{DD} = 28 Vdc, I_{DQ} = 0.33 A, T_C = 30 °C, WAVEFORM = CW.

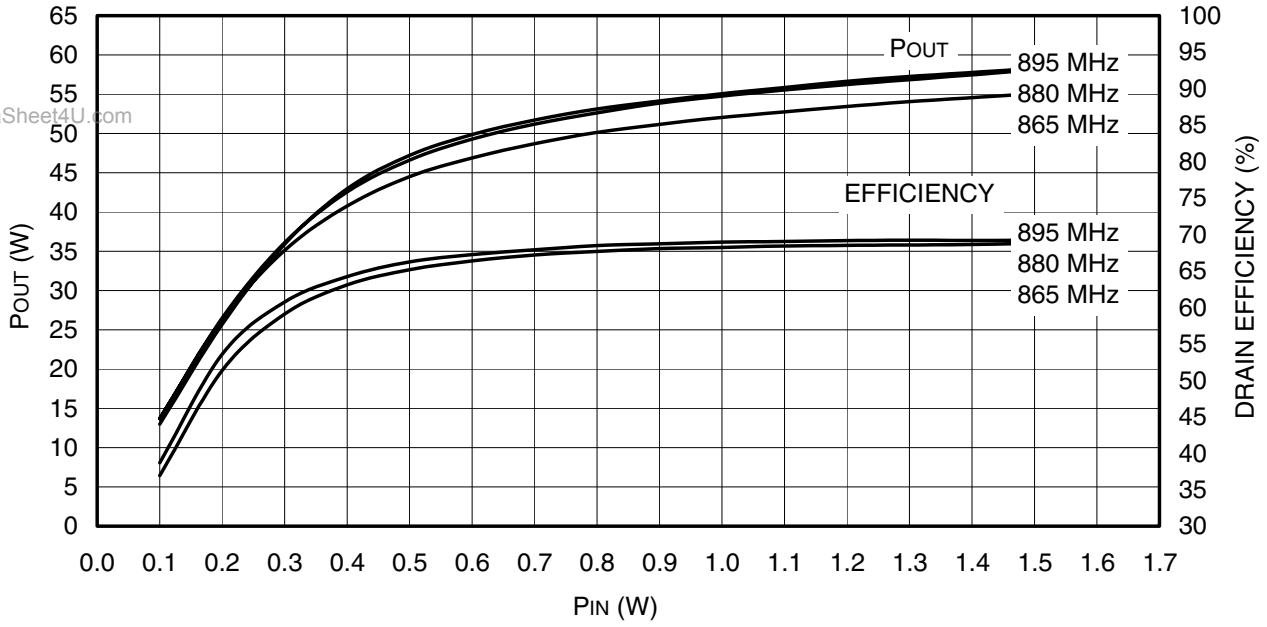
Figure 5. Power Gain and Return Loss vs. Frequency

Typical Performance Characteristics (continued)



TEST CONDITIONS:
V_{DD} = 28 Vdc, I_{DQ} = 0.33 A, T_C = 30 °C, WAVEFORM = CW.

Figure 6. Power Gain vs. Power Out



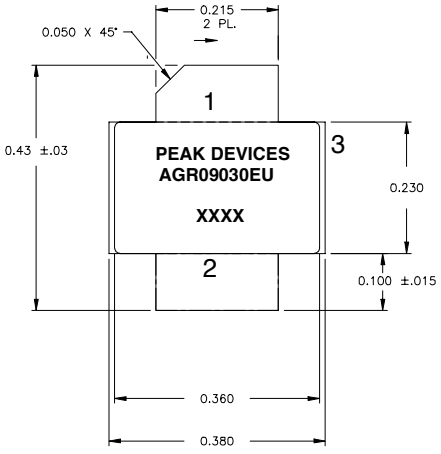
TEST CONDITIONS:
V_{DD} = 28 Vdc, I_{DQ} = 0.33 A, T_C = 30 °C, WAVEFORM = CW.

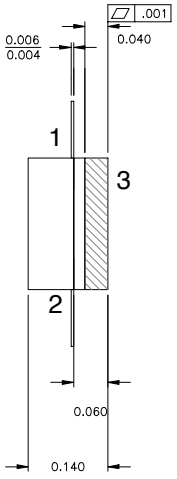
Figure 7. Power Out and Drain Efficiency vs. Input Power

Package Dimensions

All dimensions are in inches. Tolerances are ±0.005 in. unless specified.

AGR09030EU





PINS:
1. DRAIN
2. GATE
3. SOURCE

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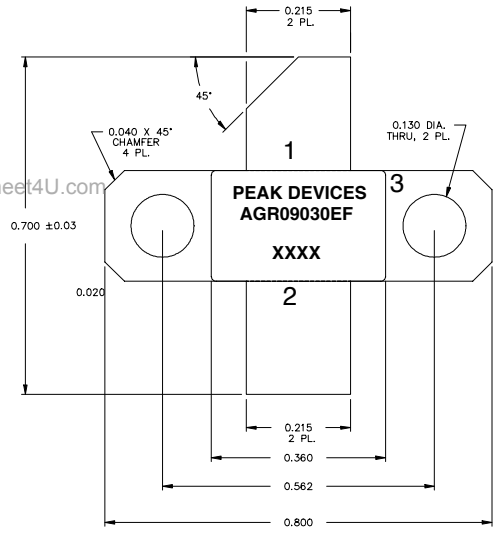

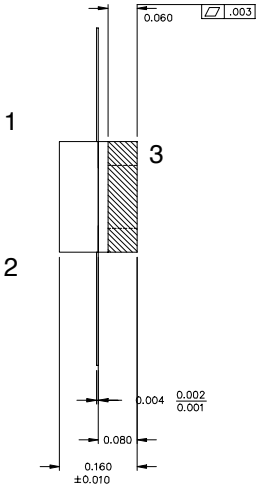

PINS:
1. DRAIN
2. GATE
3. SOURCE

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