AZ DISPLAYS,INC.

COMPLETE LCD SOLUTIONS

SPECIFICATIONS FOR LIQUID CRYSTAL DISPLAY

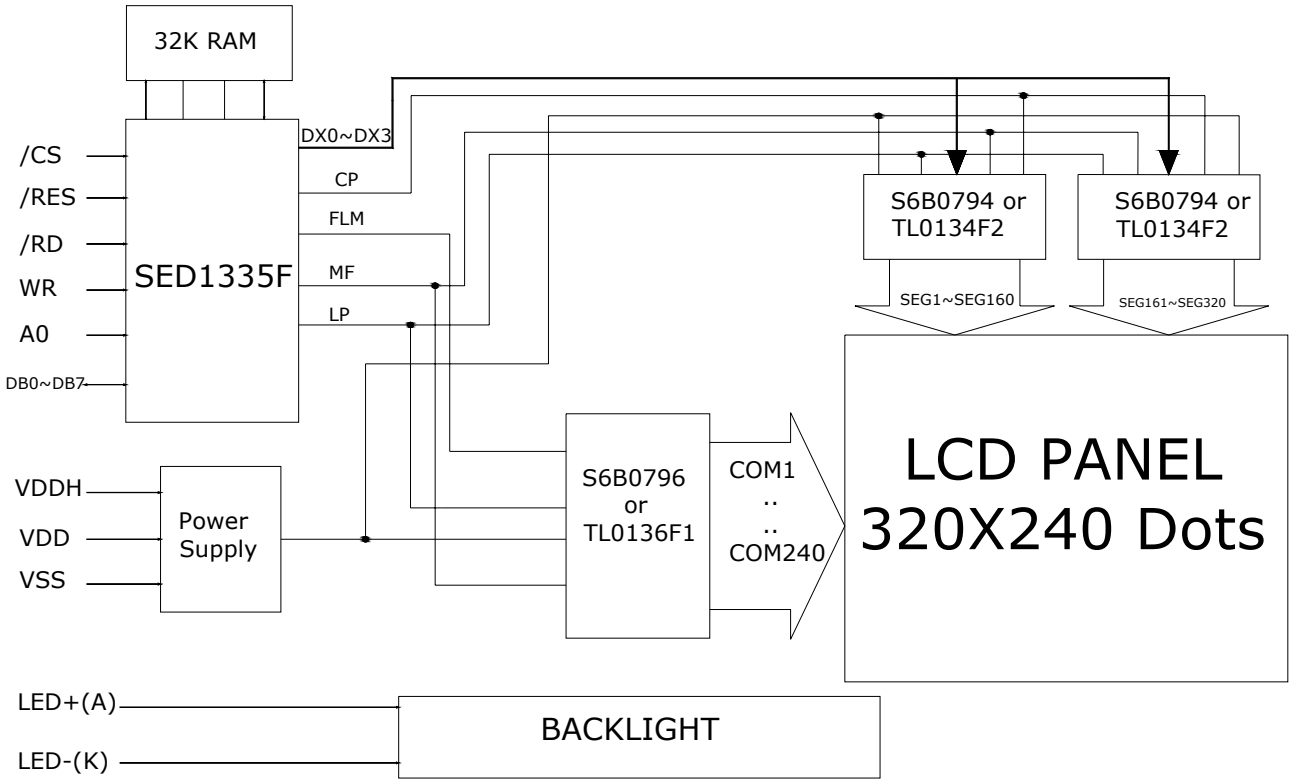
PART NUMBER: □□ □ □ AGM3224O Series

DATE:□ □ □ □ □ □ APRIL 06, 2007

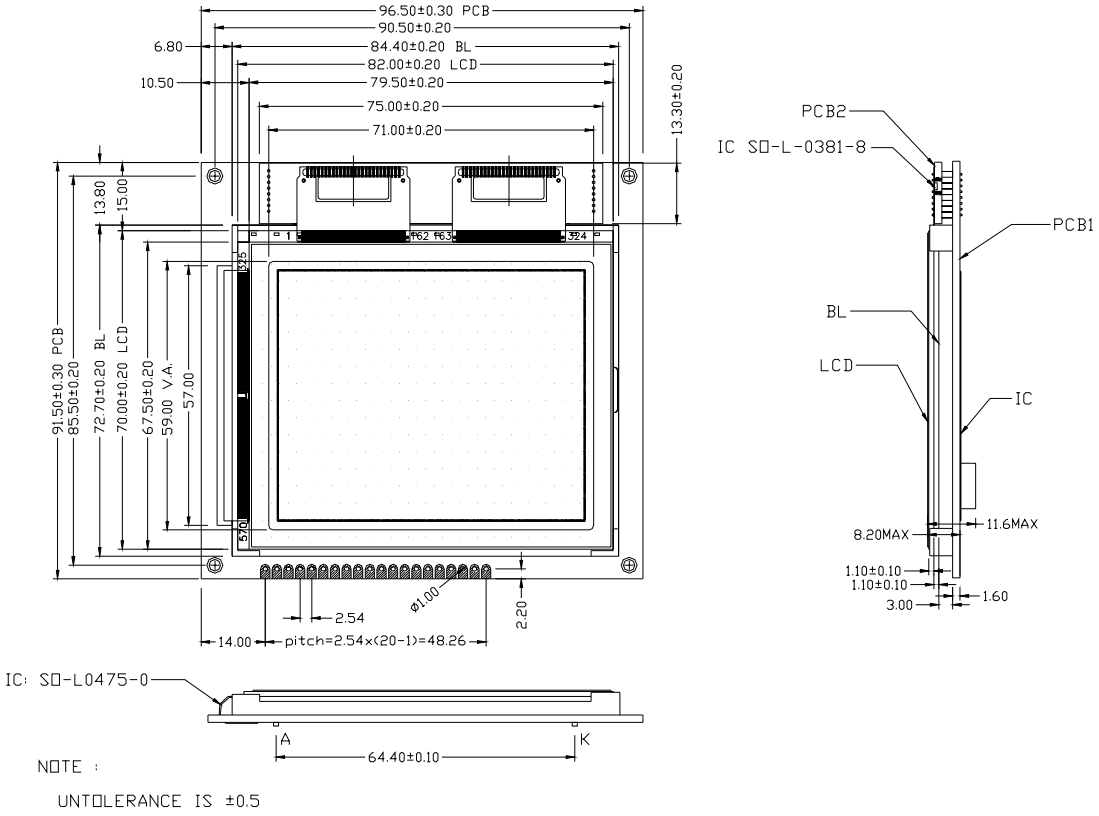
1. FUNCTIONS & FEATURES

Viewing Direction	: 6 O'clock
Driving Scheme	: 1/240 Duty Cycle, 1/17 Bias
Display Content	: 320*240 Dots
Power Supply Voltage	: +5.0V
LCD Driving Voltage ($V_{LCD}=V_{DD}-V_0$)	: 22.0V
Dot Size	: 0.20(W)*0.22(H)mm
Dot Gap	: 0.01mm

2. BLOCK DIAGRAM



3. EXTERNAL DIMENSIONS



NOTE :

UNTOLERANCE IS ±0.5

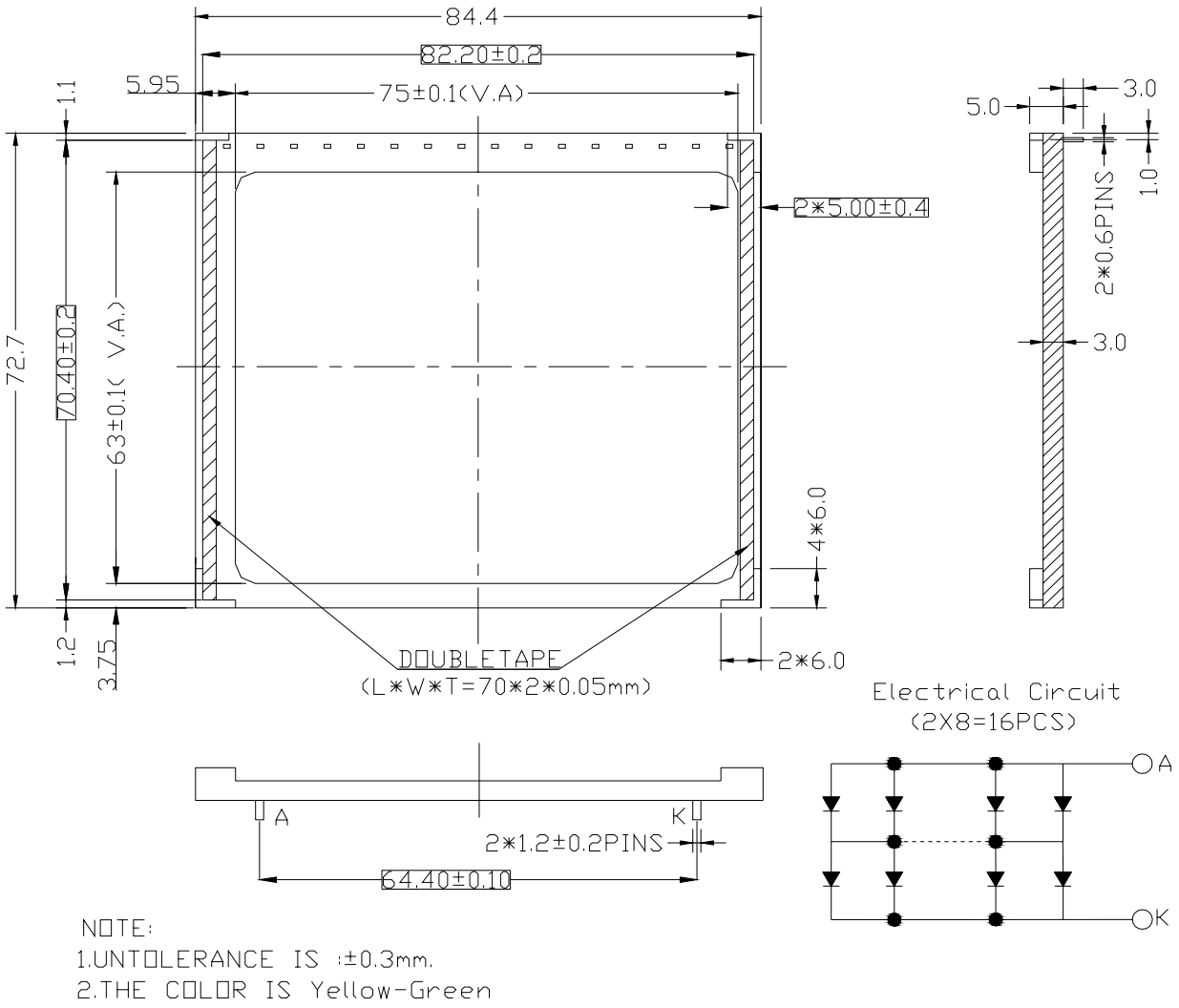
4. PIN ASSIGNMENT

Pin No.	Symbol	Function
1	VSS	Groundterminal of module
2	VDD	Power terminal of module 2.7V to 5.5V (TYP: 5.0V)
3	VDDH	Contrastvoltage for LCD d rive (variable)
4 NC		No used
5	/WR	8080family: Write signal; 6800 family: R/W signal
6	/RD	8080 family: Read signal; 6800 family: Enable clock (E)
7 /CS		Chip select
8	A0	Data type select
9	/RES	Reset
10~17 D	B0~DB7	Data bus
18 N	C	No used
19	LED-(K)	Cathodefor backlight
20	LED +(A)	Anodefor backlight

5. BACKLIGHT

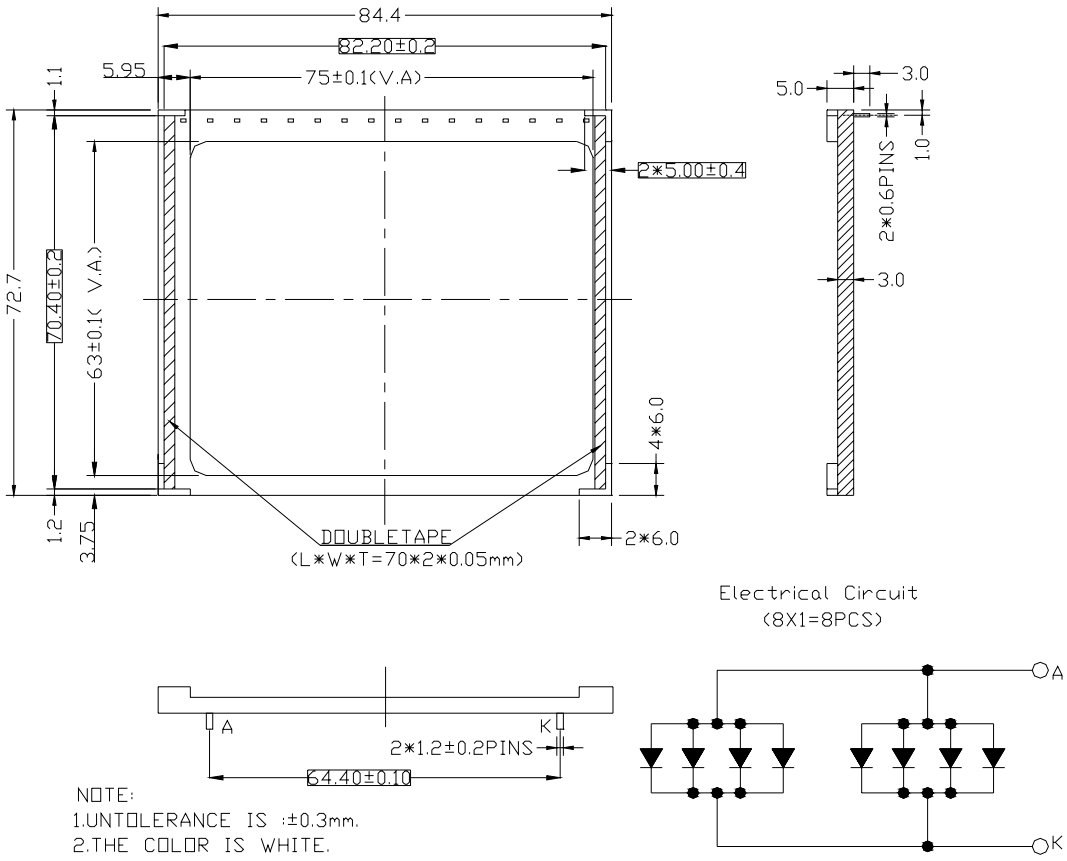
1. Electrical/Optical Sp ecifica tions & Package Dimensions :

Item	Symbol	MIN.	TYP .	MAX .	Unit	Conditions
Forward Voltage	Vf	---	4.1	---	V	
Forward Current	If ---		---	100	mA	Vf=4.1V
Power Dissipation	Pd	---	---	0.41	W	Vf=4.1V
Reverse Voltage	VR	---	10	---	V	
Reverse Current	IR	---	0.20	---	mA	
LuminousIntensity	Iv	---	20	---	Cd/m^2	Vf=4 .1V
Lu minous Uniformity	70		---	---	%	Vf=4.1V
Emission Wavelength	p ---		572	---	nm	If=10mA Ta=25℃
Spectral R ange	---		---	---	nm	Each chip



2. Electrical/Optical Sp ecifica tions & Package Dimensions :

Item	Symbol	MIN.	TYP .	MAX .	Unit	Conditions
Forward Voltage	Vf	---	4.0	---	V	
Forward Current	If ---		120	160	mA	Vf=4.0V
Power Dissipation	Pd	---	0.48	---	W	Vf=4.0V
Reverse Voltage	VR	---	5.0	---	V	
Reverse Current	IR	---	0.8	---	mA	
LuminousIntensity	Iv	---	40	---	Cd/m^2	Vf=4 .0V
LuminousUniformity		---	75	---	%	Vf=4.0V
Emission Wavelength	p X	=0.24	WHITE	X=0.28	nm	If=10mA Ta=25℃
Spectral R ange	---	Y=0 .24	---	Y=0 .30 ---	nm	Each chip



MBG24001B 02, BACKLIGHT COLOR: WHITE

6. MAXIMUM ABSOLUTE LIMIT

Item	Symbol	Standard value	Unit
Supply voltage range	V_{DD}	-0.3~+7.0	V
Input voltage range	V_{IN}	-0.3~V_{DD}+0.3	V
Power supply for liquid crystal drive	V_{DDH}	-0.3~+28	V
Voltage for BL	V_{LED1}	4~4.5	V
Operating temperature range	T_{opr}	0~+50	℃
Soldering temperature range	Tstg	-10~+60	℃

7. ELECTRICAL CHARACTERISTICS

VDD = 4 .5 to 5.5V, VSS = 0V , Ta = -10 to 60℃ unless otherwise noted.

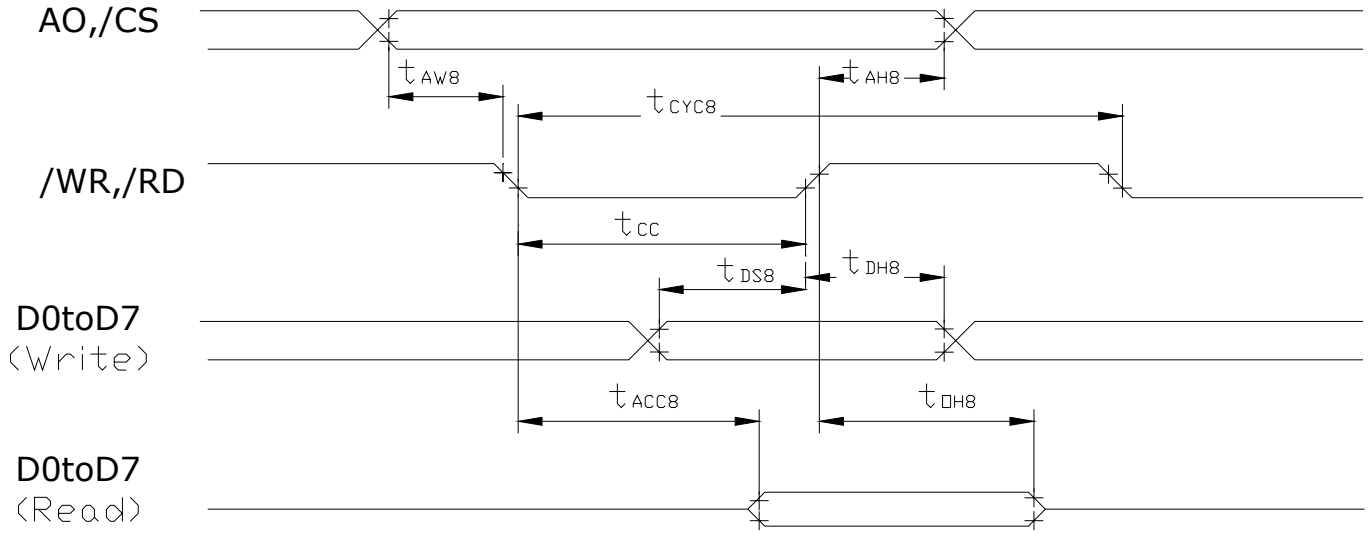
Parameter	Symbol	Condition	Ra ting			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Register data retention voltage	V_{OH}		2.0	---	6.0	V
Input leakage current	I_{LI}	Vl=VDD. See note 5.	---	0.05	2.0	uA
Output leakage current	I_{LO}	Vl=VSS. See note5.	---	0.10	5.0	uA
Operating supply current	Iopr	See note 4.	---	11	15	Ma
Quiescent supply current	I_Q	Sleep m ode, Vosc1=V/CS=V/RD=VDD	---	0.05	20.0	uA
Oscilla tor frequency	f_{OSC}	1.0 Measured at crystal, 47.5%		---	10.0	MHZ
External clock frequency	f_{C1}	1.0 duty cycle. See note		---	10.0	MHZ
Oscilla tor feedback resistance	Rf	6.	0.5	1.0	3.0	M Ω
TTL						
HIGH-level input voltage	V_{IHT}	See note1.	0.5V_{DD}	—	V_{DD}	V
LOW -level input voltage	V_{ILT}	See note1.	Vss	—	0.2V_{DD}	V
HIGH-level output voltage	V_{OHT}	I_{OH}=-5.0 mA. See note 1.	2.4	—	—	V
LO W-level output voltage	V_{OLT}	I_{OL}=5.0 mA. See note1.	—	—	Vss+0.4	V
CMOS						
HIGH-level input voltage	V_{IHC}	See note2.	0.8V_{DD}	—	V_{DD}	V
LOW -level input voltage	V_{ILC}	See note2.	Vss	—	0.2V_{DD}	V
HIGH-level output voltage	V_{OHC}	I_{OH}=-2.0 mA. See note 2.	V_{DD}-0.4	—	—	V
LO W-level output voltage	V_{OLC}	I_{OH}=1.6 mA. See note2.	—	—	V_{ss}+0.4	V
Open-drain						
LO W-level output voltage	V_{OLN}	IOL=6.0 mA	---	---	Vss+0.4	V
Schmitt-trigger						
Ri sing-edge threshold voltage	V_{T+}	See note3.	0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V
Fal ling-edge threshold voltage	V_{T-}	See note3.	0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V

Notes: 1. D0 to D 7, A0, /CS, /RD, /WR are TTL-level inputs.

2. SEL is CO MS-lev el inputs. YD, XD0 to XD3 , XSCL , LP , WF , YDIS are COMS-leve l output.
3. RES is a Sc hmitt-trigger input. The pulse width on RE S must be at least 200 us. Note that pulses of more than a few seconds will cause DC v oltages to be applied to the LCD panel.
4. Fosc=10MHz , no load (no display memory), internal character generator, 256 x 200 pixel display. Th e operating supply current can be reduced by approximately 1 mA by setting both CL O and the display OFF .
5. V D0 to V D7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance, the input state immediately prior to that is held. Bec ause of the feedback circuit, i nput current flow occurs when the inputs are in an intermediate state.
6. B ecause the oscill ator circuit input bias current is in the order of uA, design the printed so as to reduce leakage currents.

8. SED1335F TIMING DIAGRAMS

8.1. 8080 Family Interface Timing



Ta=-10 to 60℃

Signal	Symbol	Parameter	VDD=4 .5 to 5.5V		VDD=2 .7 to 4.5V		Unit	Conditi on
			min	max	min	max		
A0, CS	t_{AH8}	Address hold time	10	-	10	-	ns	CL=1 00 p_F
	$t_{AW 8}$	Address setup time	0	-	0	-	ns	
WR, RD	t_{CYC8}	System cycle time	See note.	-	See note.	-	ns	
	t_{CC}	Strobe pulsewidth	120	-	150	-	ns	
D0 to D7	t_{DS8}	Data setup time	120	-	120	-	ns	
	t_{DH8}	Data hold time	5	-	5	-	ns	
	t_{OH8}	Output disable time	10	50	10	55	ns	
	t_{ACC8}	RD access time	-	50	-	80	ns	

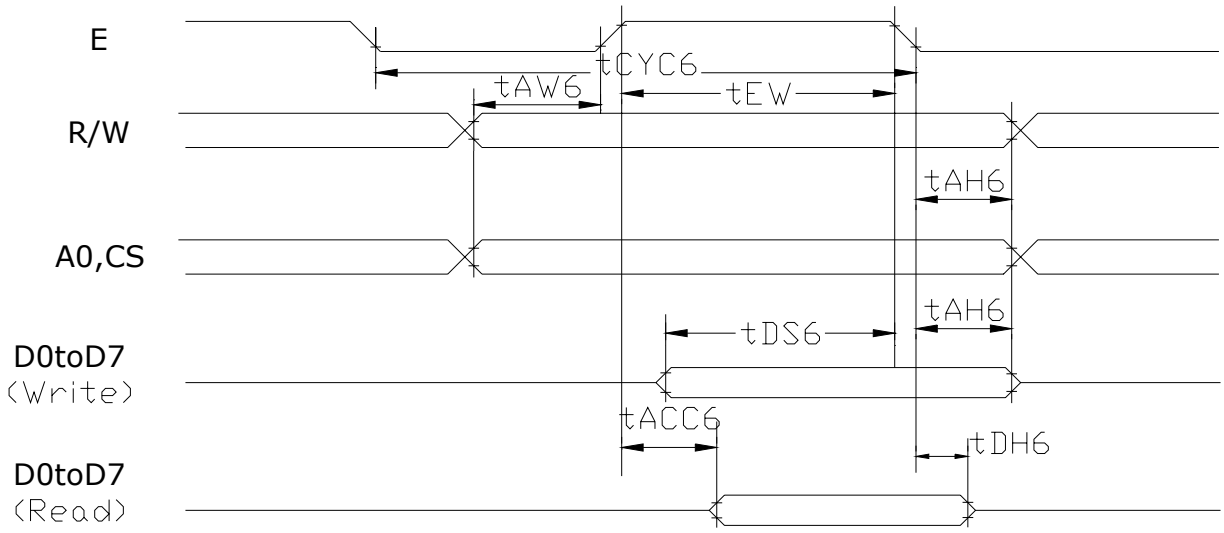
Note: For memory controland system control commands:

$t_{CYC8} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC8} = 4t_C + t_{CC} + 30$

8-2. 6800 Family In terface timing



Note : tCYC 6 indicates the interval during which CS is LOW and E is HIGH .

Ta=-10 to 60℃

Signal	Symbol	Parameter	VDD=4 .5 to 5.5V		VDD=2 .7 to 4.5V		Unit	Conditi on
			min	max	min	max		
E t	t_{EW}	Enable pulsewidth	120	---	150	---	ns	CL=1 00 p_F
A0, CS WR, RD	t_{AH6}	Address hold time	0	-	10	-	ns	
	$t_{AW 6}$	Address setup time	0	-	0	-	ns	
	t_{CYC6}	System cycle time	See note.	-	See note.	-	ns	
D0 to D7	t_{DS6}	Data setup time	120	-	120	-	ns	
	t_{DH6}	Data hold time	5	-	5	-	ns	
	t_{OH6}	Output disable time	10	50	10	55	ns	
	t_{ACC6}	RD access time	-	50	-	80	ns	

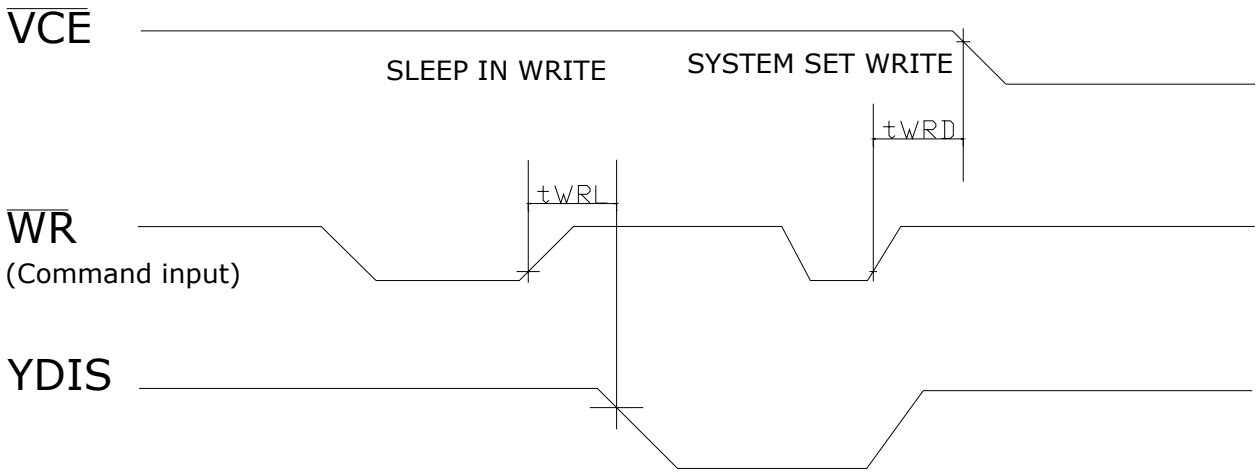
Note: For memory controland system control commands:

$t_{CYC6} = 2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC6} = 4t_C + t_{EW} + 30$

8-3. Sleep in Command Timing



Ta=-10 to 60

Signal	Symbol	Parameter	VDD=4 .5 to 5.5V		VDD=2 .7 to 4.5V		Unit	Conditi on
			min	max	min	max		
/WR	$t_{WR D}$	/VCE fa lling-edge ddelay time	See note 1	---	See note 1	---	ns	CL=1 00 pF
	$t_{WR L}$	YDIS falling-ed ge ddelay time	---	See note 2	---	See note 2	ns	

Notes: 1. Twrd=18tC+tOSS+40 (T oss is the time delay from the sleep state until stable operation)
2. Twrl=36tC* ［TC /R ］* ［L/F ］+70

9. INSTRUCTION SET

9.1. The Command Set

Class	Command	Code Command										Hex	Description Paramet ers	command read	
		/RD	/WR	A0	D7	D6	D5	D4	D3	D2	D1	D0			No. of B ytes	Section
System control	Initia SYSTEM SET	1	0	1	0	1	0	0	0	0	0	0	40	lize device and display	8	
S	LEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Enter standby mode 0		
Display control	DISP ON/OFF	1	0	1	0	1	0	1	1	0	0	D	58, 59	Enable anddisable display and displayflashing	1	
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Set display start address and displayregions	10	
	CSRFOR M	1	0	1	0	1	0	1	1	1	0	1	5D	Set cursor type 2		
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Set start addres s of character generator RAM	2	
	CSRDIR	1	0	1	0	1	0	0	1	1	CD 1	CD 0	4C to 4F	Set direction of cursor movement	0	
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Set horizontal scroll position	1	
	OVLA Y	1	0	1	0	1	0	1	1	0	1	1	5B	Set display overlay format	1	
Drawing control	CSR W	1	0	1	0	1	0	0	0	1	1	0	46	Set cursor address	2	
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Read cursor addres s 2		
Memory control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Write to display memory	--------	
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Read from display memory	--------	

Notes: 1. In general, the internal registers of the SED1335 series are modified as each command parameter is input. However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. Th e internal registers for the parameters thathave been input will have been changed but the remaining parameter registers are unchanged.

2-byte parameter (where two bytes are treated as 1 data item) are handled as follows:

a. CSR W, CSRR: E ach byte is processed individually. The microprocessor may read or write just the low byte of the cursor address.

b. Sy stem Set, Scr oll, CGRAM ADR: Bo th parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is i gnored.

2. APL and APH are 2-byte parameters, but are treated as two 1-byte parameters.