

General Description

The AGM30P05A combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

This device is ideal for load switch and battery protection applications.

Features

- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

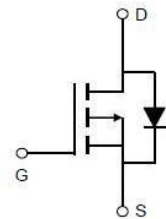
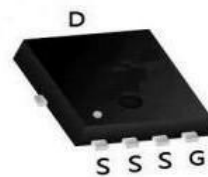
Application

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

Product Summary

BVDSS	RDSON	ID
-30V	5.5mΩ	-75A

PDFN5*6 Pin Configuration



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM30P05A	AGM30P05A	PDFN5*6	330mm	12mm	3000

Table 1. Absolute Maximum Ratings (TC=25°C)

Symbol	Parameter	Value	Unit
VDS	Drain-Source Voltage (VGS=0V)	-30	V
VGS	Gate-Source Voltage (VDS=0V)	±20	V
ID	Drain Current-Continuous(Tc=25°C) (Note 1)	-75	A
	Drain Current-Continuous(Tc=100°C)	-50	A
IDM (pluse)	Drain Current-Continuous@ Current-Pulsed (Note 2)	-240	A
PD	Maximum Power Dissipation(Tc=25°C)	59.5	w
	Maximum Power Dissipation(Tc=100°C)	24	w
EAS	Avalanche energy (Note 3)	93	mJ
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	°C

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
RθJA	Thermal Resistance Junction-ambient (Steady State) ¹	---	--	°C/W
RθJC	Thermal Resistance Junction-Case ¹	---	2.1	°C/W

Table 3. Electrical Characteristics (TJ=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V ID=250μA	-30	--	--	V
IDSS	Zero Gate Voltage Drain Current	VDS=-30V,VGS=0V	--	--	-1.0	μA
IGSS	Gate-Body Leakage Current	VGS=±20V,VDS=0V	--	--	±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS,ID=-250μA	-1.2	-1.6	-2.1	V
gFS	Forward Transconductance	VDS=-10V,ID=-10A	--	20	--	S
RDS(on)	Drain-Source On-State Resistance	VGS=-10V, ID=-15A	--	5.5	7.0	mΩ
		VGS=-4.5V, ID=-20A	--	8.5	11.3	mΩ
Dynamic Characteristics						
Ciss	Input Capacitance	VDS=-30V,F=1MHZ	--	2497	--	pF
Coss	Output Capacitance		--	240	--	pF
Crss	Reverse Transfer Capacitance		--	230	--	pF
Rg	Gate resistance	VGS=0V, VDS=0V,f=1.0MHz	--	--	--	Ω
Switching Times						
td(on)	Turn-on Delay Time	VGS=-10V,VDS=-15V, ID=-30A,RI=3.0Ω	--	14	--	nS
tr	Turn-on Rise Time		--	20	--	nS
td(off)	Turn-Off Delay Time		--	56	--	nS
tf	Turn-Off Fall Time		--	48	--	nS
Qg	Total Gate Charge	VGS=-10V, VDS=-15V, ID=-20A	--	32	--	nC
Qgs	Gate-Source Charge		--	6.6	--	nC
Qgd	Gate-Drain Charge		--	8.0	--	nC
Source-Drain Diode Characteristics						
ISD	Source-Drain Current(Body Diode)		--	--	-75	A
VSD	Forward on Voltage	VGS=0V,IS=-15A	--	--	-1.2	V
trr	Reverse Recovery Time	IF=-15A ,	--	--	--	ns
Qrr	Reverse Recovery Charge	dI/dt=-500A/μs , TJ=25℃	--	--	--	nc

Notes 1.The maximum current rating is package limited.

Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature

Notes 3.EAS condition: TJ=25°C

P- Channel Typical Characteristics

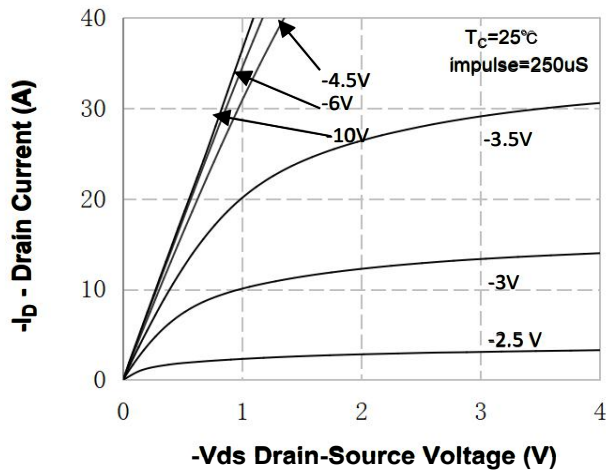


Figure 1. On-Region Characteristics

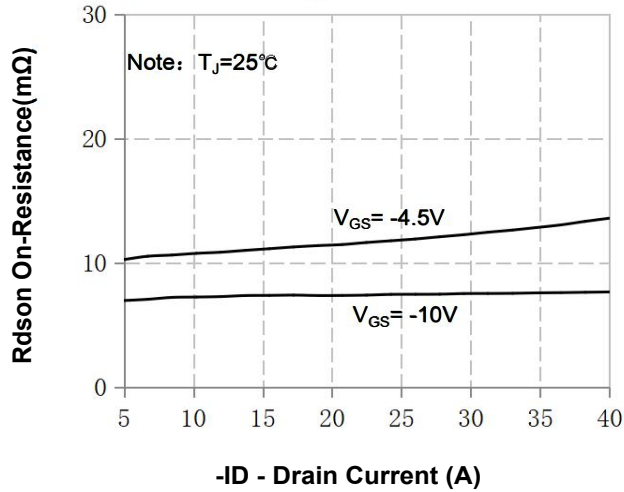


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

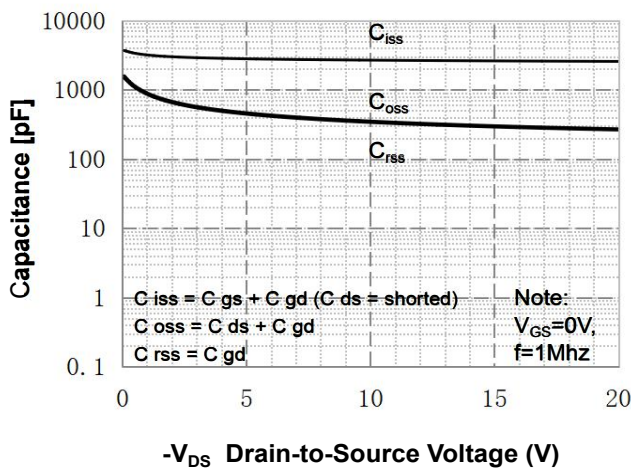


Figure 5. Capacitance Characteristics

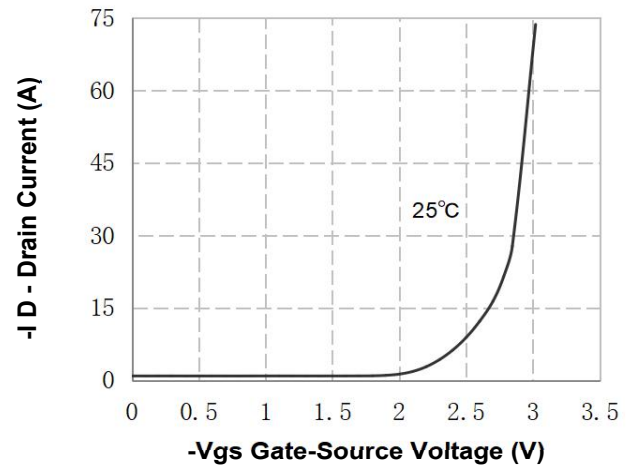


Figure 2. Transfer Characteristics

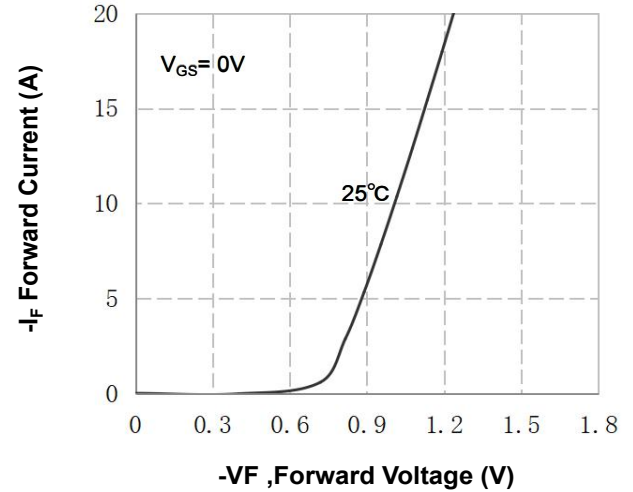


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

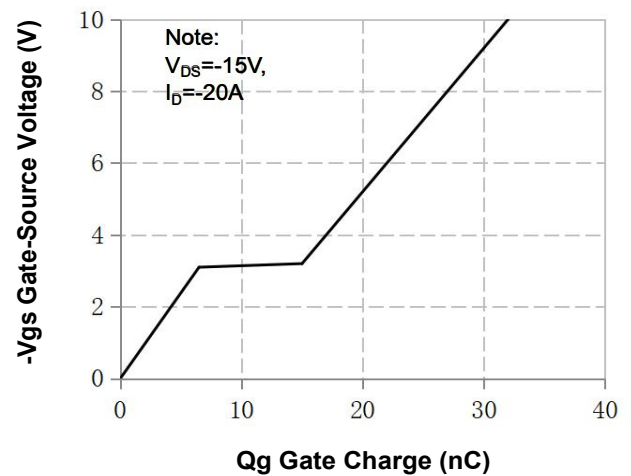


Figure 6. Gate Charge Characteristics

P- Channel Typical Characteristics (Continued)

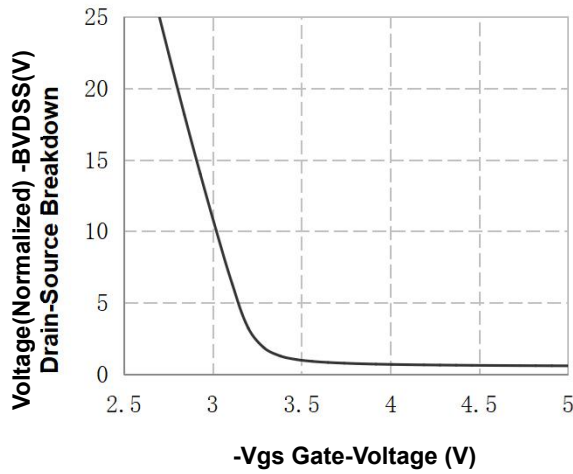


Figure 7. Breakdown Voltage Variation vs Gate-Voltage

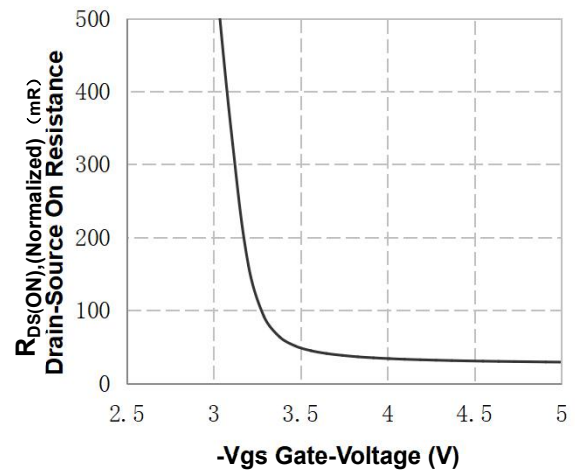


Figure 8. On-Resistance Variation vs Gate Voltage

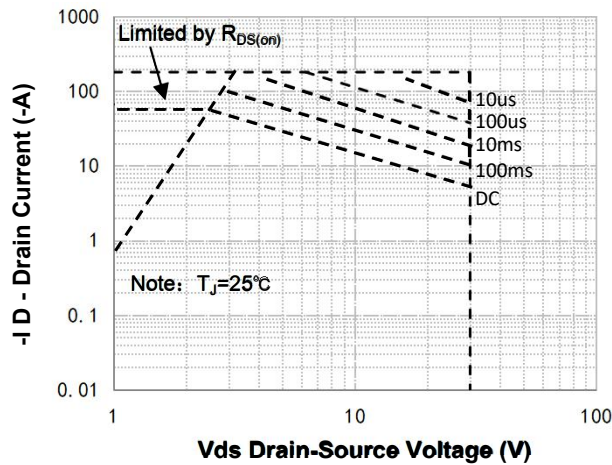


Figure 9. Maximum Safe Operating Area

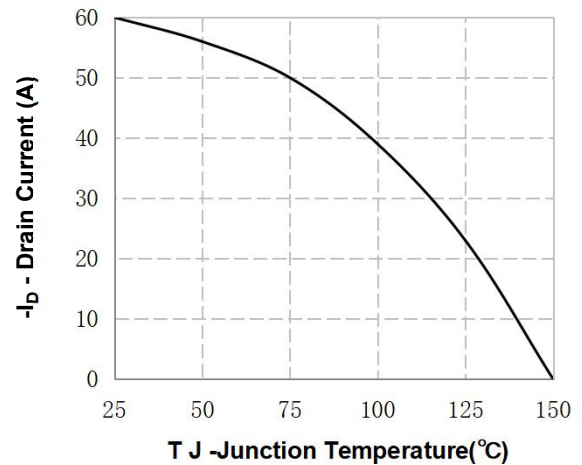


Figure 10. Maximum PContinuous Drain Current vs Case Temperature

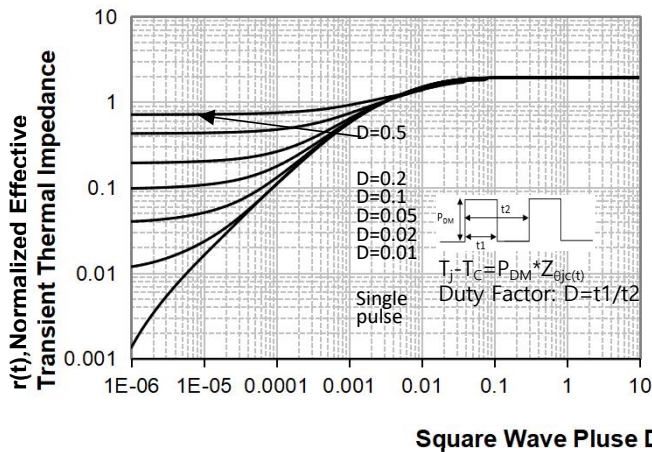
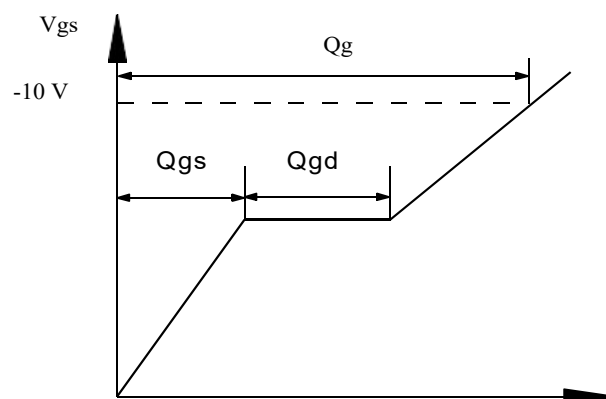
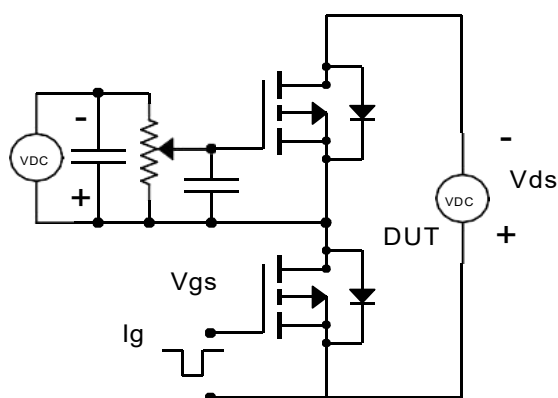
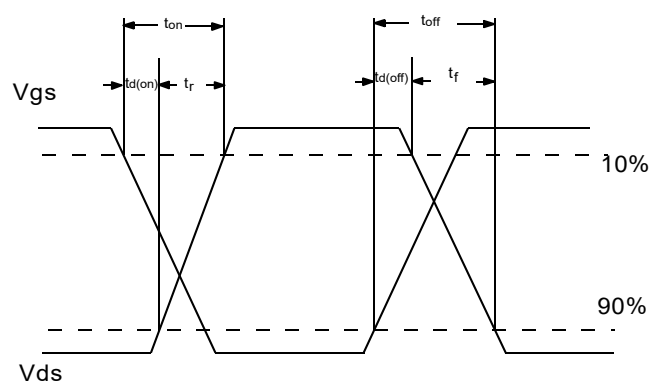
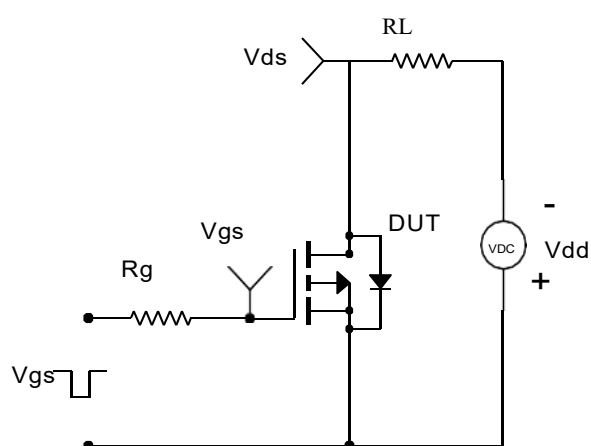


Figure 11. Transient Thermal Response Curve

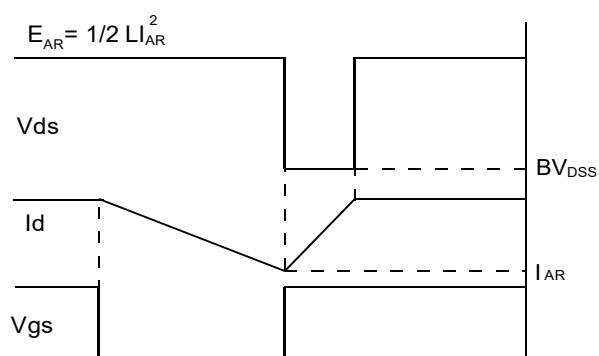
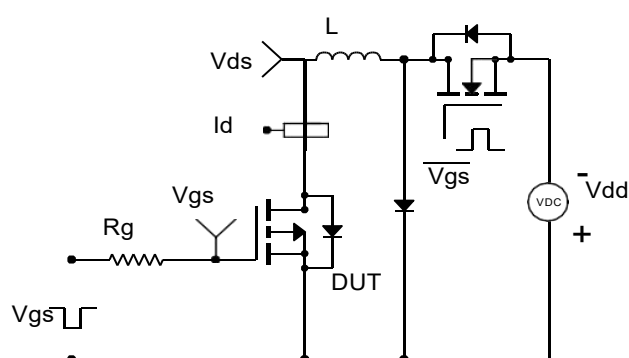
Gate Charge Test Circuit & Waveform



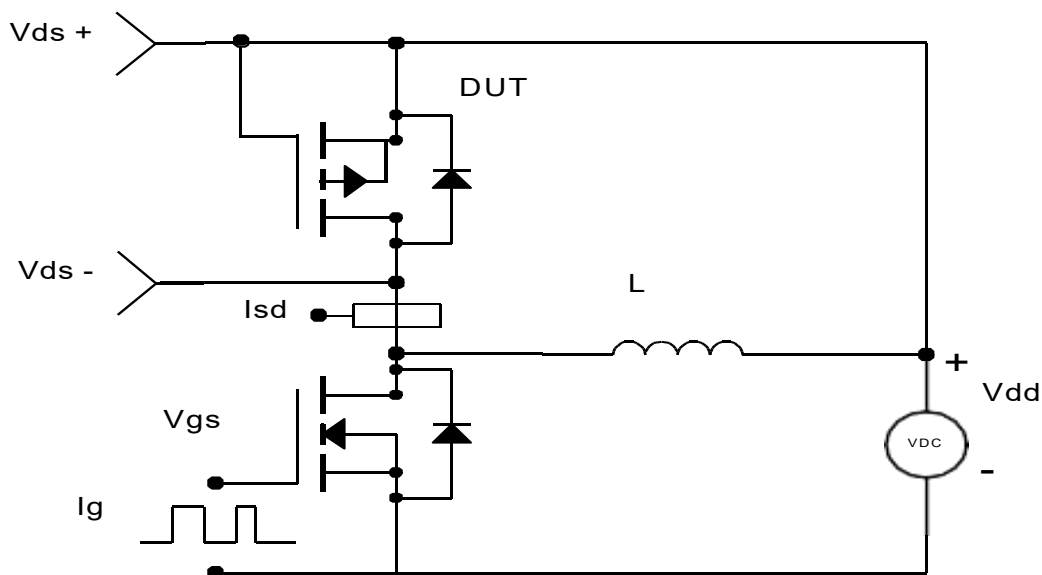
Resistive Switching Test Circuit & Waveforms



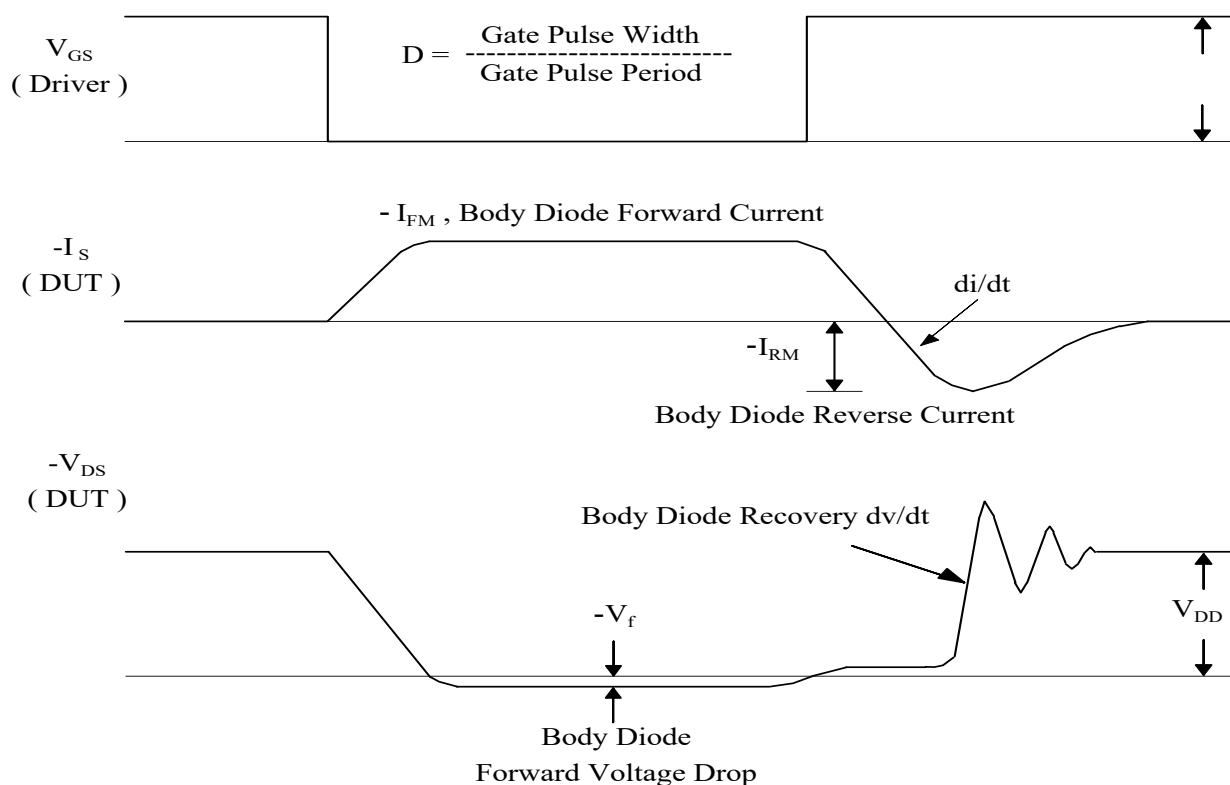
Unclamped Inductive Switching Test Circuit & Waveforms



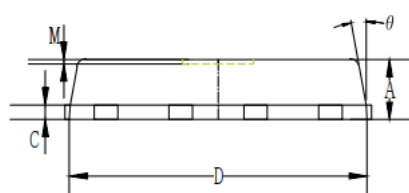
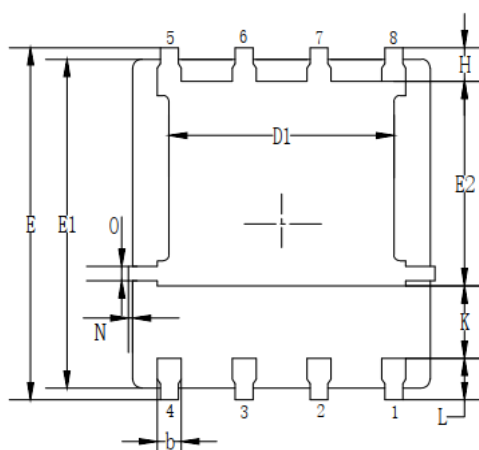
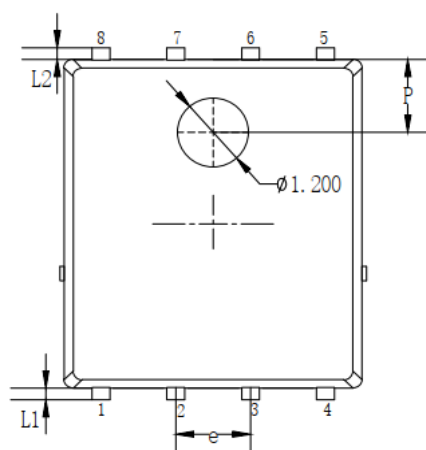
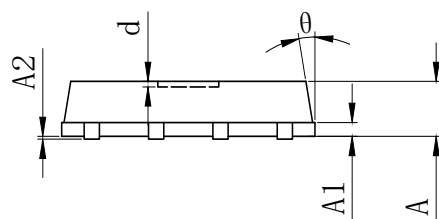
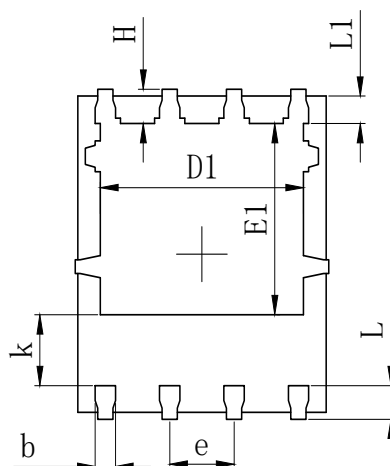
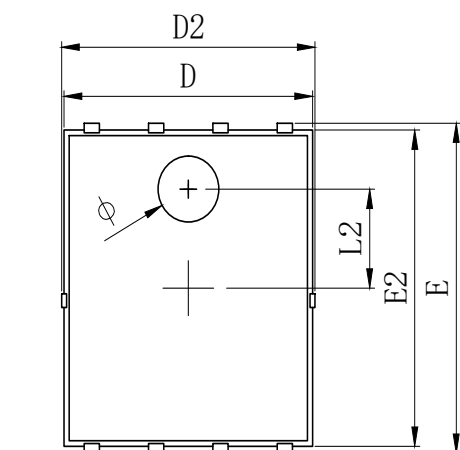
Peak Diode Recovery dv/dt Test Circuit & Waveforms



- dv/dt controlled by R_G
- I_{SD} controlled by pulse period



Dimensions (PDFN5*6)



SYMBOL	MILLIMETER		
	MIN	Typ.	MAX
A	0.900	1.000	1.100
A1	0.254 REF.		
A2	0~0.05		
D	4.824	4.900	4.976
D1	3.910	4.010	4.110
D2	4.924	5.000	5.076
E	5.924	6.000	6.076
E1	3.375	3.475	3.575
E2	5.674	5.750	5.826
b	0.350	0.400	0.450
e	1.270 TYP.		
L	0.534	0.610	0.686
L1	0.424	0.500	0.576
L2	1.800 REF.		
k	1.190	1.290	1.390
H	0.549	0.625	0.701
θ	8°	10°	12°
φ	1.100	1.200	1.300
d			0.100

Symbols	Millimeters		
	MIN.	NOM.	MAX.
A	0.90	1.05	1.20
b	0.35	0.40	0.50
c	0.20	0.25	0.35
D	4.90	5.05	5.20
D1	3.72	3.82	3.92
E	6.00	6.15	6.30
E1	5.60	5.75	5.90
E2	3.47	3.57	3.67
e	1.27 BSC.		
H	0.48	0.58	0.68
K	1.17	1.27	1.37
L	0.64	0.74	0.84
L1/L2	0.20 REF.		
θ	8°	10°	12°
M	0.08 REF.		
N	0	-	0.15
O	0.25 REF.		
P	1.28 REF.		

Disclaimer:

The information provided in this document is believed to be accurate and reliable. however, Shenzhen Core Control Electronics Technology Co., Ltd. does not assume any responsibility for the following consequences. Do not consider the use of such information or use beyond its scope.

The information mentioned in this document may be changed at any time without notice.

The products and information provided in this document do not infringe patents. Shenzhen Core Control Electronics Technology Co., Ltd. assumes no responsibility for any infringement of any other rights of third parties. The result of using such products and information.

This document is the first version issued on March 10th, 2023. This document replaces all previously provided information.

 It is a registered trademark of Shenzhen Core Control Electronics Technology Co., Ltd.

Copyright © 2017 Shenzhen Core Control Electronics Technology Co., Ltd. all rights reserved.