AZ DISPLAYS, INC.

COMPLETE LCD SOLUTIONS

SPECIFICATIONS FOR
LIQUID CRYSTAL DISPLAY

PART NUMBER: AGM1064B Series

REVISED: MAY 14, 2003

General Specification

Table 1

Item	Standard Value	Unit
Character Format	100X64 DOTS	Dots
Module Dimension	34.1(W) *25.3(H) *2.0(T)	mm
Viewing Area	28.0(W) * 20.9(H)	mm
DOT Size	0.21(W) * 0.234(H)	mm
DOT Pitch	0.24(W) * 0.264(H)	mm
Driving	1/64duty, 1/9bias	
View Direction	6H ■ 12H □ Other: □_____	
LCD Type	TN □ STN Gray □ STN Blue □ STN Yellow Green□ FSTN Positive ■ FSTN Negative □ Color STN □ FM LCD □	
Display Mode	Reflective □ Transflective□ Transmissive ■	
Driver IC	NT7532H-TABF1	
Interface	6800 □ 8080□ I^2C□	
DC/DC Converter	Internal ■ External □	
Operation Temperature	-10℃—60℃	
Storage Temperature	-20℃—70℃	

Electronic Units

3.1 Absolute Maximum Ratings

No	ITEM	Symbol	Min.	Typ.	Max.	Unit
1	OPERATING TEMPERATURE	T_{OP}	-10	-	60	℃
2	STORAGE TEMPERATURE	T_{ST}	-20	-	70	℃
3	SUPPLY VOLTAGE FOR LOGIC	V_{DD}-V_{SS}	VSS		3.6	V
4	SUPPLY VOLTAGE FOR LCD	V_{LCD}	VSS		13.5	V
5	INPUT VOLTAGE	V_I	VSS	-	VDD+0.5	V
6	STATIC ELECTRICITY	Be sure that you are grounded when handing LCM				

3.2 Electrical Characteristics

(Ta=25℃, V_{DD}=3.0V)

No	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Supply Voltage For Logic	V_{DD}-V_{SS}	/	/	3.0	/	V
2	Supply Voltage For LCD Driver	V_{DD}-V_o (V_{LCD})	/	/	10.0	/	V
3	Input High Voltage	V_{IH}	H level	0.8V_{DD}	/	V_{DD}	V
4	Input Low Voltage	V_{IL}	L level	0	/	0.2V_{DD}	V
5	Supply Current For Logic	I_{DD}	/	/	/	1	mA
9	USED IC	NT7532H-TABF1(NOVATEK)					

*Idd Measurement condition is for all pixels on display.(Unit: mA)

3.3 Interface Pin Function

Table 5

NO	SYMBOL	I/O	Description
1	NC		
2	NC		
3	NC		
4	NC		
5	FR	I/O	This is the liquid crystal alternating current signal I/O terminal M/S = "H": Output M/S = "H": Input When the NT7532 chip is used in master/slave mode, the various FR terminals must be connected.
6	CL	I/O	This is the display clock input terminal. When the NT7532 chips are used in master/slave mode, the various CL terminals must be connected.
7	/DOF	I/O	This is the liquid crystal display blanking control terminal. M/S = "H": Output M/S = "H": Input When the NT7532 chip is used in master/slave mode, the various DOF terminals must be connected.
8	NC	NC	
9	/CS1	I	This is the chip select signal. When CS1="L" and CS2="H", then the chip select becomes active, and data/command I/O is enabled.
10	CS2		
11	RES	I	When RES is set to "L", the settings are initialized. The reset operation is performed by the RES signal level
12	A0	I	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicate that D0 to D7 are display data A0 = "L": Indicates that D0 to D7 are control data
13	RD/WR	I	When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU WR signal. The signals on the data bus are latched at the rising edge of the WR signal. When connected to a 6800 Series MPU, this is the read/write control signal input terminal. When W R/ = "H": Read When W R/ = "L": Write
14	E/RD	I	When connected to an 8080 MPU, it is active LOW. This pad is connected to the RD signal of the 8080MPU, and the NT7532 data bus is in an output status when this signal is "L". When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU
15	D0	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.

<table>
<tr><td>16</td><td>D1</td><td rowspan="6"></td><td rowspan="6">When the serial interface is selected (P/S="L"), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance.
When the chip select is inactive, D0 to D7 are set to high impedance.</td></tr>
<tr><td>17</td><td>D2</td></tr>
<tr><td>18</td><td>D3</td></tr>
<tr><td>19</td><td>D4</td></tr>
<tr><td>20</td><td>D5</td></tr>
<tr><td>21</td><td>D6（SCL）</td></tr>
<tr><td>22</td><td>D7（SI）</td><td></td><td></td></tr>
<tr><td>23</td><td>DUTY0</td><td rowspan="2">I</td><td rowspan="2">Select the LCD driver duty<table><tr><th>DUTY1</th><th>DUTY1</th><th>LCD driver duty</th></tr><tr><td>0</td><td>0</td><td>1/33</td></tr><tr><td>0</td><td>1</td><td>1/49</td></tr><tr><td>1</td><td>0</td><td>1/55</td></tr><tr><td>1</td><td>1</td><td>1/69</td></tr></table></td></tr>
<tr><td>24</td><td>DUTY1</td></tr>
<tr><td>25</td><td>VDD</td><td>Supply</td><td>2.4 - 3.5V power supply input. These pads must be connected each other.</td></tr>
<tr><td>26</td><td>VDD2</td><td>Supply</td><td>This is the power supply for the step-up voltage circuit for the LCD. These pads must be connected each other.</td></tr>
<tr><td>27</td><td>VSS</td><td>Supply</td><td>Ground output for pad option.</td></tr>
<tr><td>28</td><td>VOUT</td><td>O</td><td>DC/DC voltage converter output</td></tr>
<tr><td>29</td><td>NC</td><td>NC</td><td></td></tr>
<tr><td>30</td><td>CAP3+</td><td>O</td><td>Capacitor 3+ pad for internal DC/DC voltage converter.</td></tr>
<tr><td>31</td><td>CAP1-</td><td>O</td><td>Capacitor 1- pad for internal DC/DC voltage converter.</td></tr>
<tr><td>32</td><td>CAP1+</td><td>O</td><td>Capacitor 1+ pad for internal DC/DC voltage converter.</td></tr>
<tr><td>33</td><td>CAP2+</td><td>O</td><td>Capacitor 2+ pad for internal DC/DC voltage converter.</td></tr>
<tr><td>34</td><td>CAP2-</td><td>O</td><td>Capacitor 2- pad for internal DC/DC voltage converter.</td></tr>
<tr><td>35</td><td>VEXT</td><td>I</td><td>This is the external input reference voltage (VREF) for the internal voltage regulator. It is valid only when external VREF is used. VEXT must be ≥ 2.4V and ≤ VDD2. When using internal VREF, this pad must be NC.</td></tr>
</table>

<table>
<tr><td>36</td><td>VRS</td><td>I</td><td>Select the internal voltage regulator or external voltage regulator.
VRS = 0: using the external VREF
VRS = 1: using the internal VREF</td></tr>
<tr><td>37</td><td>V1</td><td rowspan="5">Supply</td><td rowspan="5">LCD driver supplies voltages. The voltage determined by LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should be according to the following relationship:
V0 = V1 = V2 = V3 = V4 = Vss
When the on-chip operating power circuit is on, the following voltages are supplied to V1 to V4 by the on-chip power circuit. Voltage selection is performed by the Set LCD Bias command.
<table>
<tr><th>LCD</th><th>bias</th><th>V1</th><th>V2</th><th>V3</th></tr>
<tr><td>1/5</td><td>bias</td><td>4/5V0</td><td>3/5V0</td><td>2/5V0</td></tr>
<tr><td>1/6</td><td>bias</td><td>5/6V0</td><td>4/6V0</td><td>2/6V0</td></tr>
<tr><td>1/7</td><td>bias</td><td>6/7V0</td><td>5/7V0</td><td>2/7V0</td></tr>
<tr><td>1/8</td><td>bias</td><td>7/8V0</td><td>6/8V0</td><td>2/8V0</td></tr>
<tr><td>1/9</td><td>bias</td><td>8/9V0</td><td>7/9V0</td><td>2/9V0</td></tr>
</table></td></tr>
<tr><td>38</td><td>V2</td></tr>
<tr><td>39</td><td>V3</td></tr>
<tr><td>40</td><td>V4</td></tr>
<tr><td>41</td><td>V0</td></tr>
<tr><td>42</td><td>VR</td><td>I</td><td>Voltage adjustment pad. Applies voltage between V0 and VSS using a resistive divider.</td></tr>
<tr><td>43</td><td>M/S</td><td>I</td><td>This terminal selects the master/slave operation for the NT7532 chips. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals required for the liquid crystal display, synchronizing the liquid crystal display system.</td></tr>
<tr><td>44</td><td>CLS</td><td>I</td><td>Terminal to select whether enable or disable the display clock internal oscillator circuit.
CLS = “H”: Internal oscillator circuit is enabled
CLS = “L”: Internal oscillator circuit is disabled (requires external input)
When CLS = “L”, input the display clock through the CL pad.</td></tr>
<tr><td>45</td><td>C86</td><td>I</td><td>This is the MPU interface switch terminal
C86 = “H”: 6800 Series MPU interface
C86 = “L”: 8080 MPU interface</td></tr>
<tr><td>46</td><td>P/S</td><td>I</td><td>This is the parallel data input/serial data input switch terminal
P/S = “H”: Parallel data input
P/S = “L”: Serial data input
The following applies depending on the P/S status:
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial</th></tr>
<tr><td>"H"</td><td>A0</td><td>D0 to D7</td><td>RD WR</td><td>-</td></tr>
<tr><td>"L"</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
When P/S = “L”, D0 to D5 are HZ. D0 to D5 may be “H”, “L” or Open. RD(E) and WR(W R/) are fixed to either “H” or “L”.
With serial data input, RAM display data reading is not Supported.</td></tr>
<tr><td>47</td><td>/HPM</td><td>I</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
HPM = “H”, Normal mode
HPM = “L”, High power mode
This pad is enabled only when the master operation mode is selected and It is fixed to either “H” or “L” when the slave operation mode is selected.</td></tr>
<tr><td>48</td><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V0 voltage level adjustment.
IRS = “H”, Use the internal resistors
IRS = “L”, Do not use the internal resistors
The V0 voltage level is regulated by an external resistive</td></tr>
</table>

			voltage divider attached to the VR terminal. This pad is enabled only when the master operation mode is selected. It is fixed to either “H” or “L” when the slave operation mode is selected
49	**NC**	**NC**	

3.4 Commands

The display control instructions control the internal state of the NT7532H-TABF1(NOVATEK). Instruction is received from MPU to NT7532H-TABF1(NOVATEK) for the splay control. The following table shows various instructions.

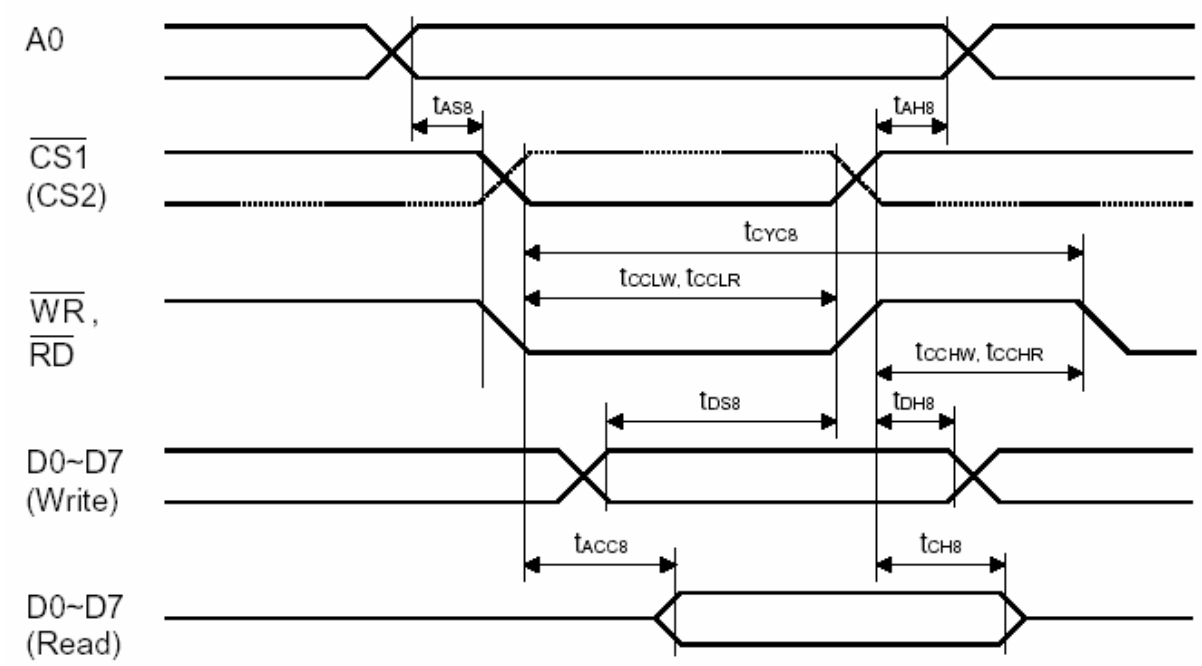
*: Don’t care

Command	A0	RD	WR	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
Display OFF	0	1	0	1	0	1	0	1	1	1	0 1	AEh AFh	Turn on LCD panel when goes high, and turn off when goes low
Set Display Start Line	0	1	0	0	1	Display Start Address						40h TO 7Fh	Specifies RAM display line for COM0
Set Page Address	0	1	0	1	0	1	1	Page Address				B0h to BFh	Set the display data RAM page in Page Address register
Set Column Address	0	1	0	0	0	0	1	Higher Column Address				00h TO 1Fh	Set 4 higher bits and 4 lower bits of column address of display data RAM in register
	0	1	0	0	0	0	0	Lower Column Address					
Read Status	0	0	1	Status				0	0	0	0	XX	Reads the status information
Write Display Data	1	1	0	Write Data								**xx**	Write data in display data RAM
Read Display Data	1	0	1	Read Data								**xx**	Read data from display data RAM
ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	A0h A1h	Set the display data RAM address SEG output correspondence
Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	A6h A7h	Normal indication when low, but full indication when high
Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	A4h A5h	Selects normal display (0) or entire display on
Set LCD Bias	0	1	0	1	0	1	0	0	0	1	01	A2h A3h	Sets LCD driving voltage bias ratio
Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	E0h	Increments column address counter during each write
End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read-Modify-Write

Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions
Common Output Mode Select	0	1	0	1	1	0	0	0 1	*	*	*	C0h to CFh	Selects COM output scan direction *: invalid data
Set Power Control	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Selects the power circuit operation mode
V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Selects internal resistor ratio Rb/Ra mode
Electronic Volume mode Set Electronic Volume Register Set	0	1	0	1	0	0	0	0	0	0	1	81h	
	0	1	0	*	*	Electronic Control Value						XX	Sets the V0 output voltage electronic volume register
Set Static indicator ON/OFF	0	1	0	0	0	1	0	1	0	1	0 1	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1: ON
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode
Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation
Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!
Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset

3.5 Timing Characteristics

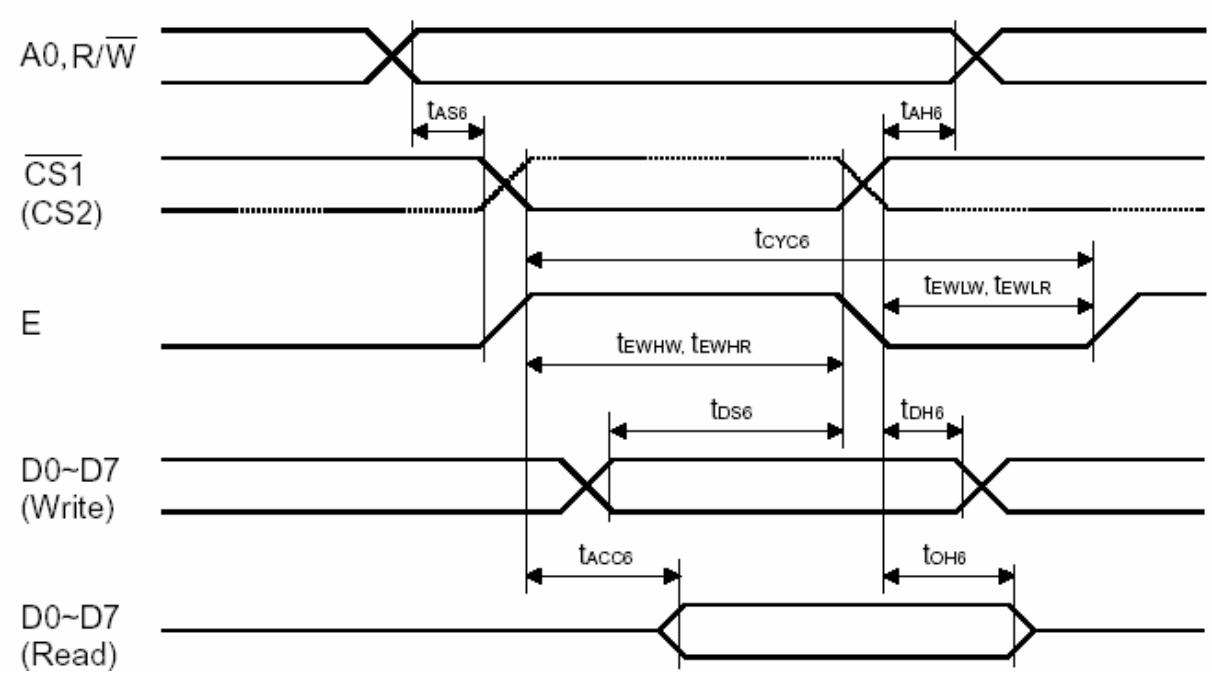
1. System Buses Read/Write Characteristics (for 8080 Series MPU)



Symbol	Parameter	Min	TYP	MAX	UNIT	Condition
T_{AH8}	Address hold time	0	-	-	ns	A0
T_{AS8}	Address setup time	0	-	-	ns	
T_{CYC8}	System cycle time	300	-	-	ns	SCL
T_{EWHW}	Control low pulse width (write)	90	-	-	ns	WR
T_{EWHR}	Control low pulse width (read)	120	-	-	ns	RD
T_{EWLW}	Control high pulse width (write)	120	-	-	ns	WR
T_{EWLR}	Control high pulse width (read)	60	-	-	ns	RD
T_{DS8}	Data setup time	40	-	-	ns	D0~D7
T_{DH8}	Data hold time	15	-	-	ns	
T_{ACC8}	/RD access time	-	-	140	ns	D0~D7, CL = 100pF
T_{OH8}	Output disable time	10	-	400	ns	

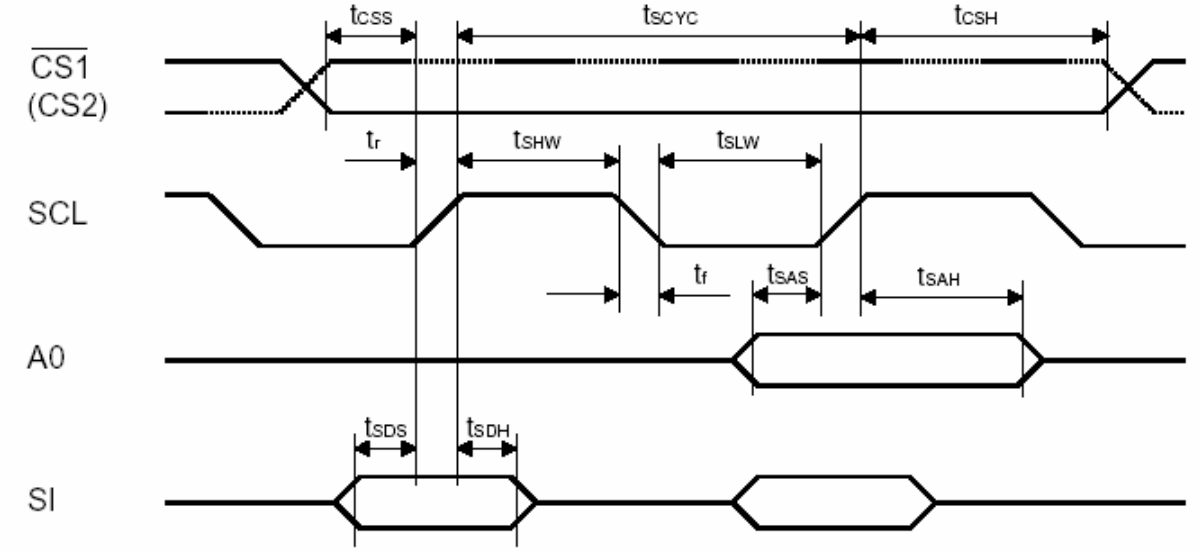
*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less.
($t_r + t_f$) < ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for write, ($t_r + t_f$) < ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) for read.
*2. All timing is specified using 20% and 80% of VDD as the reference.
*3. t_{CCLW} and t_{CCLR} are specified as the overlap interval when CS1 is low (CS2 is high) and WR or RD is low.

2. System Buses Read/Write Characteristics (for 6800 Series MPU)



Symbol	Parameter	Min	TYP	MAX	UNIT	Condition
T_{AH6}	Address hold time	0	-	-	ns	A0
T_{AS6}	Address setup time	0	-	-	ns	
T_{CYC6}	System cycle time	300	-	-	ns	SCL
T_{EWHW}	Control low pulse width (write)	90	-	-	ns	WR
T_{EWHR}	Control low pulse width (read)	120	-	-	ns	RD
T_{EWLW}	Control high pulse width (write)	120	-	-	ns	WR
T_{EWLR}	Control high pulse width (read)	60	-	-	ns	RD
T_{DS6}	Data setup time	40	-	-	ns	D0~D7
T_{DH6}	Data hold time	15	-	-	ns	
T_{ACC6}	/RD access time	-	-	140	ns	D0~D7, CL = 100pF
T_{OH6}	Output disable time	10	-	400	ns	

3. Serial Interface Timing



Symbol	Parameter	Min	TYP	MAX	UNIT	Condition
T_{SCYC}	Serial clock cycle	250	-	-	ns	SCL
T_{SHW}	Serial clock H pulse width	100	-	-	ns	SCL
T_{SLW}	Serial clock L pulse width	100	-	-	ns	SCL
T_{SAS}	Address setup time	150	-	-	ns	D/I
T_{SAH}	Address hold time	150	-	-	ns	D/I
T_{SDS}	Data setup time	100	-	-	ns	SDI
T_{SDH}	Data hold time	100	-	-	ns	SDI
T_{CSS}	Chip select setup time	150	-	-	ns	CS1, CS2
T_{CSH}	Chip select hold time	150	-	-	ns	CS1, CS2

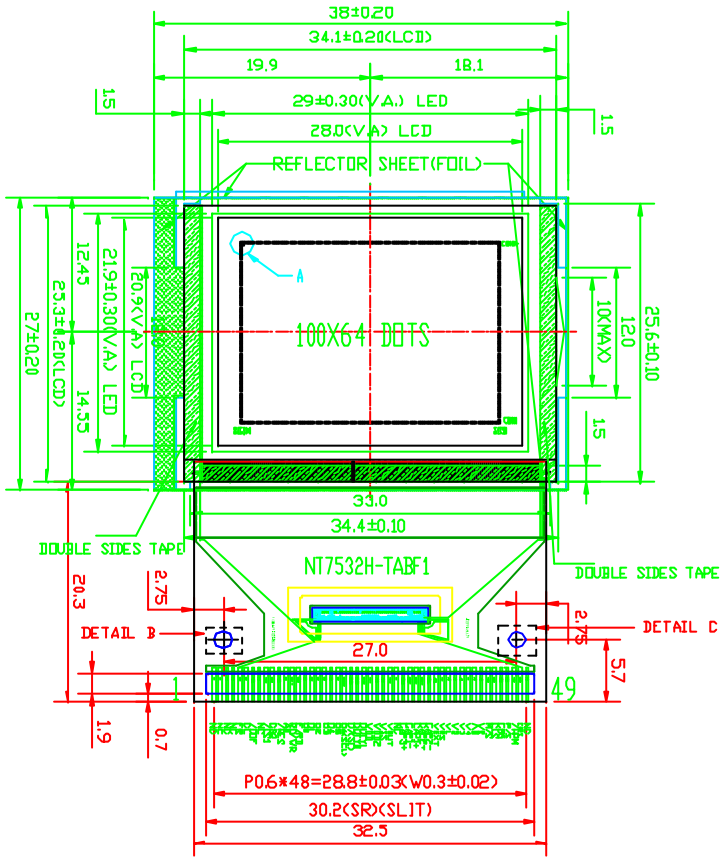
*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less.

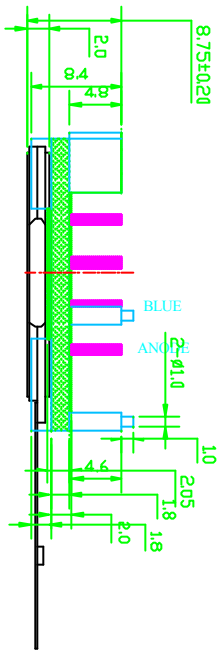
*2. All timing is specified using 20% and 80% of VDD as the standard.

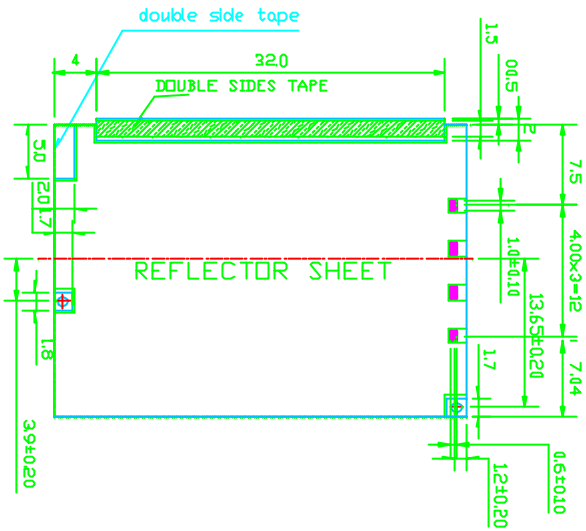
Electro-optical Units

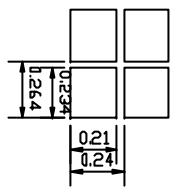
4.1 Electro-optical Characteristics

No	Item		Symbol	Condition	Min	Typ	Max	Unit	Drive
1	Contrast Ratio		C_R	T_a=23±3°C	-	5.5	-	-	
2	**Response time**	Rise	T_r	$\theta_1=\theta_2=$	-	260	-	ms	
		Down	T_f	$\theta_3=\theta_4=0$	-	200	-	ms	
3	**Viewing Angle Range**	6H ϕ=270	θ_1	T_a=23±3°C C_r=2	-	60	-	Deg	V_{op}=10V 1/64 Duty 1/9 Bias f=100H_Z
		12H ϕ=90	θ_2		-	25	-		
		3H ϕ=0	θ_3		-	50	-		
		9H ϕ=180	θ_4		-	50	-		
4	LCD Driving Voltage		V_{OP}	T_a=23±3°C	-	10	-	V	

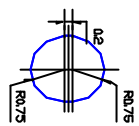




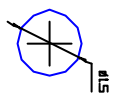




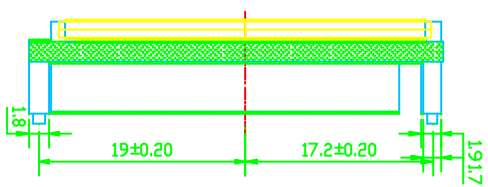
DETAIL A



DETAIL B



DETAIL C



NOTE:

1.MODE: FSTN-Transflective-Positive
2.1/65duty,1/9bias,view angle 6 o'clock
3.Vdd=3.0V Vlcd=10.0V
4.Operation temperature:-10¡ãC~+60¡ãC
5.Store temperature:-20¡ãC~+70¡ãC
6.Driver IC:NT7532H-TABF1
7.The tolerance unless classified ¡À0.2

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
SIGNAL	NC	RC	NC	RC	FR	CL	/DOF	ND	/CS1	CS2	/RES	A0	RD/WR	E/RD	R/W	D0	D1	D2	D3	D4	D5	D6/SCL	D7/SID	/WR	/CS2
PIN	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49
SIGNAL	V33	VIDO	D/IO	VOUT	NC	BUMP	CAP1-	CAP1+	CAP2+	CAP2-	VOUT	TEST	V1	V2	V3	V4	V0	VR	M/S	CLS	CSEL	P/S	/RST	DNC	NC

AZ Displays, Inc.					AGM1064B-MLB-FBW	UNITS: mm
					DWG: SM5424	SHEET 1 OF 1

CUSTOMER APPROVAL: