



General Description

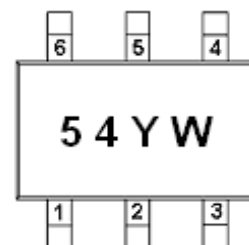
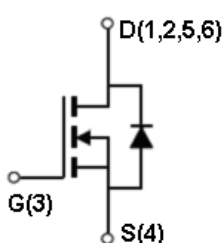
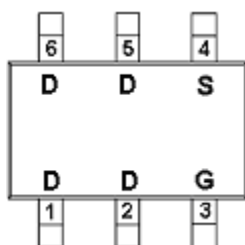
AFN3480, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- 40V/5.6A, $R_{DS(ON)} = 54m\Omega @ V_{GS} = 10V$
- 40V/3.6A, $R_{DS(ON)} = 74m\Omega @ V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- TSOP-6 package design

Pin Description (TSOP-6)



Application

- Power Management in Note book
- LED Display
- DC-DC System
- LCD Panel

Pin Define

Pin	Symbol	Description
1	D	Drain
2	D	Drain
3	G	Gate
4	S	Source
5	D	Drain
6	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN3454TS6RG	54YW	TSOP-6	Tape & Reel	3000 EA

- ※ 54 parts code
- ※ Y year code (0 ~ 9)
- ※ W week code (A ~ Z = 1 ~ 26 / a ~ z = 27 ~ 52)
- ※ AFN3454TS6RG : 7" Tape & Reel ; Pb- Free ; Halogen- Free



Absolute Maximum Ratings

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	40	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	T _A =25°C 5.6	A
		T _A =70°C 3.6	
Pulsed Drain Current	I _{DM}	15	A
Continuous Source Current(Diode Conduction)	I _S	1.7	A
Power Dissipation	P _D	T _A =25°C 2.0	W
		T _A =70°C 1.3	
Operating Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	120	°C/W

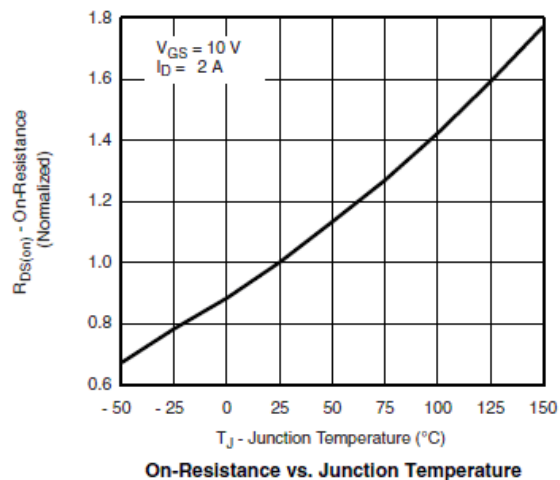
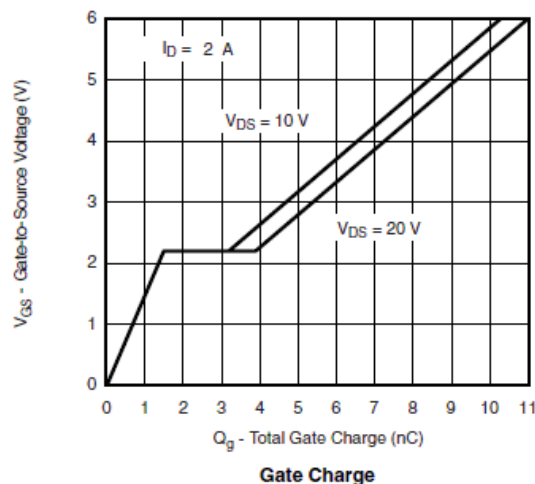
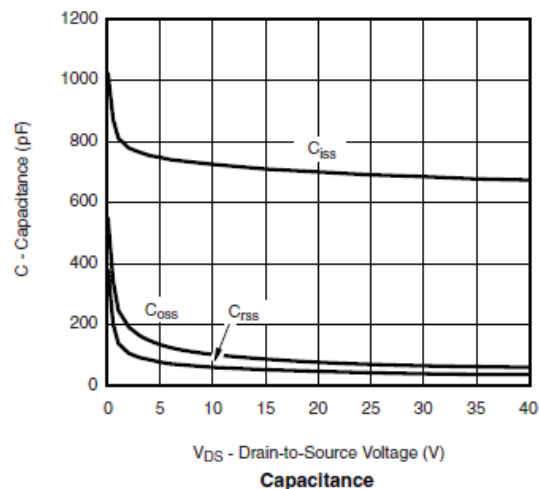
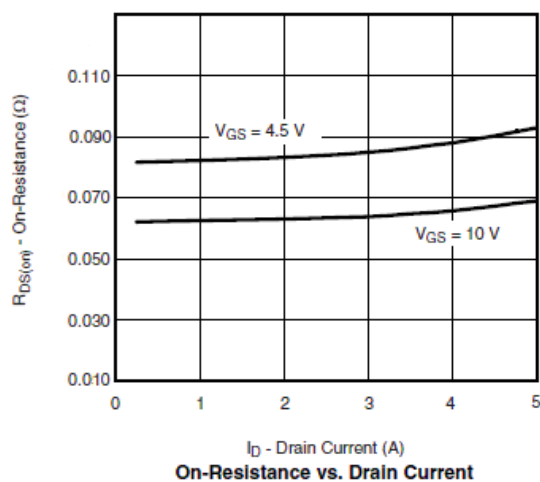
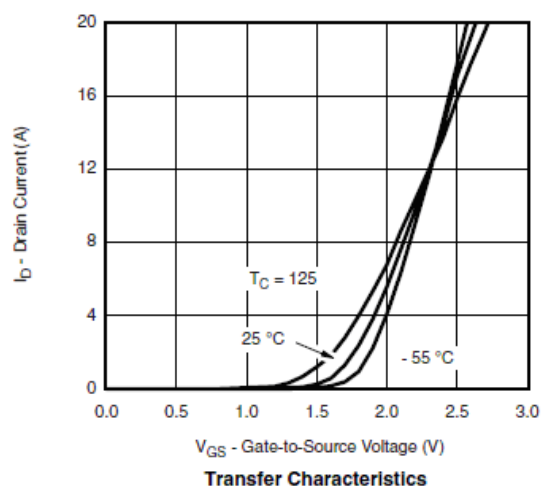
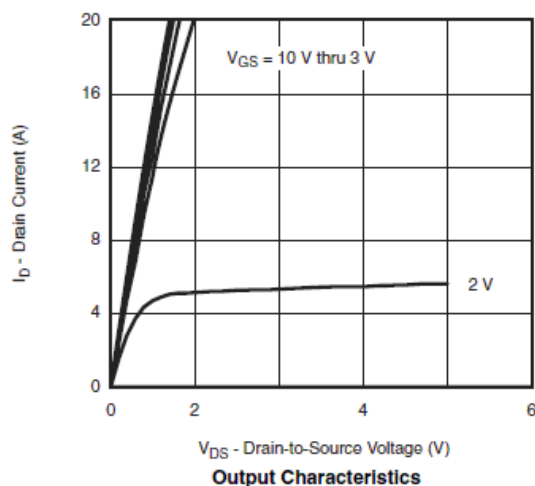
Electrical Characteristics

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250uA	40			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1.0		2.0	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	uA
		V _{DS} =40V, V _{GS} =0V T _J =85°C			10	
On-State Drain Current	I _{D(on)}	V _{DS} ≥ 5V, V _{GS} =10V	10			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =5.6A		47	54	mΩ
		V _{GS} =4.5V, I _D =3.6A		66	74	
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =2.0A		16		S
Diode Forward Voltage	V _{SD}	I _S =1.5A, V _{GS} =0V		0.85	1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =20V, V _{GS} =4.5V I _D ≡2A		10	15	nC
Gate-Source Charge	Q _{gs}			2		
Gate-Drain Charge	Q _{gd}			2.5		
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V f=1MHz		650		pF
Output Capacitance	C _{oss}			75		
Reverse Transfer Capacitance	C _{rss}			45		
Turn-On Time	t _{d(on)}	V _{DD} =15V, R _L =15Ω I _D ≡1A, V _{GEN} =10V R _G =6Ω		8	15	ns
	t _r			12	20	
Turn-Off Time	t _{d(off)}			28	40	
	t _f			8	15	

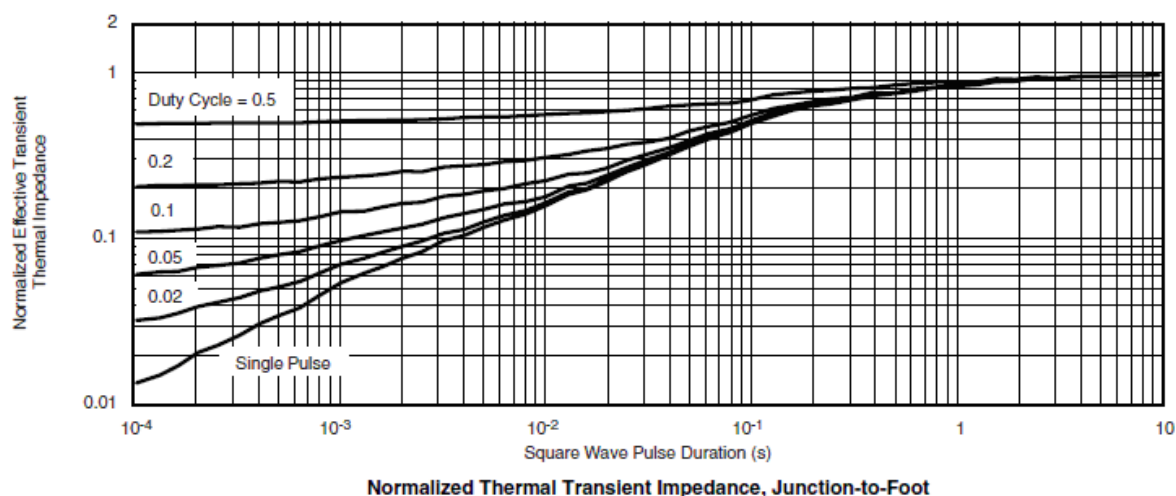
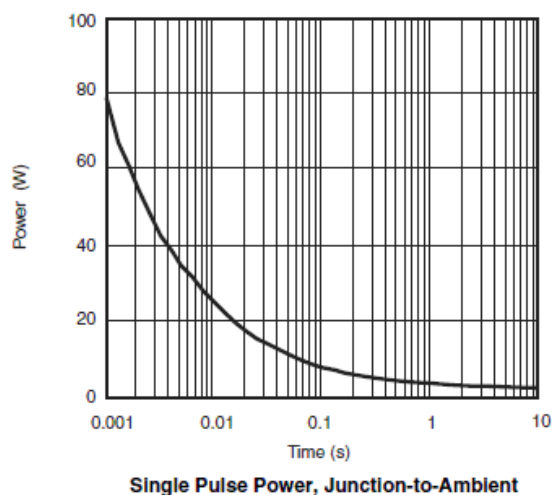
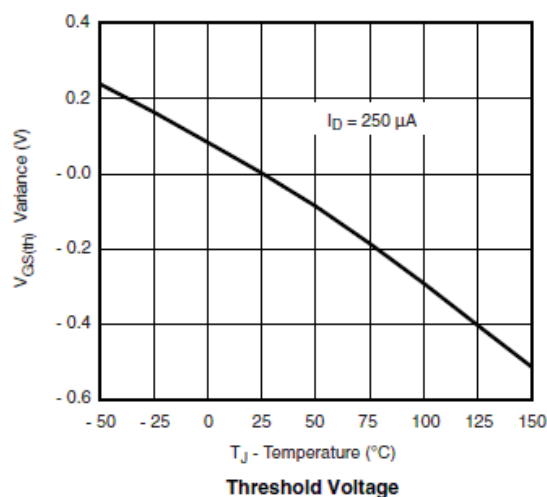
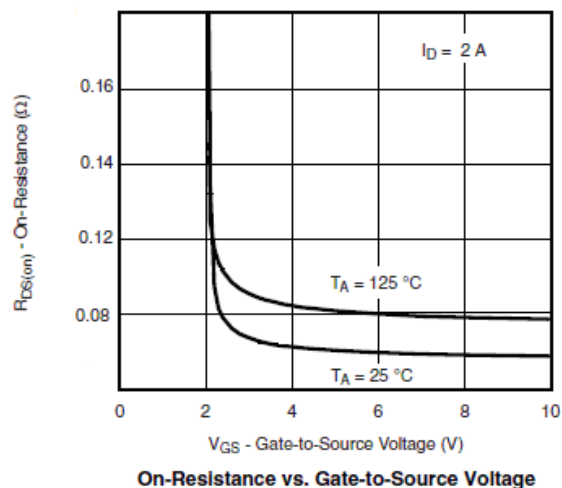
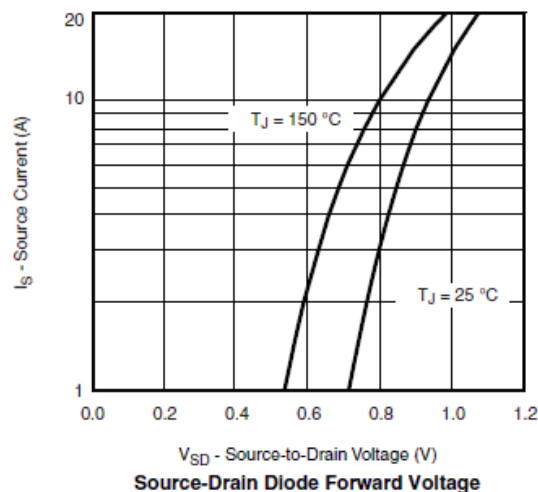


Typical Characteristics





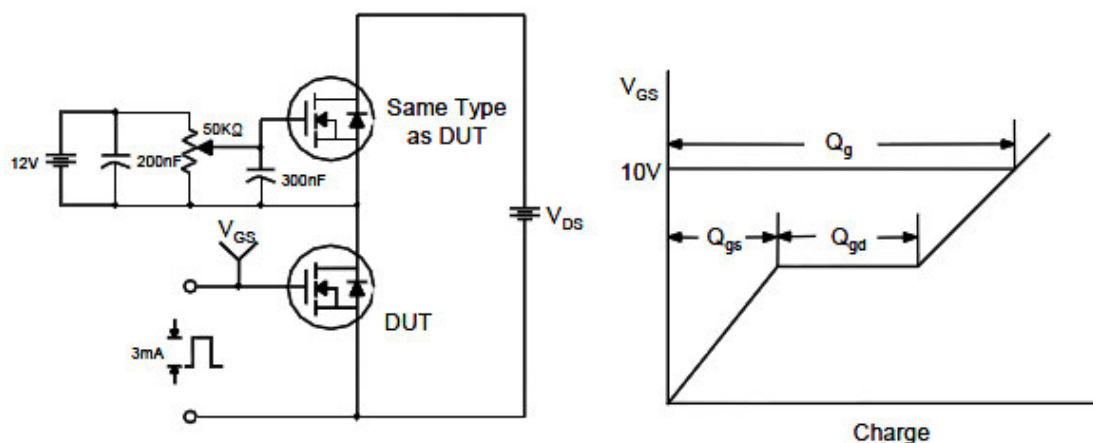
Typical Characteristics



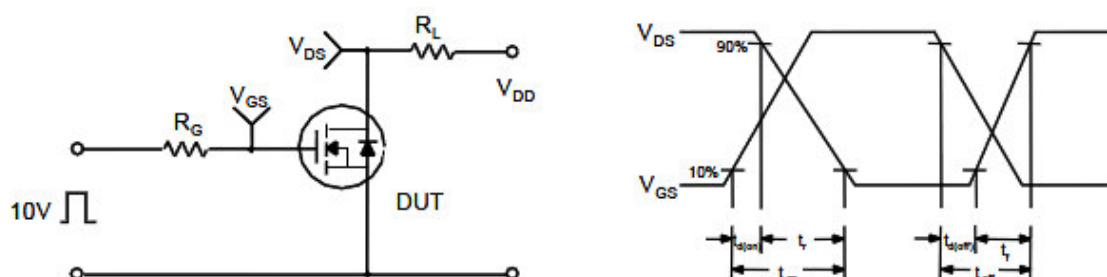


Typical Characteristics

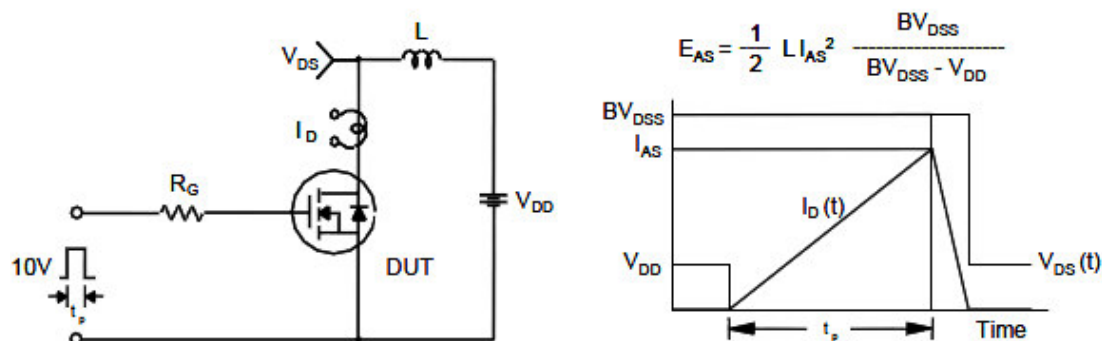
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

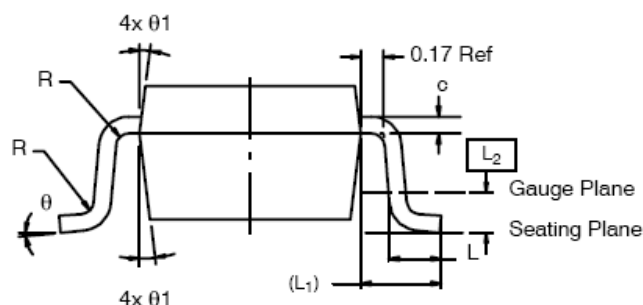
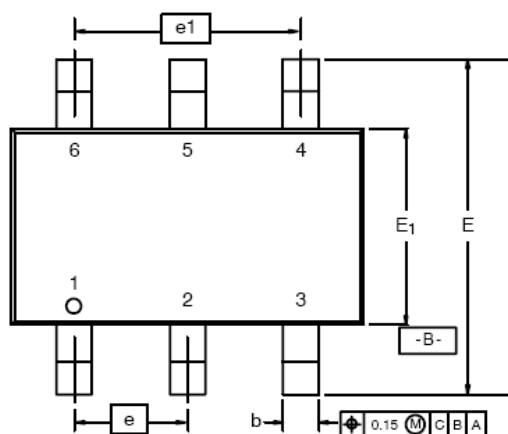


Unclamped Inductive Switching Test Circuit & Waveforms





Package Information (TSOP-6)



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.96	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	1.00 BSC			0.0394 BSC		
e ₁	1.90	2.00	2.10	0.075	0.080	0.085
L	0.35	-	0.50	0.014	-	0.020
L ₁	0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
Ø	0°	4°	8°	0°	4°	8°
Ø ₁	7° Nom			7° Nom		

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