



**Alfa-MOS
Technology**

**AFN123WS
100V N-Channel
Enhancement Mode MOSFET**

General Description

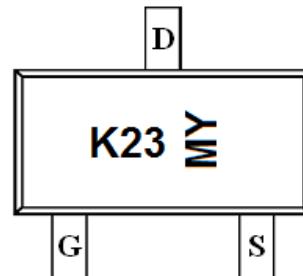
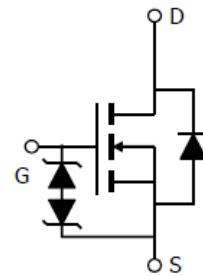
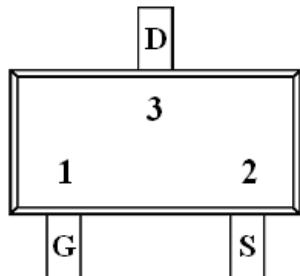
AFN123WS, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, such as smart phone and notebook computer and other battery powered circuits, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- 100V/0.17A , $R_{DS(ON)}=5.8\Omega @ V_{GS}=10V$
- 100V/0.17A , $R_{DS(ON)}=6.8\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- ESD Protection Diode design-in
- SOT-323 package design

Pin Description (SOT-323)



Application

- Drivers: Relays, Solenoids, Lamps, Hammers, Display, Memories, Transistors, etc.
- High saturation current capability. Direct Logic-Level Interface: TTL/CMOS
- Battery Operated Systems
- Solid-State Relays

Pin Define

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN123WSS32RG	K23YM	SOT-323	Tape & Reel	3000 EA

- ※ K23 Parts code
 ※ Y Year code (0 ~ 9)
 ※ M Month code (A ~ L = 1 ~ 12)
 ※ AFN123WSS32RG : 7" Tape & Reel ; Pb- Free ; Halogen- Free



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Absolute Maximum Ratings

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate –Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current($T_J=150^\circ\text{C}$)	I_D	0.17	A
$T_A=70^\circ\text{C}$		0.17	
Pulsed Drain Current	I_{DM}	0.68	A
Continuous Source Current(Diode Conduction)	I_S	0.4	A
Power Dissipation	P_D	0.35	W
$T_A=70^\circ\text{C}$		0.22	
Operating Junction Temperature	T_J	150	150
Storage Temperature Range	T_{STG}	-55/150	-55/150
Thermal Resistance-Junction to Ambient	R_{eJA}	120	120

Electrical Characteristics

($T_A=25^\circ\text{C}$ Unless otherwise noted)

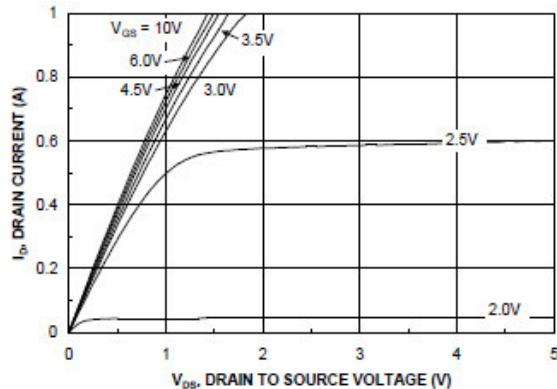
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	100			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0		3.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			10	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80\text{V}, V_{GS}=0\text{V}$			1	μA
		$V_{DS}=80\text{V}, V_{GS}=0\text{V}$ $T_J=85^\circ\text{C}$			10	
Drain-Source On-Resistance	$R_{DS(\text{on})}$	$V_{GS}=10\text{V}, I_D=0.17\text{A}$		4.0	5.8	Ω
		$V_{GS}=4.5\text{V}, I_D=0.17\text{A}$		4.6	6.8	
Forward Transconductance	g_{FS}	$V_{DS}=10\text{V}, I_D=0.17\text{A}$		0.8		S
Diode Forward Voltage	V_{SD}	$I_S=0.17\text{A}, V_{GS}=0\text{V}$		0.75	1.3	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=30\text{V}, V_{GS}=10\text{V}$ $I_D=0.22\text{A}$		1.8	3.5	nC
Gate-Source Charge	Q_{gs}			0.2		
Gate-Drain Charge	Q_{gd}			0.3		
Input Capacitance	C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0\text{V}$ $f=1\text{MHz}$		70		pF
Output Capacitance	C_{oss}			8		
Reverse Transfer Capacitance	C_{rss}			5		
Turn-On Time	$t_{d(on)}$	$V_{DD}=30\text{V}, R_G=50\Omega$ $I_D=0.28\text{A}, V_{GEN}=10\text{V}$		5	10	ns
	t_r			5	10	
Turn-Off Time	$t_{d(off)}$			7	15	
	t_f			10	20	



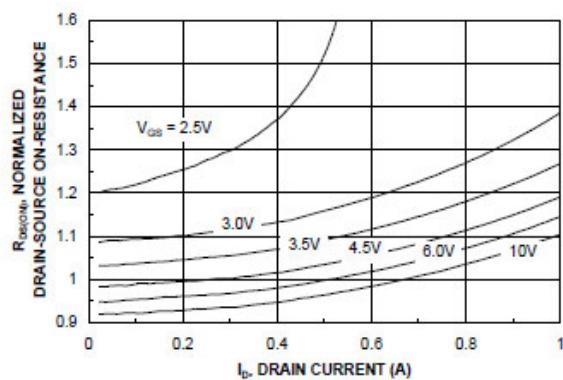
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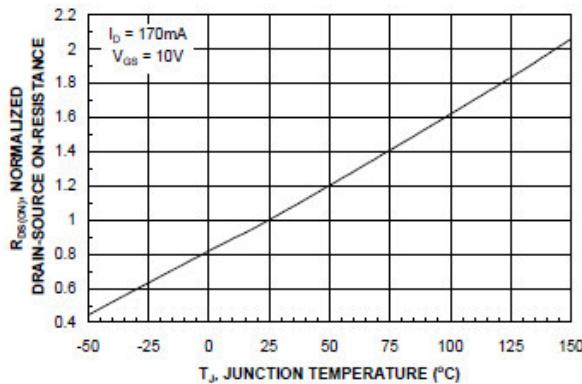
Typical Characteristics



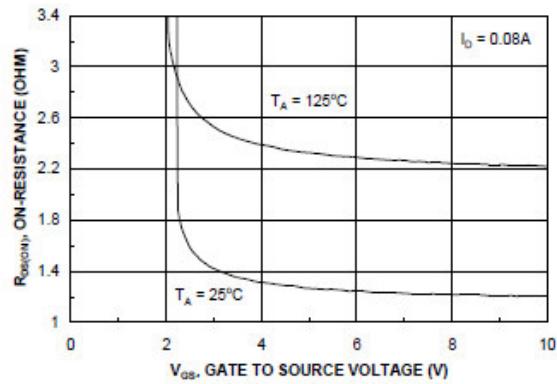
On-Region Characteristics



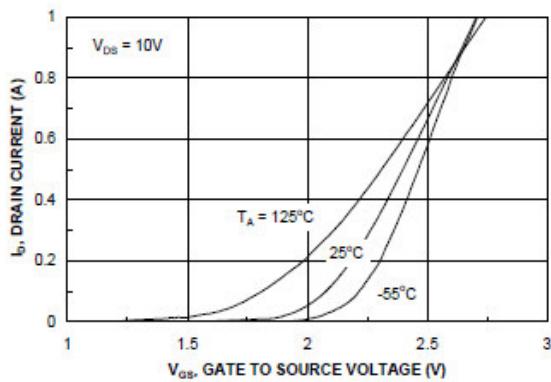
On-Resistance Variation with
Drain Current and Gate Voltage



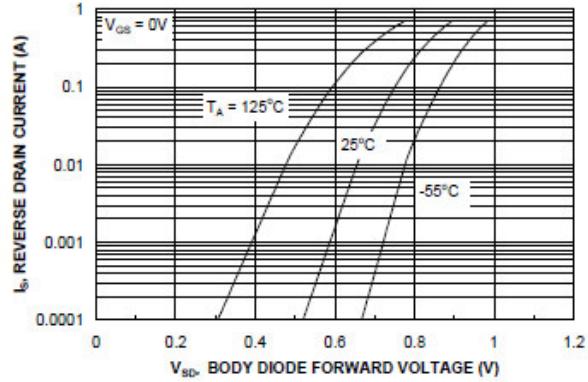
On-Resistance Variation with Temperature



On-Resistance Variation with
Gate-to-Source Voltage



Transfer Characteristics



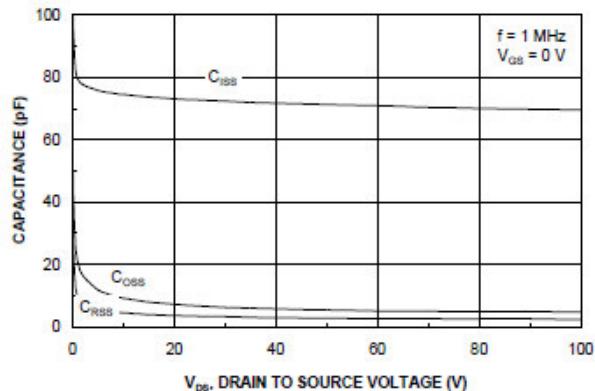
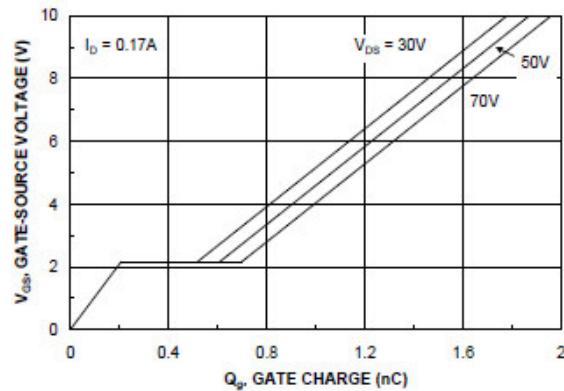
Body Diode Forward Voltage Variation
with Source Current and Temperature



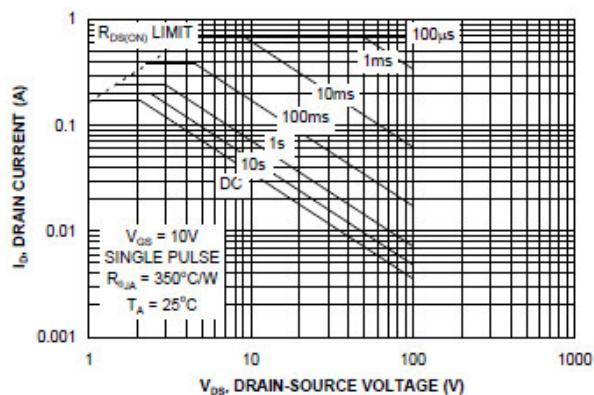
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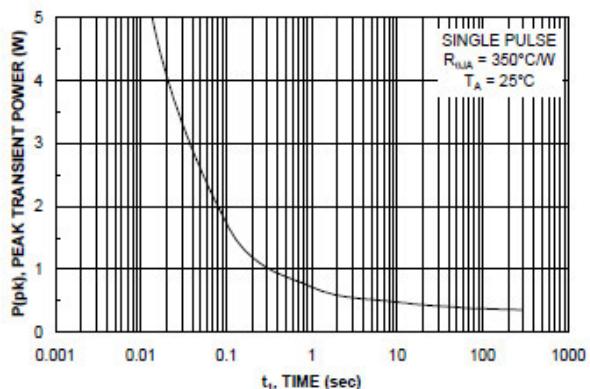


Gate Charge Characteristics

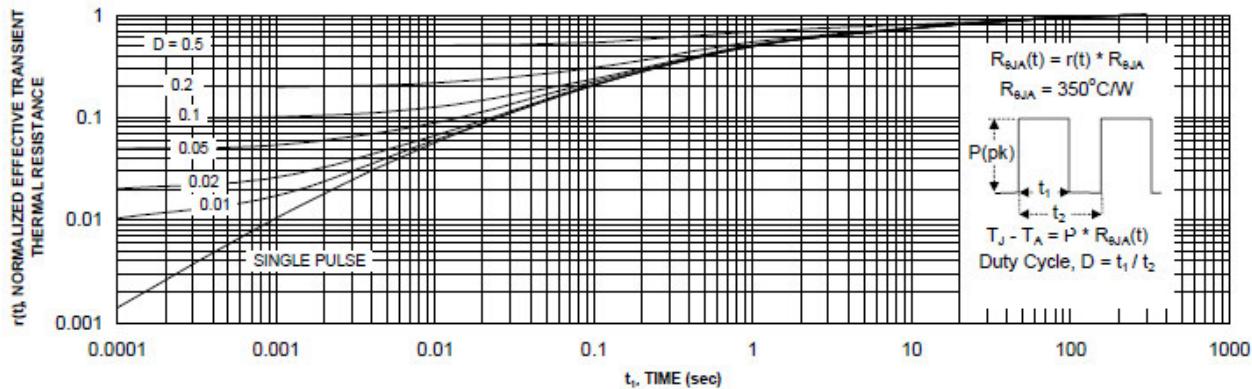


Maximum Safe Operating Area

Capacitance Characteristics



Single Pulse Maximum Power Dissipation

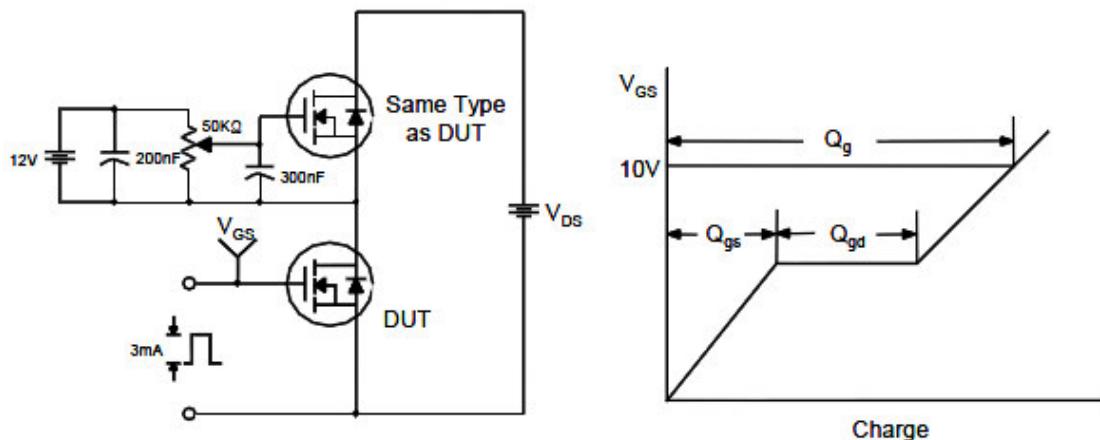


Transient Thermal Response Curve, Junction to Ambient

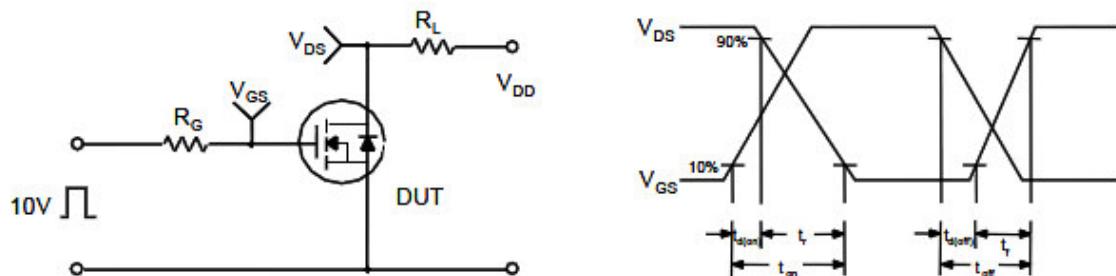


Typical Characteristics

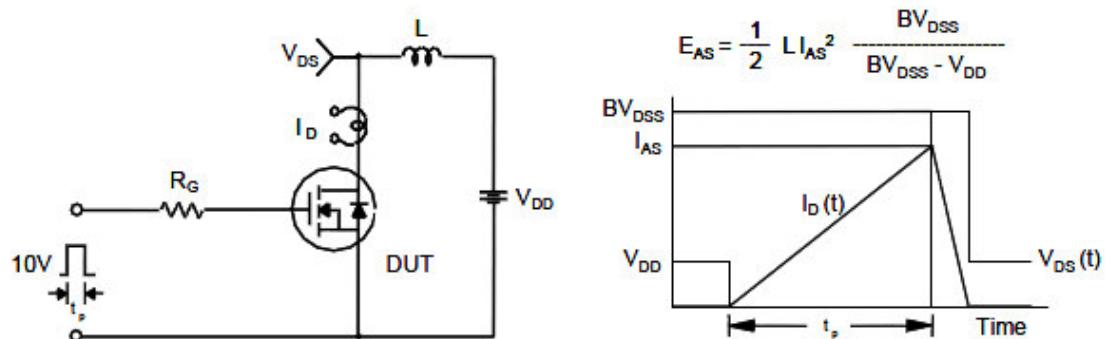
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

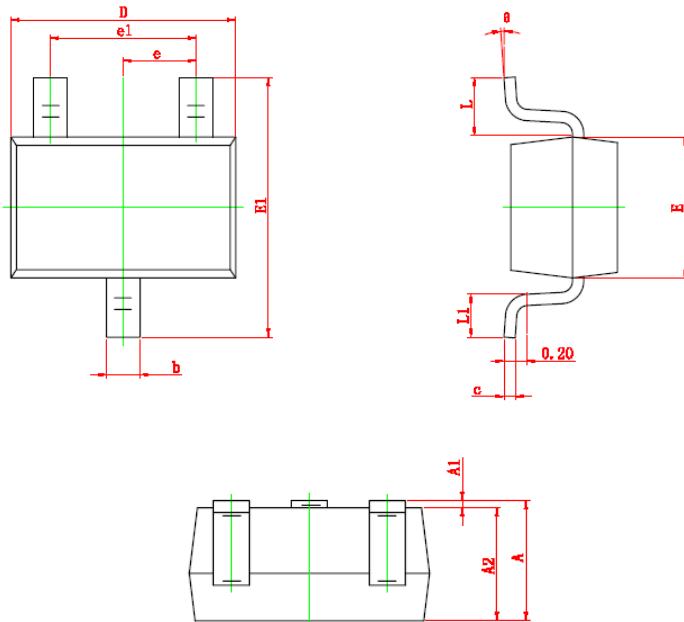




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Package Information (SOT-323)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.200	0.400	0.008	0.016
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP		0.026 TYP	
e1	1.200	1.400	0.047	0.055
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

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2F, No.80, Sec.1, Cheng Kung Rd., Nan Kang Dist., Taipei City 115, Taiwan (R.O.C.)
Tel : 886 2) 2651 3928
Fax : 886 2) 2786 8483
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