Micropower, Dual-Channel Digital Isolators

Data Sheet **ADuM1240/ADuM1241/ADuM1245/ADuM1246**

FEATURES

- **Ultralow power operation**
  - **3.3 V operation**
    - **16 µA per channel maximum quiescent current, refresh enabled**
    - **0.3 µA per channel typical quiescent current, refresh disabled**
    - **148 µA/Mbps per channel typical dynamic current**
  - **2.5 V operation**
    - **8 µA per channel maximum quiescent current, refresh enabled**
    - **0.1 µA per channel typical quiescent current, refresh disabled**
    - **116 µA/Mbps per channel typical dynamic current**
- **Small, 20-lead SSOP package**
- **Bidirectional communication**
- **Up to 2 Mbps data rate (NRZ)**
- **High temperature operation: 125°C**
- **High common-mode transient immunity: >25 kV/µs**
- **Safety and Regulatory Approvals**
  - **UL 1577 component recognition program (pending)**
    - **3750 V rms for 1 minute per UL 1577**
  - **CSA Component Acceptance Notice 5A (pending)**
  - **VDE certificate of conformity (pending)**
    - **DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12**
    - **V_{IORM} = 849 V peak**

APPLICATIONS

- **General-purpose, low power, multichannel isolation**
- **1 MHz low power SPI**
- **4 mA to 20 mA loop process control**

GENERAL DESCRIPTION

The ADuM1240/ADuM1241/ADuM1245/ADuM1246[1] are micropower, dual-channel digital isolators based on the Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic air core transformer technologies, these isolation components provide outstanding performance characteristics superior to alternatives, such as optocoupler devices, yet consume extremely low power.

Packaged in a 20-lead SSOP, this series of dual, 3.75 kV rms digital isolation devices operate with supplies as low as 2.25 V and typically consume a minimal current of less than 6 µA per channel at data rates below 20 kbps, a fraction of the power of comparable isolators at comparable data rates (up to 2 Mbps). In addition, all models provide low pulse width distortion (<8 ns) and an input glitch filter for extraneous noise disturbance protection. All models operate with an independent supply voltage on either side (between 2.25 V and 3.6 V), providing compatibility with lower voltage systems and enabling voltage level translation functionality across the isolation barrier. In the absence of input power, the products default to a predetermined output logic state: the ADuM1240 and ADuM1241 default to high output, and the ADuM1245 and ADuM1246 default to low output.

FUNCTIONAL BLOCK DIAGRAM

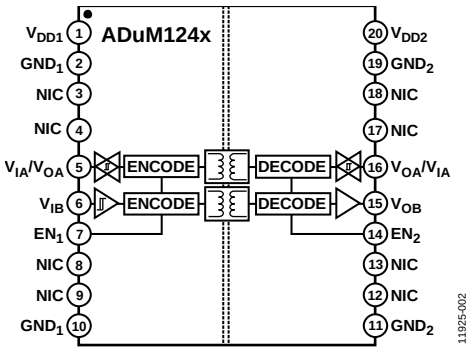

Figure 1.

PRODUCT HIGHLIGHTS

1. Microwatt Power. These 3.75 kV digital isolators consume less than 15 µW per channel quiescent and 950 µW per channel at 2 Mbps.
2. Low Supply Operation. Supports power supply voltages down to 2.25 V.
3. *i*Coupler Technology. Patented Analog Devices technology combining high speed CMOS and monolithic air core transformer technologies.

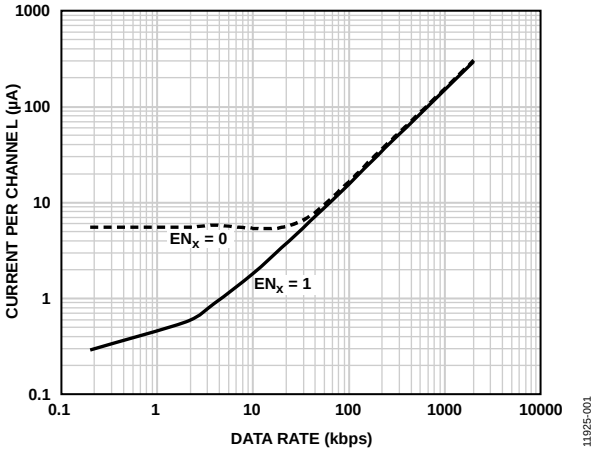

Figure 2. Typical Total Supply Current (I_{DD1} + I_{DD2}) per Channel (V_{DDx} = 3.3 V)

[1] Protected by U.S. Patents 5,952,849, 6,873,065, 7,075,329, 6,262,600. Other patents pending.

Rev. 0 **Document Feedback**

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REVISION HISTORY

12/13—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range of 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF, and CMOS signal levels, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				2	Mbps	Within pulse-width distortion (PWD) limit
Propagation Delay	t_{PHL}, t_{PLH}		80	180	ns	50% input to 50% output
Change vs. Temperature			200		ps/°C	
Minimum Pulse Width	PW	500			ns	Within PWD limit
Pulse-Width Distortion	PWD			8	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Propagation Delay Skew[1]	t_{PSK}			10	ns	
Channel Matching						
Codirectional	t_{PSKCD}			10	ns	
Opposing Direction	t_{PSKOD}			15	ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						2 Mbps, no load
ADuM1240/ADuM1245	I_{DD1}		366	600	µA	
	I_{DD2}		246	375	µA	
ADuM1241/ADuM1246	I_{DD1}		306	450	µA	
	I_{DD2}		306	450	µA	

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 V_{DDx}[1]			V	
Logic Low	V_{IL}			0.3 V_{DDx}[1]	V	
Output Voltages						
Logic High	V_{OH}	V_{DDx}[1] − 0.1	3.3		V	I_{OUTx} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx}[1] − 0.4	3.1		V	I_{OUTx} = −4 mA, V_{Ix} = V_{IxH}
Logic Low	V_{OL}		0.0	0.1	V	I_{OUTx} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{OUTx} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−1	+0.01	+1	µA	0 V ≤ V_{Ix} ≤ V_{DDx}[1]
Input Switching Thresholds						
Positive Threshold Voltage	V_{T+}		1.8		V	
Negative Going Threshold	V_{T-}		1.2		V	
Input Hysteresis	ΔV_T		0.6		V	
Undervoltage Lockout, V_{DD1} or V_{DD2}	UVLO		1.5		V	
Supply Current per Channel						
Quiescent Current						
Input Supply	$I_{DDI (Q)}$		4.8	10	µA	EN_X low
Output Supply	$I_{DDO (Q)}$		0.8	6	µA	EN_X low
Input (Refresh Off)	$I_{DDI (Q)}$		0.12		µA	EN_X high
Output (Refresh Off)	$I_{DDO (Q)}$		0.13		µA	EN_X high

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Dynamic Supply Current						
Input	$I_{DDI (D)}$		88		μA/Mbps	
Output	$I_{DDO (D)}$		60		μA/Mbps	
AC SPECIFICATIONS						
Output Rise Time/Fall Time	t_R/t_F		2		ns	10% to 90%
Common-Mode Transient Immunity[2]	|CM|	25	40		kV/μs	$V_{Ix} = V_{DDx}$[1], V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		14		kbps	

[1] $V_{DDx} = V_{DD1}$ or V_{DD2}.
[2] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{OUT} > 0.8\ V_{DDx}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

All typical specifications are at T_A = 25°C, $V_{DD1} = V_{DD2}$ = 2.5 V. Minimum/maximum specifications apply over the entire recommended operation range of 2.25 V ≤ V_{DD1} ≤ 2.75 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF, and CMOS signal levels, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				2	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		112	180	ns	50% input to 50% output
Change vs. Temperature			280		ps/°C	
Pulse-Width Distortion	PWD			12	ns	$\|t_{PLH} - t_{PHL}\|$
Minimum Pulse Width	PW	500			ns	Within PWD limit
Propagation Delay Skew[1]	t_{PSK}			10	ns	
Channel Matching						
Codirectional	t_{PSKCD}			10	ns	
Opposing Direction	t_{PSKOD}			30	ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						2 Mbps, no load
ADuM1240/ADuM1245	I_{DD1}		312	400	μA	
	I_{DD2}		168	250	μA	
ADuM1241/ADuM1246	I_{DD1}		240	375	μA	
	I_{DD2}		240	375	μA	

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 V_{DDx}[1]			V	
Logic Low	V_{IL}			0.3 V_{DDx}[1]	V	
Output Voltages						
Logic High	V_{OH}	V_{DDx}[1] − 0.1	2.5		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDx}[1] − 0.4	2.35		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.1	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−1	+0.01	+1	μA	0 V ≤ V_{Ix} ≤ V_{DDx}[1]
Input Switching Thresholds						
Positive Threshold Voltage	V_{T+}		1.5		V	
Negative Going Threshold	V_{T-}		1.0		V	
Input Hysteresis	ΔV_T		0.5		V	
Undervoltage Lockout, V_{DD1} or V_{DD2}	UVLO		1.5		V	
Supply Current per Channel						
Quiescent Current						
Input Supply	$I_{DDI (Q)}$		2.6	3.75	μA	EN_X low
Output Supply	$I_{DDO (Q)}$		0.5	3.75	μA	EN_X low
Input (Refresh Off)	$I_{DDI (Q)}$		0.05		μA	EN_X high
Output (Refresh Off)	$I_{DDO (Q)}$		0.05		μA	EN_X high
Dynamic Supply Current						
Input	$I_{DDI (D)}$		76		μA/Mbps	
Output	$I_{DDO (D)}$		41		μA/Mbps	
AC SPECIFICATIONS						
Output Rise Time/Fall Time	t_R/t_F		2		ns	10% to 90%
Common-Mode Transient Immunity[2]	|CM|	25	40		kV/μs	V_{Ix} = V_{DDx}[1], V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		14		kbps	

[1] V_{DDx} = V_{DD1} or V_{DD2}.
[2] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{OUT} > 0.8 V_{DDx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—V_{DD1} = 3.3 V, V_{DD2} = 2.5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, and V_{DD2} = 2.5 V. Minimum/maximum specifications apply over the entire recommended operation range of 3.0 V ≤ V_{DD1} ≤ 3.6 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

For dc specifications and ac specifications, see Table 3 for parameters related to Side 1 operation, and see Table 6 for parameters related to Side 2 operation.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				2	Mbps	Within PWD limit
Propagation Delay						
Side 1 to Side 2	t_{PHL}, t_{PLH}		84	180	ns	50% input to 50% output
Side 2 to Side 1	t_{PHL}, t_{PLH}		120	180	ns	50% input to 50% output
Change vs. Temperature			280		ps/°C	
Pulse-Width Distortion	PWD			12	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Pulse Width	PW	500			ns	Within PWD limit
Propagation Delay Skew[1]	t_{PSK}			10	ns	
Channel Matching						
Codirectional	t_{PSKCD}			10	ns	
Opposing Direction	t_{PSKOD}			60	ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 8.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						2 Mbps, no load
ADuM1240/ADuM1245	I_{DD1}		366	500	μA	
	I_{DD2}		168	375	μA	
ADuM1241/ADuM1246	I_{DD1}		306	400	μA	
	I_{DD2}		240	375	μA	

ELECTRICAL CHARACTERISTICS—V_{DD1} = 2.5 V, V_{DD2} = 3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 2.5 V, and V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range of 2.25 V ≤ V_{DD1} ≤ 2.75 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

For dc specifications and ac specifications, see Table 6 for parameters related to Side 1 operation, and see Table 3 for parameters related to Side 2 operation.

Table 9.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				2	Mbps	Within PWD limit
Propagation Delay						
Side 1 to Side 2	t_{PHL}, t_{PLH}		120	180	ns	50% input to 50% output
Side 2 to Side 1	t_{PHL}, t_{PLH}		84	180	ns	50% input to 50% output
Change vs. Temperature			200		ps/°C	
Pulse-Width Distortion	PWD			12	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Pulse Width	PW	500			ns	Within PWD limit
Propagation Delay Skew[1]	t_{PSK}			10	ns	
Channel Matching						
Codirectional	t_{PSKCD}			10	ns	
Opposing Direction	t_{PSKOD}			60	ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 10.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						2 Mbps, no load
ADuM1240/ADuM1245	I_{DD1}		306	500	μA	
	I_{DD2}		248	375	μA	
ADuM1241/ADuM1246	I_{DD1}		240	375	μA	
	I_{DD2}		306	450	μA	

PACKAGE CHARACTERISTICS

Table 11.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		85		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

Approvals of the ADuM1240/ADuM1241/ADuM1245/ADuM1246 by the organizations listed in Table 12 are pending. See Table 17 and the Absolute Maximum Ratings section for recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 12.

UL (Pending)	CSA (Pending)	VDE (pending)
Recognized under 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2]
Single 3750 V rms isolation voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 265 V rms (374 V peak) maximum working voltage	Reinforced insulation, 849 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL1577, each ADuM1240/ADuM1241/ADuM1245/ADuM1246 is proof tested by applying an insulation test voltage ≥3000 V rms for 1 second (current leakage detection limit = 5 μA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM1240/ADuM1241/ADuM1245/ADuM1246 is proof tested by applying an insulation test voltage ≥1050 V peak for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marked on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 13.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage (RS-20)		3750	V rms	1-minute duration
Minimum External Air Gap (Clearance, RS-20)	L(I01)	5.1	mm min	Measured from input terminals to output terminals, shortest distance through air
Printed Circuit Board (PCB) Clearance	L(PCB)	5.5	mm min	Measured line of sight in the seating plane of the PCB
Minimum External Tracking (Creepage, RS-20)	L(I02)	5.1	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017	mm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation within the safety limit data only. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marked on packages denotes DIN V VDE V 0884-10 approval.

Table 14.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V_{PEAK}
Input-to-Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m$ = 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V_{PEAK}
Input-to-Output Test Voltage, Method a				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, t_{ini} =60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1273	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1018	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	5335	V_{PEAK}
Surge Isolation Voltage	V_{PEAK} = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		T_S	150	°C
Side 1 I_{DD1} Current		I_{S1}	2.5	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

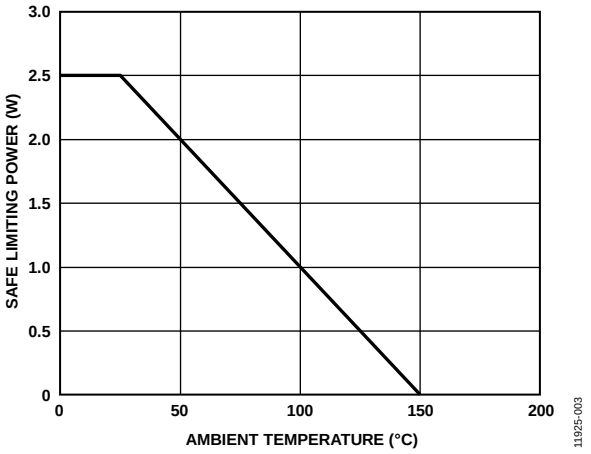


Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 15.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+125	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	2.25	3.6	V
Input Signal Rise and Fall Times			1.0	ms

[1] See the DC Correctness and Low Power Operation section for more information.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 16.

Parameter	Rating
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})	−0.5 V to +5 V
Input Voltages (V_{IA}, V_{IB})	−0.5 V to V_{DDI} + 0.5 V
Output Voltages (V_{OA}, V_{OB})	−0.5 V to V_{DD2} + 0.5 V
Average Output Current per Pin[1]	
Side 1 (I_{O1})	−10 mA to +10 mA
Side 2 (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[2]	−100 kV/µs to +100 kV/µs

[1] See Figure 3 for maximum rated current values for various temperatures.
[2] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

CONTINUOUS WORKING VOLTAGE

Table 17. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage			
Bipolar Waveform	565	V peak	50-year minimum lifetime
Unipolar Waveform	1131	V peak	50-year minimum lifetime
DC Voltage	1131	V peak	50-year minimum lifetime

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

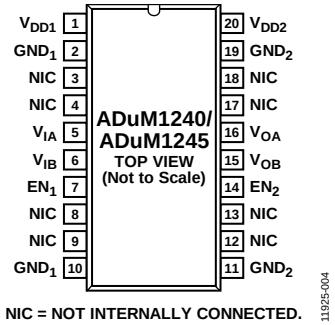


Figure 4. ADuM1240/ADuM1245 Pin Configuration

Table 18. ADuM1240/ADuM1245 Pin Function Descriptions[1]

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1 (2.25 V to 3.6 V). Connect a ceramic bypass capacitor in the range of 0.01 µF to 0.1 µF between V_{DD1} (Pin 1) and GND_1 (Pin 2).
2	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both to GND_1 is recommended.
3	NIC	Not Internally Connected. Leave this pin floating.
4	NIC	Not Internally Connected. Leave this pin floating.
5	V_{IA}	Logic Input A.
6	V_{IB}	Logic Input B.
7	EN_1	Refresh/Watchdog Enable 1. Connecting Pin 7 to GND_1 enables the input/output refresh and watchdog functionality for Side 1, supporting standard *i*Coupler operation. Tying Pin 7 to V_{DD1} disables the refresh and watchdog functionality for the lowest power operation, see the DC Correctness and Low Power Operation section for a description of this mode. EN_1 and EN_2 must be set to the same logic state
8	NIC	Not Internally Connected. Leave this pin floating.
9	NIC	Not Internally Connected. Leave this pin floating.
10	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both to GND_1 is recommended.
11	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both to GND_2 is recommended.
12	NIC	Not Internally Connected. Leave this pin floating.
13	NIC	Not Internally Connected. Leave this pin floating.
14	EN_2	Refresh/Watchdog Enable 2. Connecting Pin 14 to GND_2 enables the input/output refresh and watchdog functionality for Side 2, supporting standard *i*Coupler operation. Tying Pin 14 to V_{DD2} disables the refresh and watchdog functionality for lowest power operation, see the DC Correctness and Low Power Operation section for a description of this mode. EN1 and EN2 must be set to the same logic state.
15	V_{OB}	Logic Output B.
16	V_{OA}	Logic Output A.
17	NIC	Not Internally Connected. Leave this pin floating.
18	NIC	Not Internally Connected. Leave this pin floating.
19	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both to GND_2 is recommended.
20	V_{DD2}	Supply Voltage for Isolator Side 2 (2.25 V to 3.6 V). Connect a ceramic bypass capacitor in the range of 0.01 µF to 0.1 µF between V_{DD2} (Pin 20) and GND_2 (Pin19).

[1] Reference AN-1109 for specific layout guidelines.

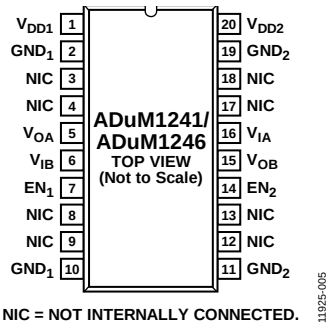


Figure 5. ADuM1241/ADuM1246 Pin Configuration

Table 19. ADuM1241/ADuM1246 Pin Function Descriptions[1]

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1 (2.25 V to 3.6 V). Connect a ceramic bypass capacitor in the range of 0.01 µF to 0.1 µF between V_{DD1} (Pin 1) and GND_1 (Pin 2).
2	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both to GND_1 is recommended.
3	NIC	Not Internally Connected. Leave this pin floating.
4	NIC	Not Internally Connected. Leave this pin floating.
5	V_{OA}	Logic Output A.
6	V_{IB}	Logic Input B.
7	EN_1	Refresh/Watchdog Enable 1. Connecting Pin 7 to GND_1 enables the input/output refresh and watchdog functionality for Side 1, supporting standard *i*Coupler operation. Tying Pin 7 to V_{DD1} disables the refresh and watchdog functionality for lowest power operation, see the DC Correctness and Low Power Operation section for a description of this mode. EN_1 and EN_2 must be set to the same logic state.
8	NIC	Not Internally Connected. Leave this pin floating.
9	NIC	Not Internally Connected. Leave this pin floating.
10	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both to GND_1 is recommended.
11	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both to GND_2 is recommended.
12	NIC	Not Internally Connected. Leave this pin floating.
13	NIC	Not Internally Connected. Leave this pin floating.
14	EN_2	Refresh/Watchdog Enable 2. Connecting Pin 14 to GND_2 enables the input/output refresh and watchdog functionality for Side 2, supporting standard *i*Coupler operation. Tying Pin 14 to V_{DD2} disables the refresh and watchdog functionality for lowest power operation, see the DC Correctness and Low Power Operation section for a description of this mode. EN1 and EN_2 must be set to the same logic state.
15	V_{OB}	Logic Output B.
16	V_{IA}	Logic Input A.
17	NIC	Not Internally Connected. Leave this pin floating.
18	NIC	Not Internally Connected. Leave this pin floating.
19	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both to GND_2 is recommended.
20	V_{DD2}	Supply Voltage for Isolator Side 2 (2.25 V to 3.6 V). Connect a ceramic bypass capacitor in the range of 0.01 µF to 0.1 µF between V_{DD2} (Pin 20) and GND_2 (Pin 19).

[1] Reference AN-1109 for specific layout guidelines.

TRUTH TABLES

Table 21 provides the truth table (positive logic) for the ADuM1240 and the ADuM1241, and Table 22 provides the truth table (positive logic) for the ADuM1245 and ADuM1246. For a description of the abbreviations used in the truth tables, see Table 20.

Table 20. Truth Table Abbreviations

Letter	Description
H	High level
L	Low level
↑	Rising data transition
↓	Falling data transition
X	Irrelevant
Q_O	Level of V_{Ox} prior to levels being established
Z	High impedance

Table 21. ADuM1240/ADuM1241 Truth Table (Positive Logic)

V_{Ix} Input[1]	V_{DDI} State[2]	V_{DDO} State[3]	EN_x State	V_{Ox} Output[1]	Description
H	Powered	Powered	L	H	Normal operation; data is high and refresh is enabled.
L	Powered	Powered	L	L	Normal operation; data is low and refresh is enabled.
X	Unpowered	Powered	L	H	Input unpowered. Outputs are in the default high state. Outputs return to the input state within 34 µs of V_{DDI} power restoration. See the pin function descriptions (Table 18 and Table 19) for details.
X	Unpowered	Powered	H	Q_O	Input unpowered. Outputs are static at the level last sent from the input or at the power up level. See the pin function descriptions (Table 18 and Table 19) for details.
↑	Powered	Powered	H	H	Output is high after propagation delay, refresh is disabled.
↓	Powered	Powered	H	L	Output is low after propagation delay, refresh is disabled.
X	Powered	Unpowered	X	Z	Output unpowered. Output pins are in high impedance state. Outputs return to the input state within 70 µs of V_{DDO} power restoration. See the pin function descriptions (Table 18 and Table 19) for details.

[1] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D).
[2] V_{DDI} refers to the power supply on the input side of a given channel (A, B, C, or D).
[3] V_{DDO} refers to the power supply on the output side of a given channel (A, B, C, or D).

Table 22. ADuM1245/ADuM1246 Truth Table (Positive Logic)

V_{Ix} Input[1]	V_{DDI} State[2]	V_{DDO} State[3]	EN_x State	V_{Ox} Output[1]	Description
H	Powered	Powered	L	H	Normal operation; data is high and refresh is enabled.
L	Powered	Powered	L	L	Normal operation; data is low and refresh is enabled.
X	Unpowered	Powered	L	L	Input unpowered. Outputs are in the default low state. Outputs return to the input state within 34 µs of V_{DDI} power restoration. See the pin function descriptions (Table 18 and Table 19) for details.
X	Unpowered	Powered	H	Q_O	Input unpowered. Outputs are static at the level last sent from the input or at the power up level. See the pin function descriptions (Table 18 and Table 19) for details.
↑	Powered	Powered	H	H	Output is high, refresh is disabled.
↓	Powered	Powered	H	L	Output is low, refresh is disabled.
X	Powered	Unpowered	X	Z	Output unpowered. Output pins are in high impedance state. Outputs return to input state within 70 µs of V_{DDO} power restoration. See the pin function descriptions (Table 18 and Table 19) for details.

[1] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D).
[2] V_{DDI} refers to the power supply on the input side of a given channel (A, B, C, or D).
[3] V_{DDO} refers to the power supply on the output side of a given channel (A, B, C, or D).

TYPICAL PERFORMANCE CHARACTERISTICS

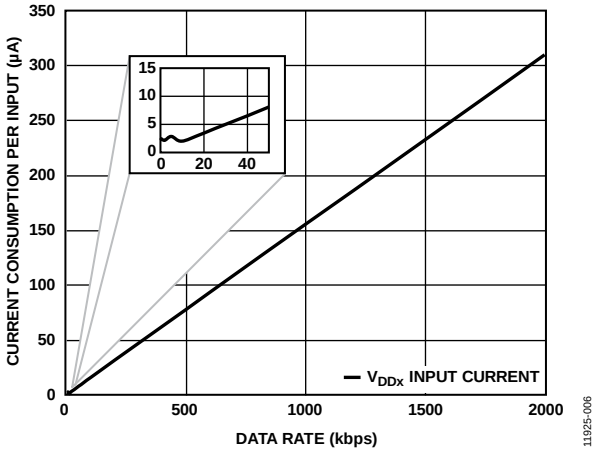


Figure 6. Current Consumption per Input vs. Data Rate for 2.5 V, EN_x = Low Operation

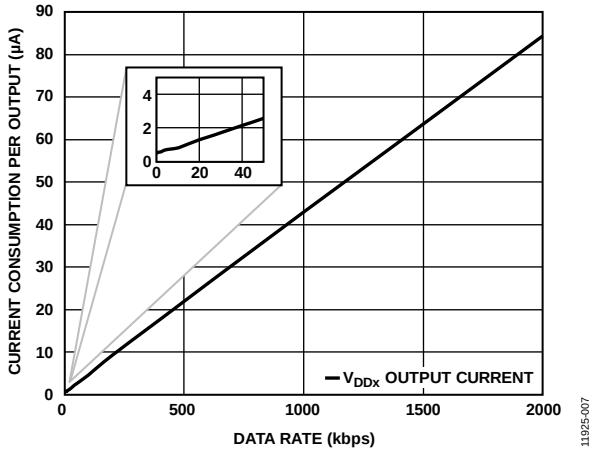


Figure 7. Current Consumption per Output vs. Data Rate for 2.5 V, EN_x = Low Operation

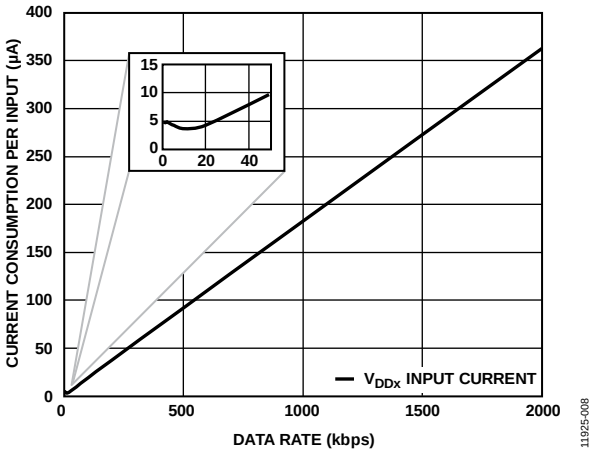


Figure 8. Current Consumption per Input vs. Data Rate for 3.3 V, EN_x = Low Operation

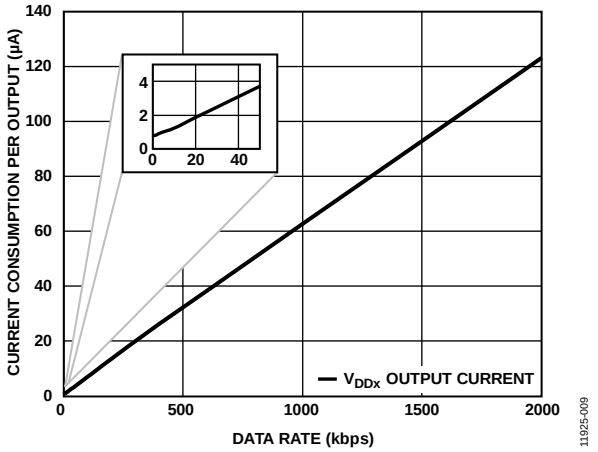


Figure 9. Current Consumption per Output vs. Data Rate for 3.3 V, EN_x = Low Operation

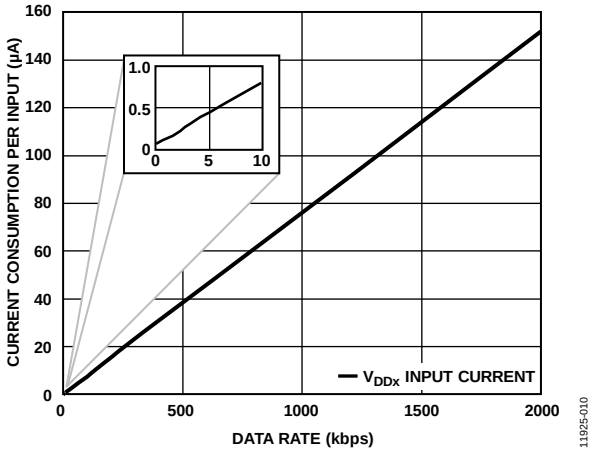


Figure 10. Current Consumption per Input vs. Data Rate for 2.5 V, EN_x = High Operation

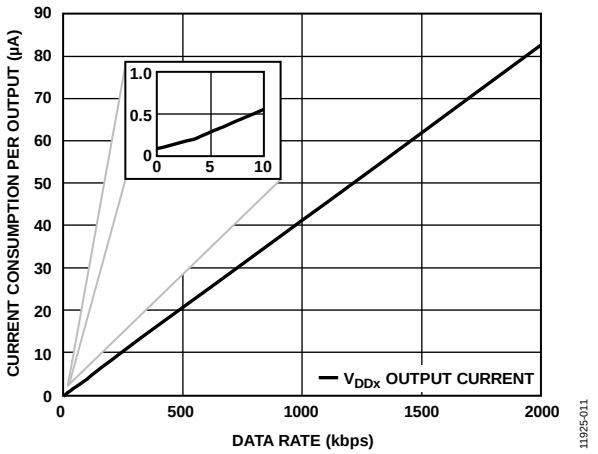


Figure 11. Current Consumption per Output vs. Data Rate for 2.5 V, EN_x = High Operation

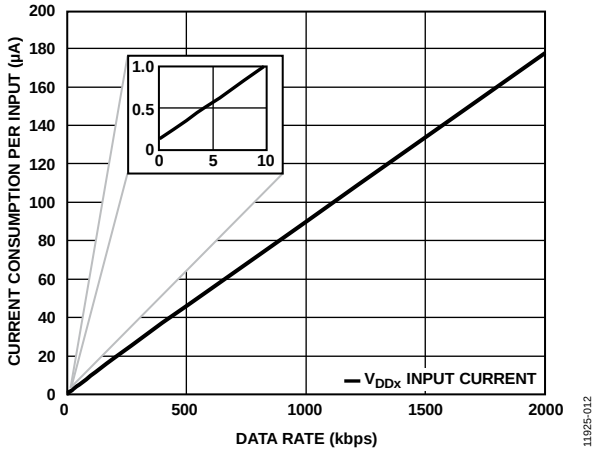


Figure 12. Current Consumption per Input vs. Data Rate for V_{DDx} = 3.3 V, EN_x = High Operation

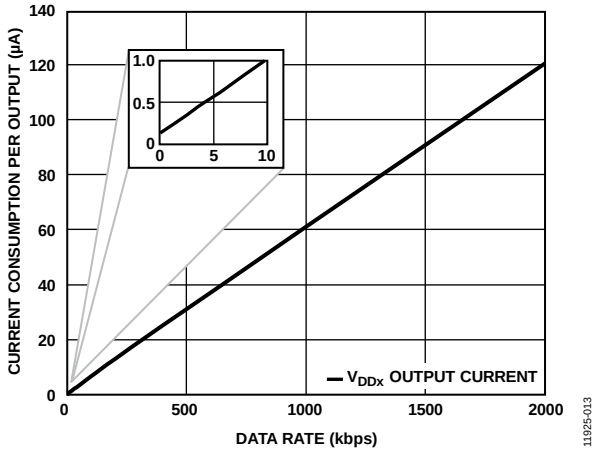


Figure 13. Current Consumption per Output vs. Data Rate for V_{DDx} = 3.3 V, EN_x = High Operation

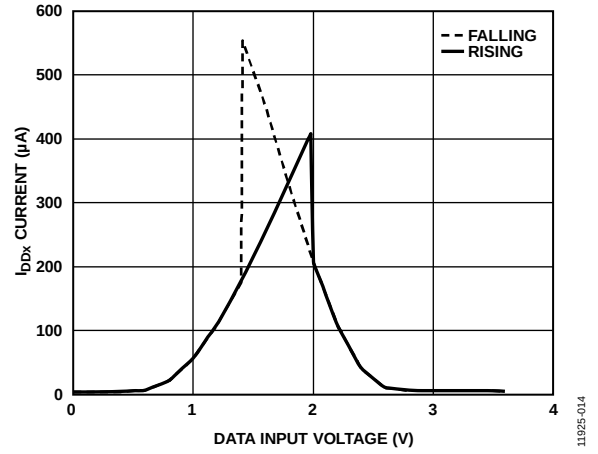


Figure 14. Typical I_{DDx} Current per Input vs. Data Input Voltage for V_{DDx} = 3.3 V

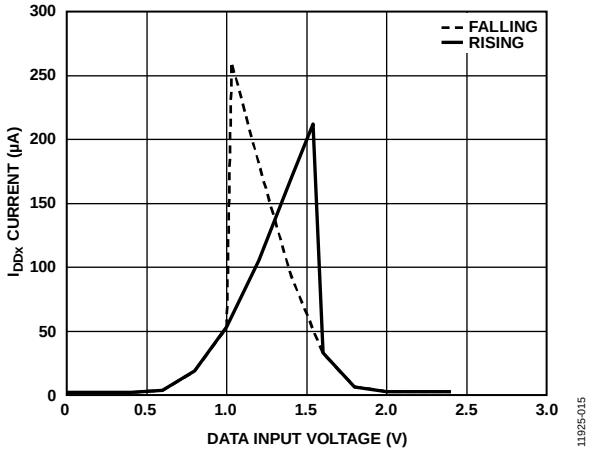


Figure 15. I_{DDx} Current per Input vs. Data Input Voltage for V_{DDx} = 2.5 V

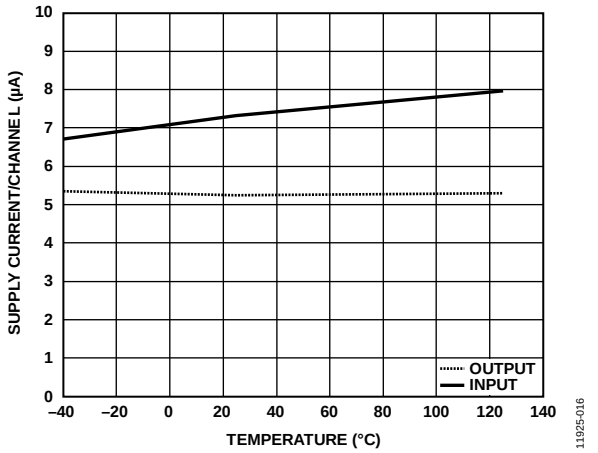


Figure 16. Typical Input and Output Supply Current per Channel vs. Temperature for V_{DDx} = 2.5 V, Data Rate = 100 kbps

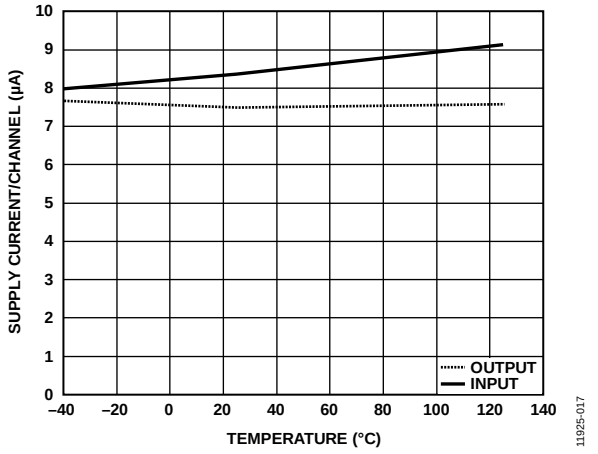


Figure 17. Typical Input and Output Supply Current per Channel vs. Temperature for V_{DDx} = 3.3 V, Data Rate = 100 kbps

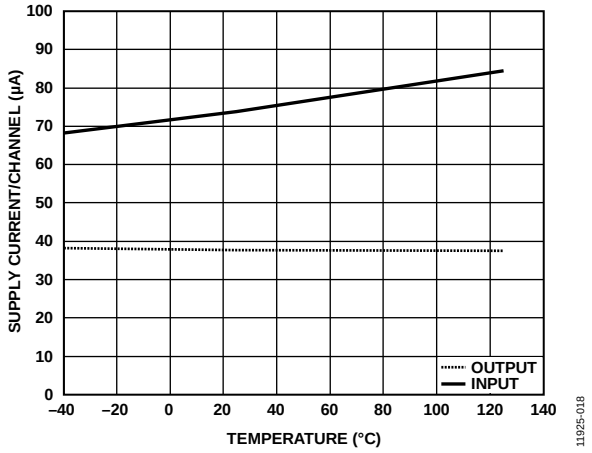


Figure 18. Typical Input and Output Supply Current per Channel vs. Temperature for V_{DDX} = 2.5 V, Data Rate = 1000 kbps

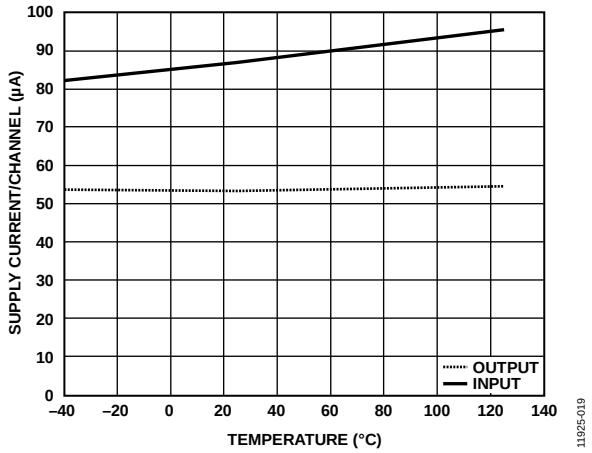


Figure 19. Typical Input and Output Supply Current per Channel vs. Temperature for V_{DDX} = 3.3 V, Data Rate = 1000 kbps

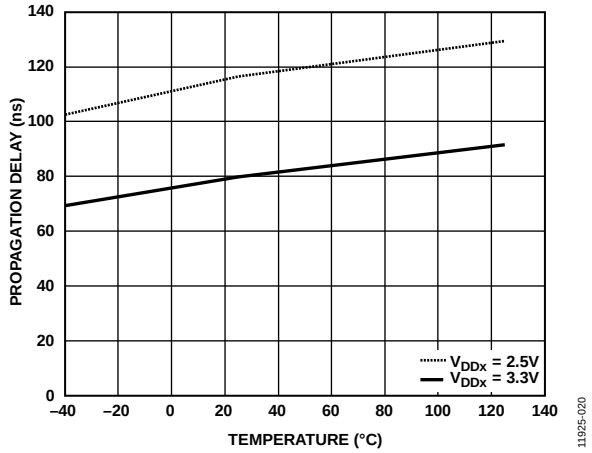


Figure 20. Typical Propagation Delay vs. Temperature for V_{DDx} = 3.3 V or V_{DDx} = 2.5 V

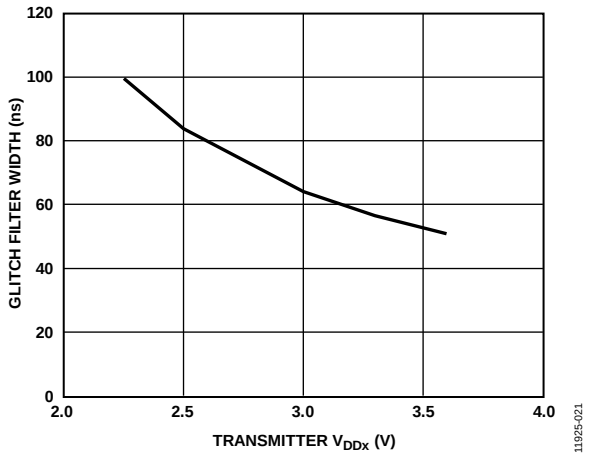


Figure 21. Typical Glitch Filter Operation Threshold

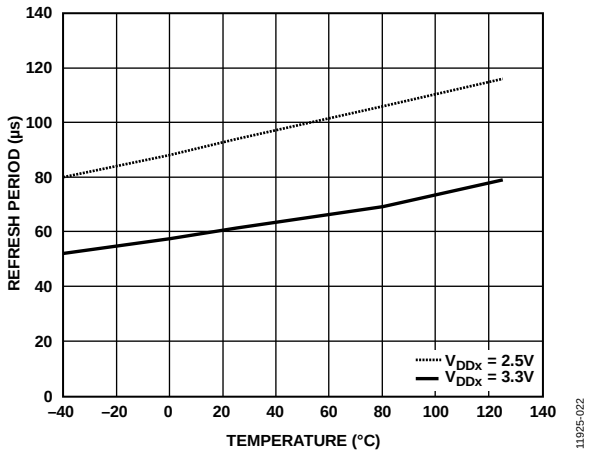


Figure 22. Typical Refresh Period vs. Temperature for 3.3 V and 2.5 V Operation

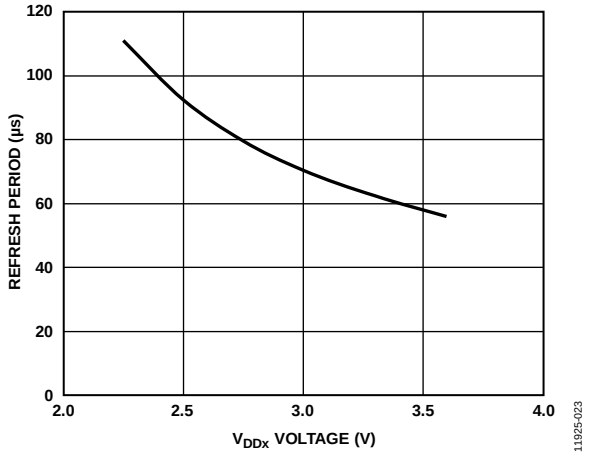


Figure 23. Typical Refresh Period vs. V_{DDx} Voltage

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM1240/ADuM1241/ADuM1245/ADuM1246 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at both the input and output supply pins: V_{DD1} and V_{DD2} (see Figure 24). Maintaining the capacitor value between 0.01 µF and 0.1 µF and not exceeding 20 mm for the total lead length between both ends of the capacitor and the input power supply produce the best results.

With proper PCB design choices, these digital isolators readily meet CISPR 22 Class A (and FCC Class A) emissions standards, as well as the more stringent CISPR 22 Class B (and FCC Class B) standards in an unshielded environment. Refer to AN-1109 for PCB related EMI mitigation techniques, including board layout and stack-up issues.

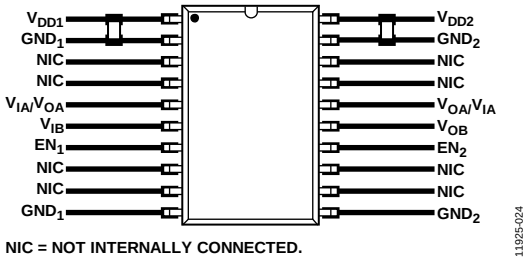


Figure 24. Recommended PCB Layout, RS-20

For applications involving high common-mode transients, it is important to minimize board coupling across the isolation barrier. Furthermore, design the board layout so that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The input-to-output propagation delay time for a high-to-low transition may differ from the propagation delay time of a low-to-high transition.

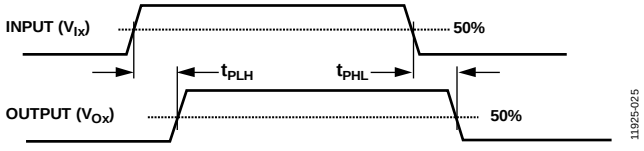


Figure 25. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single component of the ADuM1240/ADuM1241/ADuM1245/ADuM1246.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM1240/ADuM1241/ADuM1245/ADuM1246 components operating under the same conditions.

DC CORRECTNESS AND LOW POWER OPERATION

Standard Operating Mode

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder using the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. When refresh and watchdog functions are enabled by pulling EN_1 and EN_2 low, in the absence of logic transitions at the input for more than ~140 µs, a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than approximately 200 µs, the device assumes that the input side is unpowered or nonfunctional, in which case, the isolator watchdog circuit forces the output to a default state. The default state is either high, as in the ADuM1240, and ADuM1241 versions, or low, as in the ADuM1245 and ADuM1246 versions.

Low Power Operating Mode

For the lowest power consumption, disable the refresh and watchdog functions of the ADuM1240/ADuM1241/ADuM1245/ADuM1246 by pulling EN_1 and EN_2 to logic high. These control pins must be set to the same value on each side of the component for proper operation.

In this mode, the current consumption of the chip drops to the microampere range. However, be careful when using this mode because dc correctness is no longer guaranteed at start up. For example, if the following sequence of events occurs:

1. Power is applied to Side 1.
2. A high level is asserted on the V_{IA} input.
3. Power is applied to Side 2.

The high on V_{IA} is not automatically transferred to the Side 2 V_{OA}, and there can be a level mismatch that is not corrected until a transition occurs at V_{IA}. After power is stable on each side and a transition occurs on the input of the channel, the input and output state of that channel is correctly matched. This contingency can be addressed in several ways, such as sending dummy data, or toggling refresh on for a short period to force synchronization after turn on.

Recommended Input Voltage for Low Power Operation

The ADuM1240/ADuM1241/ADuM1245/ADuM1246 implement Schmitt trigger input buffers so that the devices operate cleanly in low data rate or in noisy environments. Schmitt triggers allow a small amount of shoot through current when their input voltage is not approximate to either V_{DDx} or GND_x levels. This is because the two transistors are both slightly on when input voltages are in the middle of the supply range. For many digital devices, this leakage is not a large portion of

the total supply current and may not be noticed; however, in the ultralow power ADuM1240/ADuM1241/ADuM1245/ADuM1246, this leakage can be larger than the total operating current of the device and cannot be ignored.

To achieve optimum power consumption with the ADuM1240/ADuM1241/ADuM1245/ADuM1246, always drive the inputs as near to V_{DDx} or GND_x levels as possible. Figure 14 and Figure 15 illustrate the shoot through leakage of an input; therefore, whereas the logic thresholds of the input are standard CMOS levels, optimum power performance is achieved when the input logic levels are driven within 0.5 V of either V_{DDx} or GND_x levels.

MAGNETIC FIELD IMMUNITY

The limitation on the magnetic field immunity of the device is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines such conditions. The ADuM1240 is examined in a 3 V operating condition because it represents the typical mode of operation for these products.

The pulses at the transformer output have an amplitude greater than 1.5 V. The decoder has a sensing threshold of about 1.0 V, therefore establishing a 0.5 V margin in which induced voltages are tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\pi r_n^2; n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density.
r_n is the radius of the n^{th} turn in the receiving coil.
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM1240 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 26.

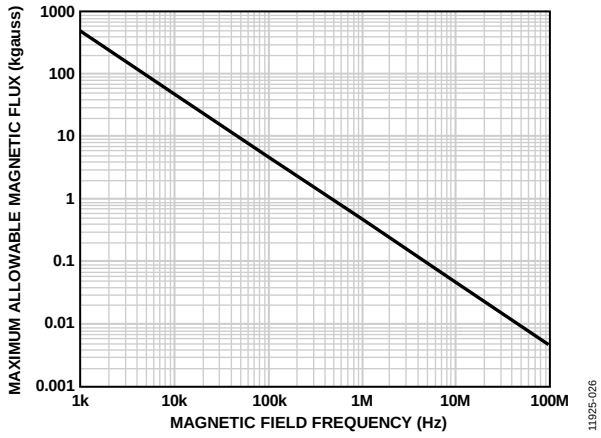


Figure 26. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.5 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. If such an event occurs, with the worst-case polarity, during a transmitted pulse, it would reduce the received pulse from >1.0 V to 0.75 V. This is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM1240 transformers. Figure 27 expresses these allowable current magnitudes as a function of frequency for selected distances. The ADuM1240 is very insensitive to external fields. Only extremely large, high frequency currents, very close to the component could potentially be a concern. For the 1 MHz example noted, one would have to place a 1.2 kA current 5 mm away from the ADuM1240 to affect component operation.

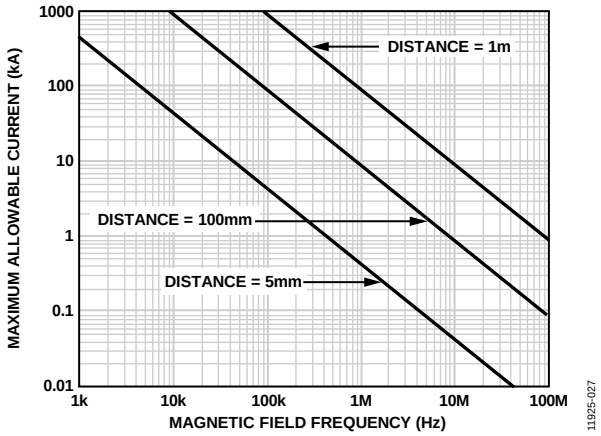


Figure 27. Maximum Allowable Current for Various Current to ADuM1240 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by PCB traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Take care to avoid PCB structures that form loops.

POWER CONSUMPTION

The supply current with refresh enabled at a given channel of the ADuM1240/ADuM1241/ADuM1245/ADuM1246 isolators is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \le 0.5\,f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5\,f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \le 0.5\,f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f > 0.5\,f_r$$

where:
$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
C_L is the output load capacitance (pF).
V_{DDO} is the output supply voltage (V).
f is the input logic signal frequency (MHz); it is half the input data rate, expressed in units of Mbps.
f_r is the input stage refresh rate (Mbps) = $1/T_r$ (µs).
$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total V_{DD1} and V_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled. Figure 6 through Figure 13 show per channel supply currents as a function of data rate for an unloaded output condition.

INSULATION LIFETIME

All insulation structures eventually degrade when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM1240/ADuM1241/ADuM1245/ADuM1246.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 17 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than 50 year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM1240/ADuM1241/ADuM1245/ADuM1246 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 16, Figure 17, and Figure 18 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 17 can be applied while maintaining the 50-year minimum lifetime provided the voltages conform to either the unipolar ac or dc voltage case. Treat any cross-insulation voltage waveform that does not conform to Figure 29 or Figure 30 as a bipolar ac waveform, and limit its peak voltage to the 50-year lifetime voltage value listed in Table 17.

Note that the voltage presented in Figure 29 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

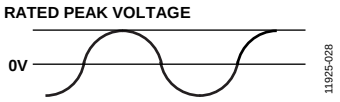


Figure 28. Bipolar AC Waveform

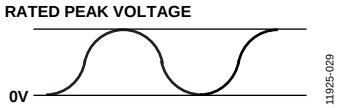


Figure 29. Unipolar AC Waveform

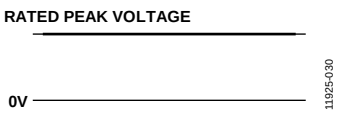
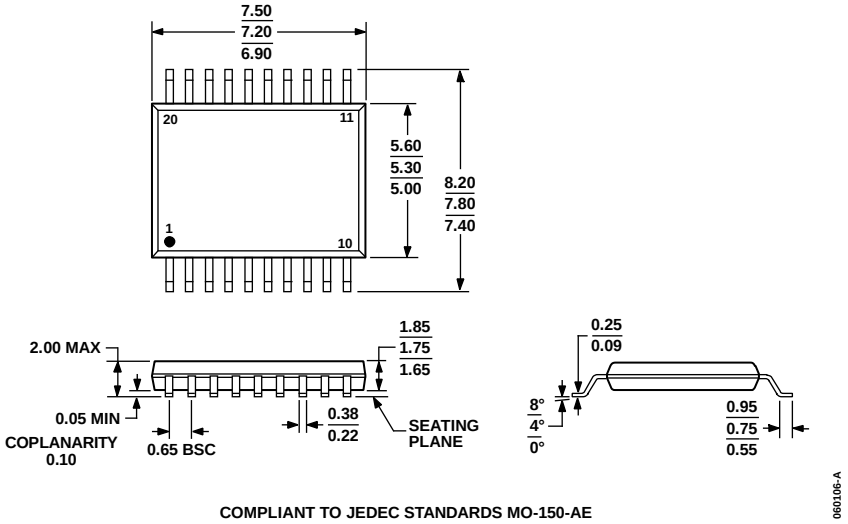


Figure 30. DC Waveform

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-150-AE

Figure 31. 20-Lead Shrink Small Outline Package [SSOP]
(RS-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Max Prop Delay, 3.3 V	Output Default State	Temperature Range	Package Description	Package Option
ADuM1240ARSZ	2	0	2	180	High	−40°C to +125°C	20-Lead SSOP	RS-20
ADuM1240ARSZ-RL7	2	0	2	180	High	−40°C to +125°C	20-Lead SSOP, 7″ Tape and Reel	RS-20
ADuM1241ARSZ	1	1	2	180	High	−40°C to +125°C	20-Lead SSOP	RS-20
ADuM1241ARSZ-RL7	1	1	2	180	High	−40°C to +125°C	20-Lead SSOP, 7″ Tape and Reel	RS-20
ADuM1245ARSZ	2	0	2	180	Low	−40°C to +125°C	20-Lead SSOP	RS-20
ADuM1245ARSZ-RL7	2	0	2	180	Low	−40°C to +125°C	20-Lead SSOP, 7″ Tape and Reel	RS-20
ADuM1246ARSZ	1	1	2	180	Low	−40°C to +125°C	20-Lead SSOP	RS-20
ADuM1246ARSZ-RL7	1	1	2	180	Low	−40°C to +125°C	20-Lead SSOP, 7″ Tape and Reel	RS-20

[1] Z = RoHS Compliant Part.

NOTES