ADSQ-1410

Quad 14-Bit, 10 MSPS Sampling A/D Converter

PRELIMINARY

PRODUCT OVERVIEW

The ADSQ-1410 is a quad 10MSPS sampling A/D optimized for applications where low noise performance and the ability to convert full-scale step input signals at a 10 MHz conversion rate are required. With excellent dynamic performance up to Nyquist frequencies, the ADSQ-1410 is also an ideal choice for multi-channel, frequency domain applications.

This functionally complete quad A/D uses a single rising edge triggered Start Convert signal to control the conversion cycles of all four A/D's. The digital CMOS outputs are multiplexed into pairs providing two parallel, 3-state output buses. Four independent Enable Control pins offer individual output data and overflow/underflow selection.

A 2.5V precision internal reference, along with individual analog input range selection pins, provides ideal tracking over temperature while allowing each channel to be independently configured for an analog input range of ±1V to ±2.5V.

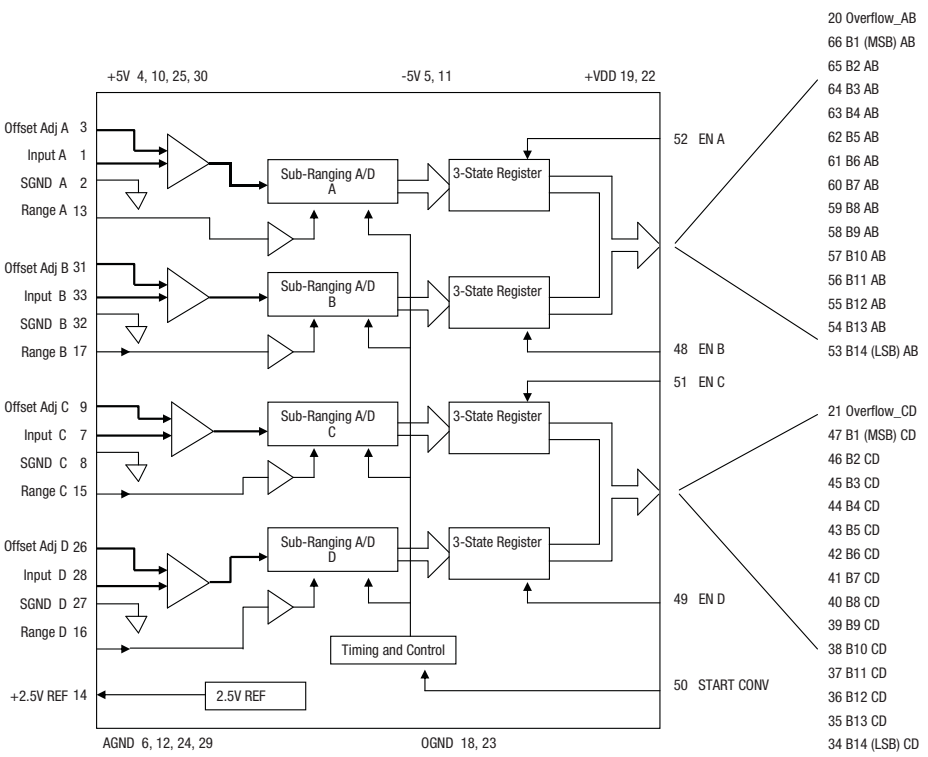
Available in both surface-mount and through-hole packages, the ADSQ-1410 requires only ±5V for internal analog supplies and 2V to 5V supply for logic outputs. Typical power dissipation is 2.7 Watts.

Common applications include medical imaging, radar, sonar, communications and instrumentation.

FEATURES

- Quad 14-bit resolution; 10 MSPS sampling rate
- Individual channel selectable ±1V to ±2.5V input range
- Individual channel offset and gain adjustment capabilities
- Functionally complete; low cost
- Low noise: 0.5 LSB RMS; no missing codes
- Excellent dynamic performance: SNR 80db
- 2V to 5V CMOS logic outputs with overflow/underflow; 3-latency delays
- Rising edge-triggered; Individual channel enable / Hi-z outputs
- ±5V and +2VDD to +5VDD logic output supplies
- 66-pin SMT or TDIP package
- Developed for image processing applications
- Ideal for both time and frequency domain applications

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameters	Min.	Typ.	Max.	Units
+5VA Supply (Pin 4,10,25,30)	0	–	+5.5	Volts
–5VA Supply (Pin 5,11)	0	–	–5.5	Volts
+VDD (Pins 19,22)	0	–	+7V	Volts
Digital Input (Pin 48,49,50,51,52)	–0.3	–	+VDD +0.5	Volts
Analog Input (Pin 1,7,13,15,16,17,28)	–5	–	+5	Volts
Lead Temperature soldering 10sec	–	–	300	°C

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, V_{CC} = +5V, $+V_{DD}$ = +3.3V, V_{EE} = –5V, 10MSPS sampling rate, V_{IN} = ±2.5V and a minimum 1 minute warmup unless otherwise specified.)

Analog Input	Min.	Typ.	Max.	Units
Input Voltage Range	±1	–	±2.5	Volts
Input Impedence	–	470	–	Ω
Input Capacitance	–	2	7	pF
Digital Inputs				
Logic Levels				
Logic 1 START CONV	+2.4	–	$+V_{DD}$	Volts
Logic 1 ENABLE V_{DD} 2V	0.5			Volts
V_{DD} 3.3V	2.1			Volts
V_{DD} 5.0V	1.6			Volts
Logic 0	–	–	+0.8	Volts
Logic Loading				
Logic 1	–	–	+10	uA
Logic 0	–	–	–10	uA
Performance				
Differential Nonlinearity (fin = 975kHz)				
+25°C	–0.99	±0.5	–	LSB
0 to 70°C	–0.99	±0.5	–	LSB
Extended temperature range	TBD	TBD	–	LSB
Integral Nonlinearity				
+25°C	–	±2.5	–	LSB
0 to 70°C	–	±3.0	–	LSB
Extended temperature range	–	TBD	–	LSB
Guaranteed No Missing Codes	0 to 70°C			
Resolution	14 Bits			
Zero Error				
+25°C	–	0.3	–	%FSR
0 to 70°C	–	0.3	–	%FSR
Extended temperature range	–	TBD	–	%FSR
Gain Error				
+25°C	–	0.6	–	%FSR
0 to 70°C	–	TBD	–	%FSR
Extended temperature range	–	TBD	–	%FSR
Output				
Output Coding	Offset Binary			
Logic Level				
Logic 1 (–4mA) $+V_{DD}$ = +3.3V	+2.9	–	–	Volts
Logic 0 (4mA) $+V_{DD}$ = +3.3V	–	–	+0.5	Volts
Logic Loading 1 $+V_{DD}$ = +3.3V	–	–	-4	mA
Logic Loading 0 $+V_{DD}$ = +3.3V	–	–	+4	mA
Internal Reference				
Voltage +25°C	2.495	+2.5	2.505	Volts
0 to 70°C	2.495	+2.5	2.505	Volts
External Current	–	–	5	mA
Dynamic Performance	**Min.**	**Typ.**	**Max.**	**Units**
Total Harmonic Distortion (–0.5dB)				
RANGE pin voltage = 1V				
500kHz	–	-89.5	–	db
1MHz to	–	-88.5	–	db
5MHz	–	-87.6	–	db
RANGE pin voltage = 2.5V				
500kHz	–	-81.3	–	db
1MHz to	–	-81	–	db
5MHz	–	-78	–	db
Signal-to-Noise Ratio (w/o distortion, –0.5dB)				
RANGE pin voltage = 1V				
500kHz	–	74.8	–	db
1MHz to	–	74.8	–	db
5MHz	–	74.6	–	db
RANGE pin voltage = 2.5V				
500kHz	–	80.4	–	db
1MHz to	–	80.2	–	db
5MHz	–	79.6	–	db
Signal-to-Noise Ratio (distortion, –0.5dB)				
RANGE pin voltage = 1V				
500kHz	–	74.6	–	db
1MHz to	–	74.6	–	db
5MHz	–	74.4	–	db
RANGE pin voltage = 2.5V				
500kHz	–	78.2	–	db
1MHz to	–	78	–	db
5MHz	–	77	–	db
Spurious Free Dynamic Range				
RANGE pin voltage = 1V				
500kHz	–	-94.9	–	db
1MHz to	–	-92.1	–	db
5MHz	–	-91.2	–	db
RANGE pin voltage = 2.5V				
500kHz	–	-85.5	–	db
1MHz to	–	-85	–	db
5MHz	–	-80	–	db
Input Bandwidth				
Small Signal (–20dB input)	–	33.5	–	MHz
Large Signal (–3dB input)	–	8.5	–	MHz
Aperture Delay Time	–	1	–	ns
Aperture Uncertainty	–	4	–	ps rms
S/H Acquisition Time, (to ±0.003% FSR)	–	TBD	–	ns
Feedthrough Rejection Channel under test Fin = 4.85MHz Other 3 channels Fin = 2.45MHz	–	-130	–	dB
Noise				
RANGE pin voltage = 1V	–	121	–	µVrms
RANGE pin voltage = 2.5V	–	150	–	µVrms
(grounded input)				
RANGE pin voltage = 1V	–	0.99	–	LSB
RANGE pin voltage = 2.5V	–	0.5	–	LSB

FUNCTIONAL SPECIFICATIONS, CONT.

Power Requirements				
Power Supply Ranges				
+5VEE Supply	+4.75	+5.0	+5.25	Volts
–5VCC Supply	–5.25	–5.0	–4.75	Volts
+VDD Supply	+2V	+3.3	+5V	Volts
Power Supply Currents				
+5V Supply	–	390	430	mA
–5V Supply	–	140	155	mA
+VDD Supply	–	12	20	mA
Power Dissipation	–	2.7	3.1	Watt
Power Supply Rejection (5%) @25°C	–	–	±0.01	%FSR/%V
Environmental				
Operating Temperature Range				
ADSQ-1410	0	–	+70	°C
ADSQ-1410EX	TBD	–	TBD	°C
Storage Temperature	–65	–	+125	°C
Package Type	66-Pin, SMT, TDIP			
Weight	23 grams			
PCB	FR-4 RoHS TG 170°C UL94-VO			
Plastic Shell	Nylon 46, 30% GFR, Stanyl, UL94-VO			
Pins	0.020 Sq. Au Plate Phosphor Bronze			

TECHNICAL NOTES

The ADSQ-1410 is a designed to function as four-independent sampling A/D converters each with a selectable analog input range of ±1 to ±2.5 Volts and with independent offset and gain capabilities. Each channel of the ADSQ-1410 operates from its independent +5V supplies and analog grounds (AGND & SGND). Channels A&B share a common -5V, +VDD and OGND_AB (output ground), similarly channels C&D share -5V, +VDD and OGND_CD. This separation of channels along with strategically placed ground connections within the ADSQ-1410 provide the excellent channel-to-channel isolation performance. For optimal performance PCB layout and high-speed / high resolution design practices should be observed. See Layout Considerations.

RANGE & FINE GAIN ADJUSTMENT:

The ADSQ-1410 allows the full-scale range of each individual channel to be adjusted from 2Vpp to 5Vpp. The ADSQ-1410 provides a precision +2.5V reference voltage that can be used with a resistor divider network to set each channel's desired full-scale range. The voltage applied to each individual RANGE pin will set the full-scale input of that channel to be:

FS = 2 x RANGE pin voltage.

Fine Gain adjustment can be attained with precision changes to the high impedance RANGE pins using a resistor divider network in conjunction with a DAC or adjustable voltage source as shown in the Gain Adjust figure.

Setting the RANGE voltage and providing the proper amount of gain adjustment can be calculated using the following equations as referred to the circuitry shown in the Gain Adjust figure.

The fine gain adjustment range is equivalent to the amount of change induced at the RANGE pin. With the desired Fine Gain Adjustment (as a percent of full scale) and the maximum voltage expected from the Fine Gain Adjust circuitry known, and we select a value for R1 that minimizes the amount of current draw from Vref (typically 1kΩ range), we can then calculate the value for R3 to be:

$$\text{Eq. 1:} \quad R3 = \frac{R1\ Vtrim}{Vref\frac{\%}{100}}$$

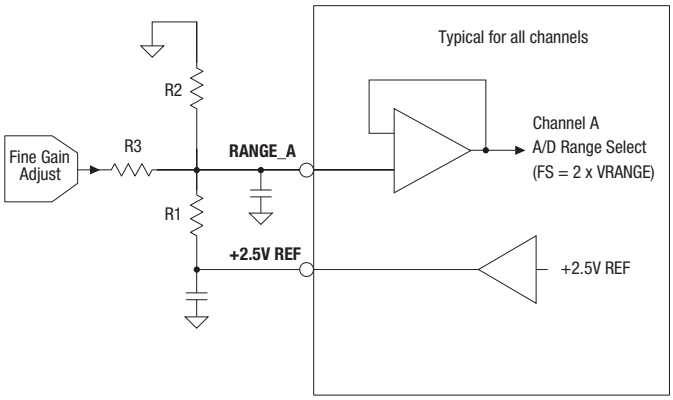
Where: Vtrim = the maximum Fine Gain Adjust voltage
% = the percentage of desired trim range as a % of full scale

Defining RANGE as the unadjusted RANGE pin voltage (R3 tied to GND or Fine Gain Adjust = 0V), we can determine the value of R2 using the following equation:

$$\text{Eq. 2:} \quad R2 = \frac{R1\ R3\ Range}{R3\ Vref - Range\ (R1 + R3)}$$

Where: RANGE is the unadjusted RANGE pin voltage

For example: Using the circuit shown, a ± 1V output DAC is used to adjust the gain of a channel with an analog input range of ±2.0V by ± 5%. Resistor R1 is selected to be 1k Ohm. From Eq. 1: R3 = (1k x 1.0) / (2.0 x 0.05) = 8k Ohm. For an analog input range of ±2.0V the unadjusted RANGE voltage must be +2.0V. From Eq. 2: R2 = (1k x 8k x 2.0) / (8k x 2.5 - 2.0(1k +8k)) = 8k.



ADSQ-1410 Range / Gain Adjust

OFFSET ADJUSTMENT

Offset adjustment is accomplished by applying a ± voltage to the OFFSET ADJ circuitry as seen in the Input Stage figure. Offset adjustment calculations can be determined using the following equations. It should be noted that the factory trims that are required in several of the converter's input stages will slightly alter the tolerance of the offset adjustment calculations. For Eq. 3 the number of desired codes of adjustment are inserted to determine the necessary voltage at the OFFSET ADJ pin. For example with RANGE voltage = 2.5 volts and ±78 codes of adjustment desired corresponds to ±1V at the OFFSET ADJ pin.

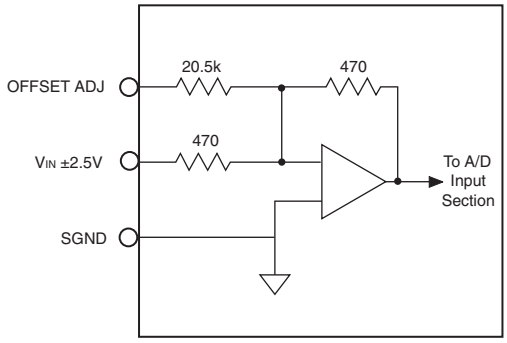
$$\text{Eq. 3:} \quad Voffset = \frac{2\ Range\ (Codes)}{0.0238}$$

Where: RANGE = the RANGE pin voltage
Codes = Desired offset adjustment range

For applications that require small full scale input ranges less sensitivity may be required for offset adjustment. In this case an external series resistor can be added with the internal 20.5kΩ resistor on the OFFSET ADJ pin. In this case the Offset Voltage can be calculated by:

Eq. 4: $$\text{Voffset} = \frac{2 \text{ Range (Codes)}}{\frac{487.9}{(\text{Rexternal} + 20500)}}$$

Where: RANGE = the RANGE pin voltage
Codes = Desired offset adjustment range
Rexternal = External Offset series resistor



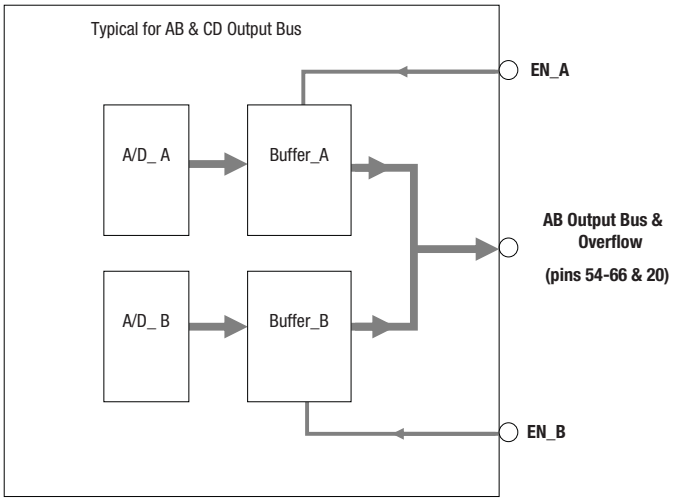
ADSQ-1410 Quad Input Stage

DIGITAL OUTPUT AND TIMING

The ADSQ-1410 is configured such that the output bits and overflow for channels A&B are multiplexed on the AB Output Bus (pins 54 - 66 & 20) and channels C&D are similarly multiplexed on the CD Output Bus (pins 34-47 & 21). See the Output Block Diagram figure. The output drivers are designed to conveniently operate from VDD = +2V to +5V and are capable of sinking and sourcing up to 4mA of current. However, switching large drive currents can cause glitches on the supplies that could couple into and create disturbances on an ongoing A/D conversion affecting the SINAD and SNR performance. Applications where high drive current is required may require additional supply voltage bypassing or external digital buffers.

The EN_ pins are used to select the appropriate output data. EN_ control pins are active LO (HI= high-z). Caution must be exercised to assure that both channels on the same bus are not enabled at the same time. Each data bus of the ADSQ-1410 is capable of providing data throughput at a 20MHz rate. See Enable and Disable timing diagrams and table.

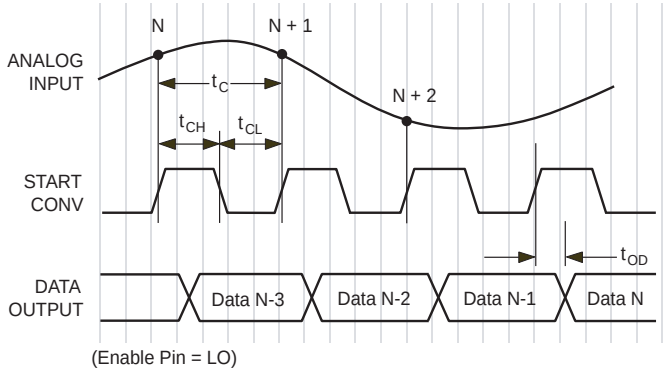
Input logic levels for EN_ pins are dictated by +VDD supply voltage; logic level for START_CONV is a function of +5V supply. See Functional Specifications: Digital Inputs.



Output Block Diagram

Parameter	Symbol	Min	Typ	Max	Unit
Start Conv Period	tc	100		$1x10^6$	ns
Start Conv Pulse High	tch	45			ns
Start Conv Pulse Low	tcl	45			ns
Output Delay	tod	13	18	27	ns

Table 1. Digital Output And Timing

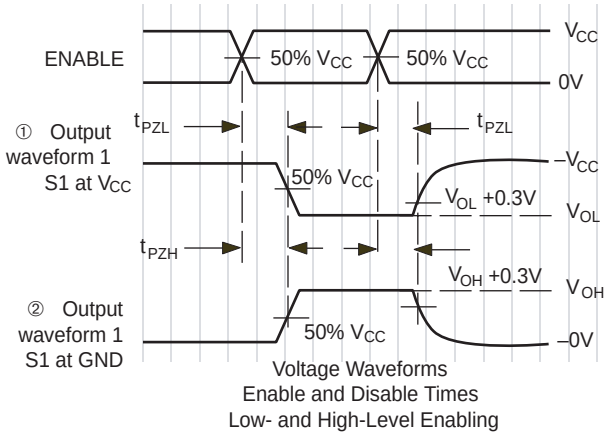


ADSQ-1410 Timing Diagram

Parameter	Symbol	Typ	Max
Hi-Z to Active HI	t-pZH	6.6ns	10.6ns
Hi-Z to Active LO	t-pZL	6.6ns	10.6ns
Active HI to Hi-Z	t-pHZ	7.8ns	11.5ns
Active LO to Hi-Z	t-pLZ	7.8ns	11.5ns

Table 2. Enable and Disable Times

NOTE: Outputs are enabled when ENABLE pins = LO (Hi-Z = HI). Caution must be taken to assure that shared outputs are not enabled at the same time.

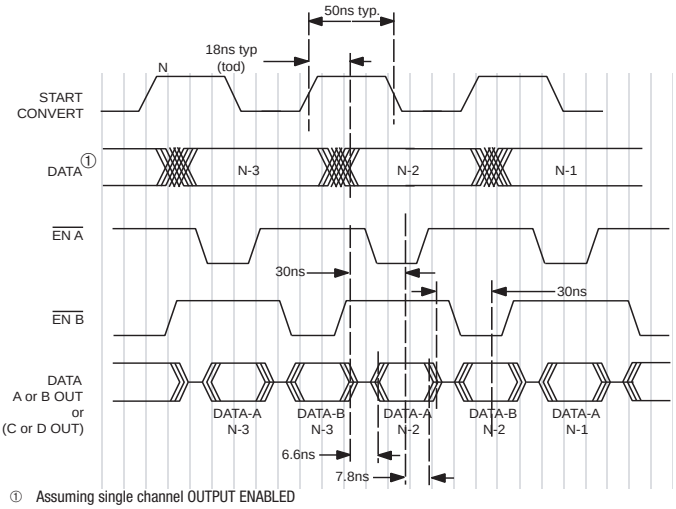


Voltage Waveforms
Enable and Disable Times
Low- and High-Level Enabling

Enable and Disable Times

① Waveform 1 is for an output with internal conditions such that the output is active LO and Hi-Z is pulled 3.3VD through 1k resistor

② Waveform 2 is for an output with internal conditions such that the output is active LO and Hi-Z is pulled GND through 1k resistor



① Assuming single channel OUTPUT ENABLED

Enable Timing Diagram

Overflow	Output Coding MSB LSB	Input Range ±2.5V	Bipolar Scale
1	11 1111 1111 1111	+2.499847	+FS – 1/2LSB
0	11 1111 1111 1111	+2.499695	+FS – 1LSB
0	11 1100 0000 0000	+1.875000	3/4 FS
0	11 0000 0000 0000	+1.250000	+1/2 FS
0	10 0000 0000 0000	±0.000000	0
0	01 0000 0000 0000	–1.250000	–1/2 FS
0	00 1000 0000 0000	–1.875000	–3/4 FS
0	00 0000 0000 0001	–2.499848	–FS +1LSB
0	00 0000 0000 0000	–2.500000	–FS
1	00 0000 0000 0000	–2.500153	–FS –1/2LSB

Table 3. Output Coding

START CONVERT CONSIDERATIONS

The START CONV command of the ADSQ-1410 is buffered internally prior to being distributed to each A/D convert. The multi-stage architecture of the internal A/D's uses both the rising and falling edges of each START CONV pulse in the conversion process and therefore requires START CONV commands that maintain a minimum of 45ns for both the high and the low times. At 10MHz clock rate this would require a 50% (±5%)duty cycle. Due to the analog pipeline architecture of the A/D section a Start Convert period that exceeds 1ms will allow internal sample and holds to discharge the held voltages thereby affecting output integrity. Consequently a minimum Start convert rate of 1 kHz is specified.

Clock jitter (aperture jitter) will result in a variation of time interval between successive A/D conversions which can adversely affect the signal to noise ratio performance. Low jitter crystal oscillators provide clock signals at a 50% duty cycle making ideal START CONV sources. Input logic levels for EN_ pins are dictated by +VDD supply voltage; logic level for START_CONV is a function of +5V supply. See Functional Specifications: Digital Inputs.

LAYOUT CONSIDERATIONS

Although the ADSQ-1410 functions in both the analog and digital realms, in regards to layout it should be treated as an analog component.

Grounding is critical in any high-speed, high resolution data acquisition system. As such a multilayer PCB is recommended to allow ground planes as well as isolation of digital and analog signals. Ground planes will significantly reduce impedance and minimize signal return loops. In addition, the power and ground planes can be arranged so as to provide inherent distributed capacitance within the PCB.

The AGND, SGND and OGND grounds should all be connected to a common ground plane directly beneath the ADSQ-1410. Although using a common plane beneath the A/D, it may be beneficial to design notches or "keep-outs" in the ground plane so as to steer ground currents away from critical signal sensitive areas in the ground plane.

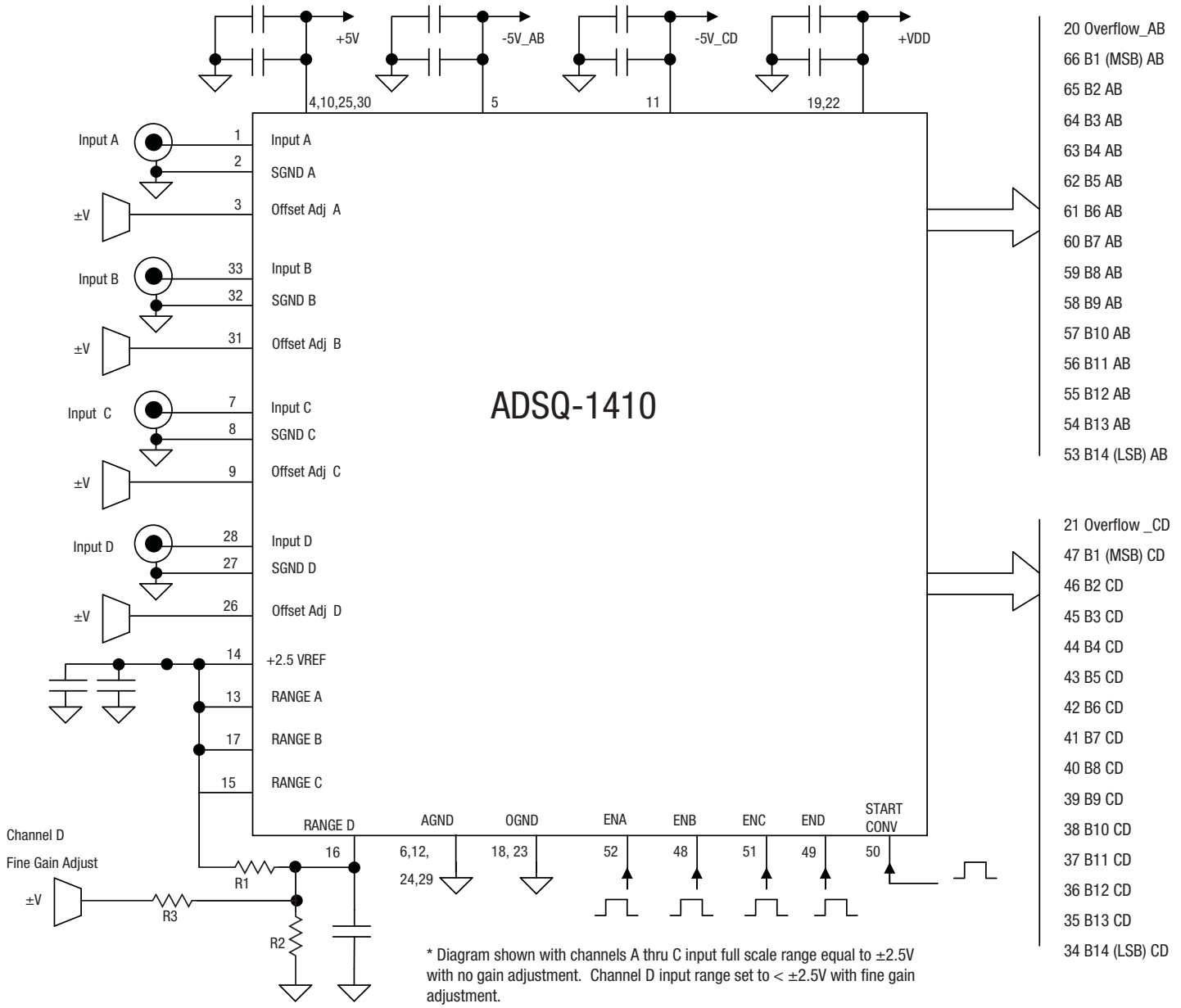
Each channel of the quad A/D operates from its own supply voltages. Bypassing from each of these supplies should be done as close to the respective power and associated ground pins as possible. Bypass ceramic capacitor values of 1uF and 0.1uF are recommended in most application.

In order to prevent digital switching noise from being coupled into sensitive analog signal paths, the layout designer should assure that digital signals do not run parallel with signal traces. For ease of layout the ADSQ-1410 is designed with all Digital Outputs and START CONVERT one side of the package and signal pins on the other.

The +2.5V REF pin is used in conjunction with external components to set the RANGE of each channel. Care should be exercised to assure that the Reference voltage and its associated divided down voltage applied to the RANGE pins are bypassed properly and not subject to noise pickup from digital paths.

TYPICAL APPLICATION CONNECTION DIAGRAM

The ADSQ-1410 is a functionally complete quad A/D and as such requires little externally circuitry for operation. The figure (connection diagram) shows the typical circuit connections with channels A, B, C operating with a ±2.5V input range and channel D operating with a gain adjustable input range less than ±2.5V.



* Diagram shown with channels A thru C input full scale range equal to ±2.5V with no gain adjustment. Channel D input range set to < ±2.5V with fine gain adjustment.

Connection Diagram

PIN FUNCTIONS

Pin Number	Name	Description
1, 7, 28, 33	INPUT (A, C, D, B)	Signal Input for Respective Channel
2, 8, 27, 32	SGND (A, C, D, B)	Signal Ground for Respective Channel
3, 9, 26, 31	OFFSET ADJ (A, C, D, B)	Offset Adjust for Respective Channel
4, 10, 25, 30	+5V (A, C, D, B)	+5V Analog Supply for Respective Channel
5, 11	-5V (A, C, D, B)	-5V Analog Supply for Respective Channel
6, 12, 24, 29	AGND (AB, CD)	Analog Ground for Respective Channel
13	RANGE_A	Channel A Range Adjustment
14	+2.5V REF	+2.5V Reference Output Voltage
15	Range_C	Channel C Range Adjustment
16	Range D	Channel D Range Adjustment
17	Range B	Channel B Range Adjustment
18, 23	OGND_AB	Digital Ground for Respective Channel
19, 22	+VDD (AB, CD)	Output Supply for Respective Channel
34-47	DATA OUT_CD	Data Output Bits for Channels C&D
21	Overflow_CD	Overflow/Underflow for Channels C&D
48	EN_B	Output Enable Channel B
49	EN_D	Output Enable Channel D
50	START CONV	Start Convert for all Channels
51	EN_C	Output Enable Channel C
52	EN_A	Output Enable Channel A
53-66	DATA OUT_AB	Data Output Bits for Channels A&B
20	Overflow_AB	Overflow/Underflow for Channels A&B

Table 3. Pin Function Description

INPUT (A, C, D, B) - Pins 1, 7, 28, 33: Analog Input Signal for respective channels.

SGND (A, C, D, B) - Pins 2, 8, 27, 32: Signal ground for respective channels. SGND connected to AGND and DGND at strategic locations within the ADSQ-1410.

OFFSET ADJ (A, C, D, B) - Pins 3, 9, 26, 31: Provides independent offset adjustment for each channel. Designed for ± voltages applied to OFFSET ADJ pin; leave floating or tied to GND for non-adjustment applications. Applying -1V reduces output by approx. 76 codes; applying +1.0V increases output by approx. 76 codes with RANGE = 2.5V.

+5V (A, C, D, B) - Pins 4, 10, 25, 30: Individual +5V analog supply pins for each channel. Bypass to respective AGND pins with 1uF and 0.1uF ceramic capacitors.

-5V (AB, CD) - Pins 5, 11: Individual -5V analog supply pins for each channel. Bypass to respective AGND pins with 1uF and 0.1uF ceramic capacitors.

AGND (A, C, D, B) - Pins 6, 12, 24, 29: Analog ground (+5V and -5V returns) for respective channels. AGND connected to SGND and DGND at strategic locations within the ADSQ-1410.

RANGE (A, B, C, D) - Pin 13, 15, 16, 17: Used with +2.5V REF to select the respective channel's full scale input range and fine gain adjustment. See Range and Calibration section.

+2.5V REF - Pin 14: Precision +2.5V output voltage used with RANGE to select full scale input range for all channels. See Range and Calibration section. Bypass to AGND Plane.

PIN FUNCTIONS, CONT.

+VDD (AB, CD) - Pins 19, 22: Supply voltage for digital circuitry. Channels AB share common supply pin, channels CD share common supply pin. Bypass to respective OGND pins with 1uF and 0.1uF ceramic capacitors.

OGND (AB, CD) - Pins 18, 23: Output ground (OGND_AB and OGND_CD returns) for associated channels. OGND is connected to AGND and other OGND at strategic locations within the ADSQ-1410.

DATA_OUT_CD – Pins 34 – 47: Digital data from channels C&D are buffered internally, with the capability of selecting between active and High-Z states, and brought out on the DATA_OUT_CD pins. Selection between C or D is controlled by EN_C and EN_D control pins. DATA OUT employs the offset binary coding format and is powered from +VDD_CD supply.

OVERFLOW_CD - Pin 21: Overflow is a digital output that is multiplexed onto the output data bus in the same manner as the data bits and is enabled or inactive (High-Z) along with the corresponding) data outputs (same latency delay via the respective EN control pin. The signal is LO when the data is within the valid input range of the corresponding A/D converter and HI when the input signal is: +FS-1/2LSB <input> -FS-1/2LSB.

EN_C - Pin 51: Control pin for channel C output data. The data output for channel C is buffered internally with the capability to select between active and High-Z states. The channel C data output shares pins with channel D (DATA_OUT_CD). Caution must be exercised to assure that channel C and channel D are not enabled at the same time. A LO enables the corresponding channel's output data; a HI places the channel into a High-Z state.

EN_D - Pin 49: Control pin for channel D output data. The data output for channel D is buffered internally with the capability to select between active and High-Z states. The channel D data output shares pins with channel C (DATA_OUT_CD). Caution must be exercised to assure that channel D and channel C are not enabled at the same time.

DATA_OUT_AB – Pins 53 – 66: Digital data from channels A&B are buffered internally, with the capability of selecting between active and High-Z states, and brought out on the DATA_OUT_AB pins. Selection between A or B is controlled by EN_A and EN_B control pins. DATA OUT employs the offset binary coding format and is powered from +VDD_AB supply. A LO enables the corresponding channel's output data; a HI places the channel into a High-Z state.

OVERFLOW_AB - Pin 20: Overflow is a digital output that is multiplexed onto the output data bus in the same manner as the data bits and is enabled or inactive (High-Z) along with the corresponding) data outputs (same latency delay via the respective EN control pin. The signal is LO when the data is within the valid input range of the corresponding A/D converter and HI when the input signal is: +FS-1/2LSB <input> -FS-1/2LSB.

EN_A - Pin 52: Control pin for channel A output data. The data output for channel A is buffered internally with the capability to select between active and High-Z states. The channel A data output shares pins with channel B (DATA_OUT_AB). Caution must be exercised to assure that channel A and channel B are not enabled at the same time. A LO enables the corresponding channel's output data; a HI places the channel into a High-Z state.

EN_B - Pin 48: Control pin for channel B output data. The data output for channel B is buffered internally with the capability to select between active and High-Z states. The channel B data output shares pins with channel A (DATA_OUT_AB). Caution must be exercised to assure that channel B and channel A are not enabled at the same time. A LO enables the corresponding channel's output data; a HI places the channel into a High-Z state.

SPECIFICATION DEFINITIONS

Total Harmonic Distortion (THD): Ratio of total RMS harmonic power to RMS fundamental power

THD = 10 X log (RMS of all harmonics/RMS of fundamental)

SNR With Distortion (SINAD): Ratio of RMS power present in output, excluding fundamental: to the RMS fundamental power

SINAD = 10 X log (fundamental RMS / RMS of remaining output); expressed in db

SNR without Distortion (SNR): Ratio of RMS power present in output, excluding fundamental and harmonics: to the RMS power of the fundamental

SNR = 10 X log (fundamental RMS / RMS of power present in output, excluding fundamental and harmonics, to the fundamental; expressed in db

Spurious Free Dynamic Range (SFDR): Difference between fundamental peak value and the value of highest spike present in the output (harmonic or spur).

SFRD = Fundamental (dB) – Highest Spur (dB) ; expressed in db

PSSR: Servo-loop is employed applying an input voltage that forces output codes to FS-1LSB. One supply voltage is changed to the specified limits and any change in input voltage recorded. The change in input voltage is divided by the full scale voltage and then divided by percent change in power supplies. The resulting units are % / %.

Zero Error: Servo-loop is employed applying an input voltage that forces output codes to:

Unipolar devices - LSB on half of the time and all other bits off.

Bipolar devices - MSB on, the LSB on half the time and all other bits off.

The input voltage is compared to 0V.
The result is = Input voltage - 0.5 LSB.

Offset Error: Servo-loop is employed applying an input voltage that forces output codes to LSB on half of the time, and all other bits off.

The input voltage is compared to 0V for unipolar devices, and -0.5 X full scale for bipolar devices. The result is this difference - 0.5 LSBs.

Full Scale Absolute Accuracy: Servo-loop is employed applying an input voltage that forces output codes to LSB on half of the time and all other bits on. The input voltage is compared to full scale for unipolar devices, and 0.5 X full scale for bipolar devices. The result is this difference + 1.5 LSBs.

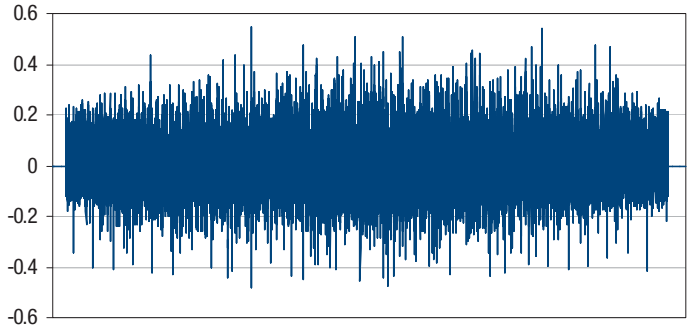
Gain Error: The result is the difference between the Offset Error result and the Full Scale Absolute Accuracy result.

Dynamic DNL Min: An AC signal is input to the device. 2^n x 128 ($2.1e^6$ for 14 bit converter) samples are taken, and the number of times each code appears is recorded. The data is normalized using ideal sine wave values. The result is the most negative and most positive numbers in the array.

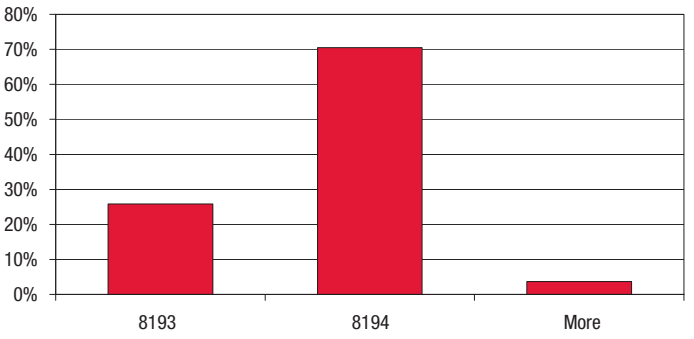
Grounded Input RMS Noise: Input to the device is tied to Signal Ground. 2^n x 128 ($2.1e^6$ for 14 bit converter) samples are taken and stored in an array. The result is the RMS value of this array.

Typical Performance Curves and Plots

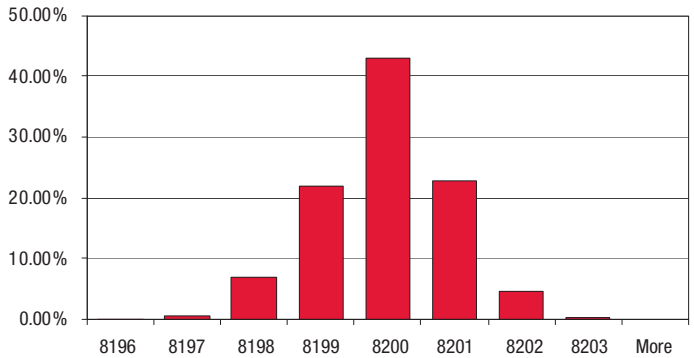
Dynamic DNL
Fs: 4.85 MHz Fs: 10MHz Range Voltage: 2.5V



Grounded Input Histogram 16384 points
RANGE pin = 2.5V

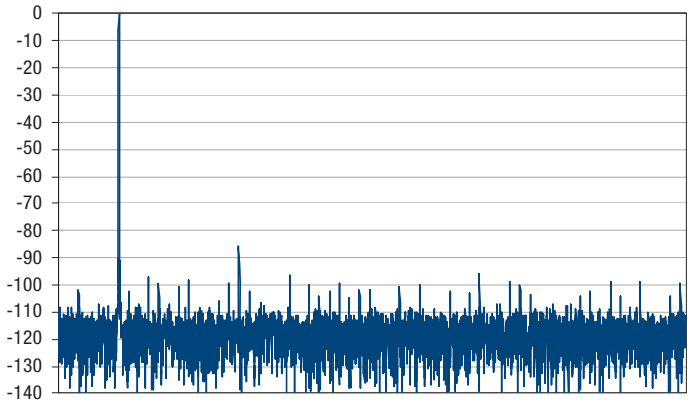


Grounded Input Histogram 16384 points
RANGE pin = 1V

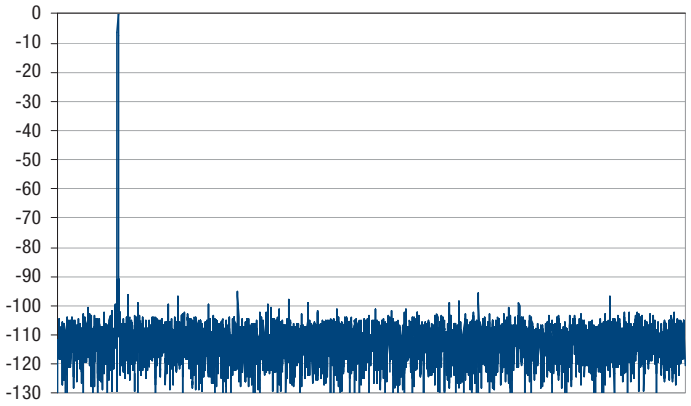


Typical Performance Curves and Plots

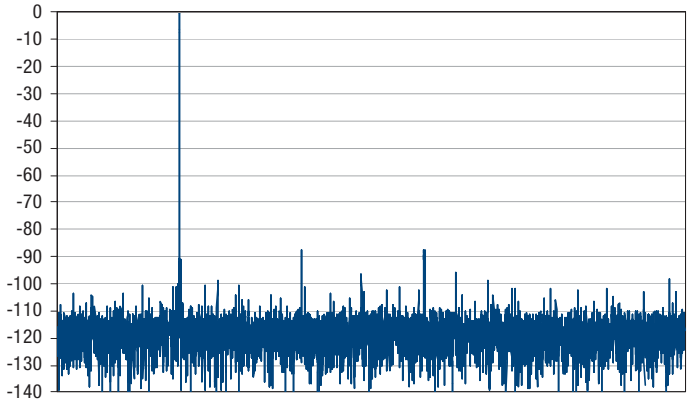
FFT 16384 points
Fs: 480 kHz Fs: 10MHz Range pin voltage: 2.5V



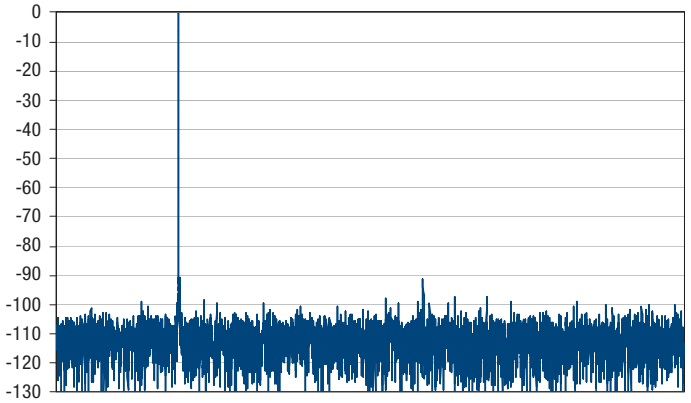
FFT 16384 points
Fs: 480 kHz Fs: 10MHz Range pin voltage: 1V



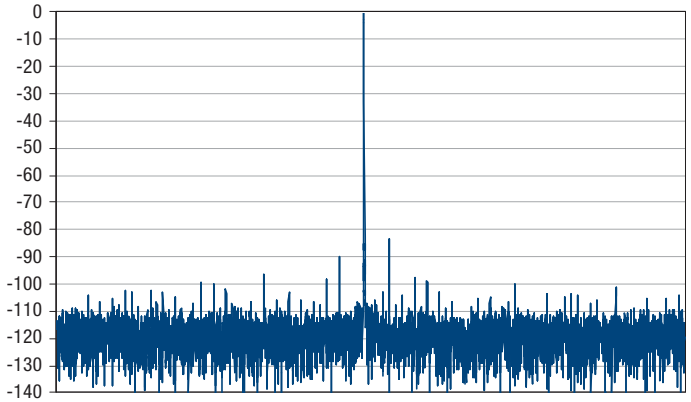
FFT 16384 points
Fs: 975 kHz Fs: 10MHz Range pin voltage: 2.5V



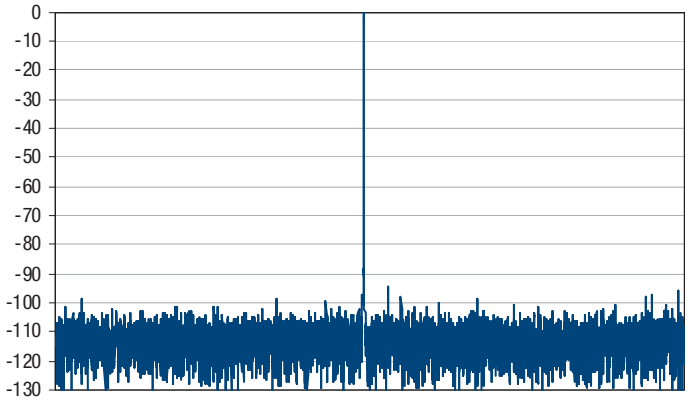
FFT 16384 points
Fs: 975 kHz Fs: 10MHz Range pin voltage: 1V



FFT 16384 points
Fs: 2.45 MHz Fs: 10MHz Range pin voltage: 2.5V

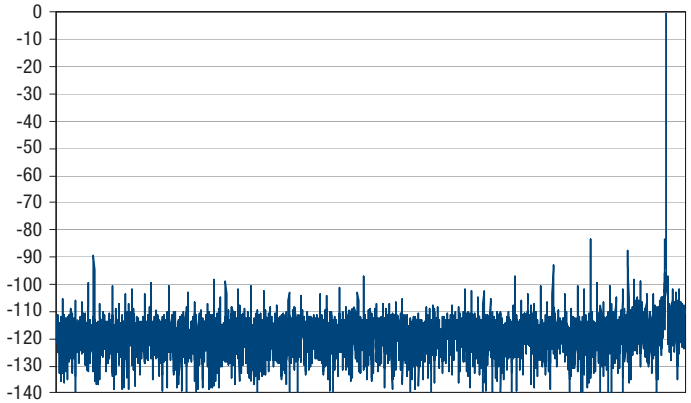


FFT 16384 points
Fs: 2.45 MHz Fs: 10MHz Range pin voltage: 1V

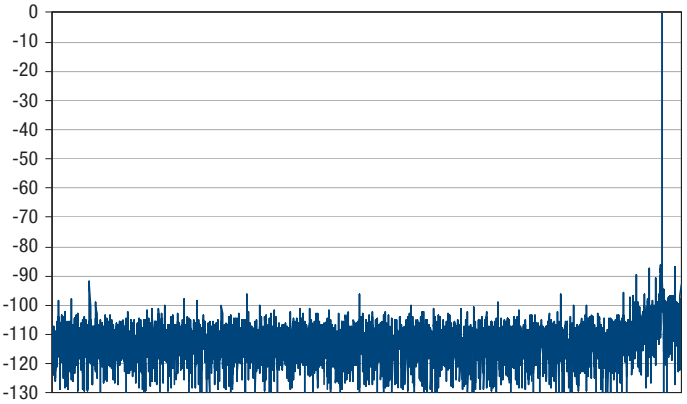


Typical Performance Curves and Plots

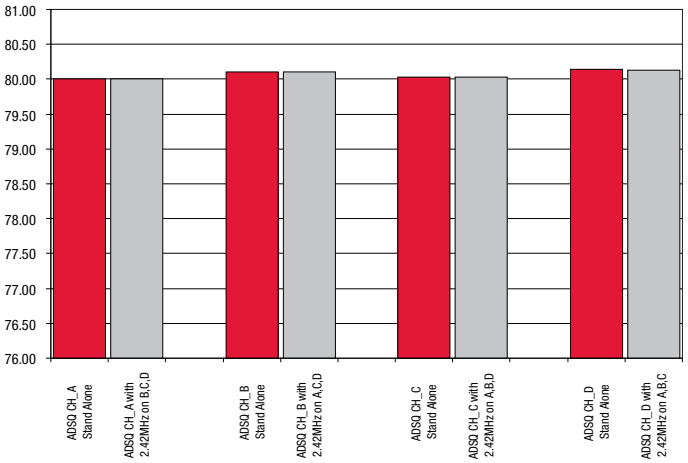
FFT 16384 points
Fs: 4.85 MHz Fs: 10MHz Range pin voltage: 2.5V



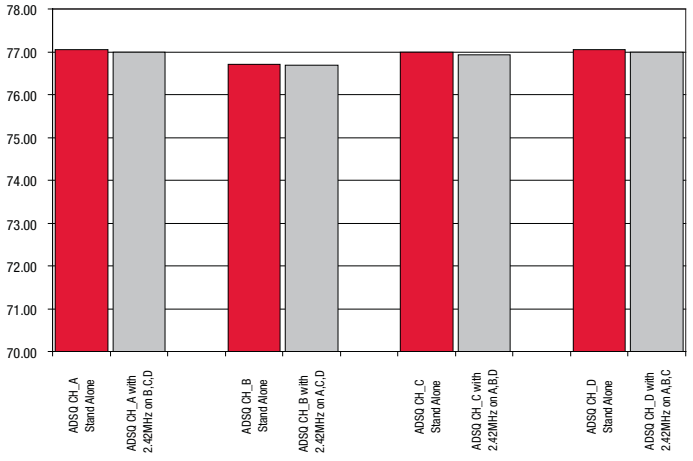
FFT 16384 points
Fs: 4.85 MHz Fs: 10MHz Range pin voltage: 1V



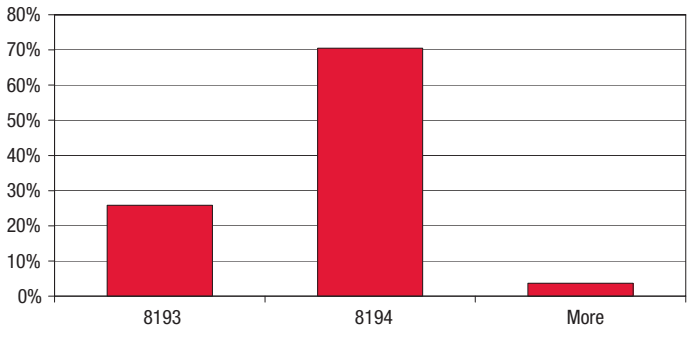
Cross-talk SNR
4.85MHz Input Frequency on Channel under Test
2.42MHz Input Frequency on other 3 Channels



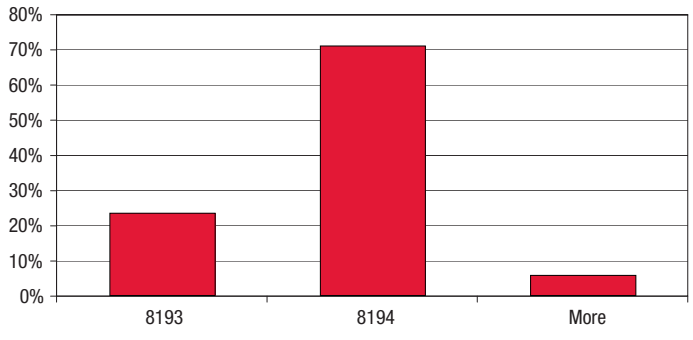
Cross-talk SINAD
4.85MHz Input Frequency on Channel under Test
2.42MHz Input Frequency on other 3 Channels



Cross-talk Grounded Input Histogram
Test channel tied to GND – Other 3 Channels Grounded



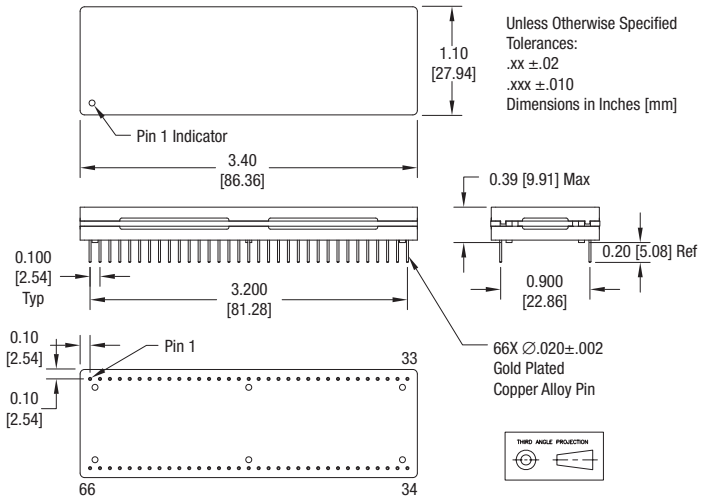
Cross-talk Grounded Input Histogram
Test Channel tied to GND – Other 3 Channels with 2.45 MHz FS Input Signal



INPUT/OUTPUT CONNECTIONS

QUAD INDEPENDENT ADSQ-1410			
PIN	FUNCTION	PIN	FUNCTION
1	INPUT A	66	B1 AB (MSB)
2	SGND A	65	B2 AB
3	OFFSET ADJ A	64	B3 AB
4	+5V A	63	B4 AB
5	–5V A	62	B5 AB
6	AGND A	61	B6 AB
7	INPUT C	60	B7 AB
8	SGND C	59	B8 AB
9	OFFSET ADJ C	58	B9 AB
10	+5V C	57	B10 AB
11	–5V CD	56	B11 AB
12	AGND C	55	B12 AB
13	RANGE A	54	B13 AB
14	+2.5V REF	53	B14 AB (LSB)
15	RANGE C	52	EN A
16	RANGE D	51	EN C
17	RANGE B	50	START CONV
18	OGND_AB	49	EN D
19	+VDD_AB	48	EN B
20	OVERFLOW_AB	47	B1 CD (MSB)
21	OVERFLOW_CD	46	B2 CD
22	+VDD_CD	45	B3 CD
23	OGND_CD	44	B4 CD
24	AGND D	43	B5 CD
25	+5V D	42	B6 CD
26	OFFSET ADJ D	41	B7 CD
27	SGND D	40	B8 CD
28	INPUT D	39	B9 CD
29	AGND B	38	B10 CD
30	+5V B	37	B11 CD
31	OFFSET ADJ B	36	B12 CD
32	SGND B	35	B13 CD
33	INPUT B	34	B14 CD (LSB)

MECHANICAL SPECIFICATIONS



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	PACKAGE	ROHS
ADSQ-1410	0 to +70°C	TDIP	No
ADSQ-1410-C	0 to +70°C	TDIP	Yes
ADSQ-1410-EX	TBD	TDIP	No
ADSQ-1410-EX-C	TBD	TDIP	Yes

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