Synchronous DRAM **4M x 8 Bit x 4 Banks**

General Description

The ADS7608A4A are four-bank Synchronous DRAMs organized as 4,194,304 words x 8 bits x 4 banks.

Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle.

Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth high performance memory system applications

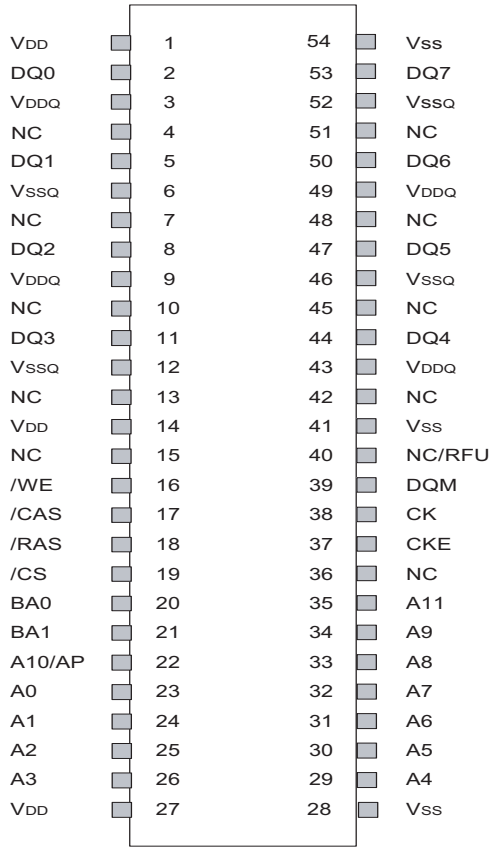
Features

- JEDEC standard LVTTL 3.3V power supply
- MRS Cycle with address key programs
  - -CAS Latency (2 & 3)
  - -Burst Length (1,2,3,8,& full page)
  - -Burst Type (sequential & Interleave)
- 4 banks operation
- All inputs are sampled at the positive edge of the system clock
- Burst Read single write operation
- Auto & Self refresh
- 4096 refresh cycle
- DQM for masking
- Package:54-pins 400 mil TSOP-Type II

Ordering Information.

Part No.	Frequency	Interface	Package
ADS7608A4A-5	200Mhz	LVTTL	400mil 54pin TSOPII
ADS7608A4A-55	183Mhz	LVTTL	400mil 54pin TSOPII
ADS7608A4A-6	166Mhz	LVTTL	400mil 54pin TSOPII
ADS7608A4A-7	143Mhz	LVTTL	400mil 54pin TSOPII
ADS7608A4A-7.5	133Mhz	LVTTL	400mil 54pin TSOPII

Pin Assignment

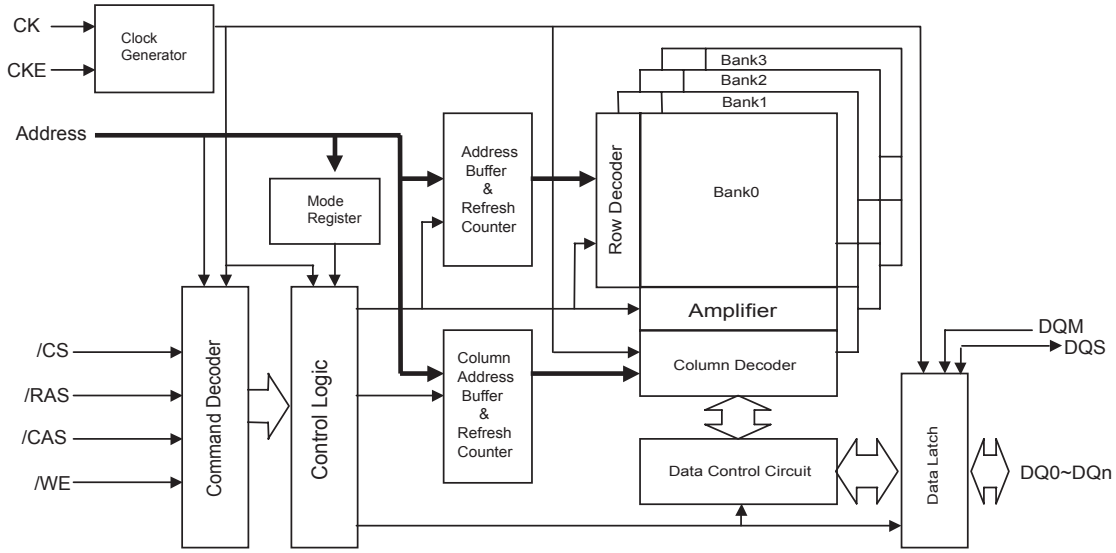


54-pin plastic TSOP II 400 mil

Pin Description

PIN	NAME	FUNCTION
CK	System Clock	Active on the positive edge to sample all inputs.
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least on cycle prior new command. Disable input buffers for power down in standby
/CS	Chip Select	Disables or Enables device operation by masking or enabling all input except CK, CKE and L(U)DQM
A0~A11	Address	Row / Column address are multiplexed on the same pins. Row address : RA0~RA11 Column address : CA0~CA9
BA0~BA1	Banks Select	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
DQ0~DQ7	Data	Data inputs / outputs are multiplexed on the same pins.
L(U)DQM	Data Mask	Makes data output Hi-Z,
/RAS	Row Address Strobe	Latches row addresses on the positive edge of the CLK with /RAS low
/CAS	Column Address Strobe	Latches Column addresses on the positive edge of the CLK with /CAS low
/WE	Write Enable	Enables write operation and row recharge.
VDD/VSS	Power Supply/Ground	Power and Ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	Data Output Power/Ground	Power supply for output buffers.
NC	No Connection	This pin is recommended to be left No Connection on the device.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{out}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATING are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operating Condition

Voltage referenced to Vss = 0V, T_A = 0 to 70 ℃

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH}=-2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL}=2mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max)=4.6V AC for pulse width ≦ 10ns acceptable.

2.V_{IL}(min)=-1.5V AC for pulse width ≦ 10ns acceptable.

3.Any input 0V ≦ V_{IN} ≦ V_{DD} + 0.3V, all other pins are not under test = 0V.

4.Dout is disabled, 0V ≦ V_{OUT} ≦ V_{DD}.

AC Operating Condition

Voltage referenced to Vss = 0V, T_A = 0 to 70 ℃

Parameter	Symbol	Value	Unit	Note
AC input high / low level voltage	V_{IH} / V_{IL}	2.4 / 0.4	V	
Input timing measurement reference level voltage	Vtrip	1.4	V	
Input rise / fall time	TR / tF	1	Ns	
Output timing measurement reference level	Voutfef	1.4	V	
Output load capacitance for access time measurement	CL	50	pF	2

Note: 1. 3.15V ≦ V_{DD} ≦ 3.6V is applied for ADS7608A4A5.

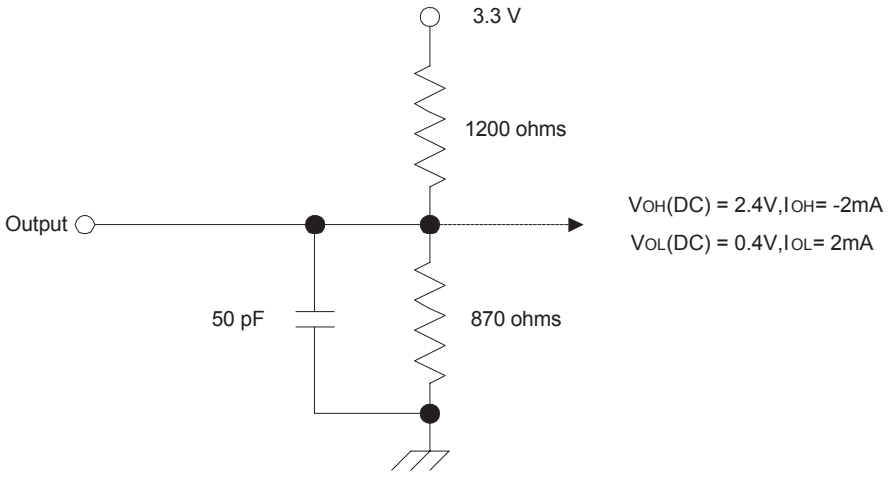
2. Output load to measure access times is equivalent to two TTL gates and one capacitor (30pF). For details, refer to AC/DC output load circuit.

Capacitance

TA=25℃, f-=1Mhz, VDD=3.3V

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CLK	CI1	2.5	4	pF
	A0~A11,BA0,BA1,CKE,/CS,/RAS, /CAS,/WE,DQM	CI2	2.5	5	pF
Data input / output capacitance	DQM	CI/O	4	6.5	pF

Output load circuit



DC Characteristics I

Parameter	Symbol	Min	Max	Unit	Note
Input leakage current	I_{LI}	-1	1	uA	1
Output leakage current	I_{LO}	-1	1	uA	2
Output high voltage	V_{OH}	2.4	-	V	I_{OH} = -4mA
Output low voltage	V_{OL}	-	0.4	V	I_{OL} = 4mA

Note : 1.V_{IN} = 0 TO 3.6V, All other pins are not tested under V_{IN} = 0V.

2.D_{OUT} is disabled, V_{OUT} = 0 to 3.6.

DC Characteristics II

Parameter	Symbol	Test condition	Speed					Unit	Note
			-5	-5.5	-6	-7	-7.5		
Operating Current	IDD1	Burst length=1, One bank active tRC≧tRC(min),I_{OL}=0mA	115	113	110	105	100	mA	1
Precharge standby current in power down mode	IDD2P	CKE≦V_{IL}(max), tCK=min	2					mA	
	IDD2PS	CKE≦V_{IL}(max), tCK=∞	2						
Precharge standby current in Non power down mode	IDD2N	CKE≧V_{IH}(min), /CS≧V_{IH}(min), tCK=min input signals are changed one time during 2clks. All other pins ≧VDD-0.2V or ≦ 0.2V	15					mA	
	IDD2NS	CKE≧V_{IH}(min), tCK=∞ Input signals are stable.	12						
Active standby current in power down mode	IDD3P	CKE≦V_{IL}(max), tCK=min	6					mA	
	IDD3PS	CKE≦V_{IL}(max), tCK=∞	5						
Active standby current in Non power down mode	IDD3N	CKE≧V_{IH}(min), /CS≧V_{IH}(min), tCK=min input signals are changed one time during 2clks. All other pins ≧VDD-0.2V or ≦ 0.2V	30					mA	
	IDD3NS	CKE≧V_{IH}(min), tCK=∞ Input signals are stable.	20						
Burst mode operating current	IDD4	t_{CK}≧t_{CK}(min),I_{OL}=0 mA All banks active	160	160	155	150	150	mA	1
Auto refresh current	IDD5	tRRC≧tRRC(min), All banks active	160					mA	2
Self refresh current	IDD6	CKE≦0.2V	1					mA	

Note: 1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open.

2. Min. of tRRC is shown at AC characteristics.

AC Characteristics

Parameter		Symbol	-5		-5.5		-6		-7		-7.5		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
System clock Cycle time	/CAS Latency = 3	tCK3	5	1000	5.5	1000	6	1000	7	1000	7.5	1000	ns	
	/CAS Latency = 2	tCK2	10		10		10		10		7.5			
Clock high pulse width		tCHW	2	-	2.25	-	2.5	-	2.5	-	2.5	-	ns	1
Clock low pulse width		tCLW	2	-	2.25	-	2.5	-	2.5	-	2.5	-	ns	1
Access time form clock	/CAS Latency = 3	tAC3	-	4.5	-	5	-	5.4	-	5.4	-	5.4	ns	2
	/CAS Latency = 2	tAC2	-	6	-	6	-	6	-	6	-	5.4		
/RAS cycle time	Operation	tRC	55	-	55	-	60	-	62	-	65	-	ns	
	Auto Refresh	tRRC	55	-	55	-	60	-	62	-	65	-		
/RAS to /CAS delay		tRCD	15	-	16.5	-	18	-	20	-	15	-	ns	
/RAS active time		tRAS	40	100K	38.5	100K	42	100K	42	120K	45	120K	ns	
/RAS precharge time		tRP	15	-	16.5	-	18	-	20	-	15	-	ns	
/RAS to /RAS bank active delay		tRRD	10	-	11	-	12	-	14	-	15	-	ns	
/CAS to /CAS delay		tCCD	1	-	1	-	1	-	1	-	1	-	CLK	
Write command to data – in delay		tWTL	0	-	0	-	0	-	0	-	0	-	CLK	
Data – in to precharge command		tDPL	1	-	1	-	1	-	1	-	1	-	CLK	
Data – in active command		tDAL	5	-	5	-	5	-	4	-	4	-	CLK	
DQM to data – out Hi-Z		tDQZ	2	-	2	-	2	-	2	-	2	-	CLK	
DQM to data – in mask		tDQM	0	-	0	-	0	-	0	-	0	-	CLK	
Data – out hold time		tOH	1.5	-	2	-	2.7	-	2.7	-	2.7	-	ns	
Data – input setup time		tDS	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	ns	1
Data – input hold time		tDH	1	-	1	-	1	-	1	-	1	-	ns	1
Address setup time		tAS	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	ns	1
Address hold time		tAH	1	-	1	-	1	-	1	-	1	-	ns	1
CKE setup time		tCKS	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	ns	1
CKE hold time		tCKH	1	-	1	-	1	-	1	-	1	-	ns	1
Command setup time		tCS	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	ns	1
Command hold time		tCH	1	-	1	-	1	-	1	-	1	-	ns	1
CLK to data output in low Z-time		tOLZ	1	-	1	-	1	-	1.5	-	1.5	-	ns	
MRS to new command		tMRD	2	-	2	-	2	-	1	-	1	-	CLK	
Power down exit time		tPDE	1	-	1	-	1	-	1	-	1	-	CLK	
Self refresh exit time		tSRE	1	-	1	-	1	-	1	-	1	-	CLK	3
Refresh time		tREF	64	-	64	-	64	-	64	-	64	-	ms	

Note : 1. Assume tR / tF (input rise and fall time) is 1 ns.

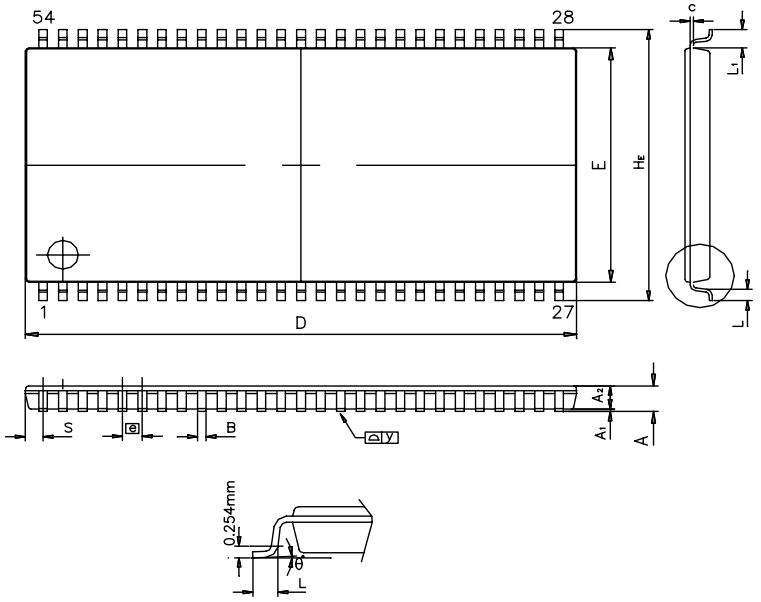
2. Access times to be measured with input signals of 1v / ns edge rate.

3.A new command can be given tRRC after self refresh exit.

Command Truth-Table

Command		CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	ADDR	A10/AP	BA
Mode Register Set		H	X	L	L	L	L	X	OP code		
No Operation		H	X	H	X	X	X	X	X		
				L	H	H	H				
Bank Active		H	X	L	L	H	H	X	RA		V
Read		H	X	L	H	L	H	X	CA	L	V
Read with Auto Precharge										H	
Write		H	X	L	H	L	L	X	CA	L	V
Write with Auto Precharge										H	
Precharge All Bank		H	X	L	L	H	L	X	X	H	X
Precharge select Bank										L	V
Burst Stop		H	X	L	H	H	L	X	X		
DQM		H	X					V	X		
Auto Refresh		H	H	L	L	L	H	X	X		
Self Refresh	Entry	H	L	L	L	L	H	X	X		
	Exit	L	H	H	X	X	X	X			
				L	H	H	H				
Precharge Power down	Entry	H	L	H	X	X	X	X	X		
				L	H	H	H				
	Exit	L	H	H	X	X	X	X			
				L	H	H	H				
Clock Suspend	Entry	H	L	H	X	X	X	X	X		
				L	V	V	V				
	Exit	L	H	X				X	X		

Package Information



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
B	0.30	0.35	0.45	0.012	0.014	0.018
c	0.12		0.21	0.005		0.008
D	22.22 BSC			0.875 BSC		
H_E	11.56	11.76	11.96	0.460	0.463	0.470
E	10.03	10.16	10.29	0.390	0.400	0.410
e	0.80 BSC			0.031		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.80 REF			0.031 REF		
S	0.71 REF			0.028 REF		
θ	0 °	-	8 °	0 °	-	8 °

400mil 54pin TSOP II Package