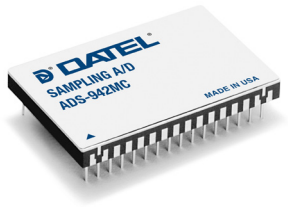
# ADS-942

## 14-Bit, 2MHz Sampling A/D Converters




## PRODUCT OVERVIEW

DATEL's ADS-942 is a functionally complete, 14-bit, 2MHz, sampling A/D converter. Its standard, 32-pin, triple-wide ceramic DIP contains a fast-settling sample/hold amplifier, a 14-bit subranging (two-pass) A/D converter, a precision reference, three-state output register and all the timing and control logic necessary to operate from a single start convert pulse.

The ADS-942 is optimized for wideband frequency-domain applications and is fully FFT tested. The ADS-942 requires ±15V and +5V supplies and typically consumes 1.4 Watts.

## FEATURES

- 14-bit resolution
- 2MHz minimum throughput
- Functionally complete
- Internal reference and sample/hold
- -85dB total harmonic distortion
- 78dB signal-to-noise ratio
- Full Nyquist-rate sampling
- Small 32-pin DIP
- Low-power, 1.7 Watts Max

**INPUT/OUTPUT CONNECTIONS**

| PIN | FUNCTION | PIN | FUNCTION |
|---|---|---|---|
| 1 | +10V REF. OUT | 32 | START CONVERT |
| 2 | BIPOLAR | 31 | BIT 1 OUT ($\overline{\text{MSB}}$) |
| 3 | ANALOG INPUT | 30 | BIT 1 OUT (MSB) |
| 4 | SIGNAL GROUND | 29 | BIT 2 OUT |
| 5 | OFFSET ADJUST | 28 | BIT 3 OUT |
| 6 | ANALOG GROUND | 27 | BIT 4 OUT |
| 7 | NC | 26 | BIT 5 OUT |
| 8 | CODING SELECT | 25 | BIT 6 OUT |
| 9 | $\overline{\text{ENABLE}}$ | 24 | BIT 7 OUT |
| 10 | +5V SUPPLY | 23 | BIT 8 OUT |
| 11 | DIGITAL GROUND | 22 | BIT 9 OUT |
| 12 | +15V SUPPLY | 21 | BIT 10 OUT |
| 13 | –15V SUPPLY | 20 | BIT 11 OUT |
| 14 | ANALOG GROUND | 19 | BIT 12 OUT |
| 15 | ANALOG GROUND | 18 | BIT 13 OUT |
| 16 | $\overline{\text{EOC}}$ | 17 | BIT 14 OUT (LSB) |

## BLOCK DIAGRAM

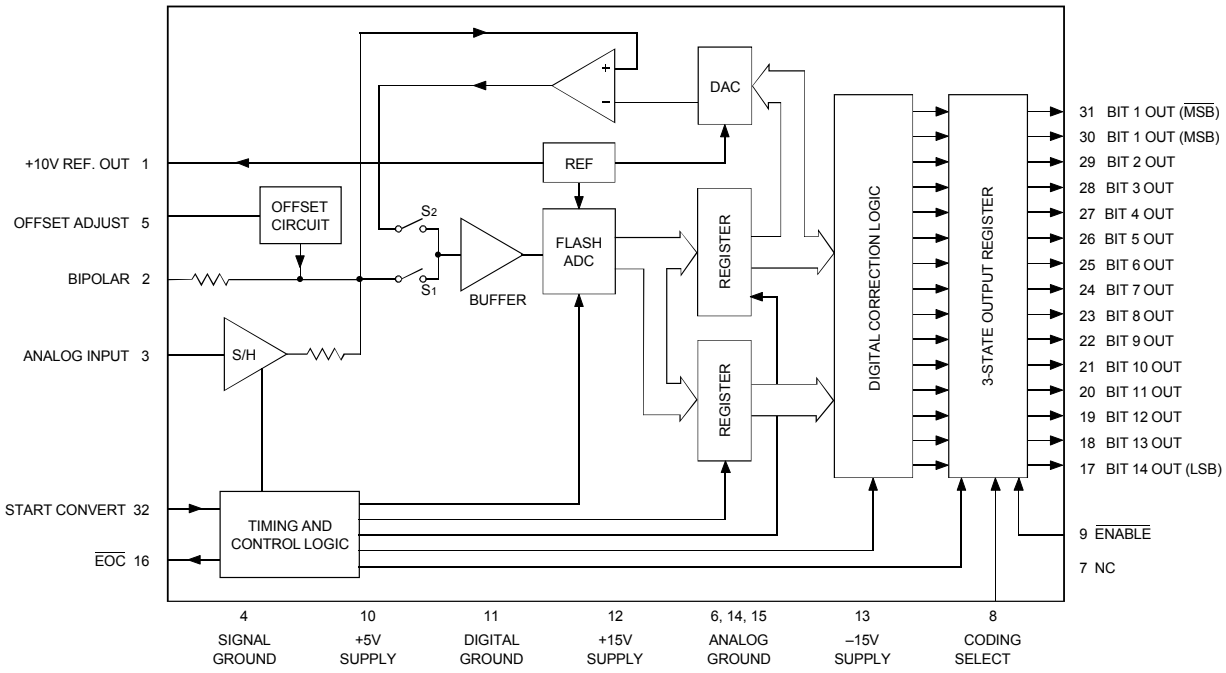



**Figure 1. ADS-942 Functional Block Diagram**

| ABSOLUTE MAXIMUM RATINGS | | |
|---|---|---|
| **PARAMETERS** | **LIMITS** | **UNITS** |
| +15V Supply (Pin 12) | 0 to +16 | Volts |
| –15V Supply (Pin 13) | 0 to –16 | Volts |
| +5V Supply (Pin 10) | 0 to +6.0 | Volts |
| Digital Inputs (Pin 8,9, 32) | –0.3 to +VDD +0.3 | Volts |
| Analog Input (Pin 3) | ±25 | Volts |
| Lead Temp. (10 seconds) | 300 | °C |

## FUNCTIONAL SPECIFICATIONS

($T_A$ = +25°C, ±$V_{CC}$ = ±15V ±$V_{DD}$ = +5V, 2MHz sampling rate, and a minimum 7 minute warmup unless otherwise specified.)

| ANALOG INPUTS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|
| Input Voltage Range | | | | |
| Unipolar | — | 0 to +10 | — | Volts |
| Bipolar | — | ±5 | — | Volts |
| Input Impedence | 4.7 | | — | k |
| Input Capacitance | — | 7 | 15 | pF |
| **DIGITAL INPUTS** | | | | |
| Logic Levels | | | | |
| Logic "1" | +2.0 | — | — | Volts |
| Logic "0" | — | — | +0.5 | Volts |
| Logic Loading "1" | — | — | +5 | µA |
| Logic Loading "0" | — | — | –600 | µA |
| **PERFORMANCE** | | | | |
| Integral Non-Linearity (fin = 1MHz) | | | | |
| +25°C | — | ±1 | ±2 | LSB |
| 0 to +70°C | — | ±1 | ±2 | LSB |
| –40 to +100°C | — | ±2 | ±3 | LSB |
| Differential Non-Linearity (fin = 1MHz) | | | | |
| +25°C | –0.99 | ±0.80 | ±1.25 | LSB |
| 0 to +70°C | –0.99 | ±090 | ±1.5 | LSB |
| –40 to +100°C | –0.99 | ±1 | +2.5 | LSB |
| Full Scale Absolute Accuracy | | | | |
| +25°C | — | ±0.1 | ±0.122 | %FSR |
| 0 to +70°C | — | ±0.12 | ±0.36 | %FSR |
| –40 to +100°C | — | ±0.45 | ±0.85 | %FSR |
| Unipolar Zero Error | | | | |
| +25°C (see Figure 3) | — | ±0.05 | ±0.122 | %FSR |
| 0 to +70°C | — | ±0.1 | ±0.2 | %FSR |
| –40 to +100°C | — | ±0.2 | ±0.3 | %FSR |
| Bipolar Zero Error | | | | |
| +25°C (see Figure 3) | — | ±0.05 | ±0.122 | %FSR |
| 0 to +70°C | — | ±0.1 | ±0.2 | %FSR |
| –40 to +100°C | — | ±0.2 | ±0.3 | %FSR |
| Bipolar Offset Error | | | | |
| +25°C (see Figure 3) | — | ±0.1 | ±0.2 | %FSR |
| 0 to +70°C | — | ±0.12 | ±0.3 | %FSR |
| –40 to +100°C | — | ±0.5 | ±0.8 | %FSR |
| Gain Error | | | | |
| +25°C (see Figure 3) | — | ±0.018 | ±0.122 | %FSR |
| 0 to +70°C | — | ±0.12 | ±0.3 | %FSR |
| –40 to +100°C | — | ±0.6 | ±0.8 | %FSR |
| No Missing Codes (fin = 500kHz) | | | | |
| 14 Bits | 0 to +70°C | | | |
| 13 Bits | –40 to +100°C | | | |
| Resolution | 14 Bits | | | |

| OUTPUTS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|
| Output Coding | Staight Bin./Offset Bin./Two's Comp. Comp. Bin./Comp. Offset Bin./C2C | | | |
| Logic Level | | | | |
| Logic "1" | +2.4 | — | — | Volts |
| Logic "0" | — | — | +0.4 | Volts |
| Logic Loading "1" | — | — | –160 | µA |
| Logic Loading "0" | — | — | +6.4 | mA |
| Internal Reference | | | | |
| Voltage, +25°C | +9.98 | +10.0 | +10.02 | Volts |
| Drift | — | ±13 | ±30 | ppm/°C |
| External Current | — | — | 5 | mA |
| **DYNAMIC PERFORMANCE** | | | | |
| Total Harm. Distort. (–0.5dB) | | | | |
| dc to 100kHz | — | –85 | — | dB |
| 100kHz to 500kHz | — | –80 | –75 | dB |
| 500kHz to 1MHz | — | –77 | — | dB |
| Signal-to-Noise Ratio (w/o distortion, –0.5dB ) | | | | |
| dc to 100kHz | 74 | 78 | — | dB |
| 100kHz to 500kHz | 73 | 75 | — | dB |
| 500kHz to 1MHz | — | 73 | — | dB |
| Signal-to-Noise Ratio (and distortion, –0.5dB) | | | | |
| dc to 100kHz | 73 | 78 | — | dB |
| 100kHz to 500kHz | 72 | 75 | — | dB |
| 500kHz to 1MHz | — | 72 | — | dB |
| Spurious Free Dyn. Range ① | | | | |
| dc to 100kHz | — | –86 | –77 | dB |
| 100 to 500kHz | — | –81 | –75 | dB |
| 500kHz to 1MHz | — | –78 | — | dB |
| Two-tone IMD Distortion (fin = 100kHz, | | | | |
| 240kHz, fs = 2.0Mhz, –0.5dB) | — | –85 | — | dB |
| Input Bandwidth (–3dB) | | | | |
| Small Signal (–20dB input) | — | 6 | — | MHz |
| Large Signal (–0.5dB input) | — | 1.75 | — | MHz |
| Slew Rate | — | ±250 | — | V/µs |
| Aperature Delay Time | — | — | 10 | ns |
| Aperature Uncertainty | — | — | ±10 | ps |
| S/H Aquisition Time (to ±0.003%FSR) | | | | |
| Sinusoidal (fin = 1MHz) | — | 120 | 150 | ns |
| Step input | — | 250 | 450 | ns |
| Conversion Rate | | | | |
| Sinusoidal (fin = 1MHz) | 2 | — | — | MHz |
| Step input | 1.3 | — | — | MHz |
| Feedthrough Rejection (fin = 1MHz) | — | 85 | — | dB |
| Overvoltage Recovery, ±12V | — | 1000 | 2000 | ns |
| Noise | — | 250 | — | µVrms |
| **POWER REQUIREMENTS** | | | | |
| Power Supply Ranges | | | | |
| +15V Supply | +14.25 | +15.0 | +15.75 | Volts |
| –15V Supply | –14.25 | –15.0 | –15.75 | Volts |
| +5V Supply | +4.75 | +5.0 | +5.25 | Volts |
| Power Supply Currents | | | | |
| +15V Supply | — | +8 | +12 | mA |
| –15V Supply | — | –58 | –70 | mA |
| +5V Supply | — | +70 | +87 | mA |
| Power Dissipation | — | 1.4 | 1.7 | Watts |
| Power Supply Rejection | — | — | ±0.05 | %FSR%V |

| PHYSICAL/ENVIRONMENTAL | | | | |
|---|---|---|---|---|
| Operating Temp. Range, Case | | | | |
| ADS-942MC, MC-C | 0 | — | +70 | °C |
| ADS-942ME, ME-C | –40 | — | +100 | °C |
| Storage Temperature Range | –65 | — | +150 | °C |
| Package Type | 32-pin, metal-sealed, ceramic TDIP | | | |
| Weight | 0.46 ounces (13 grams) | | | |

Footnote:
① Same specification as In-Band Harmonics and Peak Harmonics.

## TECHNICAL NOTES

1. Rated performance requires using good high-frequency circuit board layout techniques. Connect the digital and analog grounds to one point, the analog ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. SIGNAL GROUND (pin 4) is not internally connected to ANALOG GROUND (pins 6, 15).
2. Bypass the analog and digital supplies and the +10V REF. OUT (pin 1) to ground with a 4.7µF, 25V tantalum electrolytic capacitor in parallel with a 0.1µF ceramic capacitor.
3. CODING SELECT(pin 8) is compatible with CMOS/TTL logic levels for those users desiring logic control of this function. There is an internal pull-up resistor on this pin; connect to +5V or leave open for logic 1. See the Calibration Procedure for selecting an output coding.
4. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 9) to a logic "0" (low). To disable, connect pin 9 to a logic "1" (high).

| INPUT RANGE | INPUT PIN | TIE TOGETHER |
|---|---|---|
| 0 +10V | Pin 3 | Pins 2 and 4 |
| ±5V | Pin 3 | Pins 1 and 2 |

**Table 1. Input Connections**

## CALIBRATION PROCEDURE

1. Connect the converter per Figure 3 and Table 1 for the appropriate input voltage range. Apply a pulse of 35 nanoseconds minimum to START CONVERT (pin 32) at a rate of 200kHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.
2. Zero Adjustments

   Apply a precision voltage reference source between ANALOG INPUT (pin 3) and SIGNAL GROUND (pin 4), then adjust the reference source output per Table 2.

   For unipolar, adjust the zero trimpot so that the output code flickers equally between 00 0000 0000 0000 and 00 0000 0000 0001 with CODING SELECT (pin 8) tied low (straight binary) or between 11 1111 1111 1111 and 11 1111 1111 1110 with pin 8 tied high (complementary binary).

   For bipolar operation, adjust the trimpot until the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001 with pin 8 tied low (offset binary) or between 01 1111 1111 1111 and 01 1111 1111 1110 with pin 8 tied high (complementary offset binary).

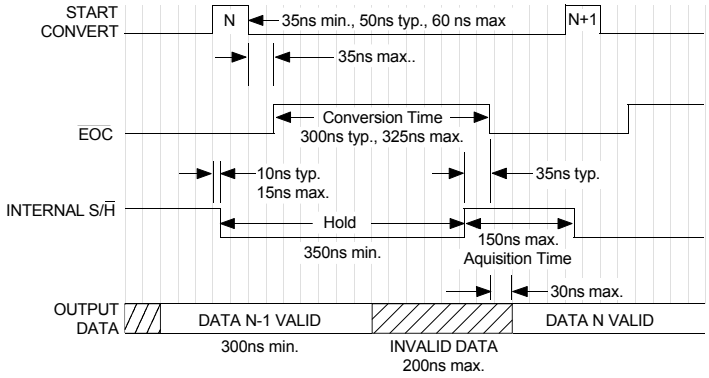
   Two's complement coding requires using BIT 1 OUT ($\overline{\text{MSB}}$) (pin 31). With pin 8 tied low, adjust the trimpot until the code flickers between 00 0000 0000 0000 and 00 0000 0000 0001.
3. Full-Scale Adjustment Set the output of the voltage reference used in step 2 to the value shown in Table 2.

   Adjust the gain trimpot until the output code flickers equally between 11 1111 1111 1110 and 11 1111 1111 1111 with pin 8 tied low for straight binary/offset binary or between 00 0000 0000 0000 and 00 0000 0000 0001 with pin 8 tied high for complementary binary/complementary offset binary.

   Two's complement coding requires using pin 31. With pin 8 tied low, adjust the gain trimpot until the output code flickers equally between 01 1111 1111 1110 and 01 1111 1111 1111.
4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

| INPUT RANGE | ZERO ADJUST +½ LSB | GAIN ADJUST FS –1½ LSB |
|---|---|---|
| 0 to +10V | +305µV | +9.999085V |
| ±5V | +305µV | +4.999085V |

**Table 2. Zero and Gain Adjustments**




Note: Scale is approximately 25ns per division.

**Figure 2. ADS-942 Timing Diagram**

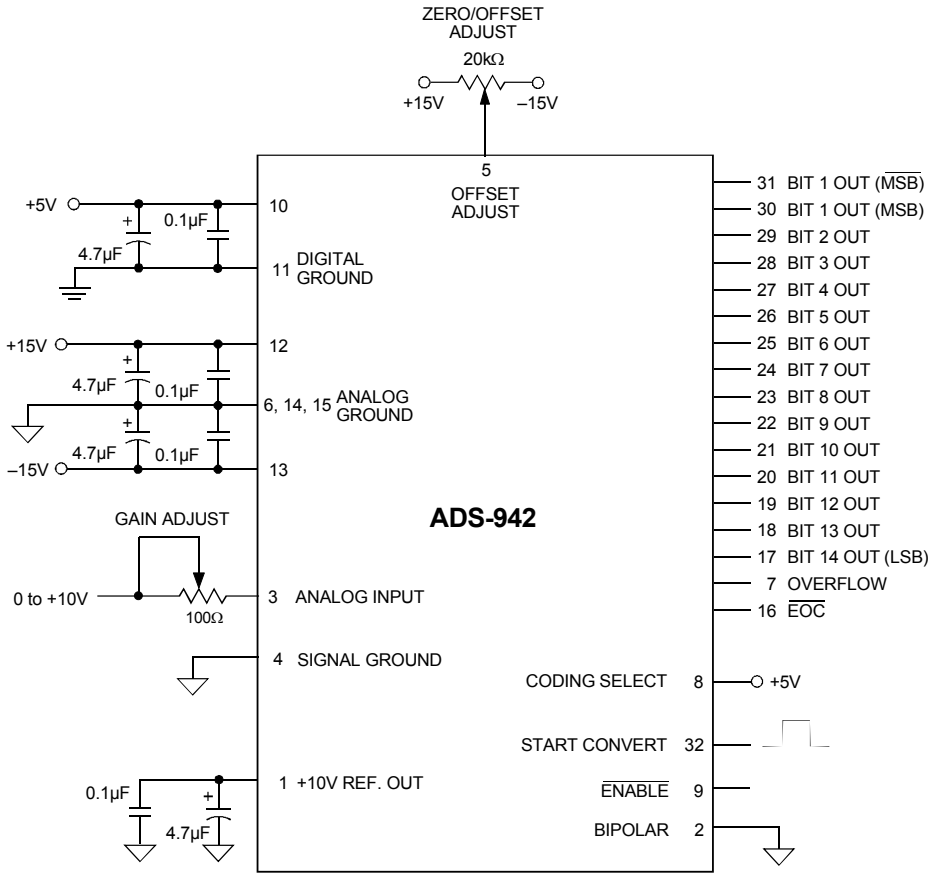



**Figure 3. Typical ADS-942 Connection Diagram**

## Removing System Errors

Use external potentiometers to remove system errors or to reduce the small initial errors to zero. Use a 100Ω trimpot in series with the analog input for gain adjustment. Use a fixed 50Ω resistor instead of the trimpot for operation without adjustment. Use a 20kΩ trimpot with the wiper tied to OFFSET ADJUST (pin 5) for zero/offset adjustment. Connect pin 5 to ANALOG GROUND (pin 6) for operation without zero/offset adjustment.

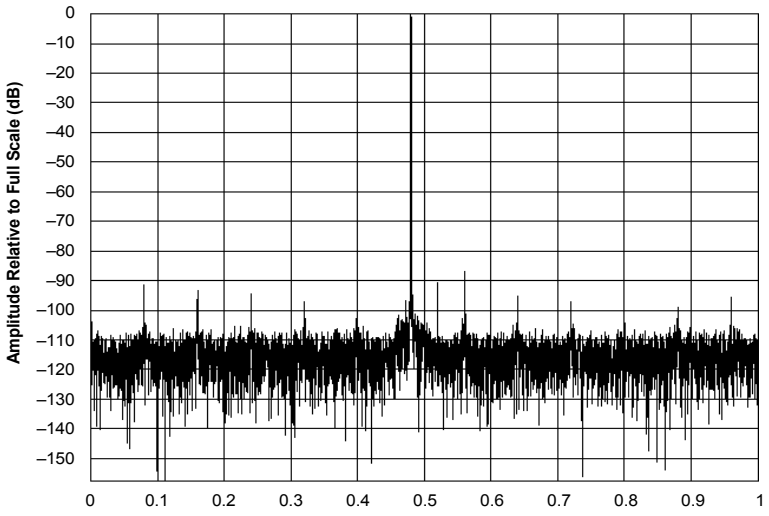
| | | STRAIGHT BINARY | COMP. BINARY | | | |
|---|---|---|---|---|---|---|
| UNIPOLAR SCALE | INPUT RANGE 0 to +10V | OUTPUT CODING MSB LSB | MSB LSB | MSB LSB | INPUT RANGE ±5V | BIPOLAR SCALE |
| +FS – 1 LSB | +9.999390 | 11 1111 1111 1111 | 00 0000 0000 0000 | 01 1111 1111 1111 | +4.999390 | +FS – 1LSB |
| +7/8 FS | +8.750000 | 11 1000 0000 0000 | 00 0111 1111 1111 | 01 1000 0000 0000 | +3.750000 | +3/4FS |
| +3/4 FS | +7.500000 | 11 0000 0000 0000 | 00 1111 1111 1111 | 01 0000 0000 0000 | +2.500000 | +1/2FS |
| +1/2 FS | +5.000000 | 10 0000 0000 0000 | 01 1111 1111 1111 | 00 0000 0000 0000 | 0.000000 | 0 |
| +1/4 FS | +2.500000 | 01 0000 0000 0000 | 10 1111 1111 1111 | 11 0000 0000 0000 | –2.500000 | –1/2FS |
| +1/8 FS | +1.250000 | 00 1000 0000 0000 | 11 0111 1111 1111 | 10 1000 0000 0000 | –3.750000 | –3/4FS |
| +1 LSB | +0.000610 | 00 0000 0000 0001 | 11 1111 1111 1110 | 10 0000 0000 0001 | –4.999390 | –FS+1LSB |
| 0 | 0.000000 | 00 0000 0000 0000 | 11 1111 1111 1111 | 10 0000 0000 0000 | –5.000000 | –FS |
| | | OFFSET BINARY | COMP. OFF. BIN. | TWO'S COMP. | | |

**Table 3. Output Coding**

## THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to +125°C. All room-temperature (TA = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

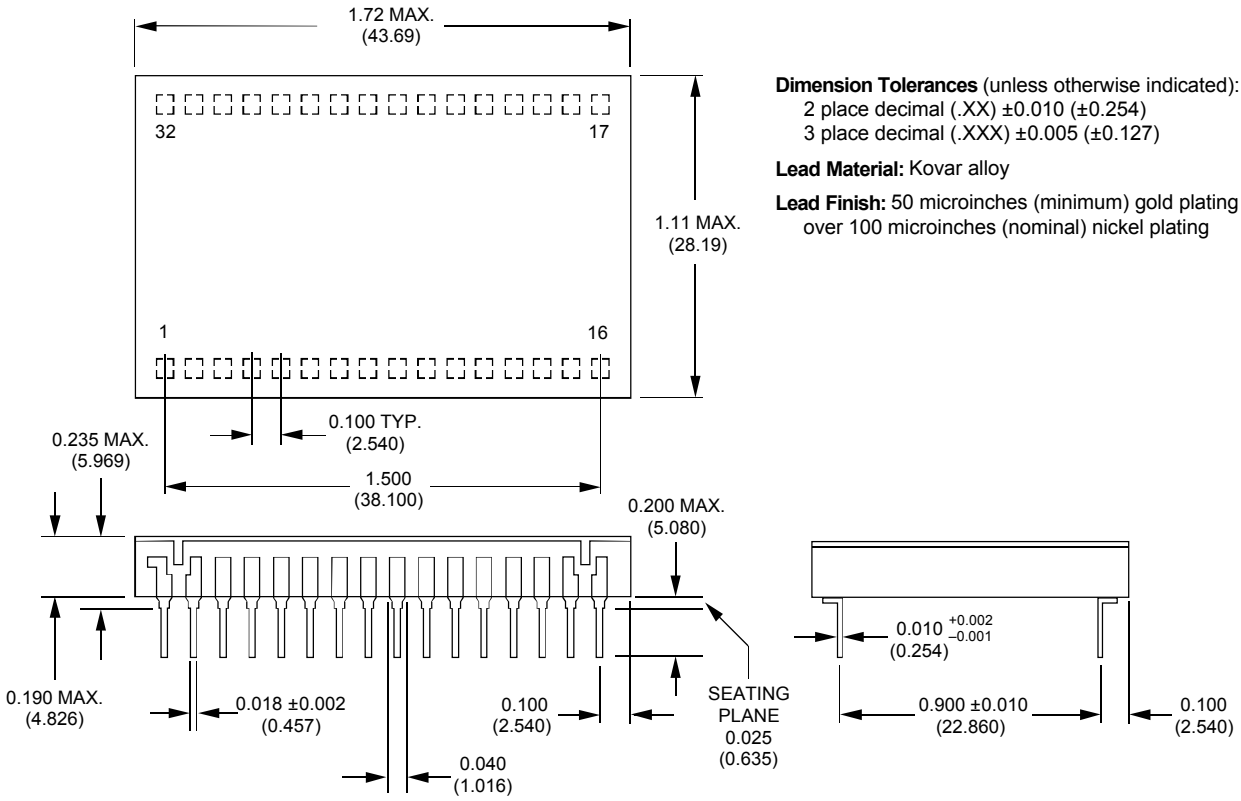
These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Electricallyinsulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.




(fs = 2MHz, fin = 490kHz, Vin = –0.5dB, 16,384-point FFT)

**Figure 4. ADS-942 FFT Analysis**

## MECHANICAL DIMENSIONS INCHES (mm)




**Dimension Tolerances** (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

**Lead Material:** Kovar alloy

**Lead Finish:** 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

**ORDERING INFORMATION**

| MODEL NUMBER | OPERATING TEMP. RANGE | PACKAGE | ROHS | ACCESSORIES | |
|---|---|---|---|---|---|
| ADS-942MC | 0 to +70°C | TDIP | No | ADS-EVAL4<br>HS-32 | Evaluation Board (without ADS-942)<br>Heat Sink for all ADS-942 models |
| ADS-942MC-C | 0 to +70°C | TDIP | Yes | | |
| ADS-942ME | –40 to +100°C | TDIP | No | | |
| ADS-942ME-C | –40 to +100°C | TDIP | Yes | | |
| Receptacles for PC mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 32 required. | | | | | |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