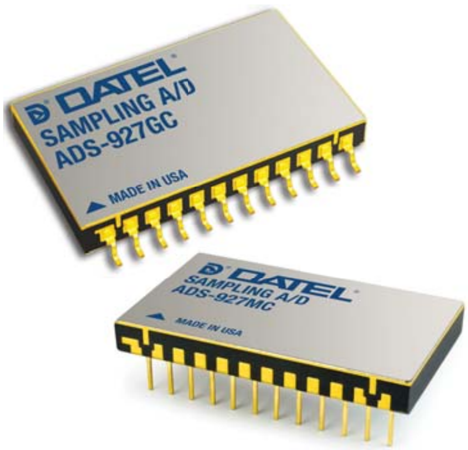
DATEL®
INNOVATION and EXCELLENCE

ADS-927

14-Bit, 1MHz, Low-Power Sampling A/D Converters



PRODUCT OVERVIEW

The ADS-927 is a high-performance, 14-bit, 1MHz sampling A/D converter. This device samples input signals up to Nyquist frequencies with no missing codes. The ADS-927 features outstanding dynamic performance including a THD of –80dB.

Housed in a small 24-pin DDIP or SMT (gull-wing) package, the functionally complete ADS-927 contains a fast-settling sample-hold amplifier, a subranging (two-pass) A/D converter, a precise voltage reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL.

Requiring ±15V (or ±12V) and +5V supplies, the ADS-927 dissipates only 1.95W (1.65W for ±12V), maximum. The unit is offered with a bipolar input (–5V to +5V). Models are available for use in either commercial (0 to +70°C), industrial (–40 to +100°C), or HI-REL (–55 to +125°C) operating temperature ranges. Applications include radar, sonar, spectrum analysis, and graphic/medical imaging.

FEATURES

- 14-bit resolution
- 1MHz sampling rate
- Functionally complete
- No missing codes
- Small 24-pin DDIP or SMT package
- Low power, 1.9 Watts maximum
- Operates from ±15V or ±12V supplies +5V supply
- Bipolar ±5V input range*

*For unipolar 0 to +10V input range, see ADS-917 data sheet.

INPUT/OUTPUT CONNECTIONS			
PIN	FUNCTION	PIN	FUNCTION
1	BIT 14 (LSB)	24	–12V/–15V SUPPLY
2	BIT 13	23	ANALOG GROUND
3	BIT 12	22	+12V/+15V SUPPLY
4	BIT 11	21	+10V REFERENCE OUT
5	BIT 10	20	ANALOG INPUT
6	BIT 9	19	ANALOG GROUND
7	BIT 8	18	BIT 1 (MSB)
8	BIT 7	17	BIT 2
9	BIT 6	16	START CONVERT
10	BIT 5	15	$\overline{\text{EOC}}$
11	BIT 4	14	DIGITAL GROUND
12	BIT 3	13	+5V SUPPLY

BLOCK DIAGRAM

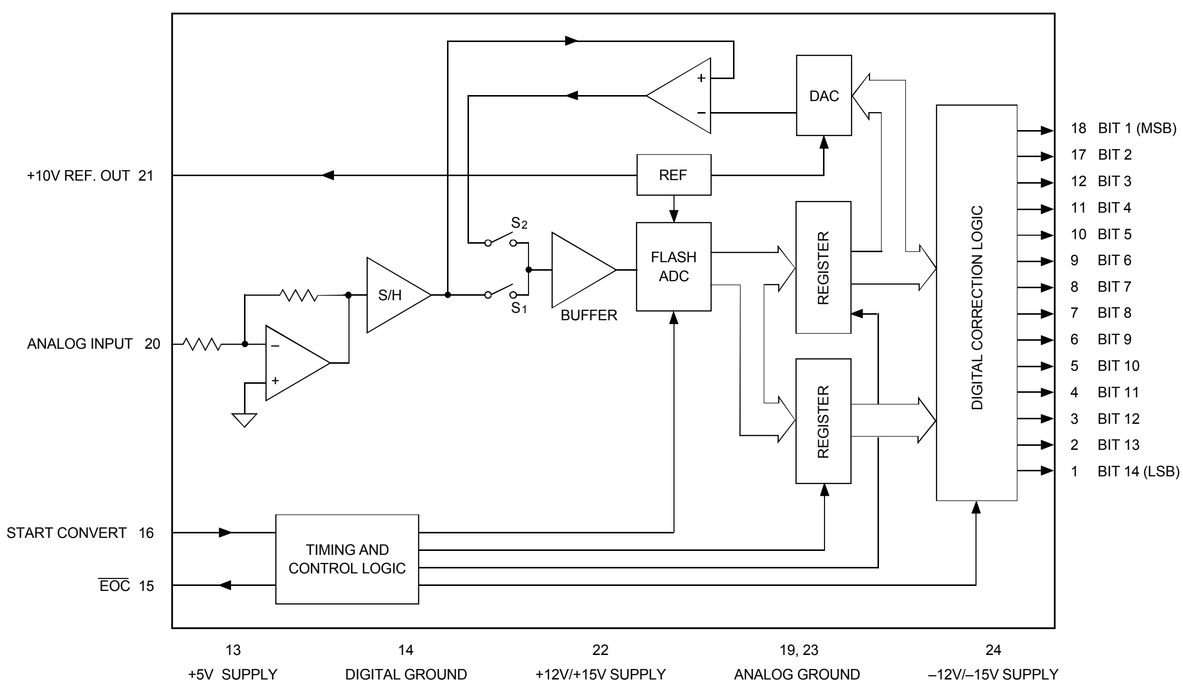


Figure 1. ADS-927 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS		
PARAMETERS	LIMITS	UNITS
+12V/+15V Supply (Pin 22)	0 to +16	Volts
–12V/–15V Supply (Pin 24)	0 to –16	Volts
+5V Supply (Pin 13)	0 to +6	Volts
Digital Input (Pin 16)	–0.3 to +VDD +0.3	Volts
Analog Input (Pin 20)	±15	Volts
Lead Temperature (10 seconds)	+300	°C

PHYSICAL/ENVIRONMENTAL				
PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS-927MC, GC	0	—	+70	°C
ADS-927ME, GE	–40	—	+100	°C
ADS-927MM, GM	–55	—	+125	°C
Thermal Impedance				
θjc	—	6	—	°C/Watt
θca	—	24	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP or SMT			
Weight	0.42 ounces (12 grams)			

FUNCTIONAL SPECIFICATIONS

(TA = +25°C, ±VCC = ±15V (or ±12V), +VDD = +5V, 1MHz sampling rate, and a minimum 1 minute warmup ① unless otherwise specified.)

	+25°C			0 TO +70°C			–55 TO +125°C			
ANALOG INPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range ②	—	±5	—	—	±5	—	—	±5	—	Volts
Input Resistance	—	1	—	—	1	—	—	1	—	kΩ
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUT										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	175	200	225	175	200	225	175	200	225	ns
STATIC PERFORMANCE										
Resolution	—	14	—	—	14	—	—	14	—	Bits
Integral Nonlinearity (fin = 10kHz)	—	±0.5	—	—	±0.75	—	—	±1.5	—	LSB
Differential Nonlinearity (fin = 10kHz)	—	±0.5	+0.95	—	±0.5	±0.95	—	±0.75	+0.99	LSB
Full Scale Absolute Accuracy	—	±0.08	±0.15	—	±0.15	±0.25	—	±0.3	±0.5	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.05	±0.1	—	±0.1	±0.25	—	±0.15	±0.3	%FSR
Bipolar Offset Error (Tech Note 2)	—	±0.05	±0.1	—	±0.1	±0.25	—	±0.25	±0.5	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.15	—	±0.15	±0.25	—	±0.25	±0.5	%FSR
No Missing Codes (fin = 10kHz)	14	—	—	14	—	—	14	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 100kHz	—	–91	–83	—	–90	—	—	–88	—	dB
100kHz to 500kHz	—	–82	–78	—	–82	–78	—	–80	–77	dB
Total Harmonic Distortion (–0.5dB)										
dc to 100kHz	—	–90	–81	—	–89	—	—	–87	—	dB
100kHz to 500kHz	—	–80	–76	—	–80	–76	—	–79	–74	dB
Signal-to-Noise Ratio (w/o distortion, –0.5dB)										
dc to 100kHz	77	79	—	74	78	—	73	77	—	dB
100kHz to 500kHz	75	78	—	74	78	—	73	76	—	dB
Signal-to-Noise Ratio (& distortion, –0.5dB) ④										
dc to 100kHz	76	78	—	73	77	—	71	76	—	dB
100kHz to 500kHz	73	76	—	73	76	—	71	75	—	dB
Two-tone Intermodulation Distortion (fin = 100kHz,										
240kHz, fs = 1MHz –0.5dB)	—	–87	—	—	–86	—	—	–85	—	dB
Noise	—	350	—	—	350	—	—	350	—	µVrms
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	7	—	—	7	—	—	7	—	MHz
Large Signal (–0.5dB input)	—	5	—	—	5	—	—	5	—	MHz
Feedthrough Rejection (fin = 500kHz)	—	84	—	—	84	—	—	84	—	dB
Slew Rate	—	±60	—	—	±60	—	—	±60	—	V/µs
Aperture Delay Time	—	±20	—	—	±20	—	—	±20	—	ns
Aperture Uncertainty	—	5	—	—	5	—	—	5	—	ps rms
S/H Acquisition Time										
(to ±0.003%FSR, 10V step)	335	390	445	335	390	445	335	390	445	ns
Overvoltage Recovery Time ⑤	—	400	1000	—	400	1000	—	400	1000	ns
A/D Conversion Rate	1	—	—	1	—	—	1	—	—	MHz

	+25°C			0 TO +70°C			–55 TO +125°C			
ANALOG OUTPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Internal Reference										
Voltage	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	Volts
Drift	—	±5	—	—	±5	—	—	±5	—	ppm/°C
External Current	—	—	1.5	—	—	1.5	—	—	1.5	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Delay, Falling Edge of $\overline{EOC}$ to Output Data Valid	—	—	35	—	—	35	—	—	35	ns
Output Coding	Offset Binary									
POWER REQUIREMENTS , ±15V										
Power Supply Ranges										
+15V Supply	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	Volts
–15V Supply	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Currents										
+15V Supply	—	+43	+70	—	+43	+70	—	+43	+70	mA
–15V Supply	—	–25	–45	—	–25	–45	—	–25	–45	mA
+5V Supply	—	+71	+80	—	+71	+80	—	+71	+80	mA
Power Dissipation	—	1.6	1.95	—	1.6	1.95	—	1.6	1.95	Watts
Power Supply Rejection	—	—	±0.02	—	—	±0.02	—	—	±0.02	%FSR/%V
POWER REQUIREMENTS, ±12V										
Power Supply Ranges										
+12V Supply	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	Volts
–12V Supply	–11.5	–12.0	–12.5	–11.5	–12.0	–12.5	–11.5	–12.0	–12.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Currents										
+12V Supply	—	+42	+70	—	+42	+70	—	+42	+70	mA
–12V Supply	—	–25	–45	—	–25	–45	—	–25	–45	mA
+5V Supply	—	+71	+80	—	+71	+80	—	+71	+80	mA
Power Dissipation	—	1.4	1.65	—	1.4	1.65	—	1.4	1.65	Watts
Power Supply Rejection	—	—	±0.02	—	—	±0.02	—	—	±0.02	%FSR/%V
Power Supply Rejection	—	—	±0.02	—	—	±0.02	—	—	±0.02	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time. There is a slight degradation in performance when using ±12V supplies.

② See Ordering Information for 0 to +10V input range. Contact DATEL for availability of other input voltage ranges.

③ A 1MHz clock with a 200ns wide start convert pulse is used for all production testing. For applications requiring less than a 1MHz sampling rate, wider start convert pulses can be used. See Timing Diagram for more details.

④ Effective bits is equal to:

$$\frac{(\text{SNR} + \text{Distortion}) - 1.76 + \left[20 \log \dfrac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}} \right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid after the analog input is back within the specified range.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-927 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 19 and 23) directly to a large **analog** ground plane beneath the package.

   Bypass all power supplies and the REFERENCE OUTPUT (pin 21) to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible. If the user-installed offset and gain adjusting circuit shown in Figure 2 is used, also locate it as close to the ADS-927 as possible.

2. The ADS-927 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the input circuit of Figure 2. When using this circuit, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. When operating the ADS-927 from ±12V supplies, do not drive external circuitry with the REFERENCE OUTPUT. The reference's accuracy and drift specifications may not be met, and loading the circuit may cause accuracy errors within the converter.

4. Applying a start convert pulse while a conversion is in progress ($\overline{EOC}$ = logic "1") initiates a new and inaccurate conversion cycle. Data from the interrupted and subsequent conversions will be invalid.

CALIBRATION PROCEDURE (Refer to Figures 2 and 3)

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuit of Figure 2 are guaranteed to compensate for the ADS-927's initial accuracy errors and may not be able to compensate for additional system errors.

All fixed resistors in Figure 2 should be metal-film types, and multiturn potentiometers should have TCR's of 100ppm/°C or less to minimize drift with temperature.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-927, offset adjusting is normally accomplished at the point where the MSB is a 1 and all other output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +½LSB (+305µV).

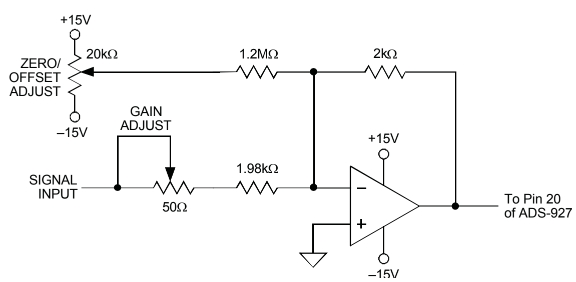


Figure 2. ADS-927 Calibration Circuit

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus 1½ LSB's (+4.999085V).

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 16) so the converter is continuously converting. If using LED's on the outputs, a 200kHz conversion rate will reduce flicker.
2. Apply +305µV to the ANALOG INPUT (pin 20).
3. Adjust the offset potentiometer until the output bits are a 1 and all 0's and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. 1. Apply +4.999085V to the ANALOG INPUT (pin 20).
2. Adjust the gain potentiometer until the output bits are all 1's and the LSB flickers between 1 and 0.

Table 1. Zero and Gain Adjust

INPUT VOLTAGE RANGE	ZERO ADJUST +½ LSB	GAIN ADJUST +FS –1½ LSB
±5V	+305µV	+4.999085V

Table 2. Output Coding

OUTPUT CODING	INPUT RANGE ±5V	BIPOLAR SCALE
MSB LSB		
11 1111 1111 1111	+4.99939	+FS –1 LSB
11 1000 0000 0000	+3.75000	+3/4 FS
11 0000 0000 0000	+2.50000	+1/2FS
10 0000 0000 0000	0.00000	0
01 0000 0000 0000	–2.50000	–1/2FS
00 1000 0000 0000	–3.75000	–3/4FS
00 0000 0000 0001	–4.99939	–FS +1 LSB
00 0000 0000 0000	–5.00000	–FS

Coding is offset binary; 1LSB = 610µV.

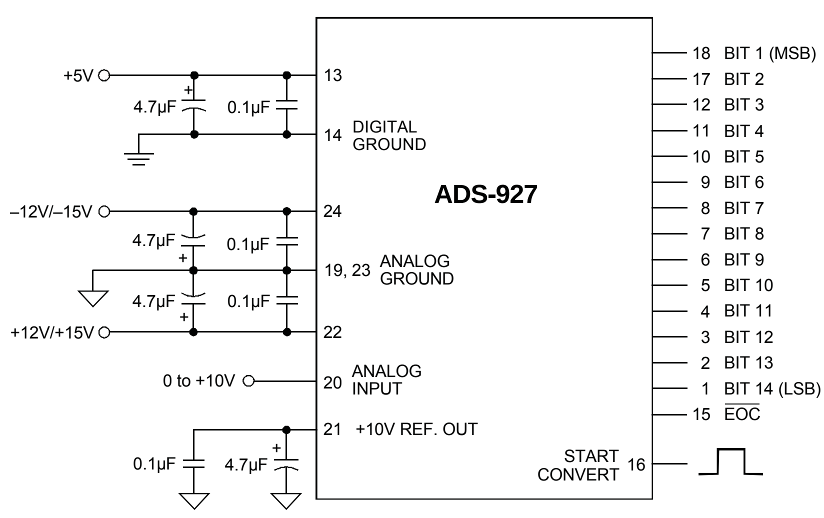


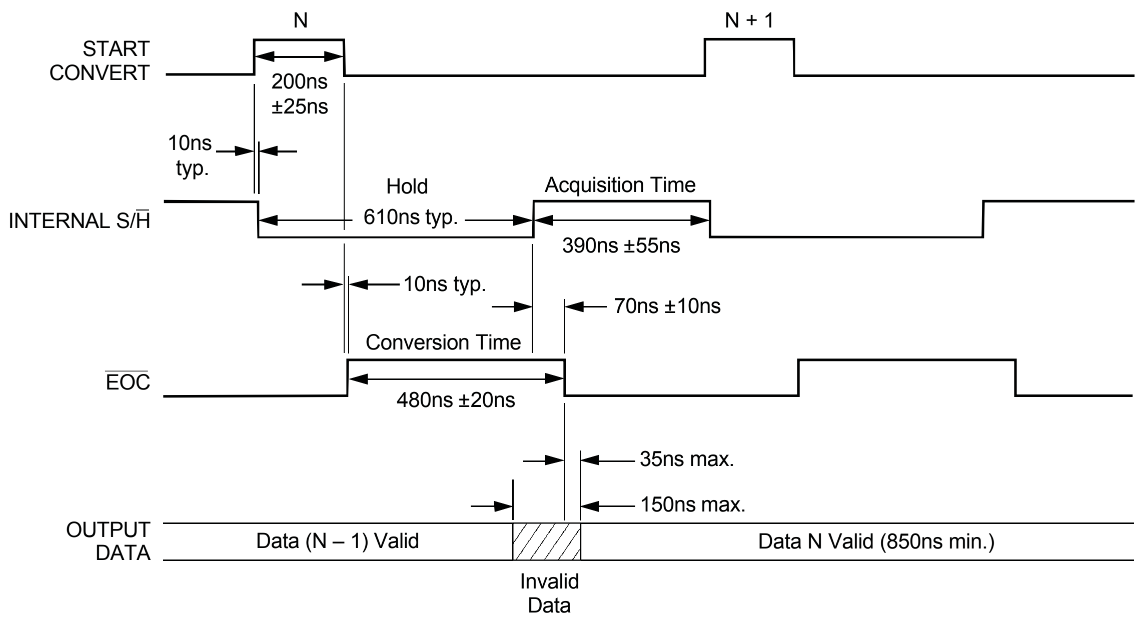
Figure 3. Typical ADS-927 Connection Diagram

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to +125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks; however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package.

Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed," and of course, minimal air flow over the surface can greatly help reduce the package temperature.



Notes: 1. f_s = 1MHz.

2. The ADS-927 is a pulse-triggered device. Its internal operations are triggered by both the rising and falling edges of the start convert pulse. When sampling at 1MHz, the start pulse must be between 175 and 225nsec wide. For lower sampling rates, wider start pulses may be used, however, a minimum pulse width low of 50nsec must be maintained.

Figure 4. ADS-927 Timing Diagram

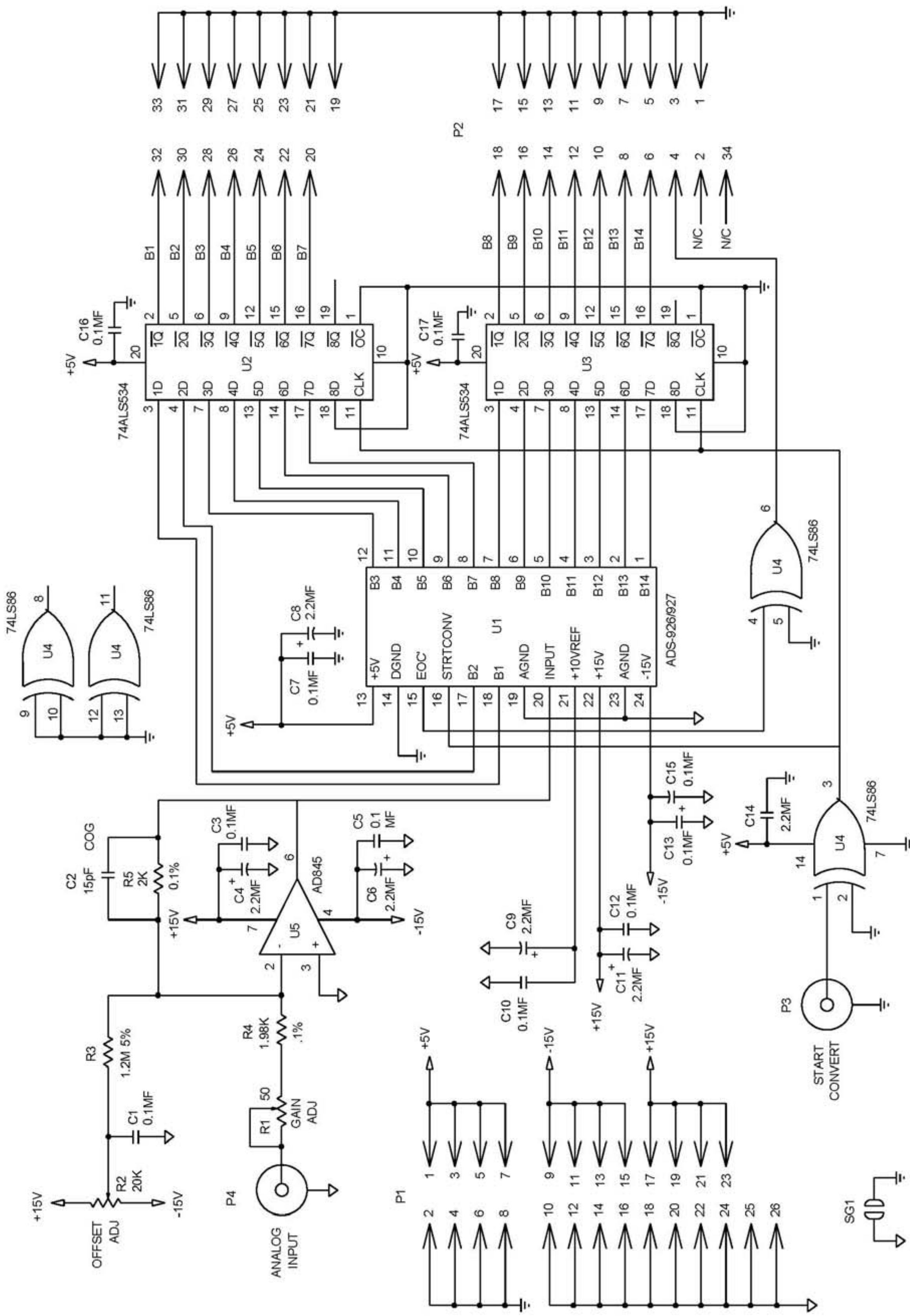


Figure 5. ADS-927 Evaluation Board Schematic

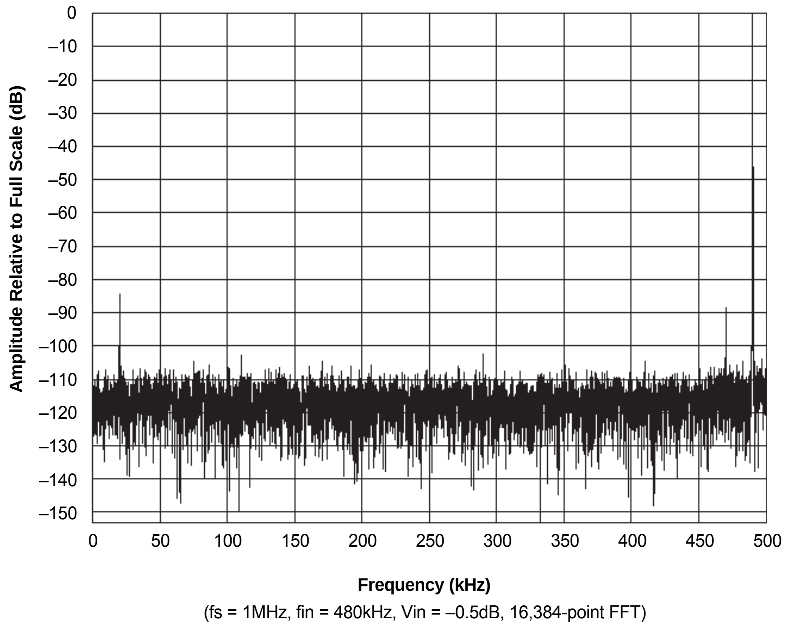


Figure 6. ADS-927 FFT Analysis

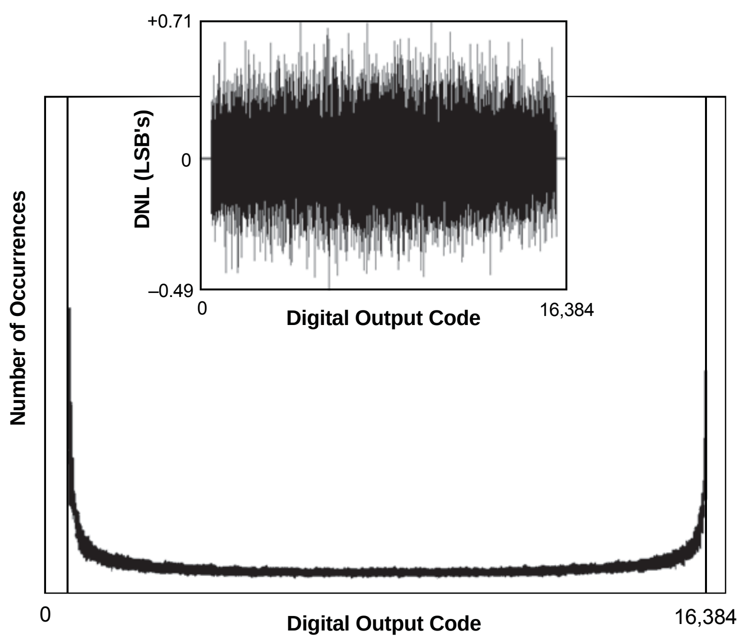
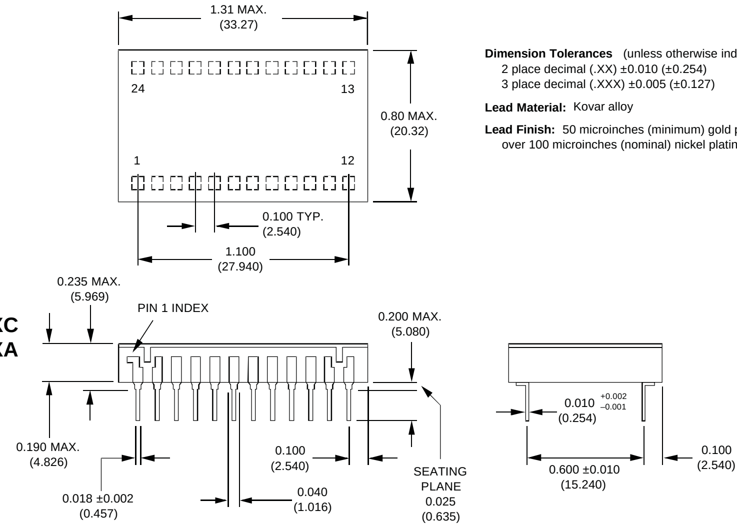


Figure 7. ADS-927 Histogram and Differential Nonlinearity

MECHANICAL DIMENSIONS - INCHES (mm)

24-Pin DDIP Versions

ADS-927MC
ADS-927MC-C
ADS-927ME
ADS-927ME-C
ADS-927MM
ADS-927MM-C
ADS-927/883
ADS-927-C/883
5962-9475701HXC
5962-9475701HXA



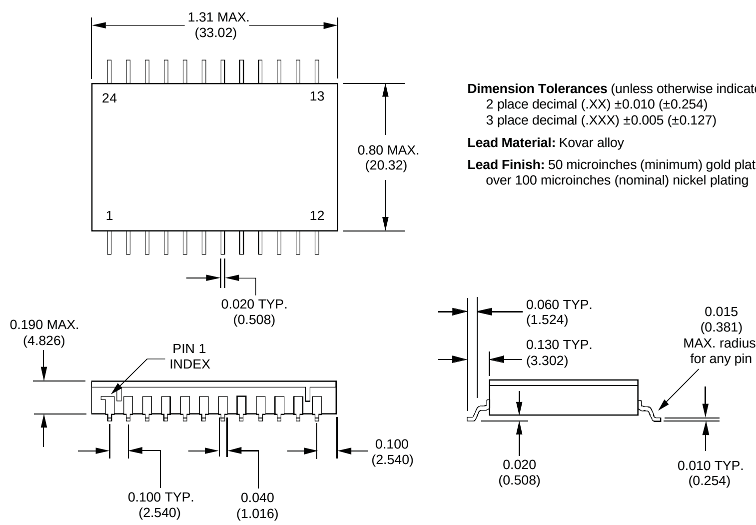
Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

24-Pin Surface Mount Versions

ADS-927GC
ADS-927GC-C
ADS-927GE
ADS-927GE-C
ADS-927GM
ADS-927GM-C
ADS-927G/883
ADS-927G-C/883



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION					
MODEL NUMBER	OPERATING TEMP. RANGE	PACKAGE	ROHS	ACCESSORIES	
ADS-927MC	0 to +70°C	DDIP	No	ADS-B926/927	Evaluation Board (without ADS-927)
ADS-927MC-C	0 to +70°C	DDIP	Yes	HS-24	Heat Sinks for all ADS-917/927 DDIP models
ADS-927ME	–40 to +100°C	DDIP	No	Receptacles for PC board mounting can be ordered through AMP Inc. Part #3-331272-8 (Component Lead Socket), 24 required. For MIL-STD-883 product specifications, contact DATEL. For unipolar analog input 0 to +10V, see ADS-917 data sheet.	
ADS-927ME-C	–40 to +100°C	DDIP	Yes		
ADS-927MM	–55 to +125°C	DDIP	No		
ADS-927MM-C	–55 to +125°C	DDIP	Yes		
ADS-927/883	–55 to +125°C	DDIP	No		
ADS-927-C/883	–55 to +125°C	DDIP	Yes		
ADS-927GC	0 to +70°C	SMT	No		
ADS-927GC-C	0 to +70°C	SMT	Yes		
ADS-927GE	–40 to +100°C	SMT	No		
ADS-927GE-C	–40 to +100°C	SMT	Yes		
ADS-927GM	–55 to +125°C	SMT	No		
ADS-927GM-C	–55 to +125°C	SMT	Yes		
ADS-927G/883	–55 to +125°C	SMT	No		
ADS-927G-C/883	–55 to +125°C	SMT	Yes		
5962-9475701HXC	–55 to +125°C	DDIP	No		
5962-9475701HXA	–55 to +125°C	DDIP	No		