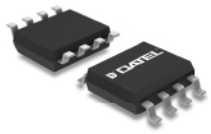
ADS-450

12-Bit, 1MSPS, Differential, SAR A/D Converters



FEATURES

- Fully Differential / Rail-Rail inputs
- 12-bit resolution
- 1MSPS minimum sampling rate
- Humidity and stress resistant ceramic LCC package for -QL and /883 models
- -40°C to +105°C and -55°C to +125°C operating temperature ranges
- 100% testing over temperature
- High-Rel process flow, burn-in, environmental, lot and ATE traceability
- No missing codes over specified temperature range
- SPI-compatible serial interface
- THD -83dB
- Very low power:
  3.9mW with +3V supply
  9mW with +5V supply
- 3V or 5V supply voltage operation
- Small, 8-pin, MSOP or ceramic LCC package
- Pb-Free (Rohs compliant)

PRODUCT OVERVIEW

The ADS-450 12-bit, 1MSPS SAR Analog to Digital Converter delivers excellent integral and differential linearity performance over changes in both supply voltage and temperature. With fully differential, high-impedance, inputs operating from rail to rail, the ADS-450 is an ideal selection for low power and battery operated data acquisition systems. The A/D is designed to accept an external reference voltage from 0.1V to 2.2V when operating with a 3V supply, and from 0.1V to 3.5V when operating with a +5V supply.

This series is offered in either a small 8-pin MSOP plastic package or a fully hermetic sealed ceramic LCC package for High-Rel or military applications. The hermetic package, offered for the –QL and /883 versions, protects the IC from the effects of moisture making the precision DC characteristics of the DAC more stable in environments where humidity is a concern. In addition, the LCC package isolates the IC from the stresses that may occur on the printed circuit board caused by variations in temperature.

Employing a serial SPI compatible digital interface, this device requires only 1.25mA from a 3V supply and 1.7mA from a 5V supply when operating at the full 1MSPS conversion rate as well as a mere 3-5µW of power during shutdown mode. The MSOP package are drop in compatible with several industry standard converters.

DATEL offers these converters fully tested over temperature with ATE results recorded and stored for the operating temperature ranges of -40°C to +105°C (Enhanced) or –55°C to +125°C (military). Burn-in and environmental screening are also available.

Products are offered in military temperature grades as well as fully screened High-Reliability -QL and /883 models.

APPLICATIONS

- MIL-STD/883 systems
- Defense/ aerospace applications
- Scientific test instruments
- Low-power Data Acquisition
- Industrial process control
- Instrumentation measurement
- Battery-powered handheld equipment
- Flow control, Pressure sensors

BLOCK DIAGRAM

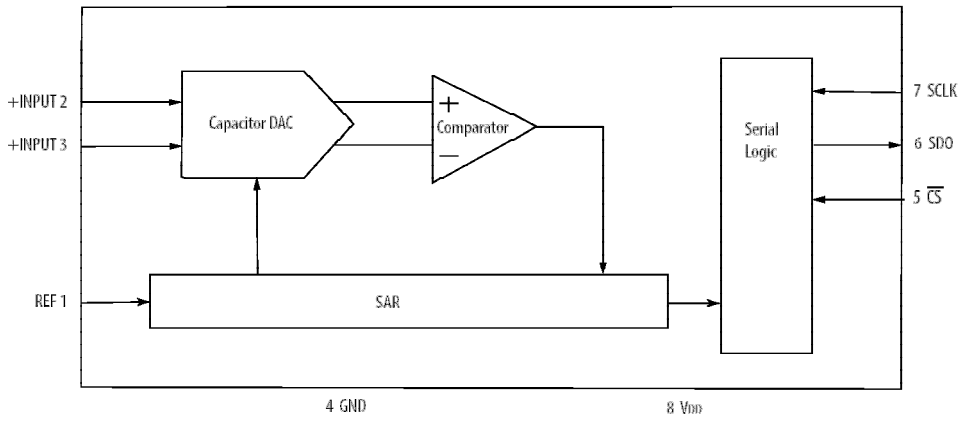


Figure 1. ADS-450 Functional Block Diagram (MSOP pinout)

ABSOLUTE MAXIMUM RATINGS		
PARAMETERS	LIMITS	UNITS
Analog Input (2,3) to GND (4)	-0.3 to V_{DD} +0.3	V
Digital Input (5,7) to GND (4)	-0.3 to V_{DD} +0.3	V
V_{DD} (pin 8) to GND (4)	-0.3 to +6.0	V
REF (pin 1) to GND (4)	-0.3 to +6.0	V
Input current - any pin	10	mA
ESD Human Body Model	8	kV

PHYSICAL / ENVIRONMENTAL		
PARAMETERS	LIMITS	UNITS
θjc MSOP package	64	°C/W
θca MSOP package	165	°C/W
Storage Temperature Range	-65 to +150	°C

FUNCTIONAL SPECIFICATIONS [1]

For V_{DD} = 3.0V to 3.6V : V_{REF} = +2.0V, F_S = 1MHz, F_{SCLK} 18MHz @ 25°C unless otherwise specified.

For V_{DD} = 4.75V to 5.25V: V_{REF} = +2.5V, F_S = 1MHz, F_{SCLK} 18MHz @ 25°C unless otherwise specified.

ANALOG INPUTS	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Input Voltage Range[1]					
INPUT+	VCM = VREF	—	VCM ± VREF/2	—	V
INPUT-	VCM = VREF	—	VCM ± VREF/2	—	V
Input Leakage Current		-1	—	+1	µA
Input Capacitance	Track Mode	—	14	—	pF
Input Capacitance	Hold Mode	—	5	—	pF
Reference		—	—	—	
Reference Input Voltage Range	V_{DD} = 3V	0.1	2.0	2.2	V
Reference Input Voltage Range	V_{DD} = 5V	0.1	2.5	3.5	V
STATIC PERFORMANCE					
Resolution		—	12	—	Bits
Integral Nonlinearity		-0.99	±0.5	+0.99	LSB
Differential Nonlinearity (Fin = 10kHz)		–0.99	±0.25	+0.99	LSB
Bipolar Zero Error		–0.15	±0.05	+0.15	%FSR
Gain Error		–0.05	±0.02	+0.05	%FSR
No Missing Codes (Fin = 10kHz)		12	—	—	Bits
DYNAMIC PERFORMANCE					
Peak Harmonics (–0.5dB)					
DC to 100kHz	V_{DD} = +3.0 Volts	—	-86	–73	dB
DC to 100kHz	V_{DD} = +5.0 Volts	—	–90	–75	dB
Total Harmonic Distortion (–0.5dB)					
DC to 100kHz	V_{DD} = +3.0 Volts	—	–85	–72	dB
DC to 100kHz	V_{DD} = +5.0 Volts	—	–87	–73	dB
Signal-to-Noise Ratio & distortion (–0.5dB)					
DC to 100kHz	V_{DD} = +3.0 Volts	68	71	—	dB
DC to 100kHz	V_{DD} = +5.0 Volts	70	72	—	dB
Two-Tone Intermodulation Distortion (–0.5dB)					
Fin = 91kHz & 109kHz, FS = 1MHz		—	–92	—	dB
Input Bandwidth (–3dB)		—	15	—	MHz
Aperture Delay Time		—	1	—	ns
Aperture Uncertainty		—	15	—	ps-rms
S/H Acquisition Time to ±0.001% of FSR		—	—	200	ns
DIGITAL INPUTS					
Logic Levels					
Logic "1"		2.4	—	—	V
Logic "0"		—	—	0.8	V
Logic Loading "1"		—	—	1	µA
Logic Loading "0"		—	—	-1	µA
Input Capacitance		—	10	—	pF
DIGITAL OUTPUTS					
Logic Levels					
Logic "1"	I OUT = 200 µA	V_{DD}-0.3	—	—	V
Logic "0"	I OUT = - 200 µA	—	—	0.4	V
Logic Loading "1"		—	—	–1	µA
Logic Loading "0"		—	—	1	µA
Output Coding		Two's Complement			

TIMING (cont.)		MIN.	TYP.	MAX.	UNITS
Conversion time t_{CONV}		—	—	900	ns
A/D Conversion Rate		1	—	—	MHz
Serial Clock Period t_{SCLK}		60	—	—	ns
Serial Clock Pulse width t_{SW}		0.4 x t_{SCLK}	—	0.6 x t_{SCLK}	ns
Serial Clock Frequency FSCLK		0.01	—	18	MHz
Chip Select (CS) Pulse Width HI t_{CSW}		10	—	—	ns
Chip Select (CS) Falling Edge to SCLK Falling Edge t_{CSdly}		10	—	—	ns
Chip Select (CS) Falling Edge to SDO Valid t_{CSDO}		—	—	20	ns
Serial Clock SCLK Falling Edge to SDO Valid t_{SCLKDV}		—	—	40	ns
Serial Clock SCLK Falling Edge to SDO Hold t_{SDH}		10	—		ns
Serial Clock SCLK Falling Edge to SDO Disable Time $t_{DISABLE}$		10	—	40	ns
Quiet Time Before Sample t_{QUIET}		60	—	—	ns
POWER REQUIREMENTS	**TEST CONDITION**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Power Supply Ranges					
V_{DD} Supply		2.7	3	5.5	V
VDD Supply	Static	—	—	1	µA
VDD Supply	+3 Volts Dynamic	—	—	1300	µA
VDD Supply	+5 Volts Dynamic		—	1800	µA
Power Dissipation	+3 Volts Static	—	—	3	µW
Power Dissipation	+5 Volts Static	—	—	5	µW
Power Dissipation	+3 Volts Dynamics @ FS=1MSPS	—	—	3.9	µW
Power Dissipation	+5 Volts Dynamics @ FS=1MSPS	—	—	9	µW
Power Supply Rejection		—	—	80	dB
OPERATING TEMPERATURE		**MIN.**	**TYP.**	**MAX.**	**UNITS**
SE models		-40	—	+105	°C
SM models		-55	—	+125	°C
-QL models		-55	—	+125	°C
/883 models		-55	—	+125	°C
PACKAGE TYPE		**MIN.**	**TYP.**	**MAX.**	**UNITS**
SE, SM models	8-pin MSOP				
-QL, /883 models	Hermetic, Ceramic LCC				

NOTES:

1. Voltage applied to ±VIN must be between GND and V_{DD}.
2. θj measured on thermally conductive test card in free air.

TECHNICAL NOTES

Theory of Operation

The ADS-450 Analog to Digital converter performs its successive approximation conversion using capacitive charge redistribution. A unique circuit design reduces power consumption by powering the SAR only during conversion time. This feature is controlled by the $\overline{CS}$ pin. When $\overline{CS}$ is high the A/D is in the power saving track mode, and when $\overline{CS}$ goes low the A/D goes into hold mode and the A/D powers up to begin a conversion cycle.

The conversion process involves three steps: the sample mode, the hold mode, and the redistribution mode where the actual A/D conversion takes place. In the sample mode, the differential inputs are switched to charge binary weighted capacitors. During this sample time the A/D is powered down. During the hold mode the binary weighted capacitors are disconnected from the input and switched to an internal comparator thereby completing the sample-hold process. During the redistribution mode the binary weighted capacitors are sequentially switched from MSB to LSB referencing them to an internal reference voltage. The comparator compares the charge of each weighted capacitor to provide a serial 12 bit digital output.

The $\overline{CS}$ signal going low places the A/D into hold mode and then a series of 16 SCLK pulses are applied. The first three SCLK pulses auto-zeros the comparator after which the successive approximation process begins. The following 12 SCLK pulses are used to sequence the binary weighted capacitors and to present the comparator decision as serial data output on the SDO pin. The conversion process is completed on the 15th SCLK cycle after which the A/D returns to track mode and is powered down. After the least significant bit (LSB) is output at SDO, a 16th SCKL pulse puts SDO to a logic low state where it remains until $\overline{CS}$ is taken high and SDO goes to a high-impedance state.

A maximum time of 200ns is required to charge the capacitors during the track period. The conversion rate as well as the SCLK rate must be considered to assure that sufficient time is allowed to acquire the input prior to bringing CS low and thereby going into hold mode.

Digital I/O

The conversion process is controlled through a 3-pin SPI compatible serial digital interface consisting of : chip select ($\overline{CS}$), serial clock (SCLK) and serial data output (SDO). A series of 16 SCLK pulses are required to complete the conversion process (see theory of operation). Serial data output is in the two's complement format presented sequentially from MSB to LSB.

TWO'S COMPLEMENT OUTPUT CODING		
INPUT	VOLTAGE	OUTPUT CODING MSB LSB
+FS	+VREF	0111 1111 1111
+FS -1 LSB	+VREF - 1LSB	0111 1111 1110
Midscale	+2.500000	0000 0000 0000
–FS +1 LSB	-VREF + 1LSB	1000 0000 0001
-FS	-VREF	1000 0000 0000

Analog Input

The ADS-450 has a fully differential input with a full scale range equal to two times the voltage of REF (pin 1). As seen in Figure 2 below, the signals present at the +INPUT and -INPUT are 180°out of phase and have a peak-to-peak amplitude equal to VREF. Because these signals are out of phase the full-scale range of the A/D becomes 2 x V_{REF}, effectively doubling the input range over a single-ended topology.

As a result, the dynamic range of the A/D is doubled resulting in improved dynamic as well as noise performance. The common mode voltage of the input signals must be such that it assure that voltage swing on +INPUT and -INPUT remain within the operating range of the A/D.

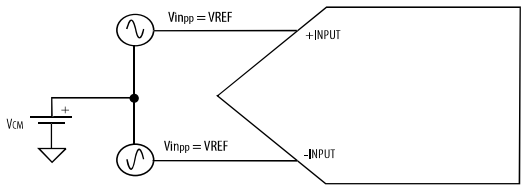


Figure 2

Reference Input

The full-scale range of the ADS-450 is determined by applying an external low-noise reference voltage to the REF pin. When operating with a 3V supply the A/D will accept a reference voltage between +0.1V and +2.2V, and for applications using 5V supplies the reference volatge can be extended to +3.5V. A decoupling capacitor of 0.1µF at the REF pin bypassed to GND is recommended.

Grounding and Layout

It is recommended that separate AGND and DGND ground planes be used. These two planes should be connected at the A/D however, the optimal connection location of the two planes may be system dependent. If separate DGND and AGND planes are used, all of the digital components and switching signals should be located over the DGND and all critical analog components and signals located over the AGND plane. In addition, a signal ground can be employed for all low current signal path grounding.

Power Supplies

To minimize power supply noise and maintain optimal SFDR and SNR performance, tantalum capacitors in parallel with 0.1uF capacitors should be placed as close as possible to the converter's power supply pins. Be assured that capacitors are bypassed to their proper AGND or DGND planes.

Humidity and Outgassing Susceptibility

Plastic mold compounds that are used to house ICs can absorb moisture. When these devices are exposed to humidity the plastic package can undergo slight changes that can apply pressure to the internal die. Stresses placed on a precision data converters can cause changes in its performance in the order of 100ppm. The fully hermetic package offered for the –QL and /883 versions are not affected by humidity, and are therefore more stable in environments where humidity is a concern. The –QL and /883 versions are recommended for all critical and High Reliability applications.

In addition to humidity concerns, the outgassing effects of plastic mold compunds that occur when exposed to temperature can have damaging effects on precision electronic circuits as well as releasing contaminants into purified environments. The hermetic properties of the ceramic LCC package offer protection not available with standard SMT packaging.

TECHNICAL NOTES

Board Mounting Considerations

For applications requiring the highest accuracy, attention should be paid to the board mounting location of SE and SM devices. These models use a plastic TSSOP package that could subject the die to mild stresses when the printed circuit board is cooled or heated. Placing the device in areas subject to slight twisting may cause die stresses and consequently degradation in the accuracy of the converter. It is preferred that the device be placed in the center of the PCB or near the edge of the shortest side where stresses due to flexing are reduced. Mounting the device in a cutout also minimizes flex. Mounting the device on an extremely thin PCB or flexprint will increase the potential for loss of accuracy due to stress. The CLCC package offered for -QL and /883 devices eliminates the potential for die stress.

Board Assembly Considerations

Precision converters provide high accuracy over temperature extremes, but some PC board assembly precautions are necessary. Changes in DC parameters can be expected with Pb-free reflow profiles or wave solder on multilayer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures, this may reduce device initial accuracy.

GLOSSARY OF SPECIFICATIONS

DIFFERENTIAL LINEARITY ERROR The maximum deviation of any quantum (LSB change) in the transfer function of a data converter from its ideal size of FSR/2n.

DIFFERENTIAL LINEARITY TEMPCO: The change in differential linearity error with temperature for a data converter, expressed in ppm/°C of FSR (Full Scale Range).

GAIN ERROR: The difference in slope between the actual and ideal transfer functions for a data converter or other circuit. It is expressed as a percent of analog magnitude.
For +FS, This is the deviation of the last code transition (011...110 to 011...111) from the ideal (+INPUT) - (-INPUT) (i.e., +REF – 1 LSB), after the zero code error has been adjusted out.
For -FS, this is the deviation of the first code transition (100...000 to 100...001) from the ideal (+INPUT) - (-INPUT) (i.e., – REF + 1 LSB), after the zero code error has been adjusted out.

GAIN TEMPCO: The change in gain (or scale factor) with temperature for a data converter or other circuit, generally expressed in ppm/°C.

INTEGRAL LINEARITY ERROR: The maximum deviation of a data converter transfer function from the ideal straight line with offset and gain errors zeroed. It is generally expressed in LSB's or in percent of FSR.

INTERNAL REFERENCE VOLTAGE DRIFT: The maximum deviation from the measured value at room temperature as compared with the value measured at either Tmin or Tmax.

OFFSET ERROR: The deviation from the ideal at analog zero output. This is the deviation of the midscale code transition (111...111 to 000...000) from the ideal (+INPUT) - (-INPUT) (i.e., 0 LSB).

OFFSET DRIFT: The change with temperature of analog zero for a data converter operating in the bipolar mode. It is generally expressed in ppm/°C of FSR.

POWER SUPPLY REJECTION RATIO (PSRR): The output change in a data converter caused by a change in power supply voltage. Power supply sensitivity is generally specified in %/V or in %/% supply change.

SETTLING TIME: The time elapsed from the application of a full scale step input to a circuit to the time when the output has entered and remained within a specified error band around its final value. This term is an important specification for operational amplifiers, analog multiplexers, and Sample-Holds and D/A converters.

SPURIOUS FREE DYNAMIC RANGE (SFDR): The largest harmonic, spurious frequency or noise component in a signal FFT. It is expressed in db with respect to the fundamental frequency.

SIGNAL TO NOISE RATIO AND DISTORTION (SINAD): Usually expressed in dB. It is the ratio of the rms of the fundamental signal amplitude taking at -0.5 dB below full scale to the rms of all the noise spectral components generated by an A/D including all the Harmonics.

SIGNAL TO NOISE RATIO (SNR): Usually expressed in dB. It is the ratio of the rms of the fundamental signal amplitude taking at -0.5 dB below full scale to the rms of all the noise spectral components generated by an A/D excluding the first five Harmonics.

TOTAL HARMONIC DISTORTION: The ratio of the rms sum of the Harmonics to the rms of the fundamental signal. It is usually expressed in dB.

TWO TONE INTERMODULATION DISTORTION: The change in a sinusoidal waveform that is caused by the presence of a second sinusoidal input of a different frequency. Typically specified in dB.

ACQUISITION TIME: For a sample-hold, the time required, after the sample command is given, for the hold capacitor to charge to a full scale voltage change and then remain within the specified error band of ±1/2 LSB.

APERTURE DELAY TIME: In a sample-hold, the time elapsed from the hold command to the actual opening of the sampling switch.

APERTURE JITTER: See Aperture uncertainty time

APERTURE TIME: The time window, or time uncertainty, in making a measurement. For an A/D converter the conversion time; for a sample- hold it is the signal averaging time during the sample to hold transition.

APERTURE UNCERTAINTY TIME: In a sample-hold, the time variation, or time jitter, in the opening of the sampling switch; also the variation in aperture delay time from sample to sample

COMMON MODE REJECTION RATIO: is defined as the ratio of power of the A/D at FS max to the power of a 250mVpp sine wave applied to +INPUT and -INPUT, generally expressed in dB.

$$CMRR = 20 \log 10\ AD / ACM$$

where AD is the power of the A/D at FS and ACM is the power of the 250mVpp sine wave applied to +INPUT and -INPUT.

TYPICAL APPLICATION CONNECTION / PIN DESCRIPTIONS

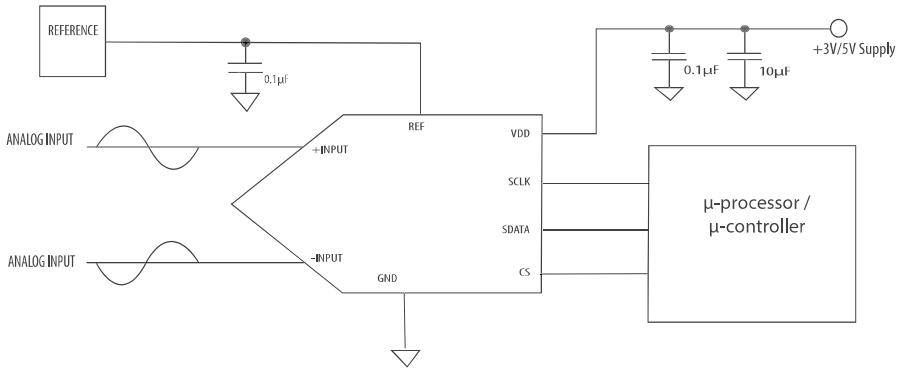


Figure 3. Typical ADS-450 Connection Diagram

PIN DESCRIPTIONS		
PIN	PIN NAME	DESCRIPTION
1	VREF	External Reference Voltge Input
2	+INPUT	Positive Analog Input
3	-INPUT	Negative Analog Input
4	GROUND	Ground
5	$\overline{CS}$	Chip select
6	SDO	Serial Data Output
7	SCLCK	Serial Clock input. Controls I/O and conversion
8	V_{DD}	Supply Voltage +2.7V to +5.25V

TIMING

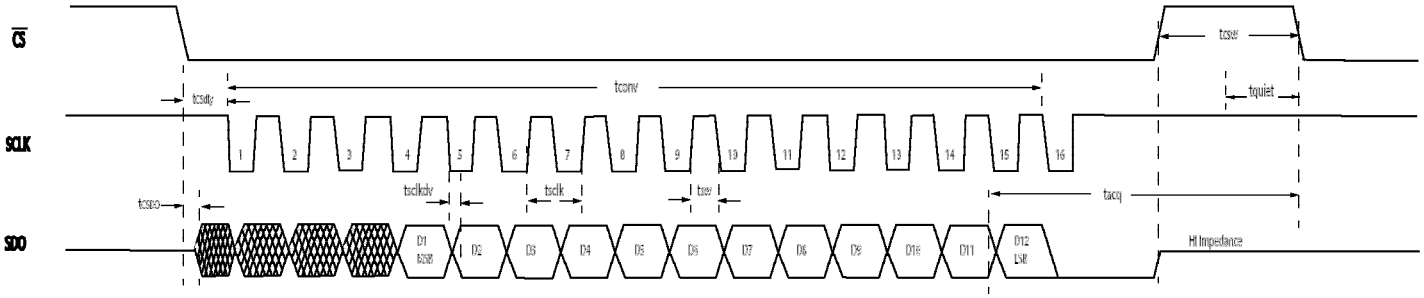
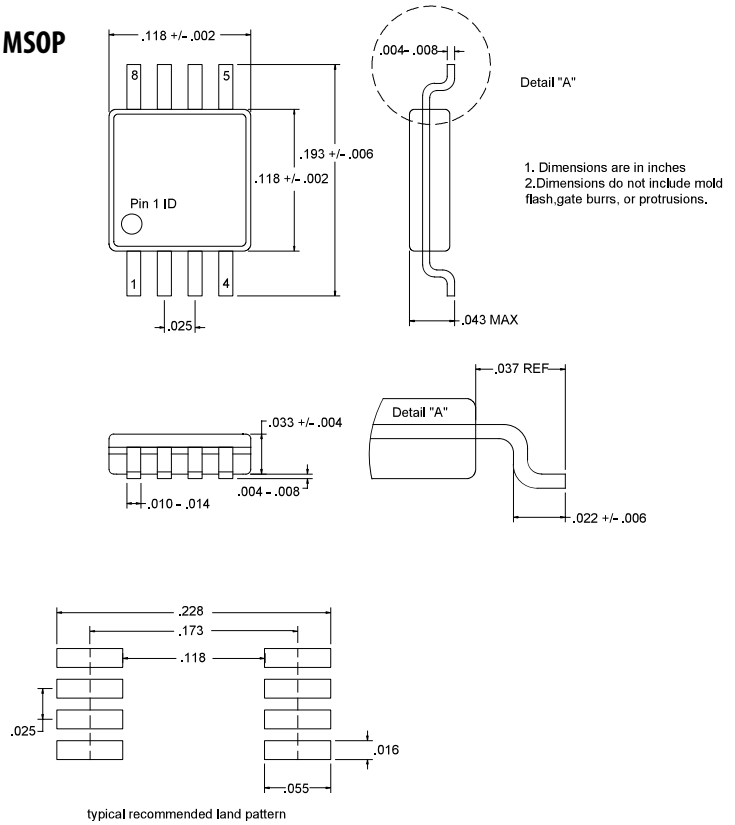


Figure 4. ADS-450 Timing Diagram

MECHANICAL DIMENSIONS – SURFACE MOUNT PACKAGE – INCHES (mm)

MSOP



typical recommended land pattern

ORDERING INFORMATION

ORDERING INFORMATION			
MODEL NUMBER	OPERATING TEMP. RANGE (°C)	PACKAGE	SHIPPING
ADS-450SE	-40 to +105	8 Pin MSOP	Tube
ADS-450SM	-55 to +125	8 Pin MSOP	Tube
ADS-450-QL	-55 to +125	Ceramic LCC	Tray
ADS-450/883	-55 to +125	Ceramic LCC	Tray

11 Cabot Boulevard, Suite 200, Mansfield, MA 02048 USA
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