Ultralow Quiescent Current, 150 mA, CMOS Linear Regulators

Data Sheet

ADP160/ADP161/ADP162/ADP163

FEATURES

- Ultralow quiescent current
  - I_Q = 560 nA with 0 µA load
  - I_Q = 860 nA with 1 µA load
- Stable with 1 µF ceramic input and output capacitors
- Maximum output current: 150 mA
- Input voltage range: 2.2 V to 5.5 V
- Low shutdown current: <50 nA typical
- Low dropout voltage: 195 mV at 150 mA load
- Initial accuracy: ±1%
- Accuracy over line, load, and temperature: ±3.5%
- 15 fixed output voltage options: 1.2 V to 4.2 V
- Adjustable output available
- PSRR performance of 72 dB at 100 Hz
- Current limit and thermal overload protection
- Logic-control enable
- Integrated output discharge resistor
- 5-lead TSOT package
- 4-ball, 0.5 mm pitch WLCSP

APPLICATIONS

- Mobile phones
- Digital cameras and audio devices
- Portable and battery-powered equipment
- Post dc-to-dc regulation
- Portable medical devices

TYPICAL APPLICATION CIRCUITS

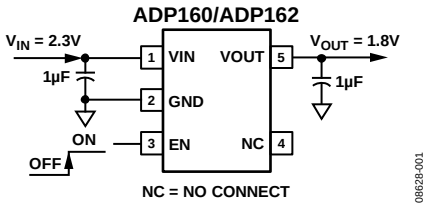

Figure 1. 5-Lead TSOT ADP160/ADP162 with Fixed Output Voltage, 1.8 V

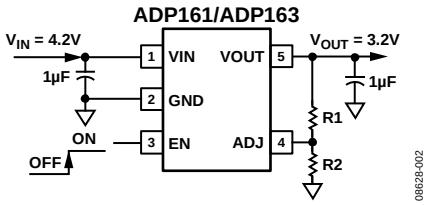

Figure 2. 5-Lead TSOT ADP161/ADP163 with Adjustable Output Voltage, 3.2 V

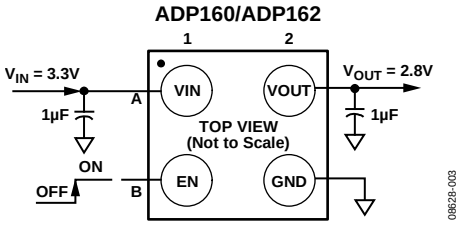

Figure 3. 4-Ball WLCSP ADP160/ADP162 with Fixed Output Voltage, 2.8 V

GENERAL DESCRIPTION

The ADP160/ADP161/ADP162/ADP163 are ultralow quiescent current, low dropout, linear regulators that operate from 2.2 V to 5.5 V and provide up to 150 mA of output current. The low 195 mV dropout voltage at 150 mA load improves efficiency and allows operation over a wide input voltage range.

The ADP16x are specifically designed for stable operation with a tiny 1 µF ± 30% ceramic input and output capacitors to meet the requirements of high performance, space-constrained applications.

The ADP160 is available in 15 fixed output voltage options, ranging from 1.2 V to 4.2 V. The ADP160/ADP161 also include a switched resistor to discharge the output automatically when the LDO is disabled. The ADP162 is identical to the ADP160 but does not include the output discharge function.

The ADP161 and ADP163 are available as adjustable output voltage regulators. They are only available in a 5-lead TSOT package. The ADP163 is identical to the ADP161 but does not include the output discharge function.

Short-circuit and thermal overload protection circuits prevent damage in adverse conditions. The ADP160 and ADP162 are available in a tiny 5-lead TSOT and a 4-ball, 0.5 mm pitch WLCSP package for the smallest footprint solution to meet a variety of portable power applications.

Rev. H

Document Feedback

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SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.5 V) or 2.2 V, whichever is greater; EN = V_{IN}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	2.2		5.5	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 µA		560	1250	nA
		I_{OUT} = 0 µA, T_J = −40°C to +125°C			2.3	µA
		I_{OUT} = 1 µA		860	1800	nA
		I_{OUT} = 1 µA, T_J = −40°C to +125°C			2.8	µA
		I_{OUT} = 100 µA		2.6	4.5	µA
		I_{OUT} = 100 µA, T_J = −40°C to +125°C			5.8	µA
		I_{OUT} = 10 mA		11		µA
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			19	µA
		I_{OUT} = 150 mA		42		µA
		I_{OUT} = 150 mA, T_J = −40°C to +125°C			65	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND		50		nA
		EN = GND, T_J = −40°C to +125°C			1	µA
OUTPUT VOLTAGE ACCURACY						
	V_{OUT}	I_{OUT} = 10 mA	−1		+1	%
		0 µA < I_{OUT} < 150 mA, V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V	−2		+2	%
		0 µA < I_{OUT} < 150 mA, V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V, T_J = −40°C to +125°C	−3.5		+3.5	%
ADJUSTABLE-OUTPUT VOLTAGE ACCURACY (ADP161/ADP163)[1]	V_{ADJ}	I_{OUT} = 10 mA	0.99	1.0	1.01	V
		0 µA < I_{OUT} < 150 mA, V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V	0.98		1.02	V
		0 µA < I_{OUT} < 150 mA, V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V, T_J = −40°C to +125°C	0.97		1.03	V
REGULATION						
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V, T_J = −40°C to +125°C	−0.1		+0.1	%/V
Load Regulation[2]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 100 µA to 150 mA		0.004		%/mA
		I_{OUT} = 100 µA to 150 mA, T_J = −40°C to +125°C			0.01	%/mA
DROPOUT VOLTAGE[3]		V_{OUT} = 3.3 V				
4-Ball WLCSP	$V_{DROPOUT}$	I_{OUT} = 10 mA		7		mV
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			13	mV
		I_{OUT} = 150 mA		105		mV
		I_{OUT} = 150 mA, T_J = −40°C to +125°C			195	mV
5-Lead TSOT		I_{OUT} = 10 mA		8		mV
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			15	mV
		I_{OUT} = 150 mA		120		mV
		I_{OUT} = 150 mA, T_J = −40°C to +125°C			225	mV
ADJ INPUT BIAS CURRENT (ADP161/ADP163)	ADJ_{I-BIAS}	2.2 V ≤ V_{IN} ≤ 5.5 V, ADJ connected to VOUT		10		nA
ACTIVE PULL-DOWN RESISTANCE (ADP160/ADP161)	$T_{SHUTDOWN}$	V_{OUT} = 2.8 V, R_{LOAD} = ∞		300	600	Ω
START-UP TIME[4]	$T_{START-UP}$	V_{OUT} = 3.3 V		1100		µs
CURRENT LIMIT THRESHOLD[5]	I_{LIMIT}		220	320	500	mA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
EN INPUT						
En Input Logic High	V_{IH}	2.2 V ≤ V_{IN} ≤ 5.5 V	1.2			V
EN Input Logic Low	V_{IL}	2.2 V ≤ V_{IN} ≤ 5.5 V			0.4	V
EN Input Leakage Current	$V_{I-LEAKAGE}$	EN = V_{IN} or GND		0.1		µA
		EN = V_{IN} or GND, T_J = −40°C to +125°C			1	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
UNDERVOLTAGE LOCKOUT	UVLO					
Input Voltage Rising	$UVLO_{RISE}$				2.19	V
Input Voltage Falling	$UVLO_{FALL}$		1.60			V
Hysteresis	$UVLO_{HYS}$			100		mV
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 3.3 V		105		μV rms
		10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 2.5 V		100		μV rms
		10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 1.2 V		80		μV rms
POWER SUPPLY REJECTION RATIO	PSRR	100 Hz, V_{IN} = 5 V, V_{OUT} = 3.3 V		60		dB
		100 Hz, V_{IN} = 5 V, V_{OUT} = 2.5 V		65		dB
		100 Hz, V_{IN} = 5 V, V_{OUT} = 1.2 V		72		dB
		1 kHz, V_{IN} = 5 V, V_{OUT} = 3.3 V		50		dB
		1 kHz, V_{IN} = 5 V, V_{OUT} = 2.5 V		50		dB
		1 kHz, V_{IN} = 5 V, V_{OUT} = 1.2 V		62		dB

[1] Accuracy when VOUT is connected directly to ADJ. When the VOUT voltage is set by external feedback resistors, the absolute accuracy in adjust mode depends on the tolerances of resistors used.
[2] Based on an end-point calculation using 0 μA and 150 mA loads.
[3] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.2 V.
[4] Start-up time is defined as the time between the rising edge of EN to V_{OUT} being at 90% of its nominal value.
[5] Current limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V or 2.7 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
MINIMUM INPUT AND OUTPUT CAPACITANCE[1]	C_{MIN}	T_A = −40°C to +125°C	0.7			μF
CAPACITOR ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		0.2	Ω

[1] The minimum input and output capacitance should be greater than 0.7 μF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; however, Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	−0.3 V to +6.5 V
VOUT to GND	−0.3 V to VIN
EN to GND	−0.3 V to VIN
ADJ to GND	−0.3 V to VIN
NC to GND	−0.3 V to VIN
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Operating Ambient Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings only apply individually; they do not apply in combination. The ADP16x can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 inches × 3 inches, circuit board. Refer to JESD 51-7 and JESD 51-9 for detailed information on the board construction. For additional information, see the AN-617 Application Note, *MicroCSP™ Wafer Level Chip Scale Package*.

Ψ_{JB} is the junction to board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
5-Lead TSOT	170	43	°C/W
4-Ball, 0.4 mm Pitch WLCSP	260	58	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

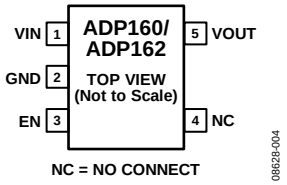

Figure 4. 5-Lead TSOT, Fixed Output Pin Configuration, ADP160/ADP162

Table 5. 5-Lead TSOT Pin Function Descriptions, ADP160/ADP162

Pin No.	Mnemonic	Description
1	VIN	Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor.
2	GND	Ground.
3	EN	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
4	NC	No Connect. This pin is not connected internally. Connect this pin to GND or leave open.
5	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 1 µF or greater capacitor.

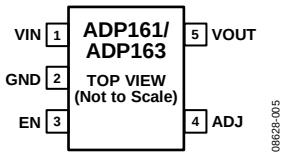

Figure 5. 5-Lead TSOT, Adjustable Output Pin Configuration, ADP161/ADP163

Table 6. 5-Lead TSOT Pin Function Descriptions, ADP161/ADP163

Pin No.	Mnemonic	Description
1	VIN	Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor.
2	GND	Ground.
3	EN	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
4	ADJ	Output Voltage Adjust Pin. Connect the midpoint of the voltage divider between VOUT and GND to this pin to set the output voltage.
5	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 1 µF or greater capacitor.

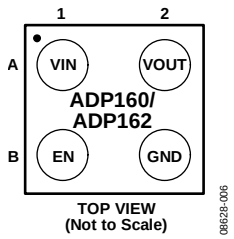

Figure 6. 4-Ball WLCSP Pin Configuration, ADP160/ADP162

Table 7. 4-Ball WLCSP Pin Function Descriptions, ADP160/ADP162

Pin No.	Mnemonic	Description
A1	VIN	Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor.
B1	EN	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
A2	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 1 µF or greater capacitor.
B2	GND	Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

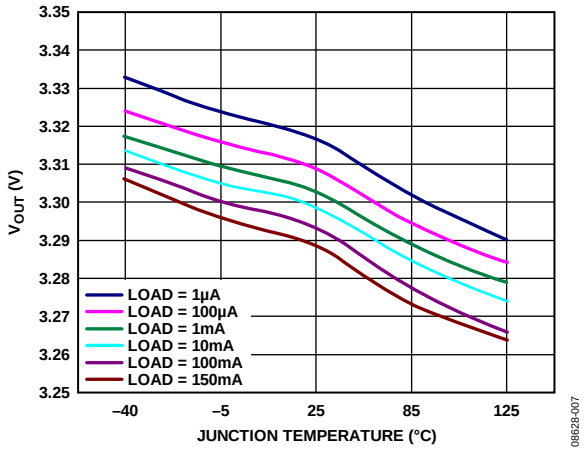

Figure 7. Output Voltage (V_{OUT}) vs. Junction Temperature

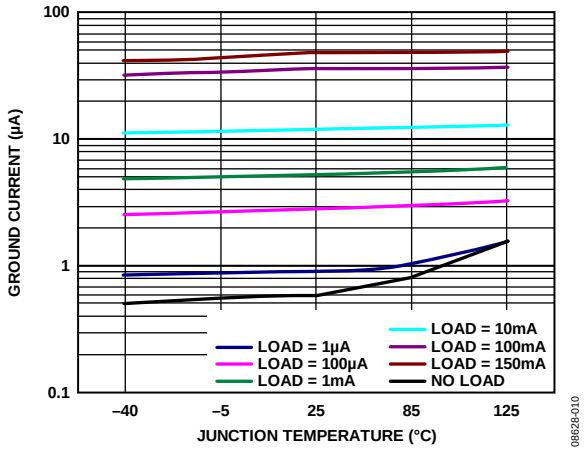

Figure 10. Ground Current vs. Junction Temperature

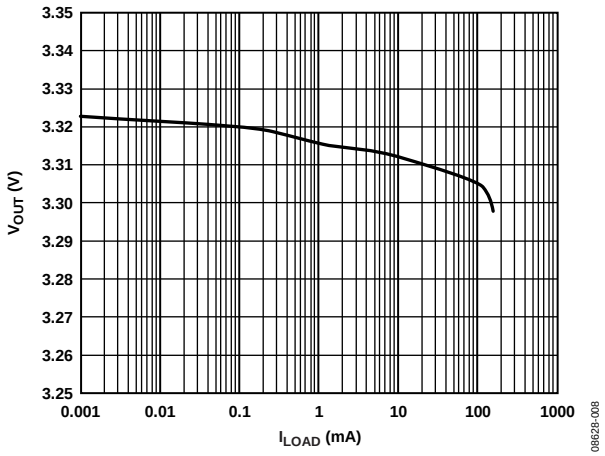

Figure 8. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD})

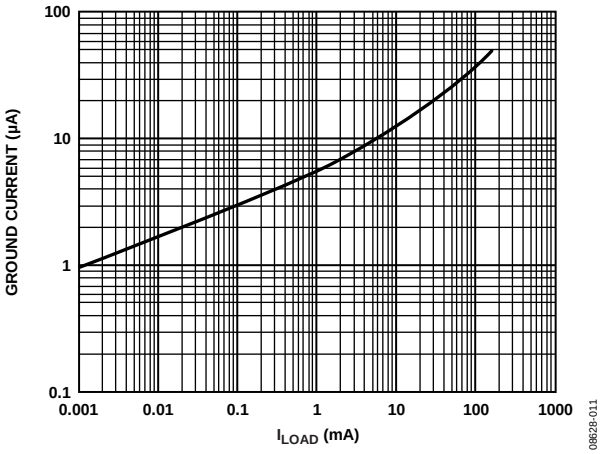

Figure 11. Ground Current vs. Load Current (I_{LOAD})

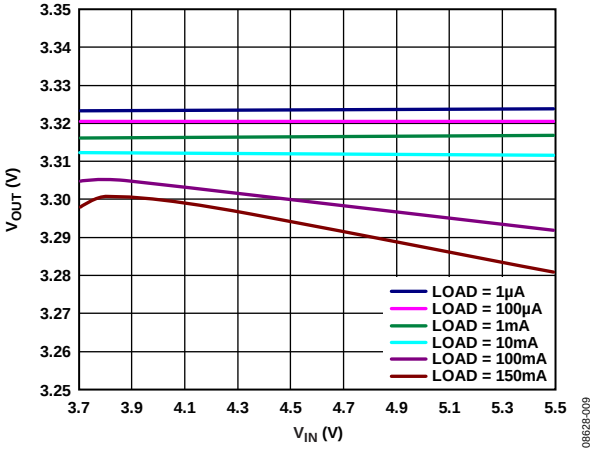

Figure 9. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN})

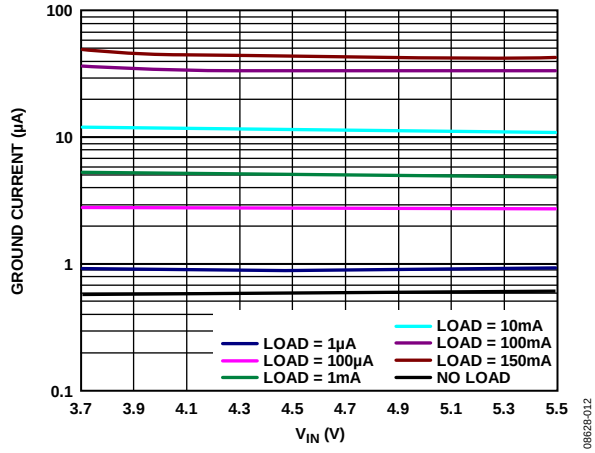

Figure 12. Ground Current vs. Input Voltage (V_{IN})

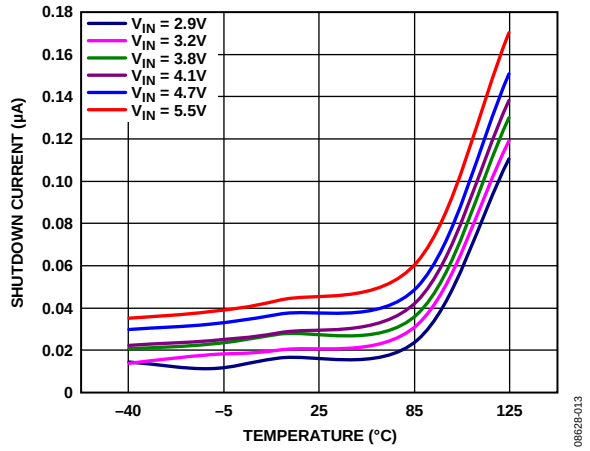

Figure 13. Shutdown Current vs. Temperature at Various Input Voltages

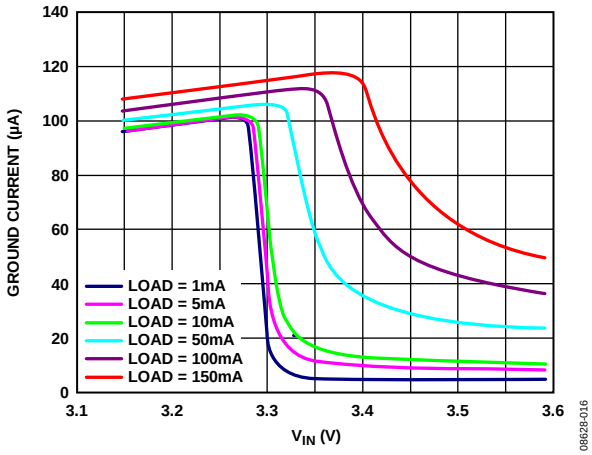

Figure 16. Ground Current vs. Input Voltage (V_{IN}) in Dropout

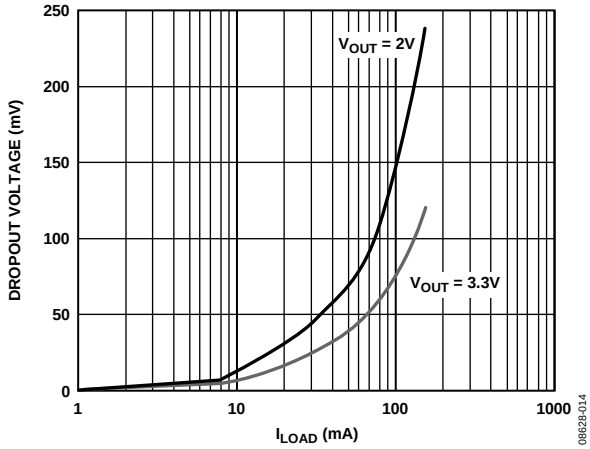

Figure 14. Dropout Voltage vs. Load Current (I_{LOAD})

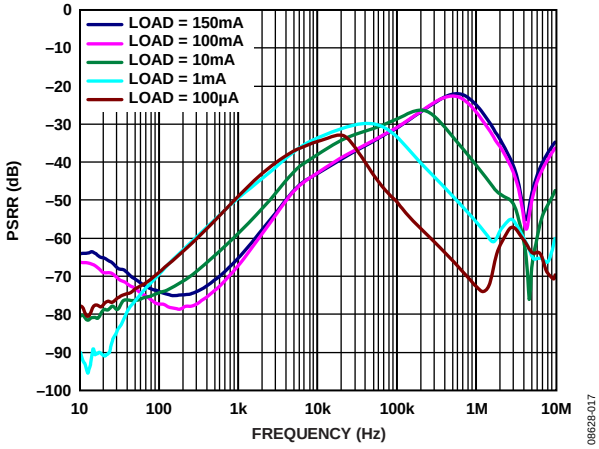

Figure 17. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 1.2 V, V_{IN} = 2.2 V

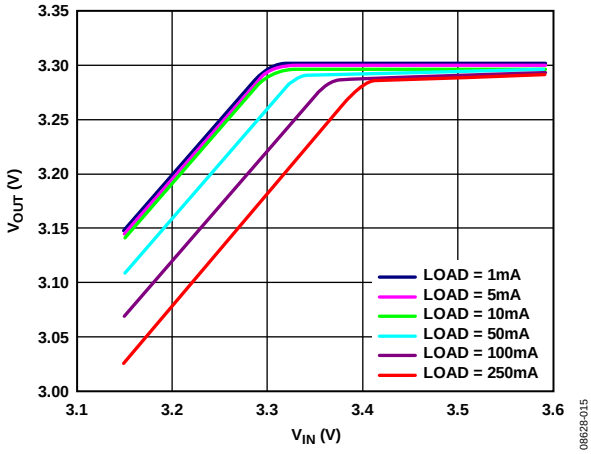

Figure 15. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout

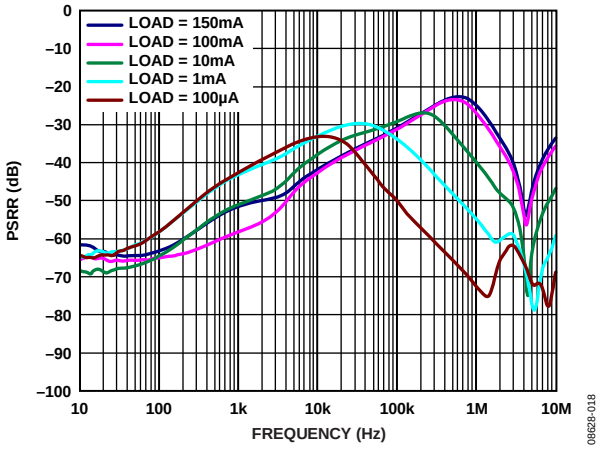

Figure 18. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 2.5 V, V_{IN} = 3.5 V

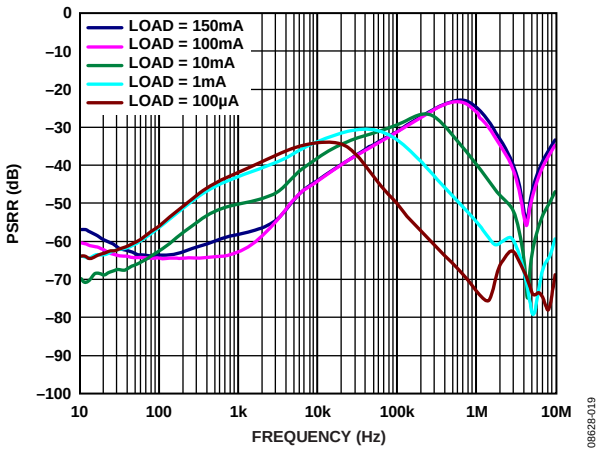

Figure 19. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 3.3 V, V_{IN} = 4.3 V

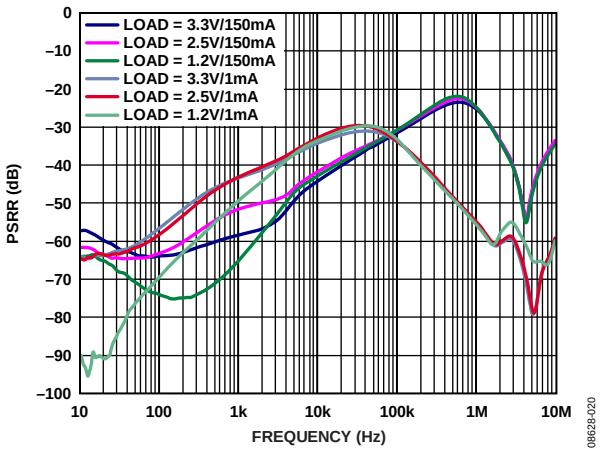

Figure 20. Power Supply Rejection Ratio vs. Frequency
Various Output Voltages and Load Currents, $V_{IN} - V_{OUT}$ = 1 V

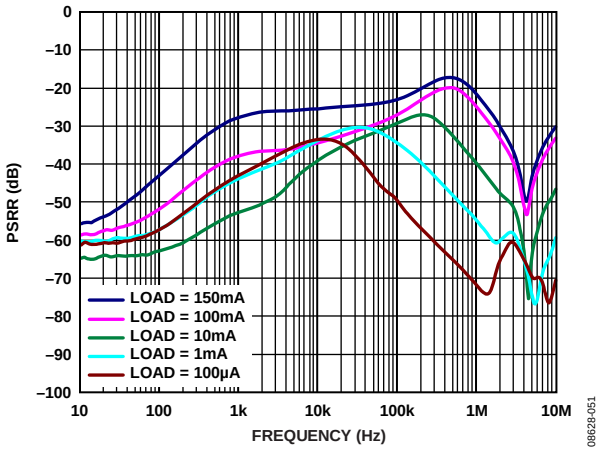

Figure 21. Power Supply Rejection Ratio vs. Frequency
Various Output Voltages and Load Currents, V_{OUT} = 2.5 V, V_{IN} = 3.0 V

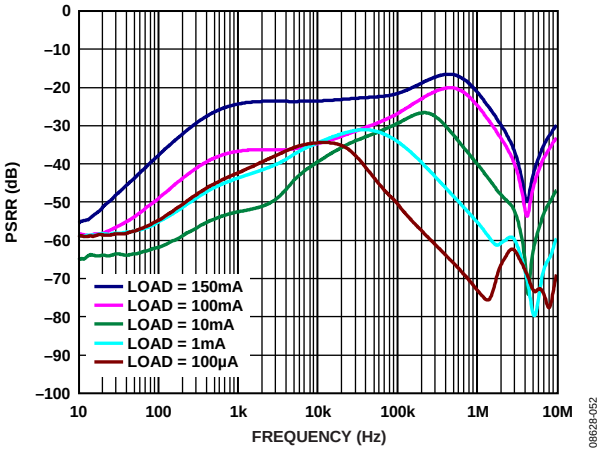

Figure 22. Power Supply Rejection Ratio vs. Frequency
Various Output Voltages and Load Currents, V_{OUT} = 3.3 V, V_{IN} = 3.8 V

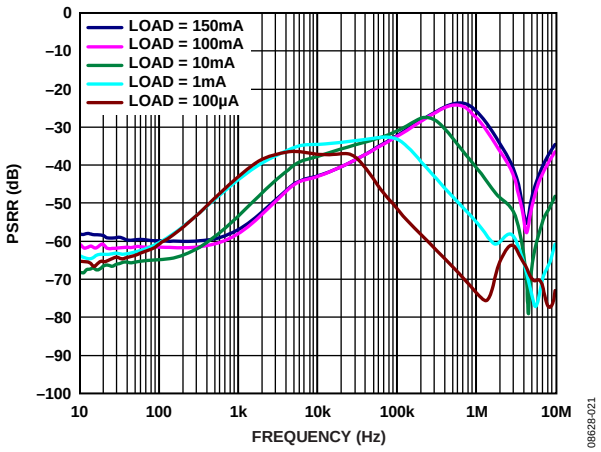

Figure 23. Adjustable ADP161 Power Supply Rejection Ratio vs. Frequency,
V_{OUT} = 3.3 V, V_{IN} = 4.3 V

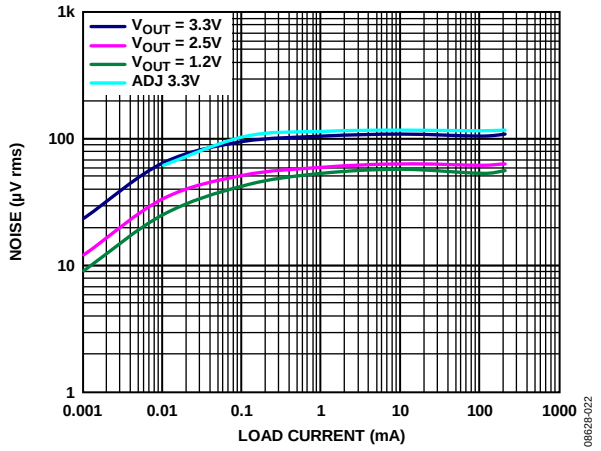

Figure 24. Output Noise vs. Load Current and Output Voltage,
V_{IN} = 5 V, C_{OUT} = 1 µF

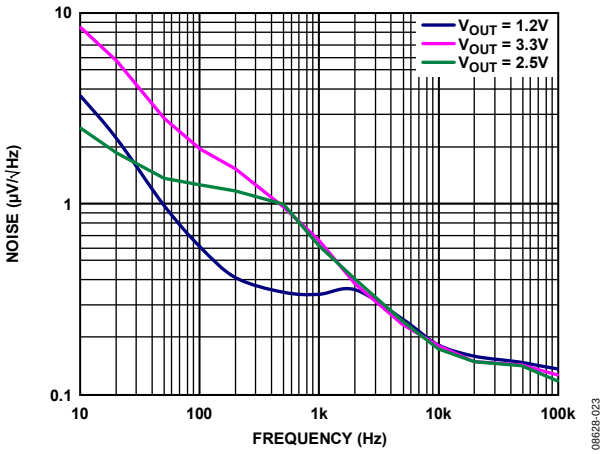

Figure 25. Output Noise Spectral Density, V_{IN} = 5 V, I_{LOAD} = 10 mA, C_{OUT} = 1 µF

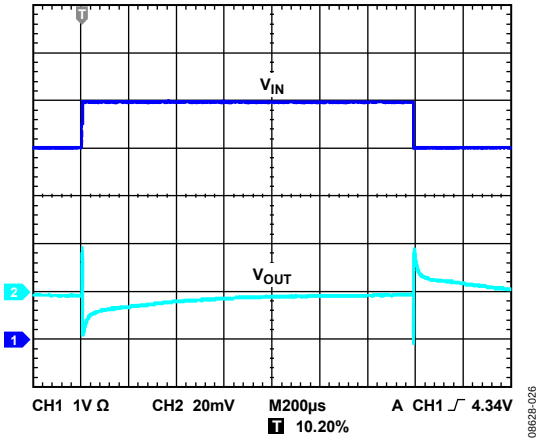

Figure 28. Line Transient Response, V_{IN} = 4 V to 5 V, C_{IN} = C_{OUT} = 1 µF, I_{LOAD} = 150 mA, CH1 = V_{IN}, CH2 = V_{OUT}

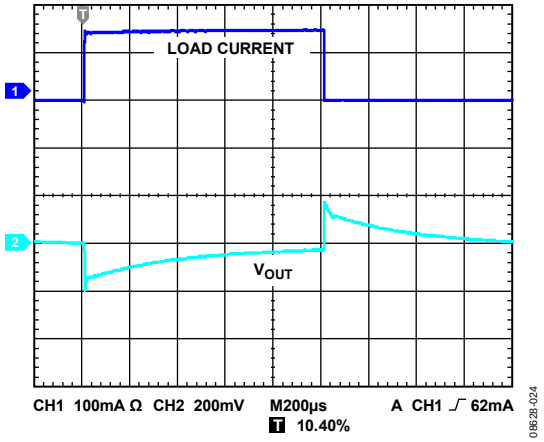

Figure 26. Load Transient Response, C_{IN}, C_{OUT} = 1 µF, I_{LOAD} = 1 mA to 150 mA, 200 ns Rise Time, CH1 = Load Current, CH2 = V_{OUT}

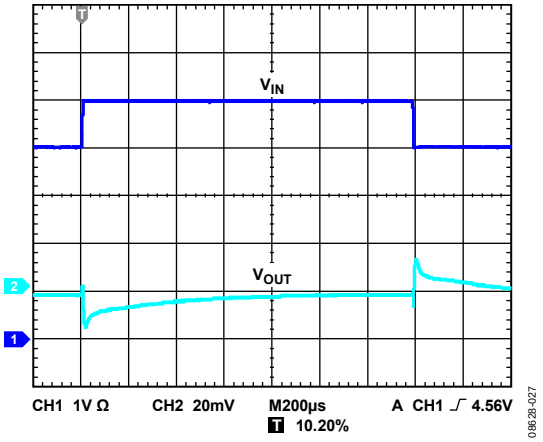

Figure 29. Line Transient Response, V_{IN} = 4 V to 5 V, C_{IN}, = 1 µF, C_{OUT} = 10 µF, I_{LOAD} = 150 mA, CH1 = V_{IN}, CH2 = V_{OUT}

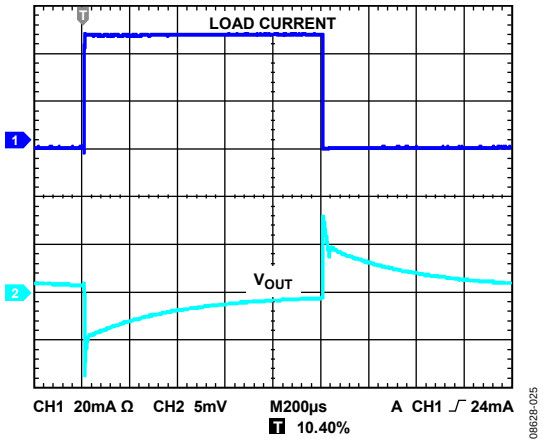

Figure 27. Load Transient Response, C_{IN}, C_{OUT} = 1 µF, I_{LOAD} = 1 mA to 50 mA, 200 ns Rise Time, CH1 = Load Current, CH2 = V_{OUT}

THEORY OF OPERATION

The ADP16x are ultralow quiescent current, low dropout linear regulators that operate from 2.2 V to 5.5 V and can provide up to 150 mA of output current. Drawing only 560 nA (typical) at no load and a low 42 µA of quiescent current (typical) at full load makes the ADP16x ideal for battery-operated portable equipment. Shutdown current consumption is typically 50 nA.

Using new innovative design techniques, the ADP16x provide ultralow quiescent current and superior transient performance for digital and RF applications. The ADP16x are also optimized for use with small 1 µF ceramic capacitors.

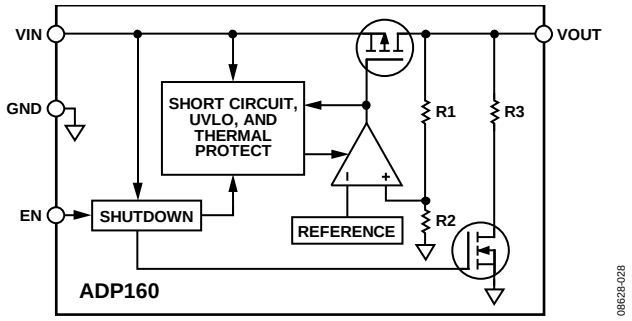

Figure 30. Internal Block Diagram, Fixed Output with Output Discharge Function

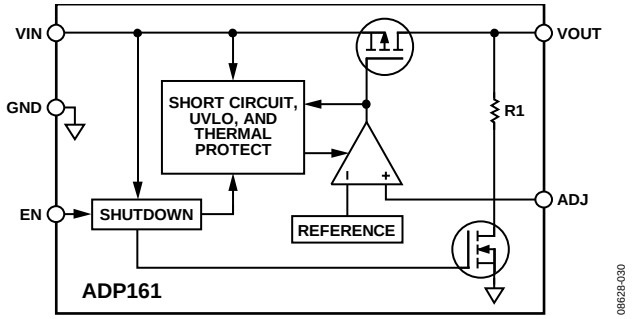

Figure 31. Internal Block Diagram, Adjustable Output with Output Discharge Function

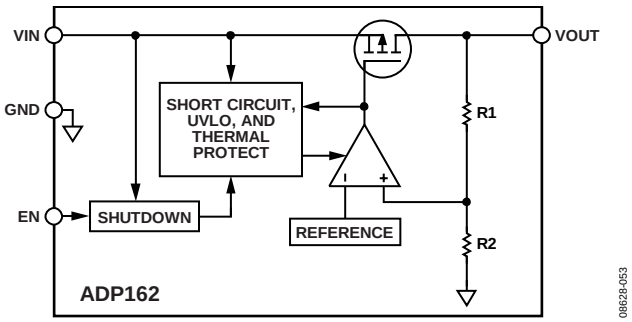

Figure 32. Internal Block Diagram, Fixed Output without Output Discharge Function

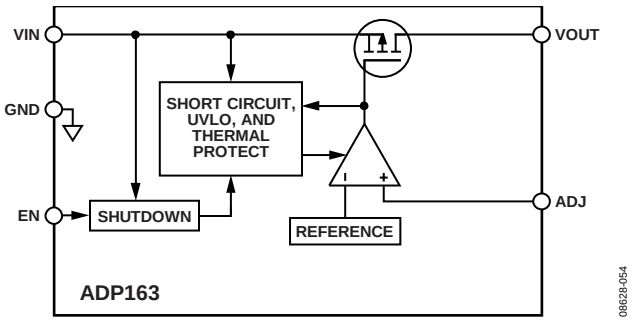

Figure 33. Internal Block Diagram, Adjustable Output without Output Discharge Function

Internally, the ADP16x consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The adjustable ADP161/ADP163 have an output voltage range of 1.0 V to 4.2 V. The output voltage is set by the ratio of two external resistors, as shown in Figure 2. The device servos the output to maintain the voltage at the ADJ pin at 1.0 V referenced to ground. The current in R1 is then equal to 1.0 V/R2, and the current in R1 is the current in R2 plus the ADJ pin bias current. The ADJ pin bias current, 10 nA at 25°C, flows through R1 into the ADJ pin.

The output voltage can be calculated using the equation:

$$V_{OUT} = 1.0\ V(1 + R1/R2) + (ADJ_{I\text{-}BIAS})(R1)$$

The value of R1 should be less than 200 kΩ to minimize errors in the output voltage caused by the ADJ pin bias current. For example, when R1 and R2 each equal 200 kΩ, the output voltage is 2.0 V. The output voltage error introduced by the ADJ pin bias current is 2 mV or 0.05%, assuming a typical ADJ pin bias current of 10 nA at 25°C.

To minimize quiescent current in the ADP161 and ADP163 Analog Devices, Inc., recommends using high values of resistance for R1 and R2. Using a value of 1 MΩ for R2 keeps the total, no load quiescent current below 2 µA. Note however, that high value of resistance introduces a small output voltage error. For example, assuming R1 and R2 are 1 MΩ, the output voltage is 2 V. Taking into account the nominal ADJ pin bias current of 10 nA, the output voltage error is 0.25%.

Note that in shutdown, the output is turned off and the divider current is zero.

The ADP160/ADP161 also include an output discharge resistor to force the output voltage to zero when the LDO is disabled. This ensures that the output of the LDO is always in a well-defined state, whether it is enabled or not. The ADP162/ADP163 do not include the output discharge function.

The ADP160/ADP162 are available in 15 output voltage options, ranging from 1.2 V to 4.2 V. The ADP16x use the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on, and when EN is low, VOUT turns off. For automatic startup, EN can be tied to VIN.

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP16x are designed for operation with small, space-saving ceramic capacitors, but function with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum of 1 µF capacitance with an ESR of 1 Ω or less is recommended to ensure stability of the ADP16x. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP16x to large changes in load current. Figure 34 and Figure 35 show the transient responses for output capacitance values of 1 µF and 10 µF, respectively.

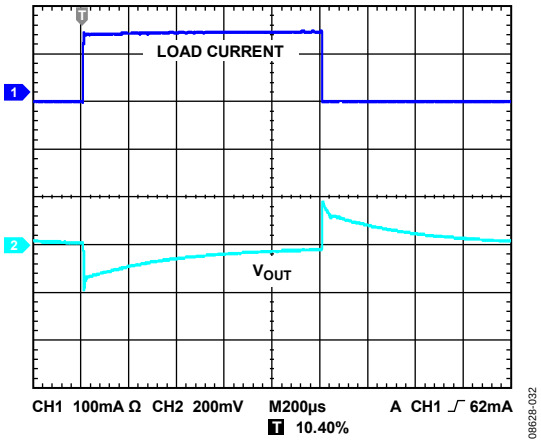

Figure 34. Output Transient Response, C_{OUT} = 1 µF, CH1 = Load Current, CH2 = V_{OUT}

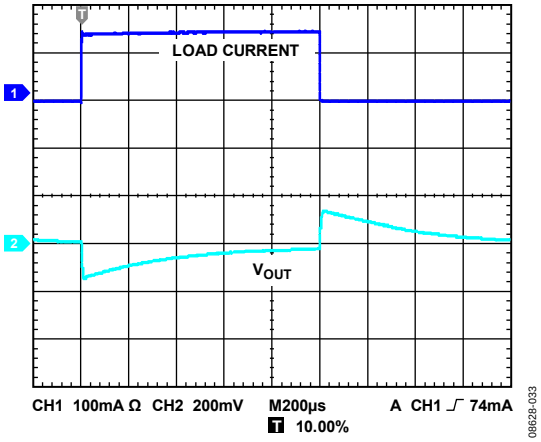

Figure 35. Output Transient Response, C_{OUT} = 10 µF, CH1 = Load Current, CH2 = V_{OUT}

Input Bypass Capacitor

Connecting a 1 µF capacitor from VIN to GND reduces the circuit sensitivity to the printed circuit board (PCB) layout, especially when long input traces or high source impedance are encountered. If greater than 1 µF of output capacitance is required, the input capacitor should be increased to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP16x, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended due to their poor temperature and dc bias characteristics.

Figure 36 depicts the capacitance vs. voltage bias characteristic of a 0402, 1 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

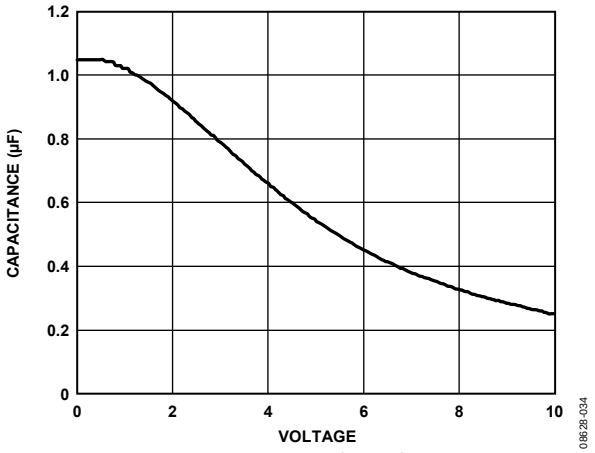

Figure 36. Capacitance vs. Voltage Characteristic

Use Equation 1 to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:

C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 0.94 µF at 1.8 V, as shown in Figure 36.

Substituting these values in Equation 1 yields

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP16x, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors are evaluated for each.

ENABLE FEATURE

The ADP16x use the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 37, when a rising voltage on EN crosses the active threshold, VOUT turns on. When a falling voltage on EN crosses the inactive threshold, VOUT turns off.

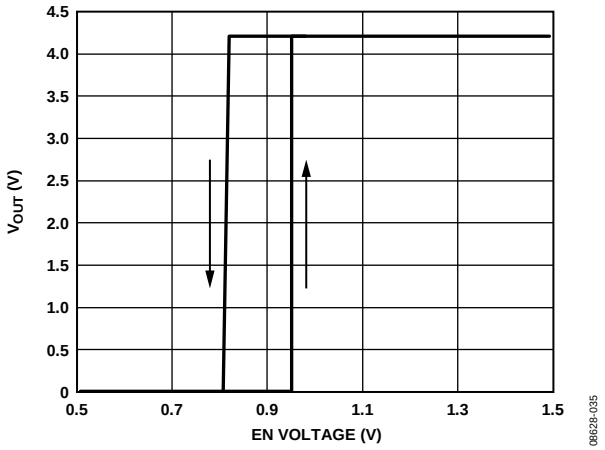

Figure 37. Typical EN Pin Operation

As shown in Figure 37, the EN pin has hysteresis built in. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds are derived from the VIN voltage. Therefore, these thresholds vary with changing input voltage. Figure 38 shows typical EN active/inactive thresholds when the input voltage varies from 2.2 V to 5.5 V.

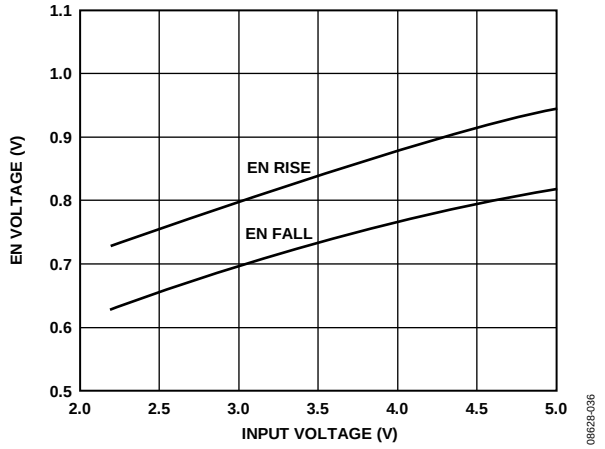

Figure 38. Typical EN Pin Thresholds vs. Input Voltage

The start-up behavior of the ADP16x is shown in Figure 39.

The shutdown behavior of the ADP160/ADP161 is shown in Figure 40.

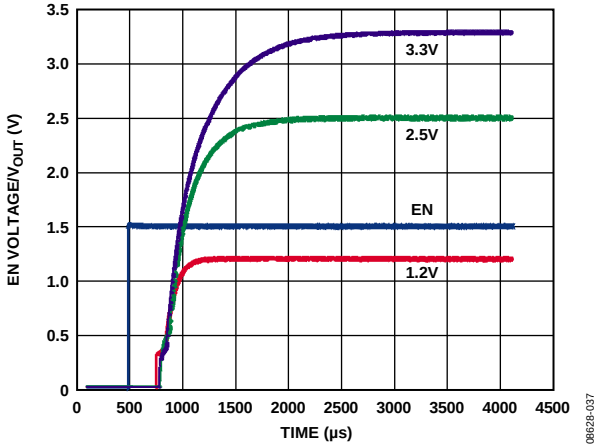

Figure 39. Typical Start-Up Behavior (ADP16x)

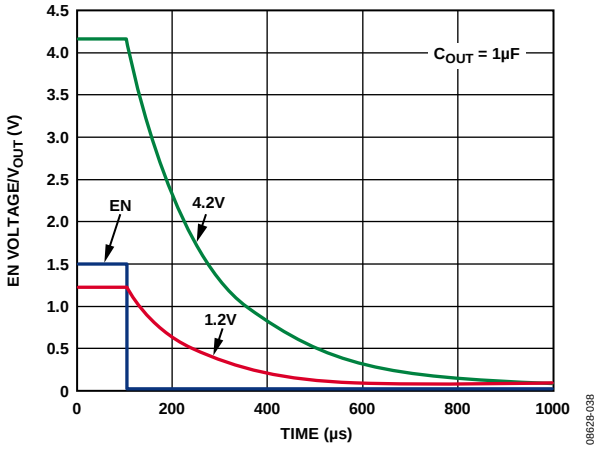

Figure 40. Typical Shutdown Behavior, No Load (ADP160/ADP161)

CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP16x are protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP16x are designed to current limit when the output load reaches 320 mA (typical). When the output load exceeds 320 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation), when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C, the output is turned on again and the output current is restored to its nominal value.

Consider the case where a hard short from OUT to ground occurs. At first, the ADP16x current limit so that only 320 mA is conducted into the short. If self-heating of the junction is great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 320 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 320 mA and 0 mA that continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so junction temperatures do not exceed 125°C.

THERMAL CONSIDERATIONS

In most applications, the ADP16x do not dissipate much heat due to their high efficiency. However, in applications with high ambient temperature and high supply voltage to output voltage differential, the heat dissipated in the package is large enough that it can cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 150°C, the converter enters thermal shutdown. It recovers only after the junction temperature has decreased below 135°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADP16x must not exceed 125°C. To ensure the junction temperature stays below this maximum value, the user needs to be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pins to the PCB. Table 8 shows the typical θ_{JA} values of the 5-lead TSOT and the 4-ball WLCSP for various PCB copper sizes. Table 9 shows the typical Ψ_{JB} value of the 5-lead TSOT and 4-ball WLCSP.

Table 8. Typical θ_{JA} Values

	θ_{JA} (°C/W)	
Copper Size (mm²)	**TSOT**	**WLCSP**
0[1]	170	260
50	152	159
100	146	157
300	134	153
500	131	151

[1] Device soldered to minimum size pin traces.

Table 9. Typical Ψ_{JB} Values

Ψ_{JB} (°C/W)	
TSOT	**WLCSP**
42.8	58.4

The junction temperature of the ADP16x can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (3)$$

where:
I_{LOAD} is the load current.
I_{GND} is the ground current.
V_{IN} and V_{OUT} are input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input-to-output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure the junction temperature does not rise above 125°C. Figure 41 to Figure 48 show the junction temperature calculations for the different ambient temperatures, load currents, V_{IN}-to-V_{OUT} differentials, and areas of PCB copper.

In the case where the board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise (see Figure 49 and Figure 50). Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

The typical value of Ψ_{JB} is 58°C/W for the 4-ball WLCSP package and 43°C/W for the 5-lead TSOT package.

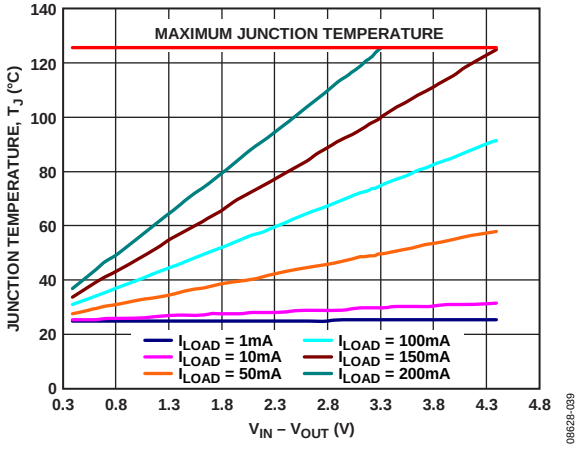

Figure 41. 500 mm² of PCB Copper, WLCSP, T_A = 25°C

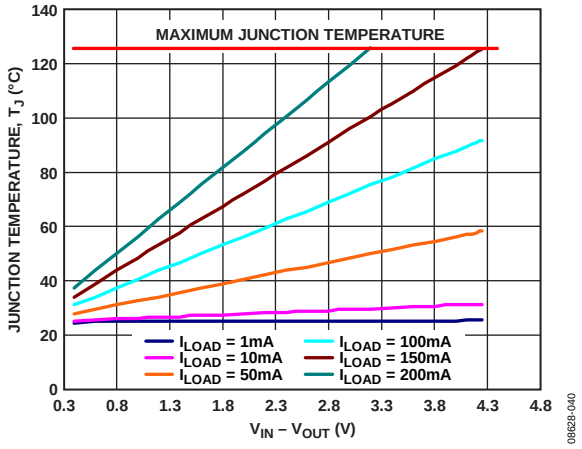

Figure 42. 100 mm² of PCB Copper, WLCSP, T_A = 50°C

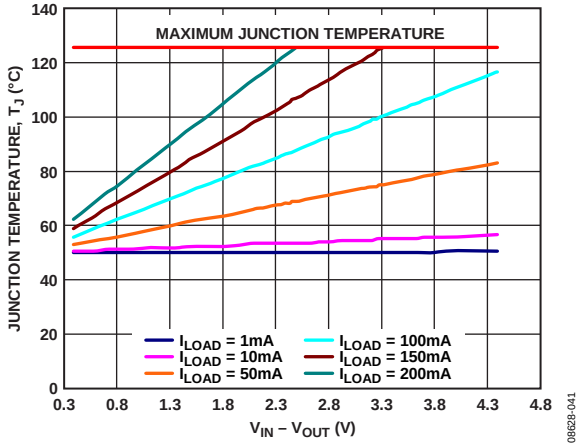

Figure 43. 500 mm² of PCB Copper, WLCSP, T_A = 85°C

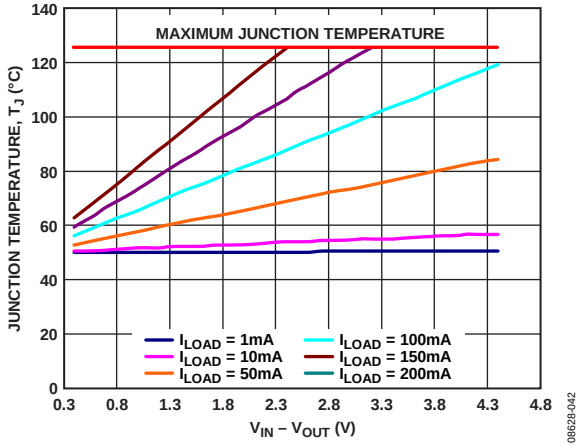

Figure 44. 100 mm² of PCB Copper, WLCSP, T_A = 50°C

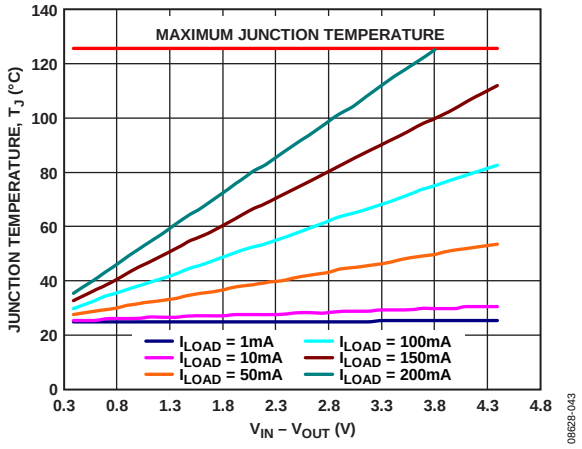

Figure 45. 500 mm² of PCB Copper, TSOT, T_A = 25°C

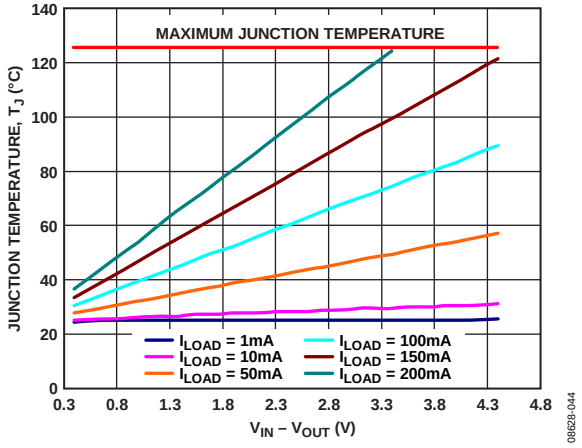

Figure 46. 100 mm² of PCB Copper, TSOT, T_A = 25°C

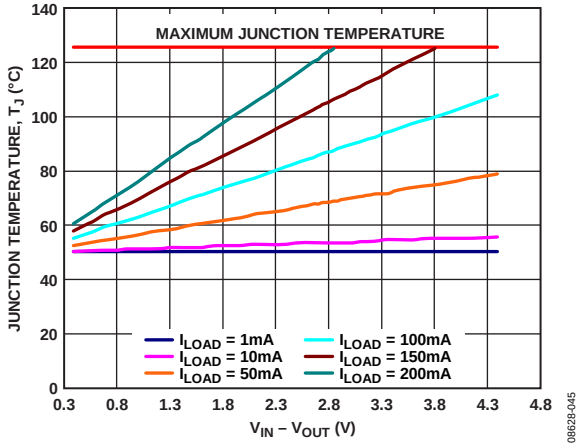

Figure 47. 500 mm² of PCB Copper, TSOT, T_A = 50°C

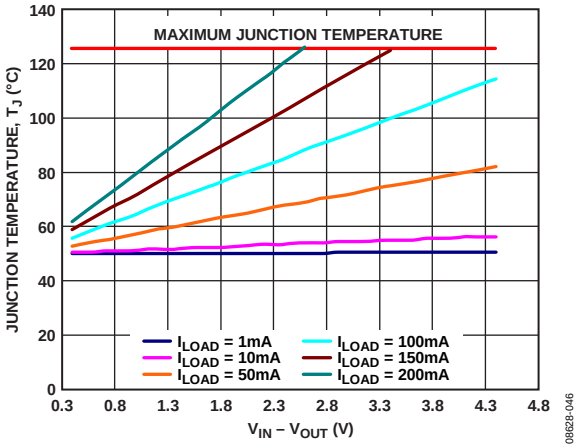

Figure 48. 100 mm² of PCB Copper, TSOT, T_A = 50°C

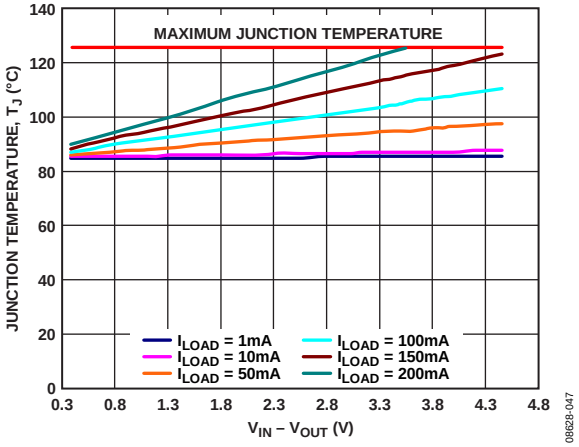

Figure 49. WLCSP, T_A = 85°C

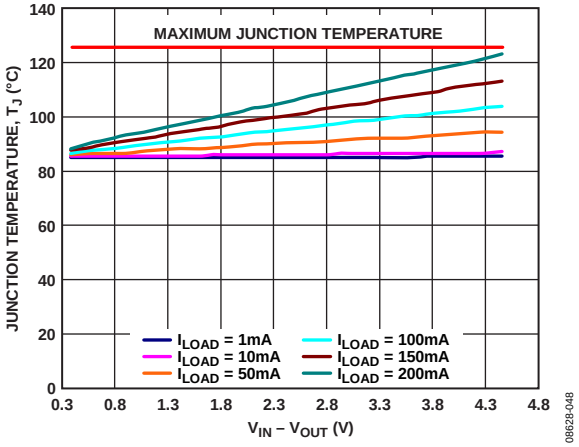

Figure 50. TSOT, T_A = 85°C

PCB LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP16x. However, as listed in Table 8, a point of diminishing returns is reached eventually, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Use of 0402 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

LIGHT SENSITIVITY OF WLCSPs

The WLCSP package option is essentially a silicon die with additional post fabrication dielectric and metal processing designed to contact solder bumps on the active side of the chip. With this package type, the die is exposed to ambient light and is subject to photoelectric effects. Light sensitivity analysis of a WLCSP mounted on standard PCB material reveals that performance may be impacted when the package is illuminated directly by high intensity light. No degradation in electrical performance is observed due to illumination by low intensity (0.1 mW/cm²) ambient light. Direct sunlight can have intensities of 50 mW/cm², office ambient light can be as low as 0.1 mW/cm².

When the WLCSP is assembled on the board with the bump side of the die facing the PCB, reflected light from the PCB surface is incident on active silicon circuit areas and results in the increased leakage currents. No performance degradation occurs due to illumination of the backside (substrate) of the WLCSP.

All WLCSPs are particularly sensitive to incident light with wavelengths in the near infrared range (NIR, 700 nm to 1000 nm). Photons in this waveband have a longer wavelength and lower energy than photons in the visible (400 nm to 700 nm) and near ultraviolet (NUV, 200 nm to 400 nm) bands; therefore, they can penetrate more deeply into the active silicon.

Incident light with wavelengths greater than 1100 nm has no photoelectric effect on silicon devices because silicon is transparent to wavelengths in this range.

The spectral content of conventional light sources varies considerably. Sunlight has a broad spectral range, with peak intensity in the visible band that falls off in the NUV and NIR bands; fluorescent lamps have significant peaks in the visible but not the NUV or NIR bands. Tungsten lighting has a broad peak in the longer visible wavelengths with a significant tail in the NIR.

Efforts have been made at a product level to reduce the effect of ambient light; the under bump metal (UBM) has been designed to shield the sensitive circuit areas on the active side (bump side) of the die. However, if an application encounters any light sensitivity with the WLCSP, shielding the bump side of the WLCSP package with opaque material should eliminate this effect. Shielding can be accomplished using materials such as silica-filled liquid epoxies like those used in flip-chip underfill techniques.

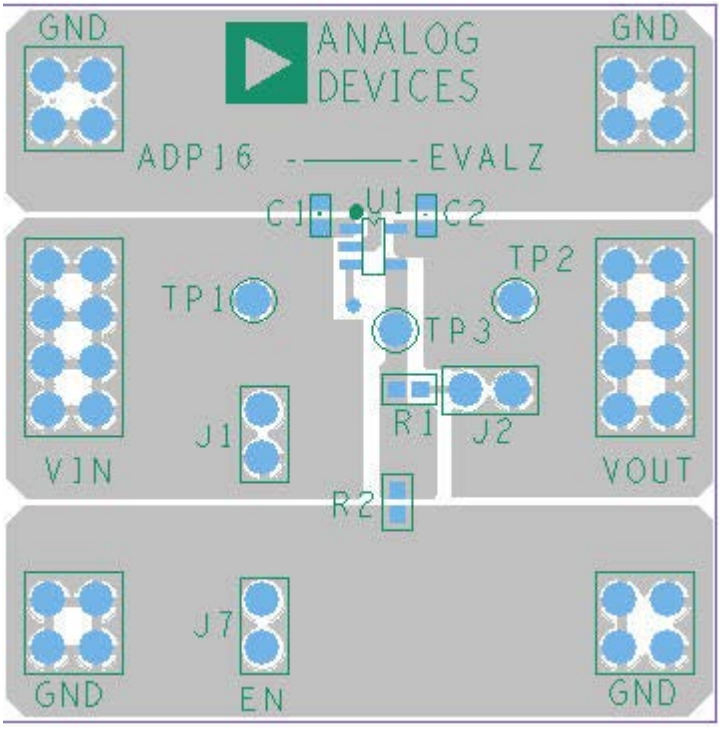

Figure 51. Example of 5-Lead TSOT PCB Layout

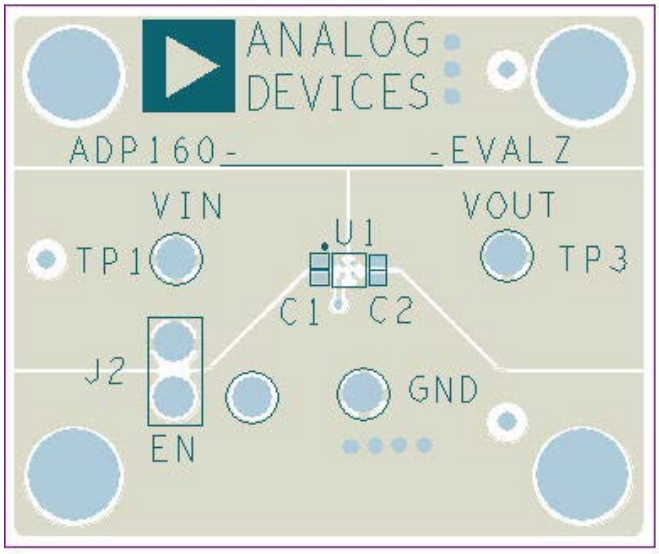

Figure 52. Example of 4-Ball WLCSP PCB Layout

OUTLINE DIMENSIONS

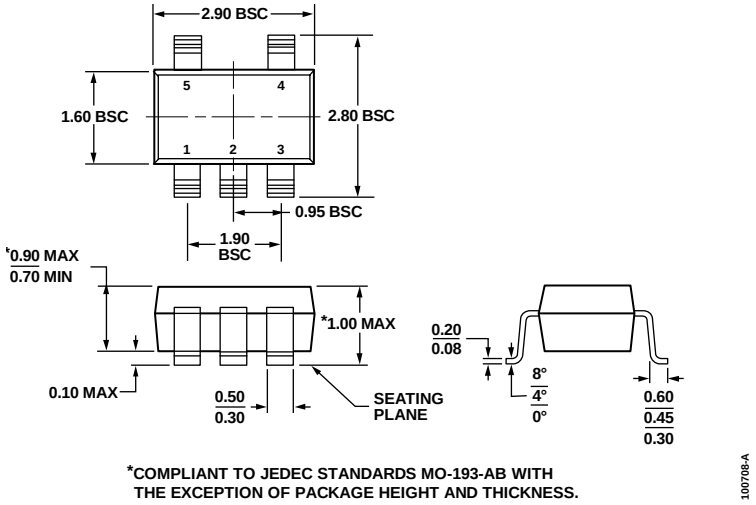

Figure 53. 5-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-5)
Dimensions shown in millimeters

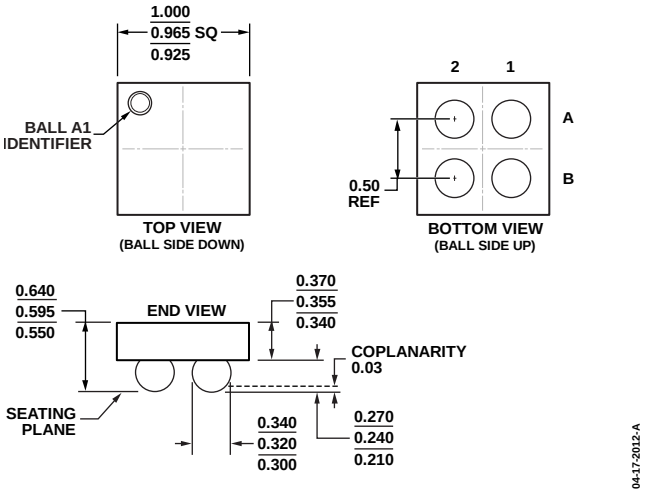

Figure 54. 4-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-4-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)	Package Description	Package Option	Branding
ADP160ACBZ-1.2-R7	−40°C to +125°C	1.2	4-Ball WLCSP	CB-4-1	5K
ADP160ACBZ-1.5-R7	−40°C to +125°C	1.5	4-Ball WLCSP	CB-4-1	5L
ADP160ACBZ-1.8-R7	−40°C to +125°C	1.8	4-Ball WLCSP	CB-4-1	5N
ADP160ACBZ-2.1-R7	−40°C to +125°C	2.1	4-Ball WLCSP	CB-4-1	5P
ADP160ACBZ-2.3-R7	−40°C to +125°C	2.3	4-Ball WLCSP	CB-4-1	AH
ADP160ACBZ-2.5-R7	−40°C to +125°C	2.5	4-Ball WLCSP	CB-4-1	5Q
ADP160ACBZ-2.7-R7	−40°C to +125°C	2.7	4-Ball WLCSP	CB-4-1	AM
ADP160ACBZ-2.75-R7	−40°C to +125°C	2.75	4-Ball WLCSP	CB-4-1	5R
ADP160ACBZ-2.8-R7	−40°C to +125°C	2.8	4-Ball WLCSP	CB-4-1	5S
ADP160ACBZ-2.85-R7	−40°C to +125°C	2.85	4-Ball WLCSP	CB-4-1	5T
ADP160ACBZ-3.0-R7	−40°C to +125°C	3.0	4-Ball WLCSP	CB-4-1	5U
ADP160ACBZ-3.3-R7	−40°C to +125°C	3.3	4-Ball WLCSP	CB-4-1	5V
ADP160ACBZ-4.2-R7	−40°C to +125°C	4.2	4-Ball WLCSP	CB-4-1	6U
ADP160AUJZ-1.2-R7	−40°C to +125°C	1.2	5-Lead TSOT	UJ-5	LDQ
ADP160AUJZ-1.5-R7	−40°C to +125°C	1.5	5-Lead TSOT	UJ-5	LDR
ADP160AUJZ-1.8-R7	−40°C to +125°C	1.8	5-Lead TSOT	UJ-5	LE0
ADP160AUJZ-2.3-R7	−40°C to +125°C	2.3	5-Lead TSOT	UJ-5	LLP
ADP160AUJZ-2.5-R7	−40°C to +125°C	2.5	5-Lead TSOT	UJ-5	LFZ
ADP160AUJZ-2.7-R7	−40°C to +125°C	2.7	5-Lead TSOT	UJ-5	LJF
ADP160AUJZ-2.8-R7	−40°C to +125°C	2.8	5-Lead TSOT	UJ-5	LG0
ADP160AUJZ-3.0-R7	−40°C to +125°C	3.0	5-Lead TSOT	UJ-5	Y2U
ADP160AUJZ-3.3-R7	−40°C to +125°C	3.3	5-Lead TSOT	UJ-5	LG1
ADP160AUJZ-4.2-R7	−40°C to +125°C	4.2	5-Lead TSOT	UJ-5	LGY
ADP161AUJZ-R7	−40°C to +125°C	Adjustable	5-Lead TSOT	UJ-5	LHW
ADP162ACBZ-1.2-R7	−40°C to +125°C	1.2	4-Ball WLCSP	CB-4-1	70
ADP162ACBZ-1.8-R7	−40°C to +125°C	1.8	4-Ball WLCSP	CB-4-1	71
ADP162ACBZ-2.1-R7	−40°C to +125°C	2.1	4-Ball WLCSP	CB-4-1	72
ADP162ACBZ-2.3-R7	−40°C to +125°C	2.3	4-Ball WLCSP	CB-4-1	BC
ADP162ACBZ-2.8-R7	−40°C to +125°C	2.8	4-Ball WLCSP	CB-4-1	73
ADP162ACBZ-3.0-R7	−40°C to +125°C	3.0	4-Ball WLCSP	CB-4-1	74
ADP162ACBZ-4.2-R7	−40°C to +125°C	4.2	4-Ball WLCSP	CB-4-1	75
ADP162AUJZ-1.5-R7	−40°C to +125°C	1.5	5-Lead TSOT	UJ-5	LH9
ADP162AUJZ-1.8-R7	−40°C to +125°C	1.8	5-Lead TSOT	UJ-5	LLN
ADP162AUJZ-2.3-R7	−40°C to +125°C	2.3	5-Lead TSOT	UJ-5	LLQ
ADP162AUJZ-2.5-R7	−40°C to +125°C	2.5	5-Lead TSOT	UJ-5	LHB
ADP162AUJZ-2.7-R7	−40°C to +125°C	2.7	5-Lead TSOT	UJ-5	LJK
ADP162AUJZ-2.8-R7	−40°C to +125°C	2.8	5-Lead TSOT	UJ-5	LHC
ADP162AUJZ-3.0-R7	−40°C to +125°C	3.0	5-Lead TSOT	UJ-5	LHD
ADP162AUJZ-3.1-R7	−40°C to +125°C	3.1 V	5-Lead TSOT	UJ-5	LQE
ADP162AUJZ-3.3-R7	−40°C to +125°C	3.3	5-Lead TSOT	UJ-5	LHE
ADP162AUJZ-4.2-R7	−40°C to +125°C	4.2	5-Lead TSOT	UJ-5	LHF
ADP163AUJZ-R7	−40°C to +125°C	Adjustable	5-Lead TSOT	UJ-5	LHG
ADP160UJZ-REDYKIT			Evaluation Board Kit		
ADP162UJZ-REDYKIT			Evaluation Board Kit		
ADP161UJ-EVALZ			Evaluation Board		
ADP163UJ-EVALZ			Evaluation Board		

[1] Z = RoHS Compliant Part.

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