



# 5 V Low Power, Slew-Rate Limited RS-485/RS-422 Transceiver

## ADM483

### FEATURES

- EIA RS-485/RS-422-compliant
- Data rates up to 250 kbps
- Slew-rate limited for low EMI
- 100 nA supply current in shutdown mode
- Low power consumption (120  $\mu$ A)
- Up to 32 transceivers on one bus
- Outputs high-z when disabled or powered off
- 7 V to +12 V bus common-mode range
- Thermal shutdown and short-circuit protection
- Pin-compatible with MAX483
- Specified over -40°C to +85°C temperature range
- Available in 8-lead SOIC package

### APPLICATIONS

- Low power RS-485 applications
- EMI sensitive systems
- DTE-DCE interfaces
- Industrial control
- Packet switching
- Local area networks
- Level translators

### GENERAL DESCRIPTION

The ADM483 is a low power differential line transceiver suitable for half-duplex data communication on multipoint bus transmission lines. It is designed for balanced data transmission, and complies with EIA Standards RS-485 and RS-422. The part contains a differential line driver and a differential line receiver. Both share the same differential pins, with either the driver or the receiver being enabled at any given time.

The device has an input impedance of 12 k $\Omega$ , allowing up to 32 transceivers on one bus. Since only one driver should be enabled at any time, the output of a disabled or powered-down driver is three-stated to avoid overloading the bus. This high impedance driver output is maintained over the entire common-mode voltage range from -7 V to +12 V.

### FUNCTIONAL BLOCK DIAGRAM

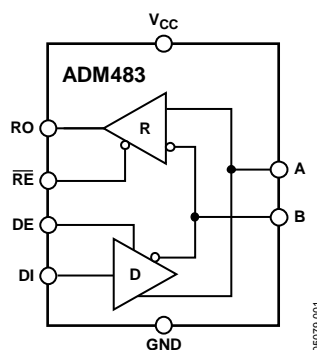


Figure 1.

The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

The driver outputs are slew-rate limited to reduce EMI and data errors caused by reflections from improperly terminated buses. Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit.

The part is fully specified over the industrial temperature range, and is available in an 8-lead SOIC package.

#### Rev. 0

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REVISION HISTORY

10/04—Revision 0: Initial Version

## SPECIFICATIONS

$V_{CC} = 5\text{ V} \pm 5\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>DRIVER</b>					
Differential Output Voltage, $V_{OD}$			5	V	$R = \infty$ , Figure 3
	2.0			V	$R = 50\ \Omega$ (RS-422), Figure 3
	1.5		5	V	$R = 27\ \Omega$ (RS-485), Figure 3
	1.5		5	V	$V_{TST} = -7\text{ V}$ to $12\text{ V}$ , Figure 4
$\Delta V_{OD} $ for Complementary Output States			0.2	V	$R = 27\ \Omega$ or $50\ \Omega$ , Figure 3
Common-Mode Output Voltage, $V_{OC}$			3	V	$R = 27\ \Omega$ or $50\ \Omega$ , Figure 3
$\Delta V_{OC} $ for Complementary Output States			0.2	V	$R = 27\ \Omega$ or $50\ \Omega$ , Figure 3
Output Short-Circuit Current, $V_{OUT} = \text{High}$	35		250	mA	$-7\text{ V} < V_{OUT} < +12\text{ V}$
Output Short-Circuit Current, $V_{OUT} = \text{Low}$	35		250	mA	$-7\text{ V} < V_{OUT} < +12\text{ V}$
<b>DRIVER INPUT LOGIC</b>					
CMOS Input Logic Threshold Low			0.8	V	
CMOS Input Logic Threshold High	2.0			V	
CMOS Logic Input Current (DI)			$\pm 2$	$\mu\text{A}$	
DE Input Resistance to GND		220		k $\Omega$	
<b>RECEIVER</b>					
Differential Input Threshold Voltage, $V_{TH}$	-200		+200	mV	$-7\text{ V} < V_{CM} < +12\text{ V}$
Input Hysteresis		70		mV	$V_{CM} = 0\text{ V}$
Input Resistance (A, B)	12			k $\Omega$	$-7\text{ V} < V_{CM} < +12\text{ V}$
Input Current (A, B)			1	mA	$V_{IN} = +12\text{ V}$
			-0.8	mA	$V_{IN} = -7\text{ V}$
CMOS Logic Input Current ( $\overline{RE}$ )			$\pm 2$	$\mu\text{A}$	
CMOS Output Voltage Low			0.4	V	$I_{OUT} = 4\text{ mA}$
CMOS Output Voltage High	3.5			V	$I_{OUT} = -4\text{ mA}$
Output Short-Circuit Current	7		95	mA	$0\text{ V} < V_{OUT} < V_{CC}$
Three-State Output Leakage Current			$\pm 2$	$\mu\text{A}$	$0.4 \leq V_{OUT} \leq 2.4\text{ V}$
<b>POWER SUPPLY CURRENT</b>					
		0.1	10	$\mu\text{A}$	$DE = 0\text{ V}$ , $\overline{RE} = V_{CC}$ (shutdown)
		120	250	$\mu\text{A}$	$DE = 0\text{ V}$ , $\overline{RE} = 0\text{ V}$
		350	650	$\mu\text{A}$	$DE = V_{CC}$

## TIMING SPECIFICATIONS

$V_{CC} = 5\text{ V} \pm 5\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>DRIVER</b>					
Maximum Data Rate	250			kbps	
Propagation Delay $t_{PLH}$ , $t_{PHL}$	250	800	2000	ns	$R_{LDIFF} = 54\ \Omega$ , $C_{L1} = C_{L2} = 100\text{ pF}$ , Figure 5
Skew $t_{SKEW}$		100	800	ns	$R_{LDIFF} = 54\ \Omega$ , $C_{L1} = C_{L2} = 100\text{ pF}$ , Figure 5
Rise/Fall Time $t_R$ , $t_F$	200		2000	ns	$R_{LDIFF} = 54\ \Omega$ , $C_{L1} = C_{L2} = 100\text{ pF}$ , Figure 5
Enable Time	125		2000	ns	$R_L = 500\ \Omega$ , $C_L = 100\text{ pF}$ , Figure 6
Disable Time	125		3000	ns	$R_L = 500\ \Omega$ , $C_L = 15\text{ pF}$ , Figure 6
Enable Time from Shutdown			5000	ns	$R_L = 500\ \Omega$ , $C_L = 100\text{ pF}$ , Figure 6
<b>RECEIVER</b>					
Propagation Delay $t_{PLH}$ , $t_{PHL}$	250		2000	ns	$C_L = 15\text{ pF}$ , Figure 7
Differential Skew $t_{SKEW}$		100		ns	$C_L = 15\text{ pF}$ , Figure 7
Enable Time		20	50	ns	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , Figure 8
Disable Time		20	50	ns	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , Figure 8
Enable Time from Shutdown			5000	ns	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , Figure 8
Time to Shutdown <sup>1</sup>	50	330	3000	ns	

<sup>1</sup> The device is put into shutdown mode by driving  $\overline{RE}$  high and DE low. If these inputs are in this state for less than 50 ns, the device is guaranteed not to enter shutdown mode. If the enable inputs are in this state for at least 3000 ns, the device is guaranteed to have entered shutdown mode.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Rating
$V_{CC}$ to GND	6 V
Digital I/O Voltage (DE, $\overline{RE}$ , DI, ROUT)	$-0.3\text{ V to }V_{CC} + 0.3\text{ V}$
Driver Output/Receiver Input Voltage	$-9\text{ V to }+14\text{ V}$
Operating Temperature Range	$-40^\circ\text{C to }+85^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+125^\circ\text{C}$
$\theta_{JA}$ Thermal Impedance (SOIC)	$110^\circ\text{C/W}$
Lead Temperature	
Soldering (10 s)	$300^\circ\text{C}$
Vapor Phase (60 s)	$215^\circ\text{C}$
Infrared (15 s)	$220^\circ\text{C}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

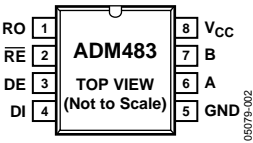


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output. When enabled, if A > B by 200 mV, then RO = high. If A < B by 200 mV, then RO = low.
2	$\overline{\text{RE}}$	Receiver Output Enable. A low level enables the receiver output, RO. A high level places it in a high impedance state.
3	DE	Driver Output Enable. A high level enables the driver differential inputs A and B. A low level places it in a high impedance state.
4	DI	Driver Input. When the driver is enabled, a logic low on DI forces A low and B high, while a logic high on DI forces A high and B low.
5	GND	Ground.
6	A	Noninverting Receiver Input A/Driver Output A.
7	B	Inverting Receiver Input B/Driver Output B.
8	V <sub>CC</sub>	5 V Power Supply.

## TEST CIRCUITS

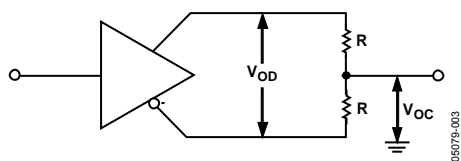


Figure 3. Driver Voltage Measurement

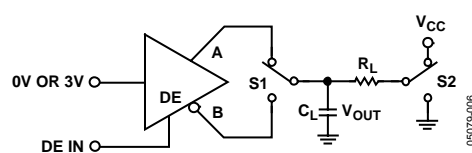


Figure 6. Driver Enable/Disable

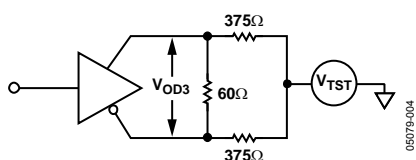


Figure 4. Driver Voltage Measurement over Common-Mode Voltage Range

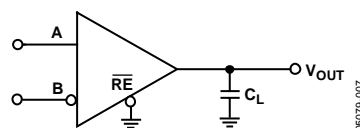


Figure 7. Receiver Propagation Delay

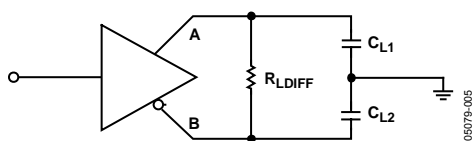


Figure 5. Driver Propagation Delay

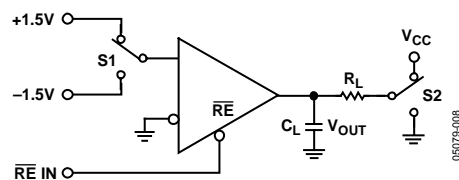


Figure 8. Receiver Enable/Disable

## SWITCHING CHARACTERISTICS

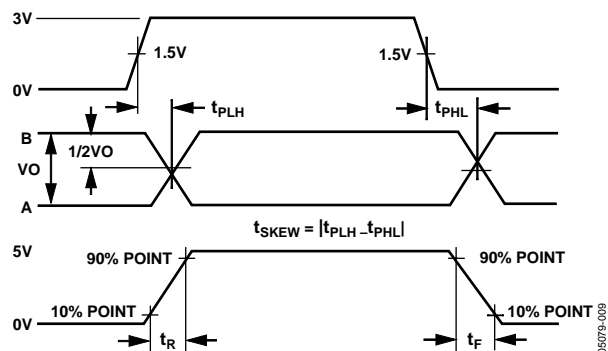


Figure 9. Driver Propagation Delay, Rise/Fall Timing

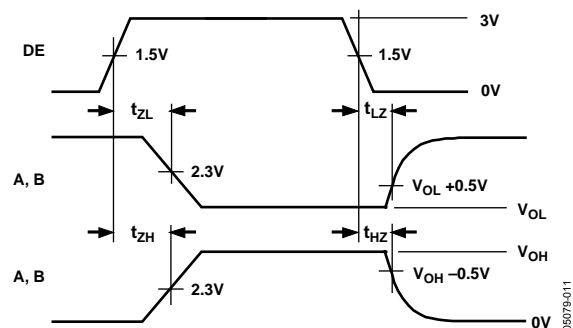


Figure 11. Driver Enable/Disable Timing

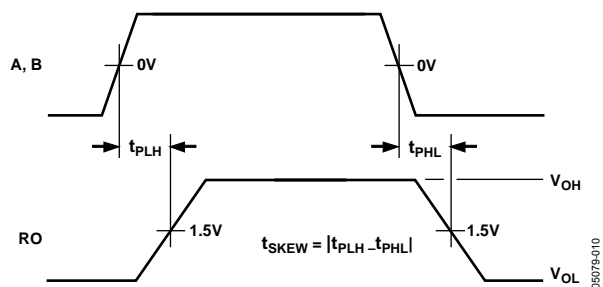


Figure 10. Receiver Propagation Delay

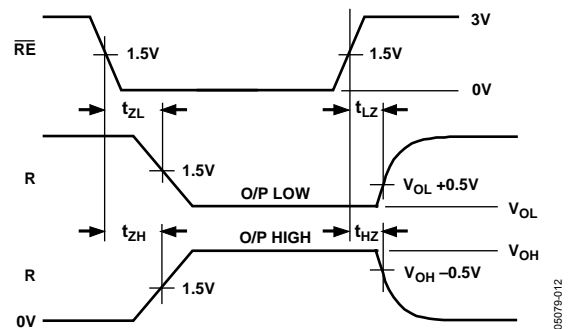


Figure 12. Receiver Enable/Disable Timing



# TYPICAL PERFORMANCE CHARACTERISTICS

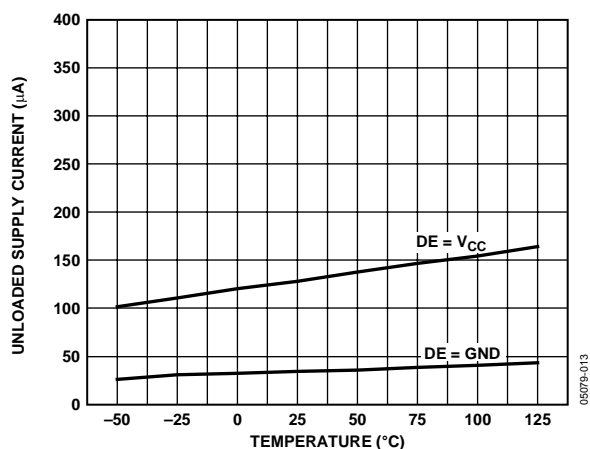


Figure 13. Supply Current vs. Temperature

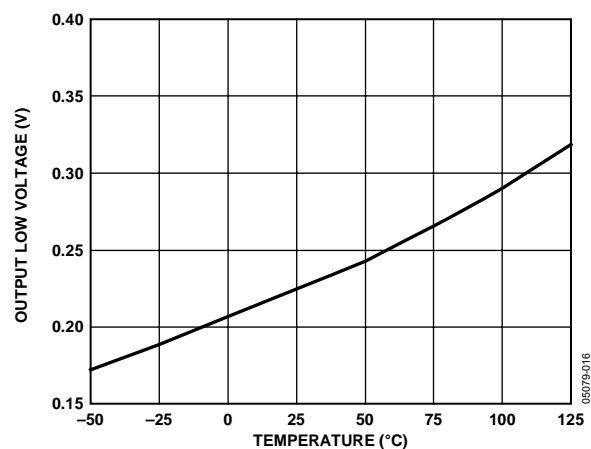


Figure 16. Receiver Output Low Voltage vs. Temperature

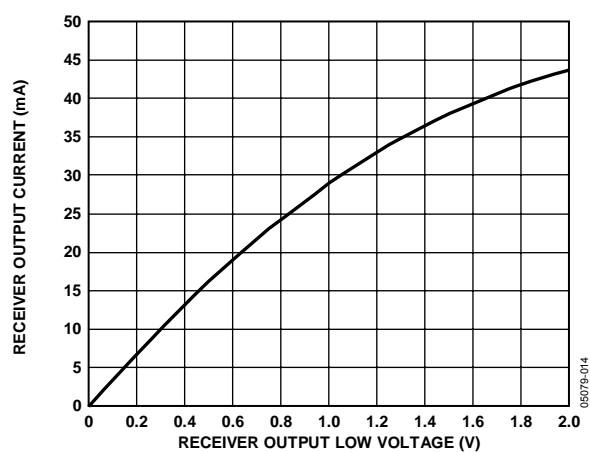


Figure 14. Output Current vs. Receiver Output Low Voltage

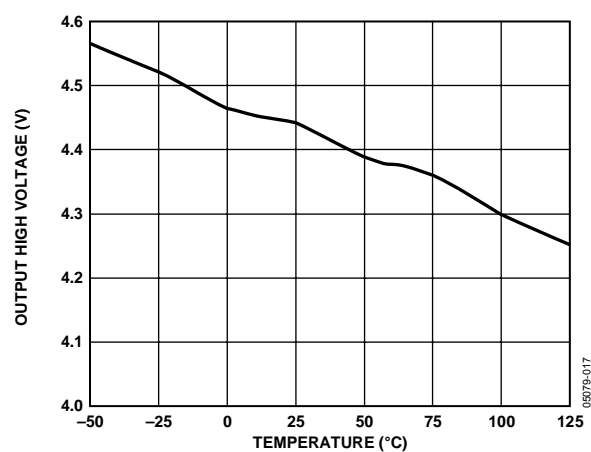


Figure 17. Receiver Output High Voltage vs. Temperature

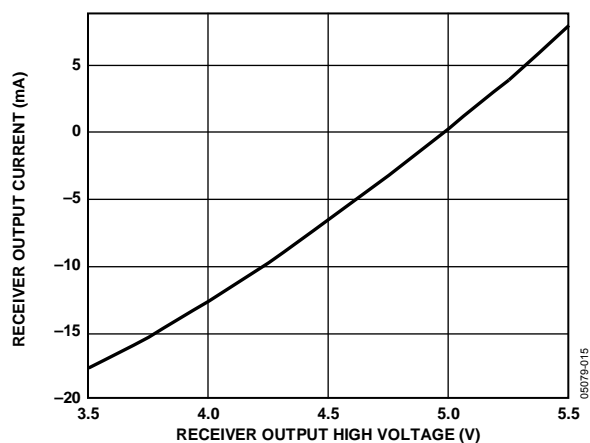


Figure 15. Output Current vs. Receiver Output High Voltage

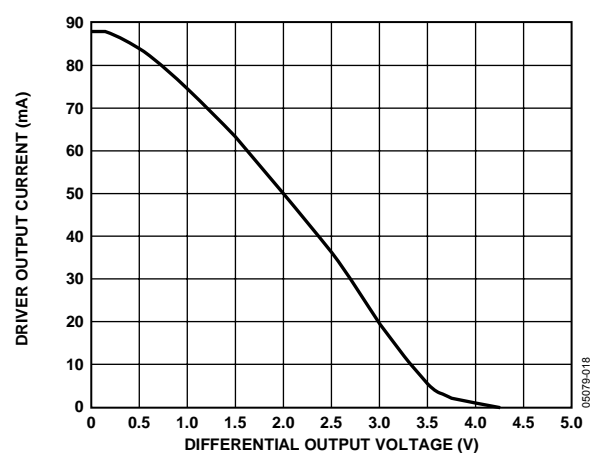


Figure 18. Driver Output Current vs. Differential Output Voltage

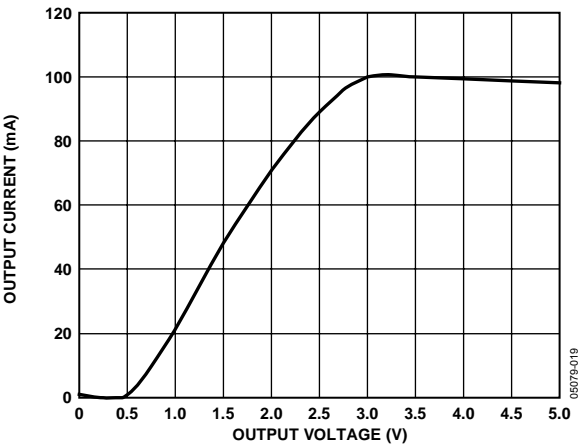


Figure 19. Output Current vs. Driver Output Low Voltage

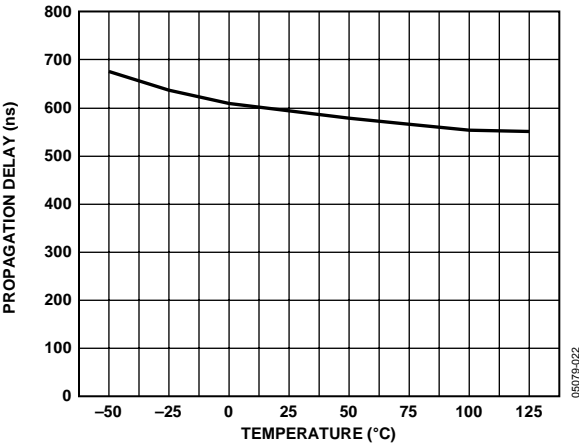


Figure 22. Receiver Propagation Delay vs. Temperature

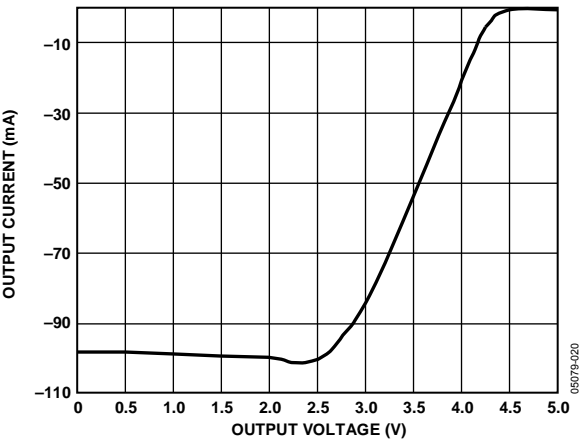


Figure 20. Output Current vs. Driver Output High Voltage

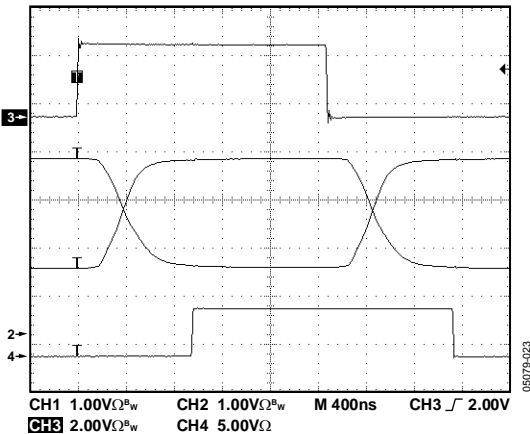


Figure 23. Driver/Receiver Propagation Delay

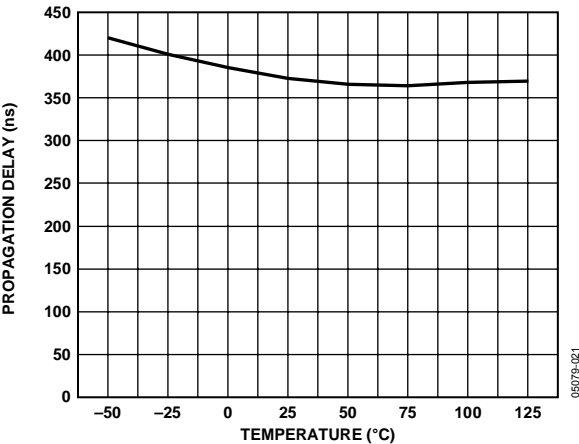


Figure 21. Driver Propagation Delay vs. Temperature

## APPLICATIONS

### DIFFERENTIAL DATA TRANSMISSION

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals that appear as common-mode voltages on the line. There are two main standards approved by the Electronics Industries Association (EIA), which specify the electrical characteristics of transceivers used in differential data transmission.

The RS-422 standard specifies data rates up to 10 Mbaud and line lengths up to 4000 ft. A single driver can drive a transmission line with up to 10 receivers.

To achieve true multipoint communications, the RS-485 standard was defined. This standard meets or exceeds all the requirements of RS-422, but also allows up to 32 drivers and 32 receivers to be connected to a single bus. An extended common-mode range of  $-7\text{ V}$  to  $+12\text{ V}$  is defined. The most significant difference between RS-422 and RS-485 is that the drivers may be disabled, allowing up to 32 to be connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

Table 5. Comparison of RS-422 and RS-485 Interface Standards

Specification	RS-422	RS-485
Transmission Type	Differential	Differential
Maximum Cable Length	4000 ft.	4000 ft.
Minimum Driver Output Voltage	$\pm 2\text{ V}$	$\pm 1.5\text{ V}$
Driver Load Impedance	$100\ \Omega$	$54\ \Omega$
Receiver Input Resistance	$4\text{ k}\Omega$ min	$12\text{ k}\Omega$ min
Receiver Input Sensitivity	$\pm 200\text{ mV}$	$\pm 200\text{ mV}$
Receiver Input Voltage Range	$-7\text{ V}$ to $+7\text{ V}$	$-7\text{ V}$ to $+12\text{ V}$
Drivers/Receivers per Line	1/10	32/32

### CABLE AND DATA RATE

The preferred transmission line for RS-485 communications is a twisted pair. Twisted pair cable tends to cancel common-mode noise and the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.

The ADM483 is designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is shown in Figure 24. An RS-485 transmission line can have as many as 32 transceivers on the bus. Only one driver can transmit at a particular time, but multiple receivers can be enabled simultaneously. As with any transmission line, it is important to minimize reflections. This can be done by terminating the extreme ends of the line by using resistors equal to the characteristic impedance of the line. Stub lengths of the main line should also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.

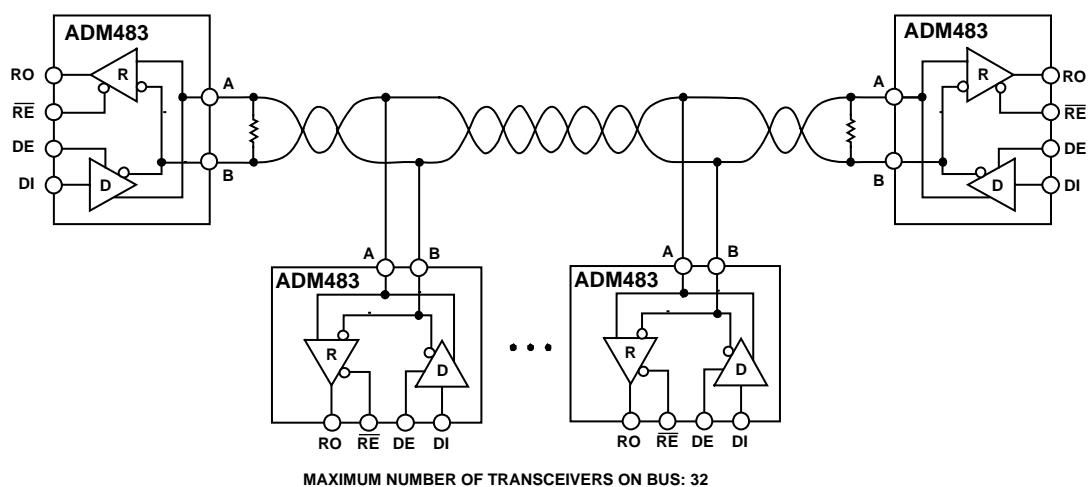


Figure 24. Typical Half-Duplex RS-485 Network Topology

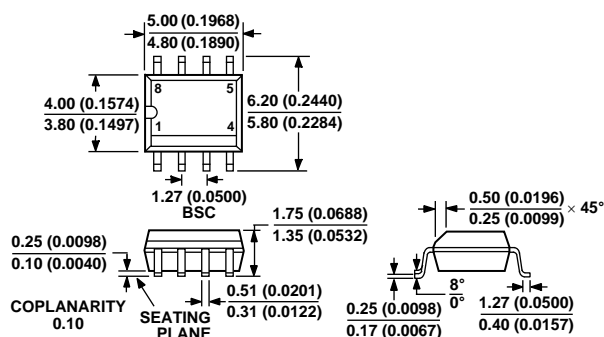
## THERMAL SHUTDOWN

The ADM483 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature and disables the driver outputs. The thermal sensing circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at 140°C.

## RECEIVER OPEN-CIRCUIT FAIL-SAFE

The receiver input includes a fail-safe feature that guarantees a logic high on the receiver when the inputs are open circuit or floating.

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 25. 8-Lead Standard Small Outline Package [SOIC]  
(R-8)

Dimensions shown in millimeters and (inches)

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM483AR	−40°C to +85°C	8-Lead Standard Small Outline Package	R-8
ADM483AR-REEL	−40°C to +85°C	8-Lead Standard Small Outline Package	R-8
ADM483AR-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package	R-8
ADM483JR	0°C to 70°C	8-Lead Standard Small Outline Package	R-8
ADM483JR-REEL	0°C to 70°C	8-Lead Standard Small Outline Package	R-8
ADM483JR-REEL7	0°C to 70°C	8-Lead Standard Small Outline Package	R-8

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