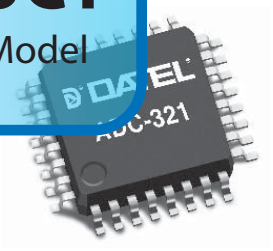
ADC-321

8-Bit, 50MHz Video A/D Converter

OBSOLETE PRODUCT

Contact Factory for Replacement Model



FEATURES

- Low power dissipation (180mW max.)
- Input signal bandwith (100MHz)
- Optional synchronized clamp function
- Low input capacitance (15pF typ.)
- +5V or +5V /+3.3V power supply operation
- Differential nonlinearity (±½LSB max.)
- Optional self-biased reference
- CMOS/TTL compatible inputs
- Outputs 3-state TTL compatible
- Surface mount package

PRODUCT OVERVIEW

The ADC-321 is an 8-bit, high speed, monolithic CMOS, sub-ranging A/D converter. The ADC-321 achieves a sampling rate comparable to flash converters by employing a sub-ran single +5V or dual +5V and +3.3V power source to allow easy interfacing with 3.3V logic.

An optional synchronous clamp function useful for video signal processing is provided. The ADC-321 is well suited for the portable video signal processors due to its low 125mW typical power dissipation. The ADC-321 also features ±0.5 LSB max. differential non-linearity, a self bias function that can eliminate the need for external references, SNR with THD of 45dB, a small 32-pin QFP package and an operating temperature range of –40 to +85°C

INPUT/OUTPUT CONNECTIONS			
Pin	Function	Pin	Function
1	BIT 8 (LSB)	32	NO CONNECTION
2	BIT 7	31	DIGITAL GROUND (DGND)
3	BIT 6	30	$\overline{\text{OUTPUT ENABLE (OE)}}$
4	BIT 5	29	$\overline{\text{CLAMP ENABLE (CLE)}}$
5	BIT 4	28	DIGITAL GROUND (DGND)
6	BIT 3	27	CLAMP CONTROL (COP)
7	BIT 2	26	CLAMP REF. (VREF)
8	BIT 1 (MSB)	25	REF. BOTTOM SENSE (VRBS)
9	TEST	24	REF. BOTTOM (VRB)
10	+DVS (Digital)	23	ANALOG GROUND (AGND)
11	TEST	22	ANALOG GROUND (AGND)
12	A/D CLOCK	21	ANALOG IN (VIN)
13	NO CONNECTION	20	+AVS (Analog)
14	NO CONNECTION	19	+AVS (Analog)
15	CLAMP IN (CLP)	18	REF. TOP (VRT)
16	+AVS (Analog)	17	REF. TOP SENSE (VRTS)

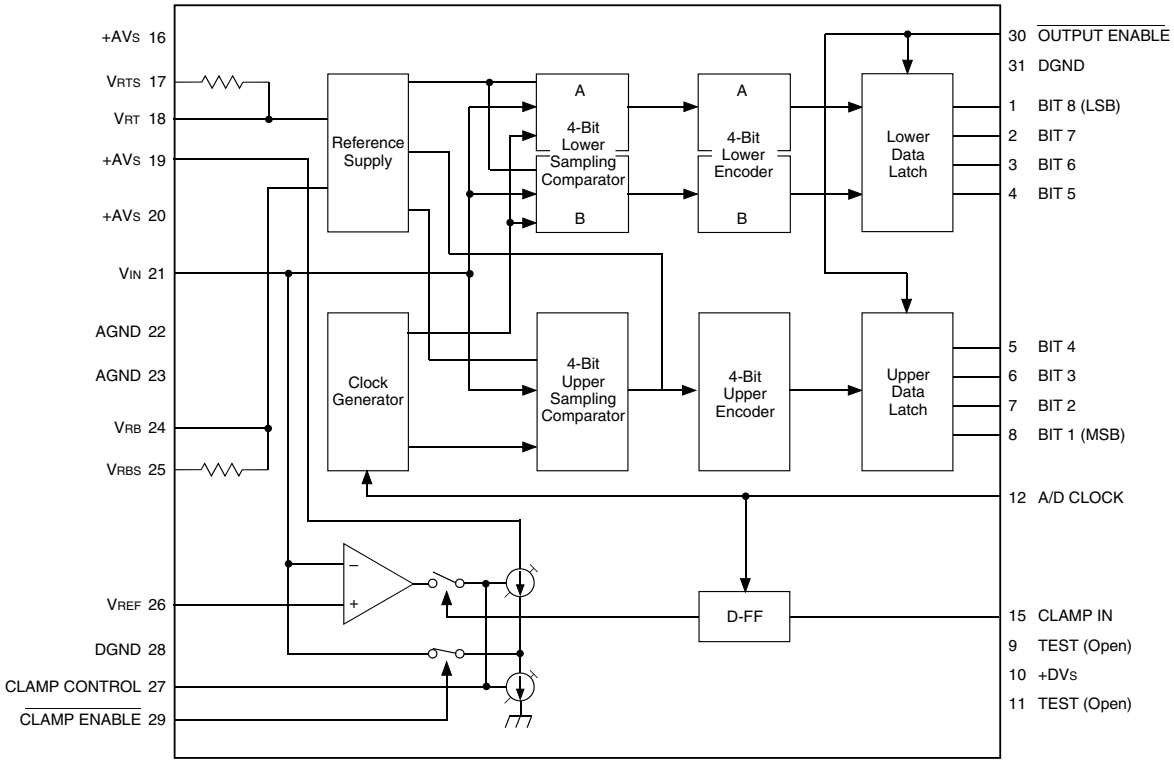


Figure 1. ADC-321 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

PARAMETERS	LIMITS	UNITS
Power Supply Voltage (+AVs, +DVs)	–0.5 to 7	Volts
Analog Input Voltage, (V_{IN})	–0.5 to +AVs + 0.5	Volts
Reference Input Voltage (V_{RT}, V_{RB})	–0.5 to +AVs + 0.5	Volts
Digital Input Voltage (V_{IH}, V_{IL})	–0.5 to +AVs + 0.5	Volts
Digital Output Voltage (V_{OH}, V_{OL})	–0.5 to +DVs + 0.5	Volts

FUNCTIONAL SPECIFICATIONS

Typical at T_A = 25°C, V_{RT} = +2.5V, V_{RB} = +0.5V, +AVs = +5V, +DVs = +3V to +5.5V, F_S = 50MHz unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range ①	+0.5	—	+2.5	Volts
Input Capacitance				
(@ V_{IN} = +1.5Vdc +0.07V_{RMS})	—	15	—	pF
Input Signal Bandwidth				
–1dB (@ R_{IN} = 33Ω)	—	60	—	MHz
–3dB (@ R_{IN} = 33Ω)	—	100	—	MHz
REFERENCE INPUTS				
Reference Resistance				
V_{RT} – V_{RB}	260	370	480	Ω
Reference Current	4.1	5.4	7.7	mA
Reference Voltage				
V_{RT}	—	—	+2.7	Volts
V_{RB}	0	—	—	Volts
|V_{RT} – V_{RB}|	1.7	—	—	Volts
Self Bias Voltage ②				
V_{RB}	+0.52	+0.56	+0.60	Volts
|V_{RT} – V_{RB}|	1.80	1.92	2.04	Volts
Capacitance (V_{RT}, V_{RTS}, V_{RB}, V_{RBS})	—	—	11	pF
Offset Voltage				
V_{RT}	–70	–50	–30	mV
V_{RB}	20	40	60	mV
DIGITAL INPUTS				
Logic Levels ③				
Input Voltage "1"	2.2	—	—	Volts
Input Voltage "0"	—	—	+0.8	Volts
Input Current ④				
A/D CLK	–240	—	240	µA
CLP, $\overline{CLE}$	–240	—	40	µA
$\overline{OE}$	–40	—	240	µA
Input Capacitance	—	—	11	pF
A/D Clock Pulse Width				
(tpw1)	10	—	—	ns
(tpw0)	10	—	—	ns

DIGITAL OUTPUTS		MIN.	TYP.	MAX.	UNITS
Output Current ($\overline{OE}$ = 0V) ⑤					
(@ +DVs = +5V)	"1"	—	—	–2	mA
	"0"	4	—	—	mA
Output Current ($\overline{OE}$ = 0V) ⑤					
(@ +DVs = +3.3V)	"1"	—	—	–1.2	mA
	"0"	2.4	—	—	mA
Output Current ⑥					
(@ $\overline{OE}$ = +3V)	"1"	–40	—	40	µA
	"0"	–40	—	40	µA
Capacitance	—	—	11	pF	

DIGITAL OUTPUTS (continued)		MIN.	TYP.	MAX.	UNITS
Output Data Delay					
($\overline{OE}$ = 0V, C_L = 15pF)					
(@ +DVs = +5V)	t_{PLH}	5.5	9.5	12.0	ns
	t_{PHL}	5.5	8.5	12.0	ns
(@+DVs = +3.3V)	t_{PLH}	4.3	11.8	16.3	ns
	t_{PHL}	4.3	7.6	16.3	ns
3-State Output Enable Time ⑦					
(R_L = 1kΩ, C_L = 15pF)					
(@ +DVs = +5V)	t_{PZH}	2.5	4.5	8.0	ns
	t_{PZL}	2.5	6.0	8.0	ns
(@+DVs = +3.3V)	t_{PZH}	3.0	7.0	9.0	ns
	t_{PZL}	3.0	5.0	9.0	ns
3-State Output Disable Time ⑧					
(R_L = 1kΩ, C_L = 15pF)					
(@+DVs = +5V)	t_{PHZ}, t_{PLZ}	3.5	5.5	7.5	ns
(@+DVs = +3.3V)	t_{PHZ}, t_{PLZ}	2.5	5.5	8.0	ns
CLAM CIRCUIT					
Clamp Offset Voltage ⑨		0	20	40	mV
Clamp Pulse Width ⑩		1.75	2.75	3.75	µA
PERFORMANCE					
Resolution		8	—	—	Bit
Sampling Rate, maximum, F_S		50	—	—	MHz
minimum, F_S		—	—	0.5	MHz
Aperature Delay (Tds)		—	0	—	ns
Integral Linearity Error		—	±0.7	±1.5	LSB
Diff. Linearity Error		—	±0.3	±0.5	LSB
Diff. Gain Error ⑪		—	3	—	%
Diff. Phase Error ⑪		—	1.5	—	deg
S/N Ratio with THD					
(f_{IN} = 100kHz)		—	45	—	dB
(f_{IN} = 500kHz)		—	44	—	dB
(f_{IN} = 1MHz)		—	44	—	dB
(f_{IN} = 3MHz)		—	43	—	dB
(f_{IN} = 10MHz)		—	38	—	dB
(f_{IN} = 25MHz)		—	32	—	dB
Spurious Free Dynamic Range					
(f_{IN} = 100kHz)		—	51	—	dB
(f_{IN} = 500kHz)		—	46	—	dB
(f_{IN} = 1MHz)		—	49	—	dB
(f_{IN} = 3MHz)		—	46	—	dB
(f_{IN} = 10MHz)		—	45	—	dB
(f_{IN} = 25MHz)		—	45	—	dB
POWER REQUIREMENTS					
Power Supply					
+AVs		+4.75	+5.0	+5.25	Volts
+DVs		+3.0	—	+5.5	Volts
|AGND – DGND|		0	—	100	mW
Power Supply Current ⑫					
1. AIs, DIs (@ +DVs = +5V)		—	25	36	mA
2. AIs		—	23	33	mA
DIs (@ +DVs = +3.3V)		—	2	3	mA
Power Dissipation		—	125	180	mW
ENVIRONMENTAL/PHYSICAL					
Operating Temp. Range, Case		–40	—	+85	°C
Storage Temperature Range		–55	—	+150	°C
Package Type		32-pin, plastic QFP			
Weight		0.007 ounces (0.2 grams)			

Footnotes:

① See technical note 6
② Pin 25 tied to AGND and pin 17 tied to +AVs
③ +AVs = +4.75 to +5.25V and +DVs = 3 to +5.5V, full operating tem. range.
④ V_{IL} = 0V and V_{IH} = +AVs, full operating temp. range
⑤ V_{OH} = +DVs–0.8V and V_{OL} = +0.4V, full operating temp. range
⑥ +DVS = +3 to +5.5V, full operating temp. range
⑦ $\overline{OE}$: +3 to 0V change
⑧ $\overline{OE}$: 0 to +3V change
⑨ 2.75µs clamp pulse width, 14.3MHz sampling, 15.75kHz clamping rate
⑩ The clamp pulse width given is for NTSC. For other processing systems adjust the rate to the clamp pulse cycle (1/15.75kHz for NTSC) to equal the value for NTSC.
⑪ NTSC 40IRE ramp, 14.3MHz sampling
⑫ 50MHz sampling, +AVs = +5V

TECHNICAL NOTES

1. The ADC-321 is a monolithic CMOS device. It should be handled carefully to prevent static charge pickup.

2. It has separate power supply terminals +AVs (pins 16, 19 and 20) and +DVs (pin 10) for the internal analog and digital circuits. It is recommended that both +AVs and +DVs be powered from a single source

   Other external digital circuits must be powered with a separate +DVs. A time lag between the two power supplies could induce latch up when power is turned on if separate supplies are used. The operating range of +DVs is from +3.0V to +5.5V and it allows the use of a common power supply with 3.3V digital systems. The +3.3V power for +DVs in this case should be taken or derived from the +AVs supply to avoid latch up. No power supply terminal should be left open.

3. The ADC-321 has separate grounds, the analog GND (pins 22 and 23) and digital GND (pins 28 and 31). Separate and substantial AGND and DGND ground planes are required. These grounds have to be connected to one earth point underneath the device. Digital returns should not flow through analog grounds. Connect all ground lines to the power point.

4. Bypass all power lines to GND with 0.1µF ceramic chip capacitors as close to the device as possible. This is very important.

5. Even though the analog input capacitance is a low 15pF, it is recommended that high frequency input be provided via a high-speed buffer amplifier. A parasitic oscillation may be generated when a high-speed amplifier is used. A 33 ohm resistor inserted between the output of an amplifier and the analog input of the ADC-321 will improve the situation. Kick back noise from A/D CLOCK pulses will be observed at the analog input terminal, but this has no influence on the ADC-321 performance.

6. Apply +2.5V to V_{RT} (pin 18, reference top) and 0.5V to V_{RB} (pin 24 reference bottom) to obtain an analog input range of +0.5V to +2.5V. Conversion accuracy is dependent on stable reference voltages. Provide reference inputs via amplifiers that have enough driving power to avoid noise problems. Keep to the following equations;

   $$0V \leq V_{RB} \leq V_{RT} \leq +2.7V, \qquad |V_{RT} - V_{RB}| \geq 1.7V$$

   The ADC-321 has a self bias function which allows the device to work without external references. Connect V_{RTS} (pin 17, self bias top) to +AVs and V_{RBS} (pin 25, self bias bottom) to the analog GND to obtain an analog input range of +0.56 to +2.48V. Typical voltages at V_{RT} (pin 18) and V_{RB} (pin 24) will then be +2.48V and +0.56V respectively. Under an application where this self bias function is used, the effects of temperature changes are minimal. Voltage changes of the +5V supply have direct influence on the performance of the device. The use of external references is recommended for applications sensitive to gain error, no ac signals can be used as references for this device.

7. A voltage up to +AVs + 0.5V can be applied to each digital input even when +3.3V is powered to +DVs, but the digital output voltage never exceeds +DVs.

8. Layout A/D CLOCK pulse input (pin 12) as short as possible for minimum influence on other signals. Use of a 100 ohm series resistor is recommended to protect the device as there may be some voltage difference and turn-on-time lag on the power supplies. Analog inputs signals are sampled at the falling edge of an A/D CLOCK pulse and digital data become available at the rising edge of an A/D CLOCK pulse that is delayed by 2.5 clock cycles. The A/D CLOCK are positive pulse that have 50% duty cycle. The minimum clock pulse width is 10 nsec for both high and low levels. Keep it low level while A/D conversions are on hold.

9. Digital output is 3-state. To enable 3-state outputs connect the $\overline{\text{OUTPUT ENABLE}}$ (pin 30) to GND. To disable, connect it to +DVs. The output is recommended to be latched and buffered through output registers. The device may be damaged if a voltage higher than +DVs + 0.5V is given to digital output pins while at high impedance level.

10. The 50MHz sampling rate is guaranteed. It is not recommended to use this device at sampling rates slower than 500kHz because the droop characteristics of the internal sample and hold exceed the limit required to maintain the specified accuracy of the device. Also, burst mode sampling is not recommended.

11. The ADC-321 has a clamp function. This clamp is enabled when $\overline{\text{CLAMP ENABLE}}$ (pin 29) is tied to GND and is disabled when tied to +DVs or left open. Clamp pulse inputs (pin 15) are effective when this clamp function is enabled and signals are clamped whole, this clamp pulse is low. The clamp reference input (pin 26) is set by an external trim. The CCP terminal (pin 27) integrates the clamp control voltage across an external capacitor. Refer to Figure 4 for examples of various ways to use this clamp function.

12. The TEST 1 and 2 (pins 9 and 11) are not used. Always leave them open.

THEORY OF OPERATION

(See Functional Block Diagram, Figure 1, and Timing Diagrams, Figure 2)

1. The DATEL ADC-321 is a 2-step parallel A/D converter featuring a 4-bit upper comparator group and two 4-bit lower comparator groups, each with built-in sample and hold. A reference voltage equal to the voltage between (V_{RT} – V_{RB})/16 is constantly applied to the 4-bit upper comparator block. A voltage corresponding to the upper data is fed through the reference supply to the lower data. V_{RTS} and V_{RBS} pins provde the self generation function for V_{RT} (reference voltage top) and V_{RB} (reference voltage bottom) voltages.

2. This converter uses an offset cancelation type comparator and operates synchronously with the external clock. It features various operating modes which are shown in the Timing Diagram (Figure 2) by the symbols S, H and C. These characters stand for Input **S**ampling (Auto Zero) Mode, Input **H**old Mode and **C**omparison Mode.

3. The operation of the respective parts is as indicated in Figure 2-3. For instance, input voltage N is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block. Input voltage N+1 is sampled with the falling edge of the second clock by means of the upper comparator block and lower comparator B block. The upper comparator block finalizes comparison data UD(N) with the rising edge of the second clock. The lower comparator block finalizes comparison data LD(N) with the rising edge of the third clock. UD(N) and LD(N) are combined and routed to the output as Output Data N with the rising edge of the fourth clock. Thus there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Table 2: Digital Output Coding

V_{IN}	OUTPUT CODE MSB	LSB
0V	0 0 0 0	0 0 0 0
+7.812mV	0 0 0 0	0 0 0 1
+0.9922V	0 1 1 1	1 1 1 1
+1.000V	1 0 0 0	0 0 0 0
+1.500V	1 1 0 0	0 0 0 0
+1.9922V	1 1 1 1	1 1 1 1

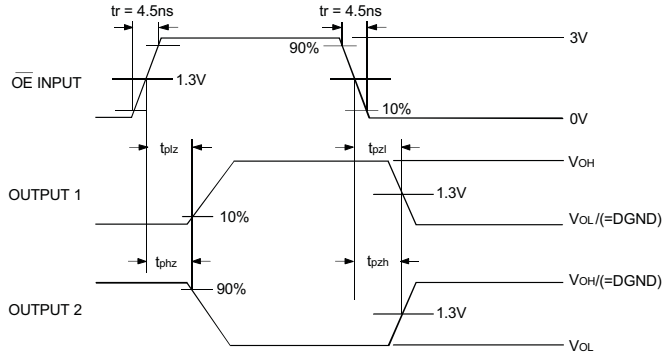


Figure 2-1. ADC-321 Timing Diagram

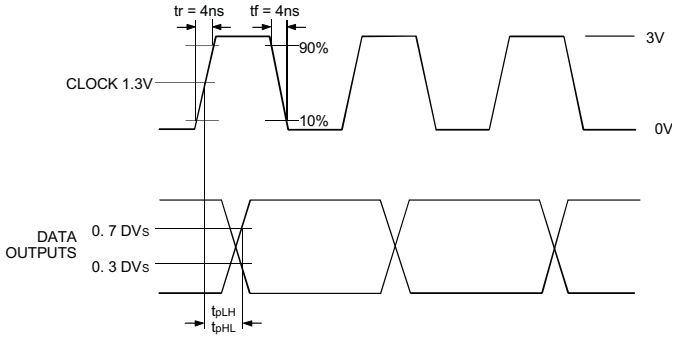


Figure 2-2. ADC-321 Timing Diagram

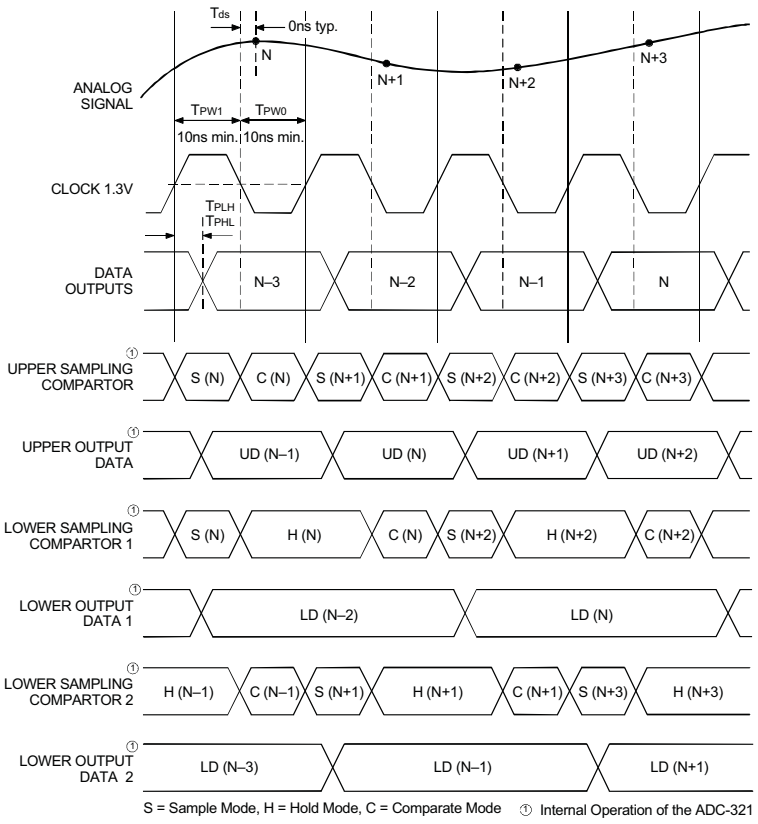


Figure 2-3. ADC-321 Timing Diagram

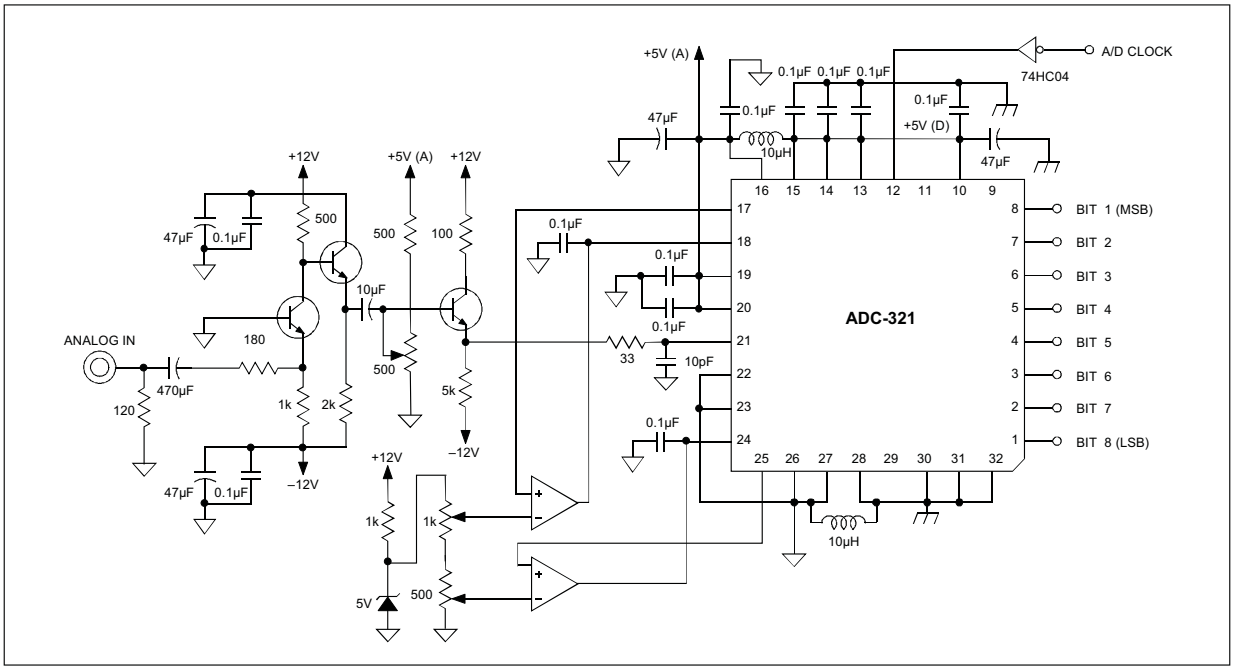


Figure 3. Typical Connection Diagram

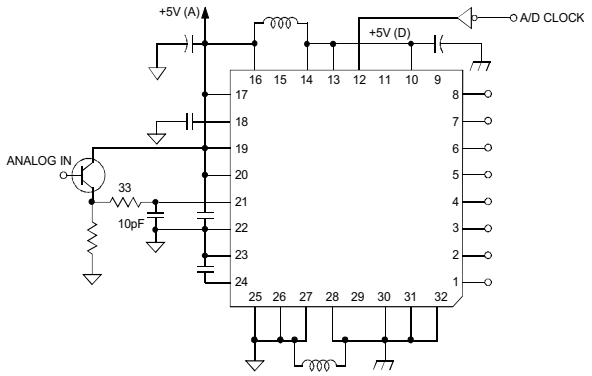


Figure 4-1. Clamp Not Used in Self Bias Mode

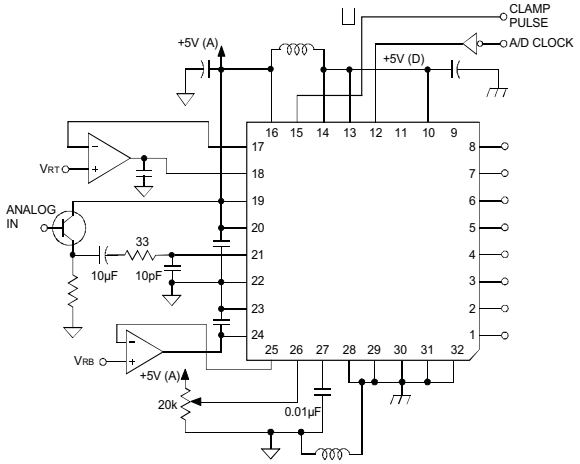


Figure 4-2. Clamp Used in External Reference Mode

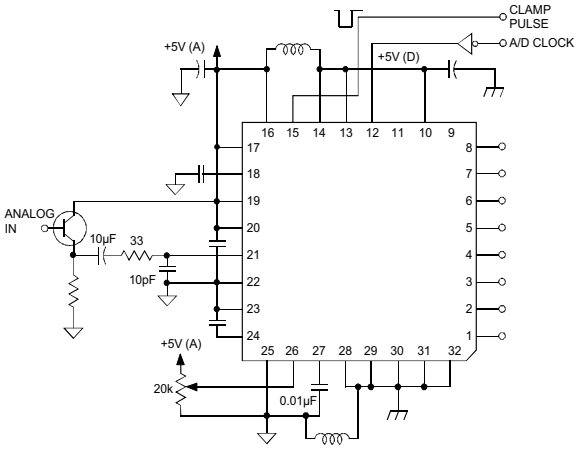


Figure 4-3. Clamp Used in Self Bias Mode

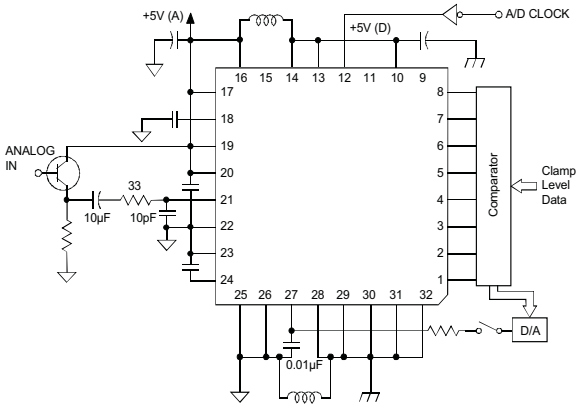


Figure 4-4. Digital Clamp Used in Self Bias Mode

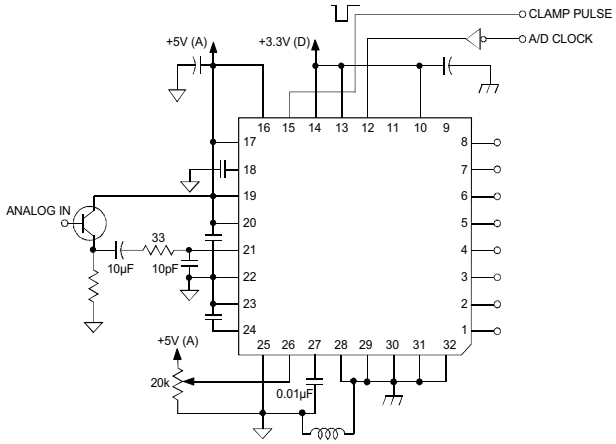


Figure 4-5. Clamp Used in Self Bias Mode With +5V/+3.3V Dual Power Supply

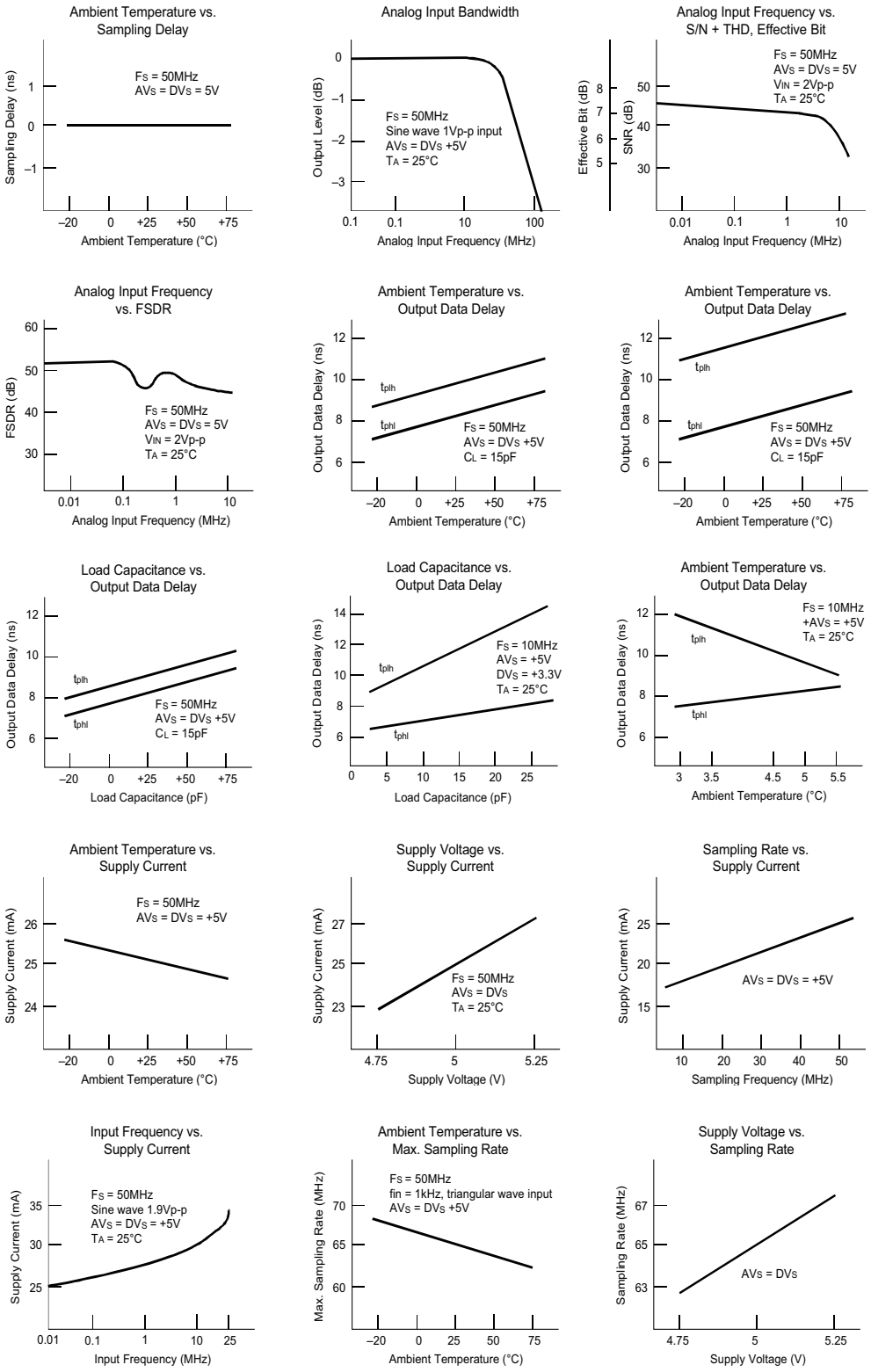


Figure 5: Typical Performance Curves

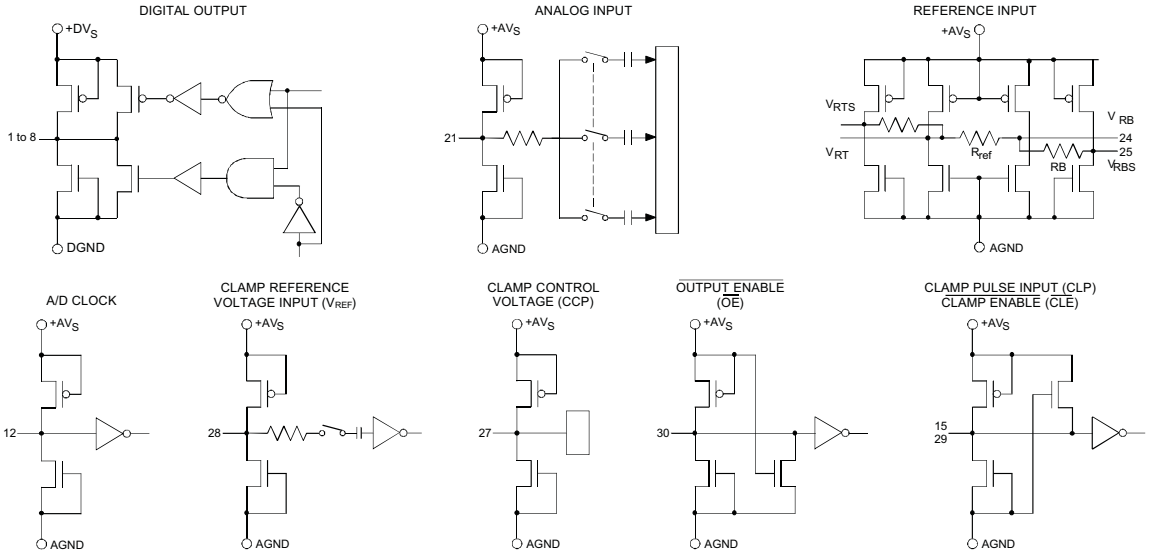
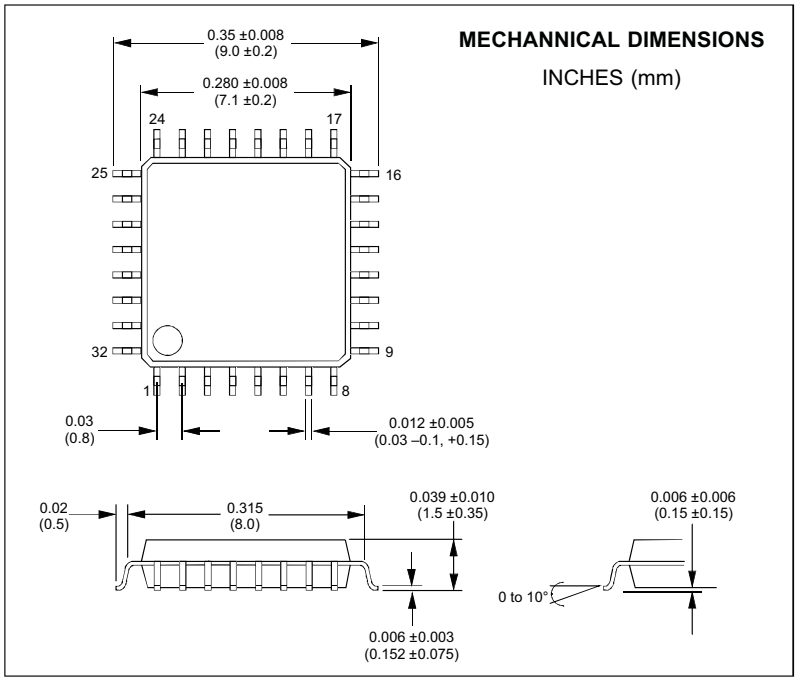


Figure 6: Equivalent Circuits



ORDERING INFORMATION

ADC-321	8-bit, 50MHz A/D converter