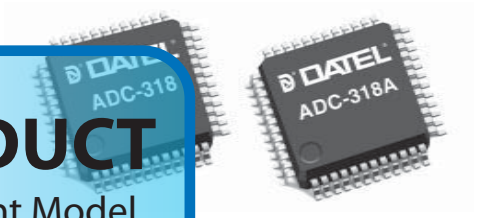
ADC-318, ADC-318A

8-Bit, 120MHz and 140MHz Full-Flash A/D Converter

OBSOLETE PRODUCT

Contact Factory for Replacement Model



FEATURES

- **Low power dissipation (960mW max.)**
- **TTL compatible output**
- **Diff./Integral nonlinearity (±1/2 LSB max.)**
- **1:2 Demultiplexed straight output programmable**
- **2:1 Frequency divided TTL Clock Output (ADC-318A)**
- **Surface mount package**
- **Selectable Input Logic (TTL, ECL, PECL)**
- **+5V or ±5V Power Supply Operation**

GENERAL DESCRIPTION

The ADC-318 and ADC-318A are 8 bit monolithic bipolar, full flash A/D converters. Though they have high, 120MHz (ADC-318) and 140MHz (ADC-318A), sampling rates, their input logic level, including the start convert pulse, is TTL, ECL and PECL compatible. Digital outputs are also TTL compatible and allow a straight output or a programmable 1:2 de-multiplexed output.

The ADC-318 and ADC-318A feature ±1/2 LSB max. integral and differential non-linearity, +5V single or ±5V dual power supply operation, a low 960mW maximum power dissipation, 150MHz wide analog input range and excellent temperature coefficient in a small 48 pin QFP package. The start convert pulse can have a 50% duty cycle.

The ADC-318 and ADC-318A offer low cost, easy to use functionality for design engineers.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	–DVs (Digital)	48	$\overline{\text{RSET}}$ ECL/PECL
2	REF. BOTTOM (V_{RB})	47	RSET ECL/PECL
3	ANALOG GROUND	46	$\overline{\text{RSET}}$ TTL
4	REF. MID POINT (V_{RM1})	45	SELECT
5	+AVs (Analog)	44	INV
6	ANALOG IN (V_{IN})	43	TTL CLOCK OUT
7	REF. MID POINT (V_{RM2})	42	+DVs2 (Digital)
8	+AVs (Analog)	41	DIGITAL GROUND 2
9	REF. MID POINT (V_{RM3})	40	A BIT 1 (MSB)
10	ANALOG GROUND	39	A BIT 2
11	REF. TOP (V_{RT})	38	A BIT 3
12	DIGITAL GROUND 3	37	A BIT 4
13	A/D CLOCK ECL/PECL	36	A BIT 5
14	$\overline{\text{A/D CLOCK}}$ ECL/PECL	35	A BIT 6
15	A/D CLOCK TTL	34	A BIT 7
16	NO CONNECTION	33	A BIT 8 (LSB)
17	NO CONNECTION	32	DIGITAL GROUND 2
18	NO CONNECTION	31	+DVs2 (Digital)
19	+DVs2 (Digital)	30	+DVs1 (Digital)
20	DIGITAL GROUND 2	29	DIGITAL GROUND 1
21	B BIT 8 (LSB)	28	B BIT 1 (MSB)
22	B BIT 7	27	B BIT 2
23	B BIT 6	26	B BIT 3
24	B BIT 5	25	B BIT 4

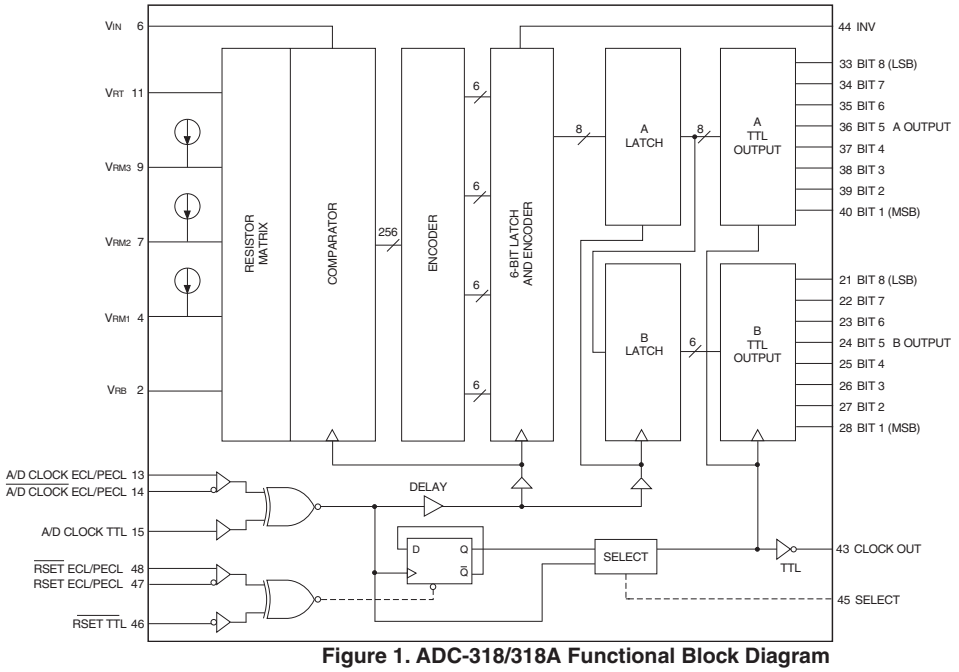


Figure 1. ADC-318/318A Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
Supply Voltage (+AVS, +DVS, 1,2)	–0.5 to +7.0	Volts
Supply Voltage (AGND, DGND 1, 2)	–0.5 to +7.0	Volts
Supply Voltage (DGND 3)	–0.5 to +7.0	Volts
Supply Voltage (–DVS) ①	–0.5 to +7.0	Volts
Supply Voltage (–DVS) ②	–7.0 to +0.5	Volts
Reference Voltage (VRT)	+2.7 to +AVS	Volts
Reference Voltage (VRB)	VIN –2.7 to +AVS	
Reference Voltage (VRT–VRB1)	2.5	Volts
Input Voltage, analog (VIN)	VRT –2.7 to +AVS	Volts
Input Voltage, digital		
ECL	–DVS to +0.5	Volts
PECL	–0.5 to DGND3	Volts
TTL	–0.5 to +DVS1	Volts
Diff. Voltage between Pin ③	2.7	Volts
Power Dissipation, max. ④	2	W

Footnote:

① Single Supply

② Dual Supply

③ A/D Clock–$\overline{\text{A/D Clock}}$ and RESET–$\overline{\text{RESET}}$ of ECL/PECL logic inputs.

④ With ADC-318 mounted on a 50x50mm glass fiber base epoxy board, 1.6mm thick.

FUNCTIONAL SPECIFICATIONS

(Typical at T_A = 25°C, VRT = +4V, VRB = +2V, DGND3 = +DVS1= +DVS2 = +AVS = +5V, –DVS = 0V, PECL Logic, unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage	—	+2 to +4	—	Volts
Input Resistance	4	—	50	kΩ
Input Current	0	—	500	µA
Input Capacitance ①	—	21	—	pF
Input Bandwidth				
V_{IN} = $2V_{p-p}$, –3dB	150	—	—	MHz
REFERENCE INPUTS				
Reference Voltage				
VRT	+2.9	—	+4.1	Volts
VRB	+1.4	—	+2.6	Volts
VRT–VRB	1.5	—	2.1	Volts
Reference Resistance	75	115	155	Ω
Reference Current	9.7	17.4	28	mA
VRT Offset Voltage	2	—	15	mV
VRB Offset Voltage	2	—	10	mV
DIGITAL INPUTS				
ECL, PECL				
Input Voltage "1"	DGND3–1.05	—	DGND3–0.5	Volts
Input Voltage "0"	DGND3–3.2	—	DGND3–1.4	Volts
Threshold Voltage	—	DGND3–1.2	—	Volts
Input Current "1" ②	–50	—	+50	µA
Input Current "0" ②	–75	—	0	µA
Voltage Difference	0.4	0.8	—	Volts
TTL				
Input Voltage "1"	+2.0	—	—	Volts
Input Voltage "0"	—	—	+0.8	Volts
Threshold Voltage	—	+1.5	—	Volts
Input Current "1" ③	–50	—	0	µA
Input Current "0" ③	–500	—	0	µA
Select				
Input Voltage "1"	—	+DVS1	—	
Output Voltage "0"	—	+DGND1	—	
Input Capacitance	—	—	5	pF

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
A/D Clock Pulse Width (T_{PW1})				
ADC-318	3.2	—	—	ns
ADC-318A	3.0	—	—	ns
A/D Clock Pulse Width (T_{PW0})				
ADC-318	3.2	—	—	ns
ADC-318A	3.0	—	—	ns
RSET Setup Time (T_{rs})	3.5	—	—	ns
RSET Hold Time (T_{rh})	0	—	—	ns
DIGITAL OUTPUTS				
Output Voltage "1" (@–2mA)	2.4	—	—	Volts
Output Voltage "0" (@1mA)	—	—	+0.5	Volts
Output Rise Time (T_r) ④	—	2	—	ns
Output Fall Time (T_f) ④	—	2	—	ns
Output Delay (T_{do1}) ⑤	1/Fc	1/Fc+1	1/Fc+2	ns
Output Delay (T_{do2}) ⑥	6.5	8	10	ns
Clockout Output Delay (T_{dclk}) ⑦	4.5	7	8	ns
PERFORMANCE				
Resolution	8	—	—	Bit
Conversion Rate (fs)				
Straight Mode				
ADC-318	100	—	—	MHz
ADC-318A	100	—	—	MHz
De-multiplexed Mode				
ADC-318	100	—	—	MHz
ADC-318A	100	—	—	MHz
Sampling Delay (T_{dS})	3	4.5	6	ns ⑲
Aperture Jitter (Taj)	—	10	—	ps ⑲
Integral Linearity Error	—	—	±0.5	LSB ⑲
Diff. Linearity Error	—	—	±0.5	LSB
S/N Ratio ⑧				
ADC-318				
(@f_{IN} = 1kHz)	—	46	—	dB
(@f_{IN} = 29.999MHz)	—	40	—	dB
ADC-318A				
(@f_{IN} = 1kHz)	—	46	—	dB
(@f_{IN} = 34.999MHz)	—	40	—	dB
Error Rate				
ADC-318				
(@f_{IN} = 1kHz) ⑨	—	—	10^{-12}	TPS
(@f_{IN} = 29.999MHz)	—	—	10^{-9}	TPS
(@fIN = 24.999MHz)⑩	—	—	10^{-9}	TPS ⑪ ⑪
ADC-318A				
(@f_{IN} = 1kHz) ⑨	—	—	10^{-12}	TPS ⑪
(@f_{IN} = 34.999MHz)	—	—	10^{-9}	TPS
(@fIN = 24.999MHz)⑩	—	—	10^{-9}	TPS ⑪ ⑪ ⑪
POWER REQUIREMENTS				
Supply Voltage				
One Power Supply				
(+AVS, +DVS 1,2)	+4.75	+5.0	+5.25	Volts
One Power Supply (DGND3)	+4.75	+5.0	+5.25	Volts
One Power Supply (–DVS)	–0.05	0	+0.05	Volts
Two Power Supply				
(+AVS, +DVS 1,2)	+4.75	+5.0	+5.25	Volts
Two Power Supply (DGND3)	–0.05	0	+0.05	Volts
Two Power Supply (–DVS)	–5.5	–5.0	–4.75	Volts
ADC-318				
Supply Current (+Is)	125	145	185	mA
Supply Current (–Is)	0.4	0.6	0.8	mA
ADC-318A				
Supply Current (+zs)	110	150	185	mA
Supply Current (–zs)	0.4	0.6	0.8	mA

POWER REQUIREMENTS (cont.)				
Power Dissipation				
ADC-318	680	780	980	mW
ADC-318A	570	790	960	mW
PARAMETERS				
Operating Temp. Range, Case				
ADC-318, 318A	–20	—	+75	°C
Thermal Impedance				
θja ⑫	—	62.5	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	48-pin, plastic QFP			
Weight	0.25 ounces (0.7 grams)			

Footnotes:

① VIN = +3V +0.07Vrms
② VIH = DGND3–0.8V
VIL = DGND3–1.6V
③ VIH = 3.5V
VIL = 0.2V
④ TTL, 0.8 to 2.0V, CL = 5pF
⑤ DMUX Mode, CL = 5pF; FC = Clock frequency
⑥ Straight Mode, CL = 5pF
⑦ CL = 5pF
⑧ VIN = FS, DMUX mode
⑨ VIN = FS, DMUX mode, Error >16LSB
⑩ VIN = FS, Straight mode, Error >16LSB
⑪ "Times Per Sample"
⑫ Mounted on 50x50mm, 1.6mm thick glass fiber base epoxy board

TECHNICAL NOTES

1. The ADC-318 and ADC-318A are ultra high speed full flash A/D converters that have 120MHz and 140MHz sampling rates respectively. The ADC-318 and ADC-318A are fully interchangeable products with the exception of their sampling rates. Their inputs are TTL, ECL and PECL compatible and their outputs are TTL compatible. Obtaining fully specified performance from the ADC-318 and ADC-318A requires that the characteristic impedance of all input/output logic and analog input lines be properly matched.
2. Power supply lines and grounding may effect the performance of the ADC-318 and ADC-318A. Separate and substantial AGND and DGND ground planes are required. These grounds have to be connected to one earth point underneath the device. There are three digital grounds, DGND1 (pin 29), DGND2 (pins 20, 32, 41) and DGND3 (pin 12). These DGND 's are separated internally. DGND1 and DGND2 are always connected externally but DGND3 shall be connected differently depending on whether the single or dual power supply mode is used, as explained later.

   The ADC-318 and ADC-318A have separate +AVs and +DVs pins. It is recommended that both +AVs and +DVs be powered from a single source. Other external digital circuits must be powered with a separate +DVs. Layouts of +AVs and +DVs lines must be separated like the GND lines to avoid mutual interference and are connected to a point through an LC filter. There are two digital supplies +DVs1 (pin 30) and +DVs2 (pins 19, 31, 42). These are also separated internally. These must be tied together outside while in use. Bypassing all power lines with a 0.1uF ceramic chip capacitor and the use of multilayered PC boards is recommended.
3. The analog input terminal (pin 6) has 21pF of input capacitance. The input signal has to be given via a buffer amplifier which has enough driving power. Make lead wires as short as possible and use chip resistors and capacitors to avoid parasitic capacitance and inductance.
4. The use of a buffer amplifier and bypass capacitors is also recommended on the reference input terminals VRT (pin 11) and VRB (pin 2). The analog input range is determined by

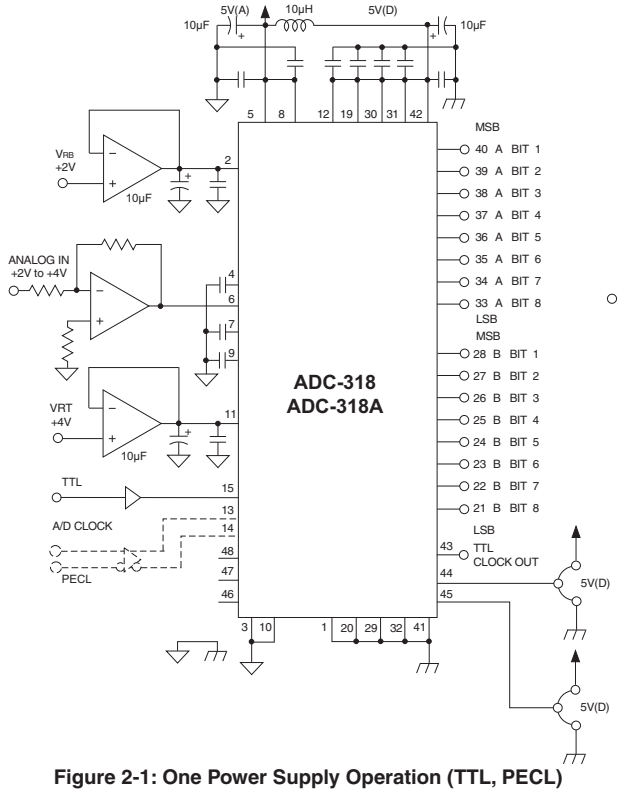


Figure 2-1: One Power Supply Operation (TTL, PECL)

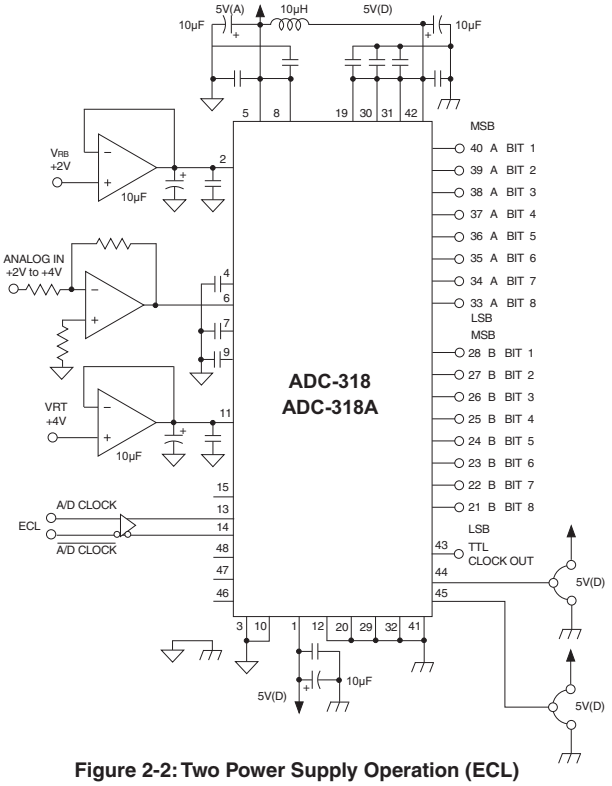


Figure 2-2: Two Power Supply Operation (ECL)

Note: All capacitors not otherwise designated are 0.1µF

the reference input voltages given to VRT and VRB. Keep the ranges of V within values shown in this data sheet. Standard settings are VRT = +4.0V, V input range from +2 to +4V. This setting can be varied to VRT = +3.5V, VRB = +2V and 1.5V p-p analog input range, depending on your selection of amplifiers which may provide less than +4V output.

5. The ADC-318 and ADC-318A have resistor matrix taps at VRM1 (pin 4), VRM2 (pin 7) and VRM3 (pin 9). These pins provide ¼, ½ and ¾ full scale of VRT-VRB voltage respectively. These outputs may be used to adjust the integral non-linearity. Bypass these pins to GND with 0.1uF ceramic chip capacitors.

6. A/D CLK input and $\overline{\text{RSET}}$/RSET inputs are TTL or ECL, PECL (Positive ECL) compatible. Pins are provided individually. TTL or PECL is available with +5V single power applied. ECL is available with ±5V dual power applied. The connections of –DVs (pin 1) and DGND3 (pin12) are different depending on the power supply mode used. Refer to Figures 2-1 and 2-2.
   a. For +5V single power (TTL or PECL) –DVs (pin 1) is connected to DGND. DGND3 (pin 12) is connected to +5V power.
   b. For ±5V dual power (ECL) –DVs (pin 1) is connected to –5V power. DGND3 (pin 12) is connected to DGND.

7. When the A/D CLK is driven with ECL or PECL, A/D CLK (pin 13) and $\overline{\text{A/D CLK}}$ (pin 14) are to be driven by differential logic inputs to avoid unstable performance at critically high speeds. If a risk of unstable performance is acceptable, single logic input can be used opening $\overline{\text{A/D CLK}}$ (pin 14). The $\overline{\text{A/D CLK}}$ pin should be bypassed to DGND with a 0.1uF ceramic capacitor. When connected this way there will be a voltage of DGND –1.2V on the $\overline{\text{A/D CLK}}$ pin. This voltage can not be used as a threshold voltage for ECL or PECL. Input the A/D CLK pulse to pin 15 when TTL is selected.

8. The ADC-318 and ADC-318A have $\overline{\text{RSET}}$/RSET input pins. An internal frequency half divider can be initialized with inputs to these pins. With ECL or PECL, differential inputs are given to $\overline{\text{RSET}}$ (pin 48) and RSET (pin 47). This function can be achieved with a single input, leaving pin 47 open and bypassing to DGND with a 0.1uF ceramic chip capacitor. The voltage level of pin 47 is the threshold voltage of ECL or PECL. Use RSET (pin 46) for TTL.

9. SELECT (pin 45) is used to set output mode. Connection of this pin to DGND selects the straight output mode and connection to +DVs selects the 1:2 de-multiplexed output mode. The maximum sampling rates are 100MHz for straight mode (For both models, ADC-318 and ADC-318A) and 120MHz (ADC-318) and 140MHz (ADC-318A) for de-multiplexed mode. Refer to figure 2-4. There is an application where a multiple number of ADC-318/318A's are used with a common A/D CLK and outputs are in de-multiplexed mode. In this case, the initial conditions of the frequency half divider of each A/D Converter are not synchronized and it is possible that each converter may have one clock maximum of timing lag. This lag can be avoided by giving a common $\overline{\text{RSET}}$ pulse to all converters at power ON. (See Figure 3-3 and 3-4, timing diagrams.)

10. The ADC-318 and ADC-318A have a TTL compatible CLK OUT (pin 43). Since the rising edge of this pulse can provide Setup and Hold time of output data, regardless of the output mode, this signal can be used as synchronization pulse for external circuits. Data output timing is different for the straight mode and the de-multiplexed mode. See the timing chart Figure 3.

11. INV (pin 44) is used to invert polarity of the TTL compatible output data from both A and B ports. Leaving this pin open or connected to +DVs makes the output positive true and connection to DGND makes it negative true logic. See input/output code table, Table 4.

Table 3: Logic Input Level vs. Power Supply Settings

DIGITAL INPUT LEVEL	–DVS	DGND3	SUPPLY VOLTAGES
TTL	0V	+5V	+5V
PECL	0V	+5V	+5V
ECL	–5V	0V	±5V

Table 4: Digital Output Coding

SIGNAL INPUT VOLTAGE	DIGITAL OUTPUT CODE (A,B OUTPUT)	
	INV=1	INV=0
	LSB MSB	LSB MSB
VRT	11111111	00000000
VRM2	10000000 01111111	01111111 10000000
VRB	00000000	11111111

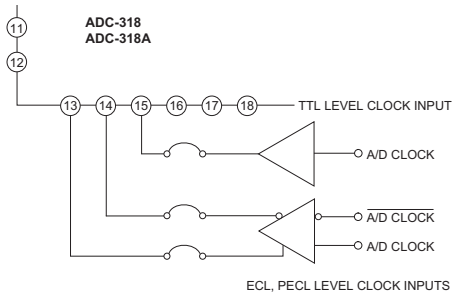


Figure 2-3: A/D Clock Input Connection

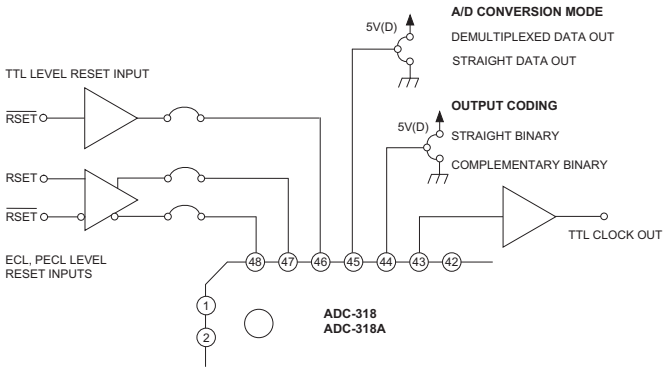


Figure 2-4: Digital Input/Output Connections

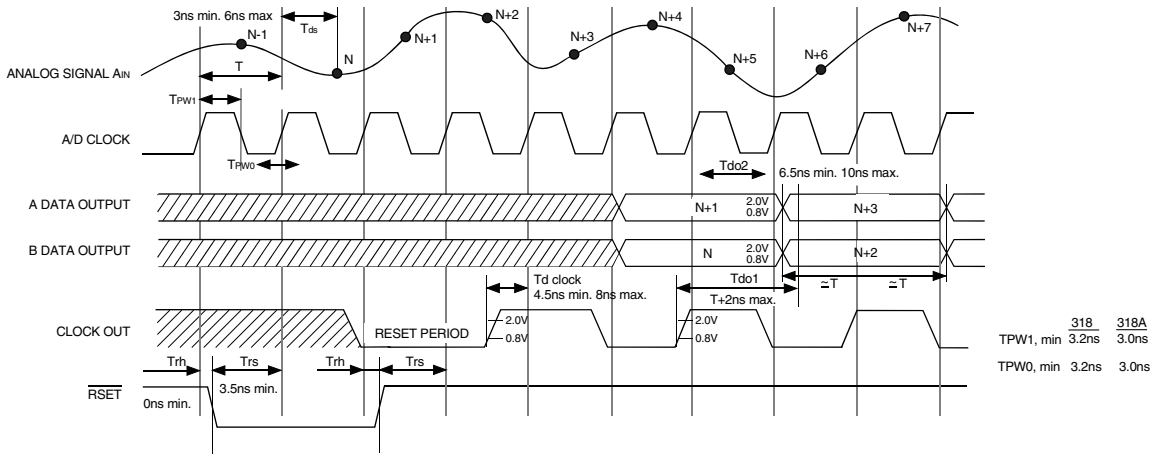


Figure 3-1: Demultiplexed Data Output (Select-Pin: +DVS or left open, 120MHz max. Clock Frequency)

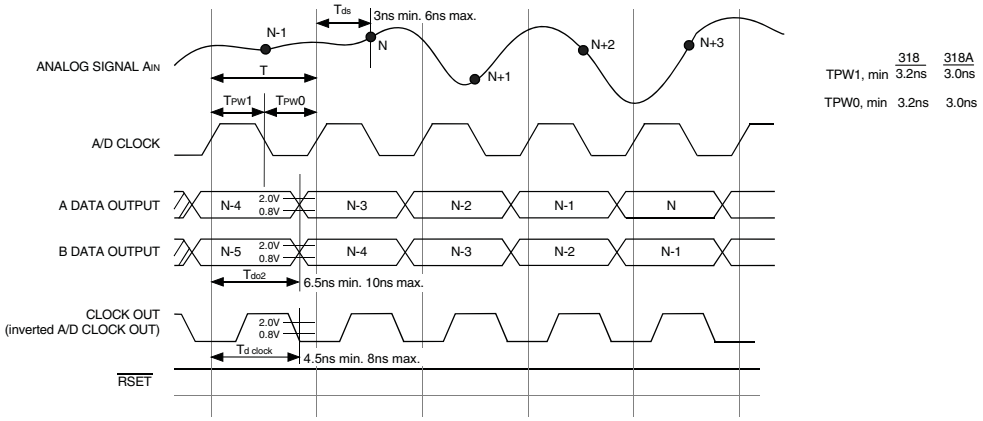


Figure 3-2: Straight Data Output (Select-Pin: DGND, 100MHz max. Clock Frequency)

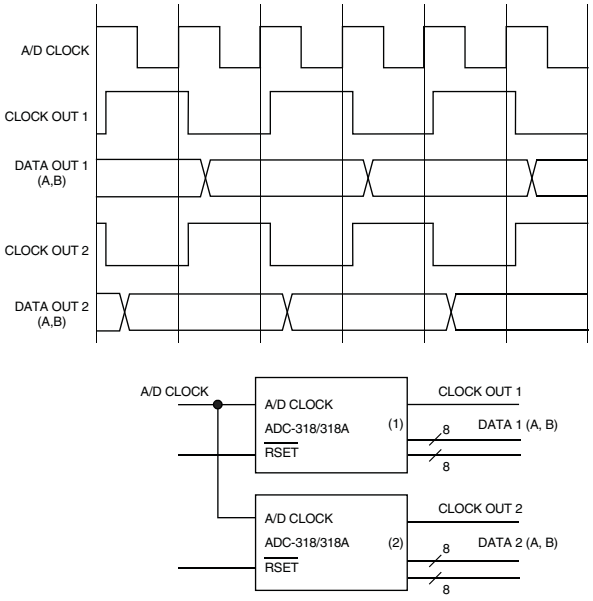


Figure 3-3: Parallel Operation without RSET Pulse

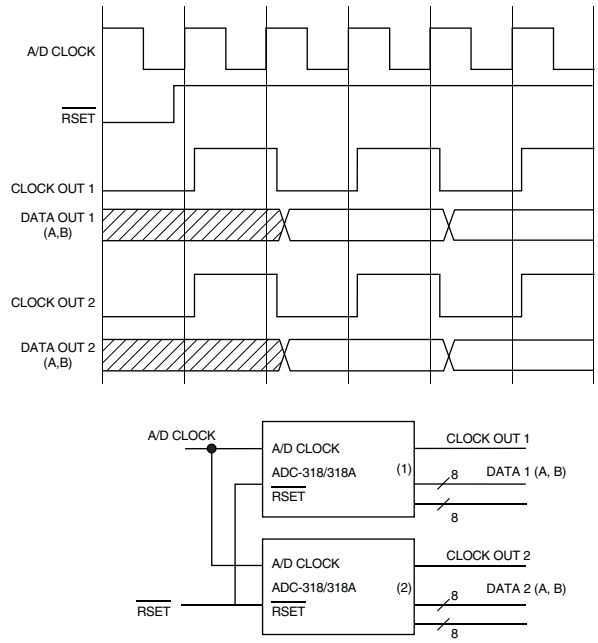


Figure 3-4: Parallel Operation using RSET Synchronization

APPLICATION

This device can be used in applications where 3 parallel channels are synchronized. Conversion speed is the highest in the de-multiplexed mode. It is difficult to control timing of three channels at such a high speed. Two practical ways to maintain timing for reading data into the system are given.

1. Clock output of one A/D is used in reading data of other channels

Time delay of Clock Output and Output Data are specified as:

Td clk (CLK OUT Delay) ; 4.5nSec min., 8.0nsec max.

Tdo2 (Output Data Delay); 6.5nSec min., 10nsec max.

These values apply over the operating temperature and supply voltage ranges. Timing control of Tset (Setup Time) seems to be very critical. It tends to lead by 0.5nsec as temperature and supply voltages go lower. When A/D converters for 3 channels are used on the same board, temperature and supply voltages tend to change in the same direction and effects caused by these changes are negligible.

Tdclk and Tdo2 at Ta=25°C , +Vs=+5.0V are;

Td clk: 5.0nsec min., 7.5nsec max.

Tdo2: 7.0nsec min., 9.5nsec max.

So long as devices are located on the same board and take power from the same source, 2.5nsec min. of setup time for data reading can be secured even though temperature and power supply voltages vary. A timing diagram at 140MHz sampling rate is shown in Figure 4a.

2. To read output data of 3 channels into a gate array

Both output data lines and each clock output are read into a gate array if the digital circuits after the A/D conversion consist of one high speed gate array. An AND gate is prepared to take the AND of each output signal which is used for reading output data. The slowest rise time clock determines the system clock. Thus adequate setup time is secured. This method can be employed only when a high speed gate array is used. The setup time is delayed by the delay time of the AND gate. The use of a discrete IC gate is not recommended because of its time delay characteristics. See Figure 4b

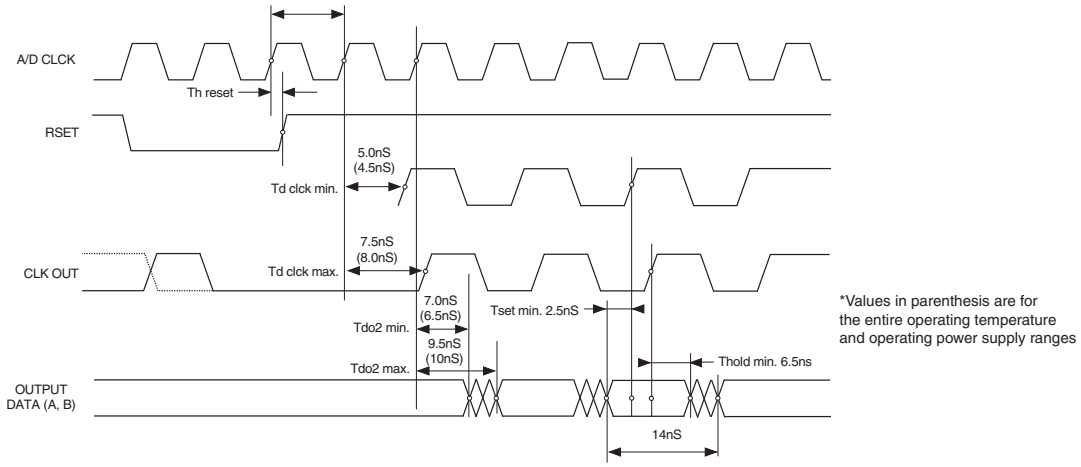


Figure 4a: Timing diagram 1

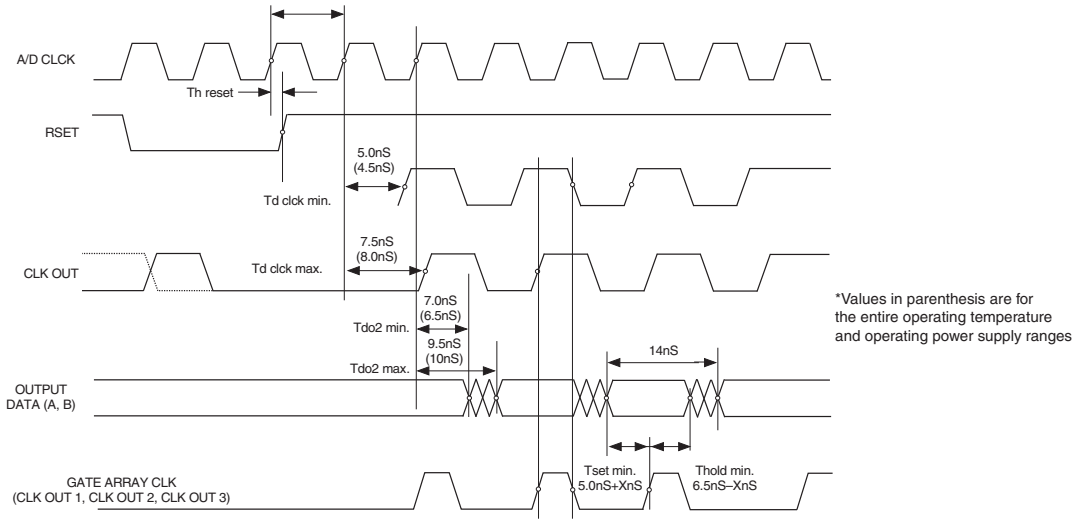
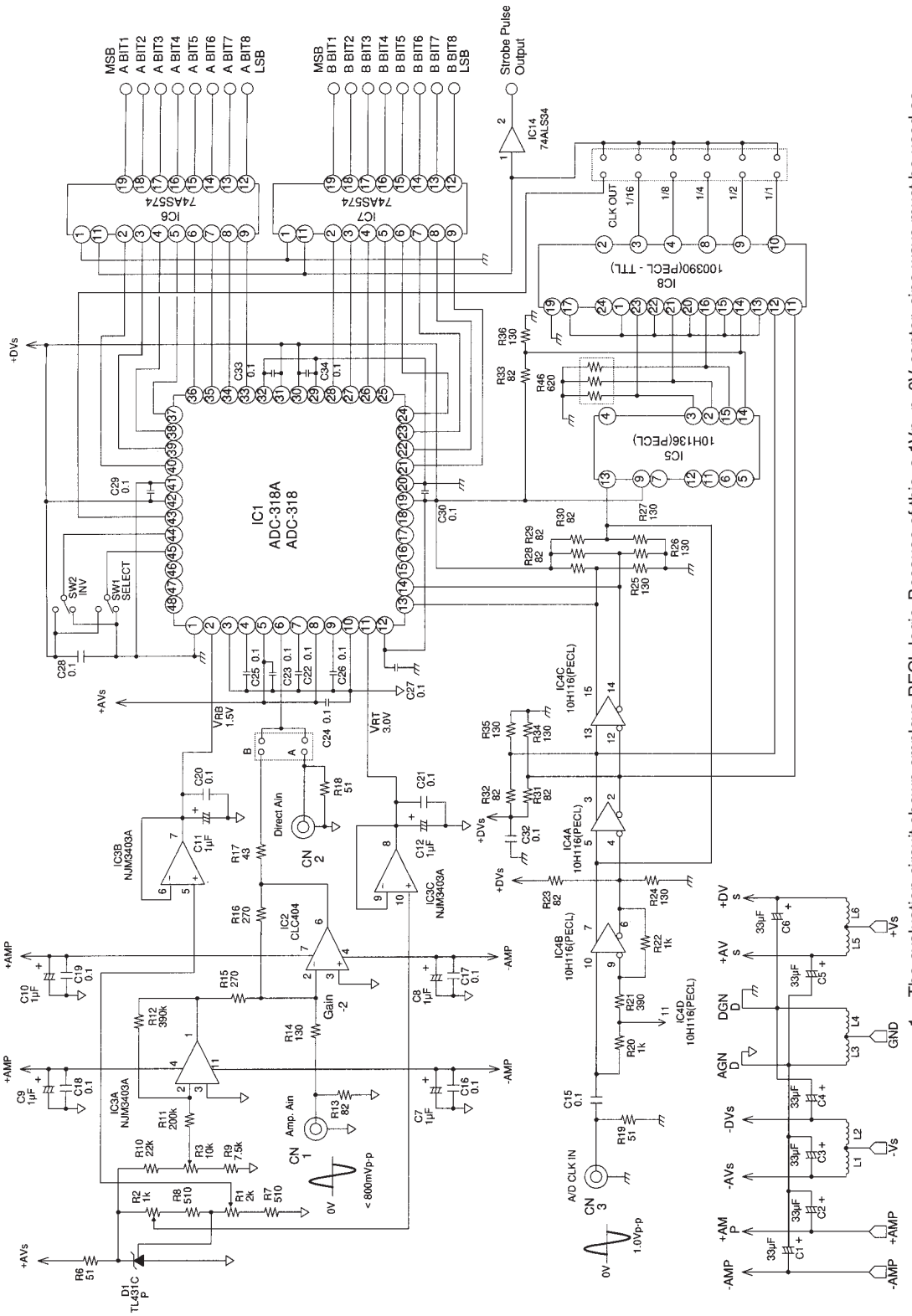


Figure 4b: Timing diagram 2



1. The evaluation circuit shown employs PECL logic. Because of this, a 1Vp- p, 0V center, sine wave must be used as the clock input (A/ D CLK) at CN3.
2. When analog signals are taken from the CN1 amplifier input "A" must be left open while "B" is short circuited. The analog input signals at CN1 must be less than 800mVp- p, 0V and zero centered. The +AMP and –AMP supply pins on the input amplifier are normally connected to +/- 5V which, along with the gain of -2 used with the CLC- 404 in this circuit, will limit the amplifiers output dynamic range. To increase the amplifiers output dynamic range the +AMP pin can be connected to +7V and the –AMP connected to -3V. V_{RT} and V_{RB} may require adjustment in this case.
3. When analog signals are input from CN2, the direct input, AC coupling can be achieved by inserting a 0.1µF capacitor at" A" and a 10kOhm resistor at "B". It is not necessary to be concerned about the output voltage of the input amplifier. V_{RT} may be limited in this case by NJM3403. The input voltage to the NJM3403 amplifier can be adjusted to correct. Both V_{RT} and V_{RB} can be trimmed.

Figure 5: Evaluation Circuit Diagram

Figure 6: Typical Performance Curve

Fig. 4-1: Supply Current vs. Temperature

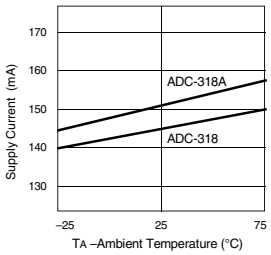


Fig. 4-2: Supply Current vs. Conversion Rate

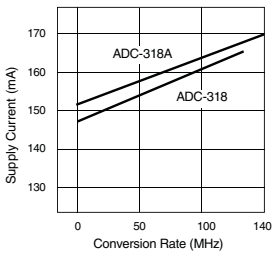


Fig. 4-3: Reference Current vs.Temperature

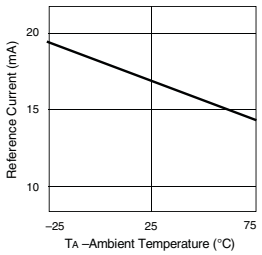


Fig. 4-4: Error Rate vs. Conversion Rate

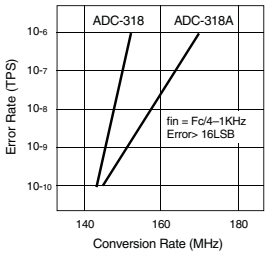


Fig. 4-5: SNR+THD vs. Input Signal Frequency

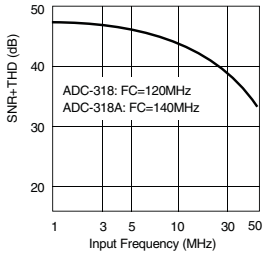


Fig. 4-6: Allowable Ambient Temperature vs. Air Flow

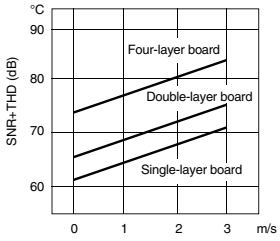


Fig. 4-7: Analog Input Current vs.Voltage Inputs

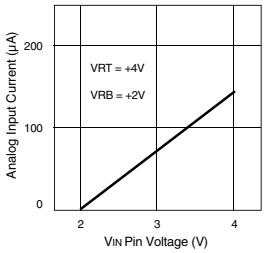


Fig. 4-8: Maximum Conversion Rate vs.Temperature

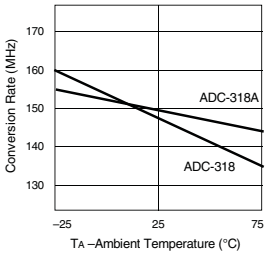
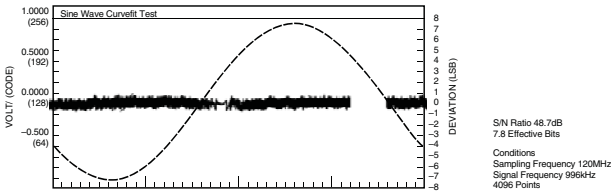
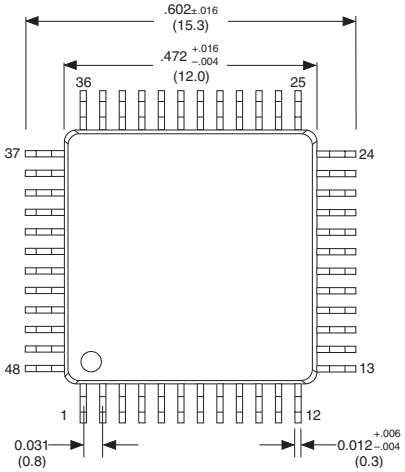
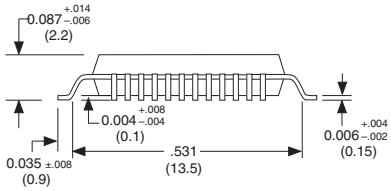


Fig. 4-9: Sine Wave Curvefit Test



MECHANICAL DIMENSIONS INCES (MM)





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ADC-318	**8-bit, 120MHz Flash A/D**
ADC-318A	**8-bit, 140MHz Flash A/D**