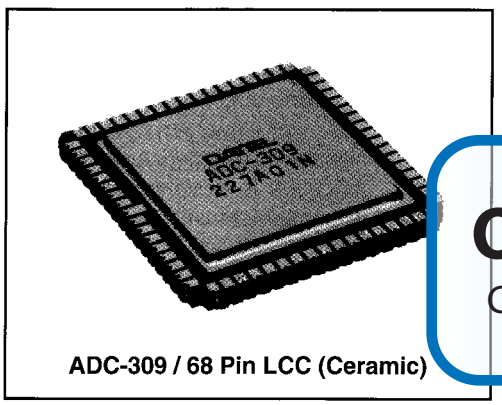
DATEL
INNOVATION and EXCELLENCE

ADC-309

8-BIT, 500 MHz FLASH A/D CONVERTER

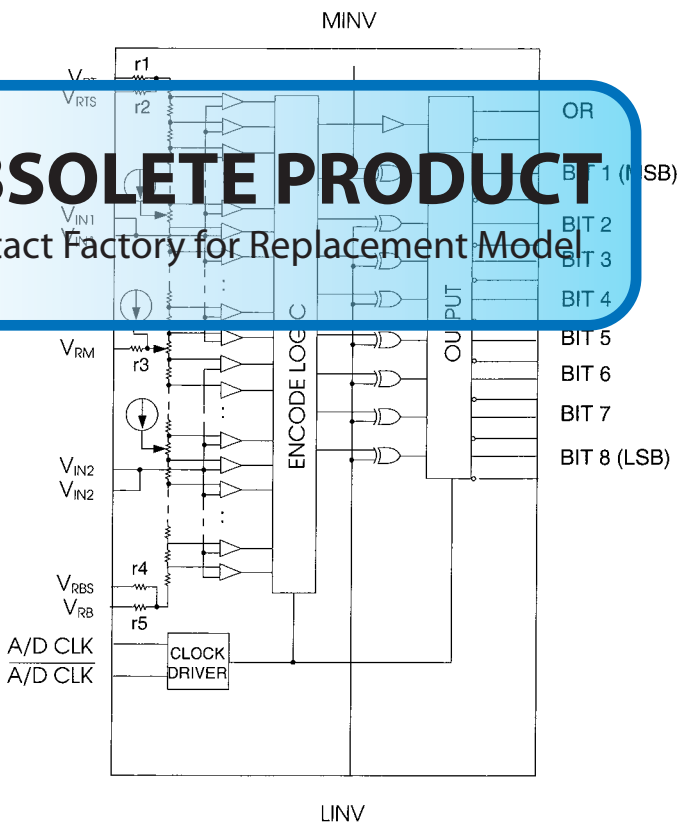
PRODUCT DATA SHEET



ADC-309 / 68 Pin LCC (Ceramic)

OBSOLETE PRODUCT
Contact Factory for Replacement Model

ADC-309 Block Diagram



Features

- 8-bit resolution
- ±1/2 LSB differential non-linearity max.
- ±0.7 LSB integral non-linearity max.
- 500 MHz conversion rate min.
- Low power consumption (2.8 W)
- Analog input bandwidth 300 MHz
- Low input capacity 20 pF typ.
- Capable of driving 50 Ω loads
- Single -5.2 V power supply

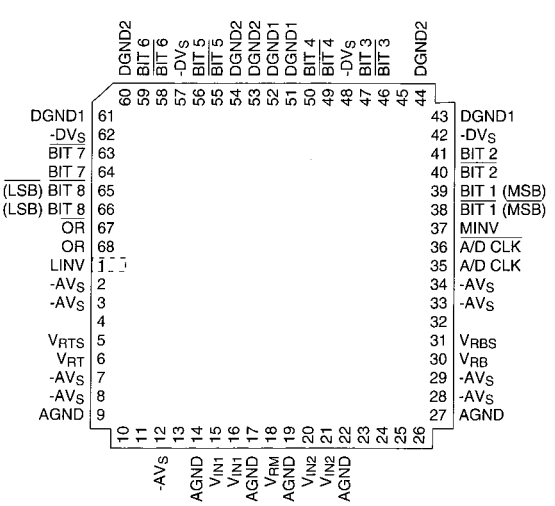
Applications

- Digital oscilloscopes
- Radar systems
- Other high-speed data acquisition systems

General Description

The ADC-309 is a monolithic 8-bit ultrahigh-speed bipolar silicon flash A/D converter IC capable of digitizing analog signals from -2 V to 0 V at a maximum rate of 500 MSPS. The digital I/O levels of this A/D converter are compatible with the ECL 100 k/10 kH/10 k.
It features a built-in integral linearity compensation circuit, low error rate and excellent temperature characteristics.

ADC-309 Input/Output Connections (Top View)
Pins without names are NC pins (internally not connected)



Description

Electrical Characteristics:

$-AV_S = -DV_S = -5.2\ V_{DC}$, $V_{RT} = V_{RTS} = 0\ V$, $V_{RB} = V_{RBS} = -2\ V_{DC}$

Analog Inputs		Min.	Typ.	Max.	Units
Analog Input Voltage		–	-2 to 0	–	V_{DC}
Analog Input Capacitance ($V_{IN} = -1\ V_{DC}$)		–	20	–	pF
Analog Input Resistance		30	70	–	kΩ
Input Bias Current ($V_{IN} = -1V_{DC}$)		–	–	620	µA
Full Scale Input Bandwidth ($V_{IN} = 2\ V_{p-p}$)		300	–	–	MHz
Reference					
Reference Input Voltage	V_{RT}	-0.1	0	+0.1	V_{DC}
	V_{RB}	-2.2	-2	-1.8	V_{DC}
Reference Resistance *1	R_{REF}	70	110	160	Ω
Residual Resistance	r1	0.1	0.5	2.0	Ω
(see block diagram)	r2	0.5	5.2	10	Ω
	r3	0.5	1.6	5.0	Ω
	r4	0.5	8.7	20	Ω
	r5	0.1	0.5	2.0	Ω
Digital Inputs					
Logic High Level	V_{IH}	-1.10	–	–	V_{DC}
Logic Low Level	V_{IL}	–	–	-1.55	V_{DC}
Logic High Current $V_{IH} = -0.8V$	I_{IH}	0	–	70	µA
Logic Low Current $V_{IL} = -1.6V$	I_{IL}	-50	–	60	µA
Input Capacitance		–	6	–	pF
Clock Duty Cycle *2		45	50	55	%
Digital Outputs (50 Ω Load to -2 V_{DC})					
Logic High Level	V_{OH}	-1.03	–	–	V_{DC}
Logic Low Level	V_{OL}	–	–	-1.58	V_{DC}
Output Rise Time *3	T_r	0.5	0.7	1.0	ns
Output Fall Time *4	T_f	0.5	0.7	1.0	ns
Output Delay	T_{do}	1.5	1.9	2.3	ns
Performance					
Resolution		–	8	–	bits
Max. Conversion Rate	F_c	500	–	–	MHz
Sampling Delay	T_{ds}	0.2	0.8	1.5	ns
Aperture Jitter	T_{aj}	–	11	–	ps
Integral Linearity Error		–	–	±0.7	LBS
Differential Linearity Error		–	–	±0.5	LBS
Differential Gain Error *)		–	1.0	–	%
Differential Phase Error *)		–	0.5	–	deg.
*) NTSC 40IRE mod. ramp, $F_C = 500MHz$					
S/N ratio (Clock Rate 500 MHz)					
$f_{IN} = 1$ kHz		44	46	–	dB
$f_{IN} = 125$ MHz		30	34	–	dB
Error Rate (Error > 16 LSB)					
$f_{IN} = 100$ MHz (Clock Rate 400 MHz)		–	10^{-11}	10^{-9}	TPS *5
$f_{IN} = 125$ MHz (Clock Rate 500 MHz)		–	10^{-8}	10^{-6}	TPS *5

*1) Between V_{RT} and V_{RB} pins
*2) (A/D CLK, $\overline{A/D\ CLK}$)
*3) 20 % to 80 %
*4) 80 % to 20 %
*5) TPS: Times Per Sample

OPERATIONAL NOTES

1. The ADC-309 is an ultra-high speed AD converter with ECL level I/O. As the high-speed digital signal is next to analog signal, the following precautions must be taken in order to obtain optimum performance.
2. Properly match the impedance (using micro strip line) to prevent distortion of waveform by the digital signal circuit (clock/data output). The ADC-309 is designed to use line with characteristic impedance of 50 Ω.
3. The ADC-309 operates on single -5.2 V power supply. However, AGND and DGND, and AV_S and DV_S are separated to prevent the noise from the digital circuit from leaking to the analog circuit. The board also should be a multi-layer board separated analog region and digital region. Avoid overlapping signal lines and power supply GND in the two regions. Connect AGND and DGND at one location (using a ferrite-bead) to avoid DC offset. The same processing is also necessary for AV_S and DV_S.
4. Connect all power supply pins and GND pins, not leaving them open.
5. Bypass capacitors (approx. 0.1 µF) with high frequency characteristics should be used to bypass between AV_S – AGND and DV_S – DGND.
6. Make complimentary use of clock input and data output as much as possible in order to obtain stable high performance.
7. When mounting the ADC in a socket, use the one with shortest leads.
8. The analog input pin V_{IN}'s have relatively large input capacitance (approx. 20 pF) for high frequency circuit. The input bandwidth of the ADC-309 is determined mainly by how much the driver can drive this capacitance rather than the characteristics of the IC.
9. All four V_{IN} pins should be connected directly at shortest distance as possible. The difference in delay between pins causes the distortion at high frequency input signals.

Description (cont'd)

Power Supply Requirements		Min.	Typ.	Max.	Units
Supply Voltage	$-AV_S$, $-DV_S$	-5.5	-5.2	-4.95	V_{DC}
	$(-AV_S) - (-DV_S)$	–50	0	+50	mV
	AGND - DGND	–50	0	+50	mV
Supply Current	I_S	-680	-520	–	mA
Power Consumption	P_d	–	2.8	3.6	W
Physical / Environmental					
Operating Temperature (Case)		-20	–	+100	°C
Storage Temperature		-65	–	+150	°C
Package		68 Pin LCC (Ceramic)			

Absolute Maximum Ratings (Ta = 25°C)

Analog			
Supply Voltage	$-AV_S$, $-DV_S$	-7 to +0.5	V_{DC}
Analog Input Voltage	V_{IN}	-2.7 to +0.5	V_{DC}
Reference Input Voltage	V_{RT}, V_{RB}, V_{RM}	$-AV_S$ to +0.5	V_{DC}
	$\lvert V_{RT} - V_{RB} \rvert$	2.5	V_{DC}
V_{RM} Pin Input Current	I_{VRM}	-3 to +3	mA
Digital			
Digital Input Voltage	MINV, LINV	-4 to +0.5	V_{DC}
	A/D CLK, $\overline{\text{A/D CLK}}$	$-DV_S$ to +0.5	V_{DC}
	I A/D CLK - $\overline{\text{A/D CLK}}$ I	2.7	V_{DC}
Digital Output Current		-30 to 0	mA
Bit 1-8, $\overline{\text{Bit 1-8}}$, OR, $\overline{\text{OR}}$			

OPERATIONAL NOTES (cont'd)

10. The voltages at V_{RT} and V_{RB} pins and the internal reference voltages are slightly different due to residual resistance. Therefore, V_{RTS} and V_{RBS} are provided to increase their precision. The reference voltage for over range is at 1/2 LSB below V_{RTS} and the lowest input voltage at which the output code changes is at 1/2 LSB above V_{RBS}.
11. VRM is originally provided to reduce integral linearity error, but there is no need for this. It should simply be kept open.

OPERATIONAL NOTES (cont'd)

12. OR and $\overline{\text{OR}}$ pins are outputs indicating that the input is over range. These pins do not invert at MINV nor LINV.
13. When there is noise in the MINV or LINV pins, it is difficult to find the cause from the resulting error. Therefore, provide sufficient margins for the High/Low voltage levels and connect as close to DGND as possible through bypass capacitor (approx. 0.1 µF) with high frequency characteristics. Stable low level can be obtained. The recommended high level input voltage is between -0.5 V and -1.0 V and the low level input voltage is between -1.6 V and -2.5 V.
14. Although the electrical characteristics of the ADC-309 depends on the clock duty cycle, this is not significant. Therefore, the electrical characteristics are defined at 50% duty cycle taking into consideration the ease of generating the clock signal.
15. Error rate changes with input frequency and input amplitude. The error rate, at the electrical characteristics specific condition which is full scale sine wave input at 1/4 the clock frequency, can be considered close to the upper limit during actual use (when the input signal is below Nyquist frequency).
16. When the chip temperature rises, current dissipation increases and the error rate also increases. Sufficient cooling is necessary in order to prolong product life.

Mechanical Dimension ADC-309

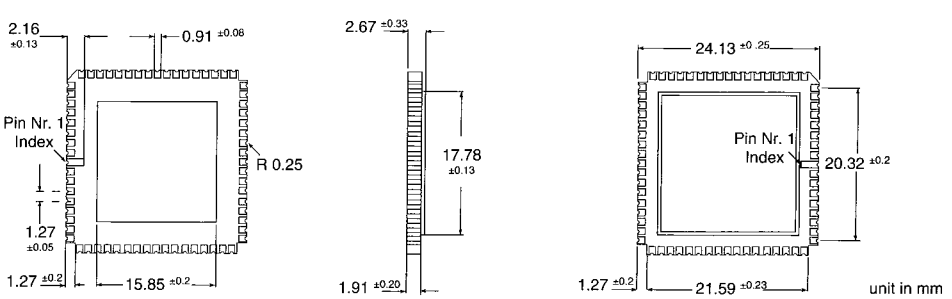
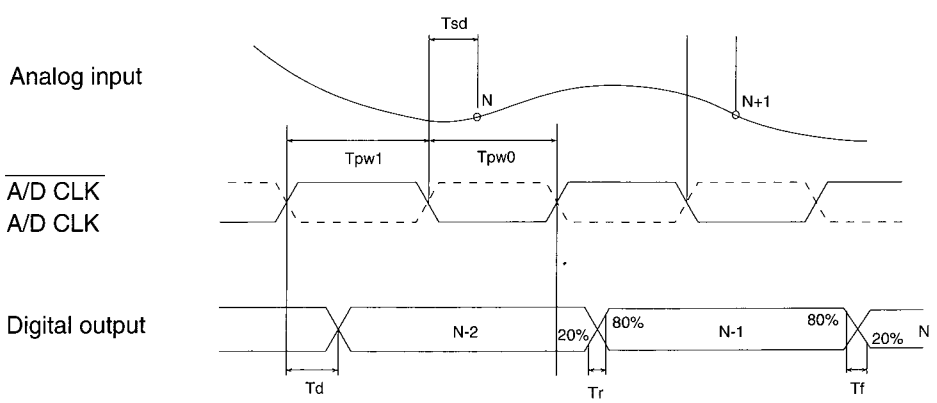


Table 4: Digital Output

This table and the chart below indicate the compatibility between the analog input and the digital output code.

MINV LINV	0 0			0 1			1 0			1 1		
Input Voltage	OR	MSB	LSB	Output Coding						OR	MSB	LSB
0.0000 V	1	1111	1111	1	1000	0000	1	0111	1111	1	0000	0000
	0	1111	1111	0	1000	0000	0	0111	1111	0	0000	0000
- 0.0078 V	0	1111	1110	0	1000	0001	0	0111	1110	0	0000	0001
:												
- 0.9922 V	0	1000	0000	0	1111	1111	0	0000	0000	0	0111	1111
- 1.0000 V	0	0111	1111	0	0000	0000	0	1111	1111	0	1000	0000
:												
- 1.5000 V	0	0011	1111	0	0100	0000	0	1011	1111	0	1100	0000
:												
- 1.7500 V	0	0001	1111	0	0110	0000	0	1001	1111	0	1110	0000
:												
- 1.9844 V	0	0000	0001	0	0111	1110	0	1000	0001	0	1111	1110
- 1.9922 V	0	0000	0000	0	0111	1111	0	1000	0000	0	1111	1111
- 2.0000 V	0	0000	0000	0	0111	1111	0	1000	0000	0	1111	1111

Timing Chart



Tsd = 0.8 ns, Td = 1.9 ns, Tr = Tf = 0.7 ns