DATEL
INNOVATION and EXCELLENCE

ADC-306

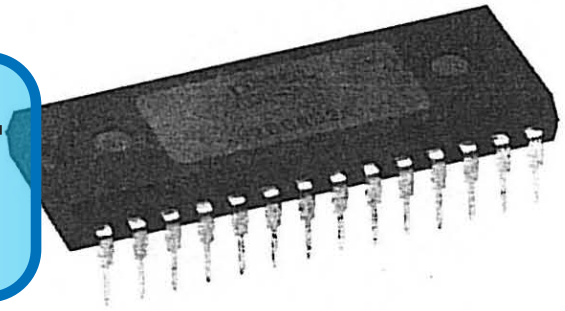
8-BIT, 75 MHz LOW POWER FLASH A/D

PRODUCT DATA SHEET

OBSOLETE PRODUCT
Contact Factory for Replacement Model

Features

- 8-bit resolution
- ±1/2 LSB non-linearity
- 75 MHz conversion rate
- Low power consumption (280 mW)
- Analog input bandwidth 150 MHz
- Low input capacitance 7 pF
- Single supply operation -5.2 V



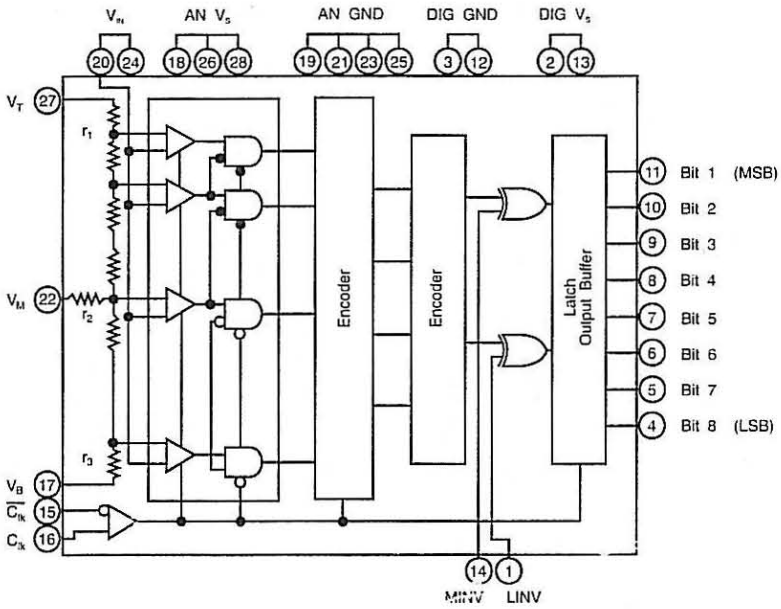
Applications

- Digital oscilloscopes
- High-speed data acquisition
- TV video encoding
- VCR digital systems
- Radar pulse analysis
- Transient analysis
- Medical electronics
- Sonar systems

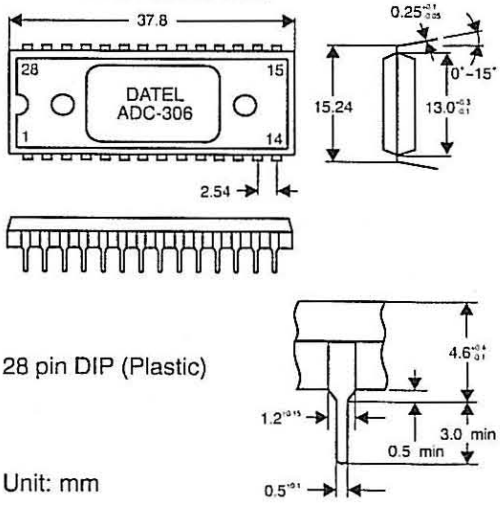
General Description

DATEL's ADC-306 is an 8-bit high-speed flash A/D converter IC capable of digitizing analog signals at a maximum rate of 75 MSPS. The ADC-306 is sparkle code error free up to Nyquist frequency. The digital I/O levels of this A/D converter are compatible with the ECL 100K/ 10KH/10K.

The ADC-306 is pin-compatible with the earlier models ADC-301/ADC-302. These can be replaced by the ADC-306 without any design changes in most cases. Compared with the earlier models, this new model has been greatly improved in performance, by incorporating advanced process, new circuit design and carefully considered layout.



Mechanical Dimensions



28 pin DIP (Plastic)

Unit: mm

Table 1: ADC-306 Input/Output Connections

Pin	Function	Pin	Function
1	OUTPUT POL (LINV)	28	ANALOG V_S (-5.2V)
2	DIGITAL V_S (-5.2V)	27	REF INPUT V_T (0V)
3	DIGITAL GROUND	26	ANALOG V_S (-5.2V)
4	BIT 8 (LSB)	25	ANALOG GROUND
5	BIT 7	24	ANALOG INPUT
6	BIT 6	23	ANALOG GROUND
7	BIT 5	22	REFERENCE V_M
8	BIT 4	21	ANALOG GROUND
9	BIT 3	20	ANALOG INPUT
10	BIT 2	19	ANALOG GROUND
11	BIT 1 (MSB)	18	ANALOG V_S (-5.2V)
12	DIGITAL GROUND	17	REF INPUT V_B (-2V)
13	DIGITAL V_S (-5.2V)	16	CLOCK INPUT
14	OUTPUT POL (MINV)	15	$\overline{\text{CLOCK}}$ INPUT

Table 2: Description

Inputs	Min.	Typ.	Max.	Units
Analog Input Voltage	–	0 ~ -2	–	V
Analog Input Capacitance	–	17	–	pF
Analog Input Resistance	–	390	–	kΩ
Analog Input Bias Current	–	–	200	µA
Digital Input Voltage V_H	-1.13	–	–	V
V_L	–	–	-1.50	V
Digital Input Current I_H	–	–	50	µA
I_L	–	–	50	µA
Reference Inputs				
Reference Input Voltage V_B	-2.2	-2.0	-1.8	V
V_T	-0.1	0	+0.1	V
Reference resistance R_{REF}	75	110	155	Ω
Residual resistance r1	–	0.6	–	Ω
(see block diagram) r2	–	2.0	–	Ω
r3	–	0.6	–	Ω
Offset Voltage V_B	10	15	20	mV
V_T	16	19	24	mV
Outputs				
Resolution	8	–	–	Bits
Digital output Logic "H" level	-1.03	–	–	V
Logic "L" level	–	–	-1.62	V
Output rising time T_r	–	0.9	–	ns
Output falling time T_f	–	2.1	–	ns
Performance				
Conversion rate	75	–	–	MHz
Int. non-linearity	–	± 0.3	± 0.5	LSB
Diff. non-linearity	–	± 0.3	± 0.5	LSB
Diff. gain error	–	1.0	–	%
Diff. phase error	–	0.5	–	deg.
Aperture jitter	–	10	–	ps
Sampling delay T_{sd}	–	3	–	ns
Output delay T_d	4.0	6.5	9.0	ns
Clock pulse width T_{PW1}	6.6	–	–	ns
T_{PW0}	6.6	–	–	ns
Dynamic characteristics (for Conv. Rate of 75 MSPS)				
Full scale Input Bandwidth V_{IN}=2Vp-p	150	–	–	MHz
Bandwidth				
S/N ratio Input=1MHz, FS	–	48	–	dB
Input=20MHz, FS	–	40	–	dB
Error rate Input=18.749MHz, FS	–	–	10^{-9}	
(Error=16LSB min.)				

Technical Notes

1. Even with the input capacitance down to 17pF, or less, the converter still requires an input amplifier with good drive capability. The amplifier will require wide band width and high slew rate (250V/µS typical) to take full advantage of the input band width of the converter.
2. The input impedance of the A/D's are capacitive which may result in the input amplifier becoming unstable and cause oscillations. A resistor with a value between 2 and 10 Ohms between the amplifier and the input to the converter will stop any oscillations.
3. Clock and $\overline{\text{Clock}}$ (ECL) are usually differentially supplied to pins 16 and 15.
4. The polarity of the output data is controlled by inputs MINV (pin 14) which controls the MSB alone and LINV (pin 1) which controls Bit 2 to Bit 8 (LSB). The combination of '0' s and '1' on these inputs offer the user various code options. Detailed coding shown on page 4. Logic level '0' is obtained by leaving inputs open, logic level '1' is obtained by connecting a 3.9K Ohm resistor to GND.
5. The digital outputs Bits 1 to 8 require pull down resistors, 620 Ohms, connected to the negative supply rail.
6. The reference voltage range (-2.0V to 0V typical) determines the dynamic range of the input voltage. Adjustments to this range can be made within the range V_B = -2 ± 0.2V and V_T = 0V ± 0.1V. The reference input V_B (pin 17) should be decoupled to GND using 1µF and 0.01µF capacitors. Improvement in the high frequency stability can be achieved by decoupling terminal V_M (pin 22) using a 0.01µF.
7. Terminal V_M is used when a more accurate linearity than that specified is required. The external circuit to achieve this is shown on page 3.
8. All pins not being used should be grounded.
9. Substantial analog and digital ground planes must be provided. It is recommended that these ground planes are taken to a common point, the power ground line, as close to the ADC as possible.

Table 2: Description (cont'd)

Power Supply Requirements	Min.	Typ.	Max.	Units
Supply Voltage AV_S, DV_S	-5.5	-5.2	-4.95	V
Supply Current	150	104	–	mA
Power Dissipation	–	580	–	mW
DGND - AGND	–50	–	+50	mV
AV_S - DV_S	–50	–	+50	mV
Physical / Environmental				
Operating temperature	-25	–	+100	°C
Storage temperature	-65	–	+150	°C

Table 3: Absolute Maximum Ratings (Ta = 25°C)

Supply Voltage V_S	+0.5 to -7	V
Input Voltage V_{IN}	+0.5 to -2.7	V
Reference Voltage V_T, V_B, V_M	+0.5 to -2.7	V
Reference Voltage $\lvert V_T - V_B \rvert$	2.5	V
Digital Inputs	+0.5 to -4	V
| Clock - $\overline{\text{Clock}}$ |	2.7	V
V_M Input Current	-3 to +3	mA
Digital Output Current	0 to -30	mA

TECHNICAL NOTES (cont'd)

10. The power supplies to analog and digital inputs (-5.2V) should be supplied from separate, isolated power supplies. If one of the power supplies fails or is shorted to ground for more than 1 second there is a possibility the device may be destroyed. Both -5.2V lines should be decoupled using 1µF and 0.01µF capacitors located as close to the pins as possible.

Application Circuit (Example)

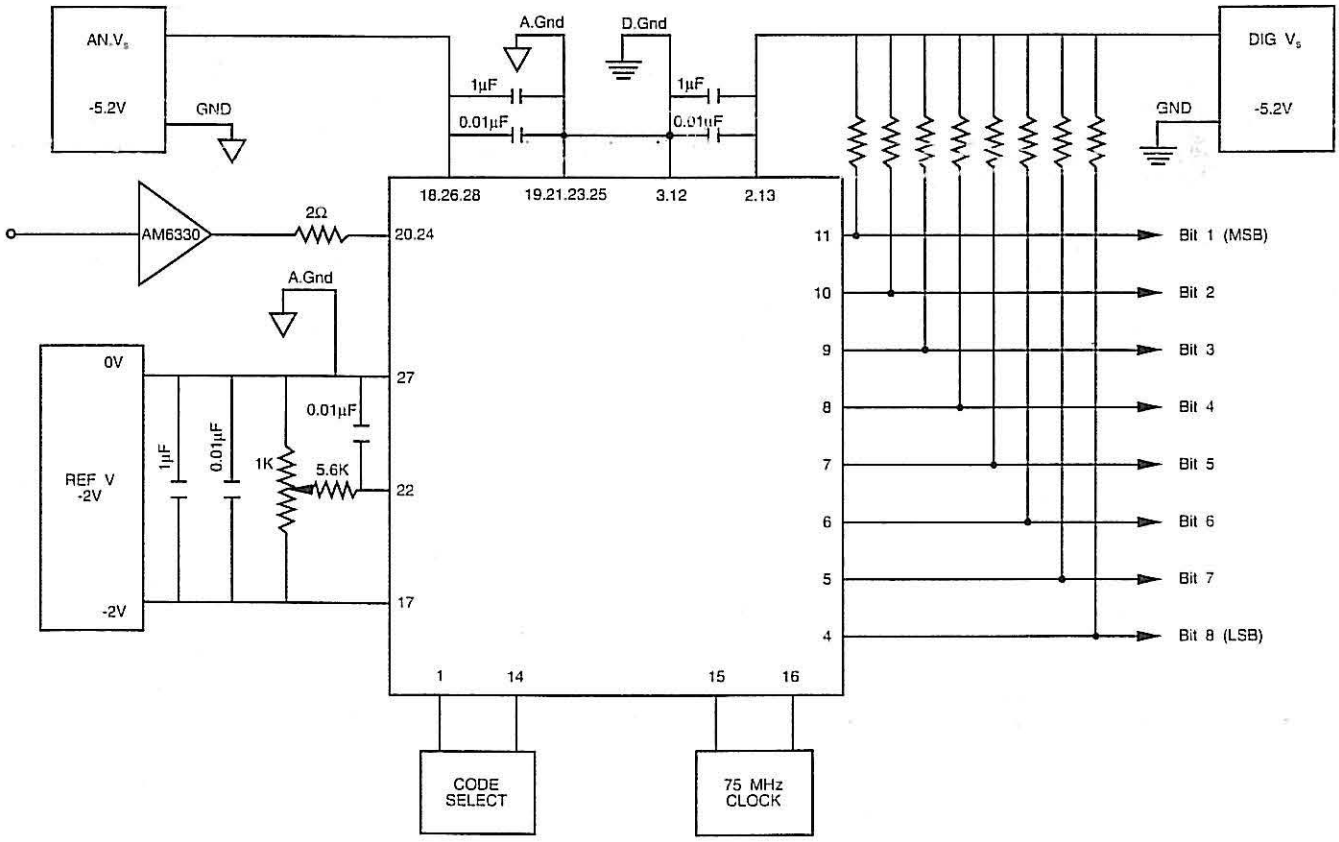
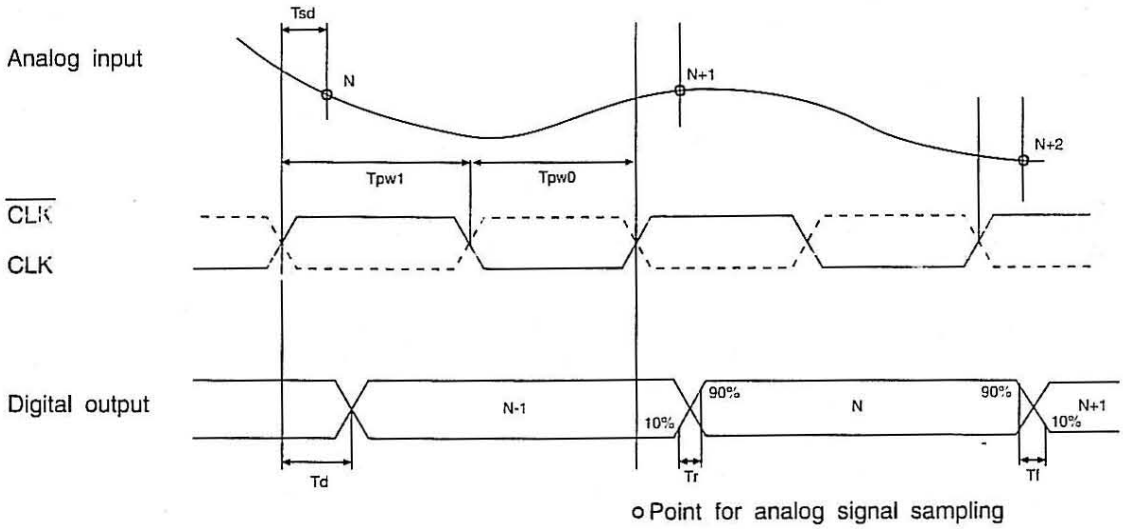


Table 4: Digital Output

This table and the chart below indicate the compatibility between the analog input and the digital output code.

VIN	Step	MINV 1 LINV 1	0 1	1 0	0 0
		D7.....D0	D7.....D0	D7.....D0	D7.....D0
		000.....00	100.....00	011.....11	111.....11
0V	0	000.....00	100.....00	011.....11	111.....11
	1	000.....01	100.....01	011.....10	111.....10
		:	:	:	:
		:	:	:	:
-1V	127	011.....11	111.....11	000.....00	100.....00
	128	100.....00	000.....00	111.....11	011.....11
		:	:	:	:
		:	:	:	:
	254	111.....10	011.....10	100.....01	000.....01
	255	111.....11	011.....11	100.....00	000.....00
-2V		111.....11	011.....11	100.....00	000.....00

Timing Chart



o Point for analog signal sampling