

Dual-Channel, 14-Bit CCD Signal Processor with $Precision\ Timing^{TM}$ Core

AD9973

FEATURES

1.8 V analog and digital core supply voltage
Serial data link with reduced range LVDS outputs
Correlated double sampler (CDS) with -3 dB, 0 dB, +3 dB,
+6 dB gain
6 dB to 42 dB, 10-bit variable gain amplifier (VGA)
14-bit, 65 MHz analog-to-digital converter
Black level clamp with variable level control
Complete on-chip timing generator

WWW. Precision Timing core with 240 ps resolution @ 65 MHz
On-chip 3 V horizontal and RG drivers
6 mm × 6 mm, 84-ball CSP_BGA package

APPLICATIONS

Professional HDTV camcorders
Professional, high-end digital cameras
Broadcast cameras
Industrial high speed cameras

GENERAL DESCRIPTION

The AD9973 is a highly integrated dual channel CCD signal processor for high speed digital video camera applications. Each channel is specified at pixel rates of up to 65 MHz, and consists of a complete analog front end with analog-to-digital conversion, combined with a programmable timing driver. The *Precision Timing* core allows adjustment of high speed clocks with 240 ps resolution at 65 MHz operation. The AD9973 also contains a reduced range LVDS interface for the dual-channel data outputs.

Each analog front end (AFE) includes black level clamping, CDS, VGA, and a 65 MSPS, 14-bit analog-to-digital converter. The timing driver provides the high speed CCD clock drivers for RG, HL, and H1 to H4. Operation is programmed using a 3-wire serial interface.

Packaged in a space-saving 6 mm \times 6 mm, 84-ball CSP_BGA, the AD9973 is specified over an operating temperature range of -25° C to $+85^{\circ}$ C.

REFT A REFB A AD9973 VREF A VREF_B DOUTOP A DOUTON A CCDINP_A CDS ADC DOUT1P A CCDINM A DOUT1N A 6dB ~ 42dB REDUCED RANGE TCLKP A CLAMP TCLKN_A DOUTOP B CLAMP DOUTON B -3dB, 0dB, +3dB, +6dB 6dB ~ 42dB DOUT1P_B CCDINP_B DOUT1N_B ADC CCDINM B C TCLKP B TCLKN B LDO_OUT_A I DO A 1.8V OUTPUT INTERNAL CLOCKS LDO OUT B LDO B RG A PRECISION CLI_A RG B TIMING CLI_B HORIZONTAL DRIVERS HLA. H1A TO H4A SCK A SYNC GENERATOR INTERNAL REGISTERS HLB, H1B TO H4B SCK B

Figure 1.

FUNCTIONAL BLOCK DIAGRAM

For more information about the AD9973, contact Analog Devices, Inc. via email at afe.ccd@analog.com.

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NOTES

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