# ANALOG DEVICES

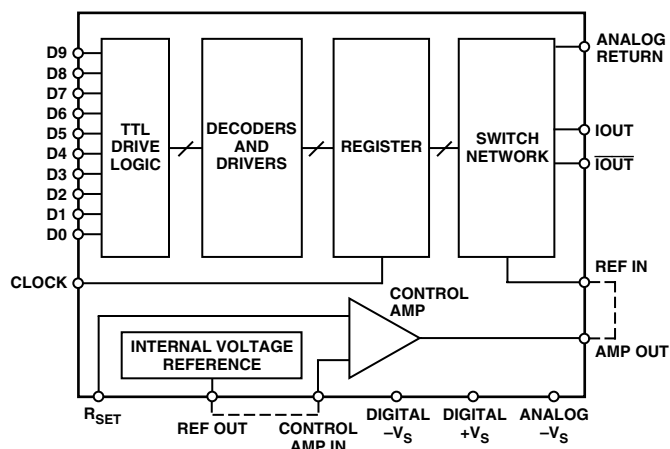# 10-Bit, 170 MSPS D/A Converter

# AD9731

## FEATURES
**170 MSPS Update Rate**
**TTL/High Speed CMOS-Compatible Inputs**
**Wideband SFDR: 66 dB @ 2 MHz/50 dB @ 65 MHz**
**Pin-Compatible, Lower Cost Replacement for Industry Standard AD9721 DAC**
**Low Power: 439 mW @ 170 MSPS**
**Fast Settling: 3.8 ns to 1/2 LSB**
**Internal Reference**
**Two Package Styles: 28-Lead SOIC and SSOP**

## APPLICATIONS
**Digital Communications**
**Direct Digital Synthesis**
**Waveform Reconstruction**
**High Speed Imaging**
**5 MHz to 65 MHz HFC Upstream Path**

## FUNCTIONAL BLOCK DIAGRAM



## GENERAL DESCRIPTION

The AD9731 is a 10-bit, 170 MSPS, bipolar D/A converter that is optimized to provide high dynamic performance, yet offer lower power dissipation and more economical pricing than afforded by previous bipolar high performance DAC solutions. The AD9731 was designed primarily for demanding communications systems applications where wideband spurious-free dynamic range (SFDR) requirements are strenuous and could previously only be met by using a high performance DAC such as the industry-standard AD9721. The proliferation of digital communications into base station and high volume subscriber-end markets has created a demand for excellent DAC performance delivered at reduced levels of power dissipation and cost. The AD9731 is the answer to that demand.

Optimized for direct digital synthesis (DDS) waveform reconstruction, the AD9731 provides 50 dB of wideband harmonic suppression over a dc-to-65 MHz analog output bandwidth. This signal bandwidth addresses the transmit spectrum in many of the emerging digital communications applications where signal purity is critical. Narrowband, the AD9731 provides an SFDR of greater than 79 dB. This excellent wideband and narrowband ac performance, coupled with a lower pricing structure, make the AD9731 the optimum high performance DAC value.

The AD9731 is packaged in 28-lead SOIC (same footprint as the industry-standard AD9721) and super space-saving 28-lead SSOP; both are specified to operate over the extended industrial temperature range of –40°C to +85°C.

REV. B

| Parameter | Temp | Test Level | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RESOLUTION | | | | 10 | | Bits |
| MAX CONVERSION RATE | $-40°C$ to $+85°C$ | IV | 170 | | | MHz |
| DC ACCURACY | | | | | | |
| Differential Nonlinearity | 25°C | I | | 0.25 | 1 | LSB |
| | Full | VI | | 0.35 | 1.5 | LSB |
| Integral Nonlinearity | 25°C | I | | 0.6 | 1 | LSB |
| | Full | VI | | 0.7 | 1.5 | LSB |
| INITIAL OFFSET ERROR | | | | | | |
| Zero-Scale Offset Error | 25°C | I | | 35 | 70 | µA |
| | Full | VI | | 40 | 100 | µA |
| Full-Scale Gain Error[1] | 25°C | I | | 2.5 | 5 | % FS |
| | Full | VI | | 2.5 | 5 | % FS |
| Offset Drift Coefficient | | V | | 0.04 | | µA/°C |
| REFERENCE/CONTROL AMP | | | | | | |
| Internal Reference Voltage[2] | 25°C | I | $-1.35$ | $-1.25$ | $-1.15$ | V |
| Internal Reference Voltage Drift | Full | IV | | 100 | | µV/°C |
| Internal Reference Output Current[3] | Full | VI | $-50$ | | $+500$ | µA |
| Amplifier Input Impedance | 25°C | V | | 50 | | kΩ |
| Amplifier Bandwidth | 25°C | V | | 2.5 | | MHz |
| REFERENCE INPUT[4] | | | | | | |
| Reference Input Impedance | 25°C | V | | 4.6 | | kΩ |
| Reference Multiplying Bandwidth[5] | 25°C | V | | 75 | | MHz |
| OUTPUT PERFORMANCE | | | | | | |
| Output Current[4, 6] | 25°C | V | | 20 | | mA |
| Output Compliance | 25°C | IV | $-1.5$ | | $+3$ | V |
| Output Resistance | 25°C | V | | 240 | | Ω |
| Output Capacitance | 25°C | V | | 5 | | pF |
| Voltage Settling Time to 1/2 LSB ($t_{ST}$)[7] | 25°C | V | | 3.8 | | ns |
| Propagation Delay ($t_{PD}$)[8] | 25°C | V | | 2.9 | | ns |
| Glitch Impulse[9] | 25°C | V | | 4.1 | | pVs |
| Output Slew Rate[10] | 25°C | V | | 400 | | V/µs |
| Output Rise Time[10] | 25°C | V | | 1 | | ns |
| Output Fall Time[10] | 25°C | V | | 1 | | ns |
| DIGITAL INPUTS | | | | | | |
| Input Capacitance | Full | IV | | 2 | | pF |
| Logic "1" Voltage | Full | VI | 2.0 | | | V |
| Logic "0" Voltage | Full | VI | | | 0.8 | V |
| Logic "1" Current | 25°C | VI | | 8 | 50 | µA |
| Logic "0" Current | 25°C | VI | | 30 | 100 | µA |
| Data Setup Time ($t_S$)[11] | 25°C | IV | 2 | | | ns |
| | Full | IV | 2.5 | | | ns |
| Data Hold Time ($t_H$)[12] | 25°C | IV | 1.0 | 0.1 | | ns |
| | Full | IV | 1.0 | 0.1 | | ns |
| Clock Pulsewidth Low ($pw_{MIN}$) | 25°C | IV | 2 | | | ns |
| Clock Pulsewidth High ($pw_{MAX}$) | 25°C | IV | 2 | | | ns |
| SFDR PERFORMANCE (Wideband)[13] | | | | | | |
| $A_{OUT}$ = 0 dBFS | | | | | | |
| 2 MHz $f_{OUT}$ | 25°C | V | | 66 | | dB |
| 10 MHz $f_{OUT}$ | 25°C | V | | 62 | | dB |
| 20 MHz $f_{OUT}$ | 25°C | V | | 61 | | dB |
| 40 MHz $f_{OUT}$ | 25°C | V | | 55 | | dB |
| 65 MHz $f_{OUT}$ (Clock = 170 MHz) | 25°C | V | | 50 | | dB |
| 70 MHz $f_{OUT}$ (Clock = 170 MHz) | 25°C | V | | 47 | | dB |

# SPECIFICATIONS

| Parameter | Temp | Test Level | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SFDR PERFORMANCE (Narrowband)[13] | | | | | | |
|   2 MHz; 2 MHz Span | 25°C | V | | 79 | | dB |
|   25 MHz, 2 MHz Span | 25°C | V | | 61 | | dB |
|   10 MHz, 5 MHz Span (Clock = 170 MHz) | 25°C | V | | 73 | | dB |
| INTERMODULATION DISTORTION[14] | | | | | | |
|   F1 = 800 kHz, F2 = 900 kHz | 25°C | V | | 58 | | dB |
| POWER SUPPLY[15] | | | | | | |
|   Digital –V Supply Current | 25°C | I | | 27 | 37 | mA |
| | Full | VI | | 27 | 42 | mA |
|   Analog –V Supply Current | 25°C | I | | 45 | 53 | mA |
| | Full | VI | | 45 | 66 | mA |
|   Digital +V Supply Current | 25°C | I | | 13 | 20 | mA |
| | Full | VI | | 15 | 22 | mA |
|   Power Dissipation | 25°C | V | | 439 | | mW |
| | Full | V | | 449 | | mW |
|   PSRR | 25°C | V | | 100 | | µA/V |

NOTES

[1]Measured as an error in ratio of full-scale current to current through $R_{SET}$ (640 µA nominal); ratio is nominally 32. DAC load is virtual ground.

[2]Internal reference voltage is tested under load conditions specified in Internal Reference Output current specification.

[3]Internal reference output current defines load conditions applied during Internal Reference Voltage test.

[4]Full-scale current variations among devices are higher when driving REFERENCE IN directly.

[5]Frequency at which a 3 dB change in output of DAC is observed; $R_L$ = 50 Ω; 100 mV modulation at midscale.

[6]Based on $I_{FS}$ = 32 (CONTROL AMP IN/$R_{SET}$) when using internal control amplifier. DAC load is virtual ground.

[7]Measured as voltage settling at midscale transition to ±0.5 LSB, $R_L$ = 50 Ω.

[8]Measured from 50% point of rising edge of CLOCK signal to 1/2 LSB change in output signal.

[9]Peak glitch impulse is measured as the largest area under a single positive or negative transient.

[10]Measured with $R_L$ = 50 Ω and DAC operating in latched mode.

[11]Data must remain stable for specified time prior to rising edge of CLOCK.

[12]Data must remain stable for specified time after rising edge of CLOCK.

[13]SFDR is defined as the difference in signal energy between the full-scale fundamental signal and worst-case spurious frequencies in the output spectrum window. The frequency span is dc-to-Nyquist unless otherwise noted.

[14]Intermodulation distortion is the measure of the sum and difference products produced when a two-tone input is driven into the DAC. The distortion products created will manifest themselves at $(2F_2–F_1)$ and $(2F_1–F_2)$ of the two tones.

[15]Supply voltages should remain stable within ±5% for nominal operation.
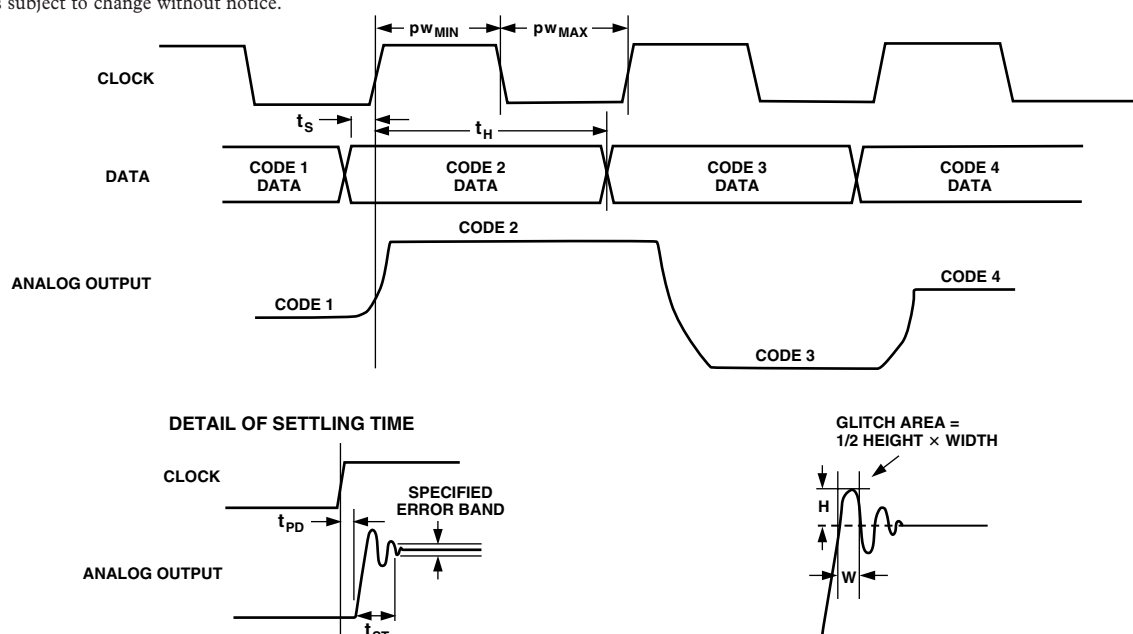
Specifications subject to change without notice.



*Figure 1. Timing Diagrams*

# AD9731

## ABSOLUTE MAXIMUM RATINGS*

Analog Output . . . . . . . . . . . . . . . . . . . . . . . . . . . . $-V_S$ to $+V_S$
$+V_S$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $+6$ V
Digital Inputs . . . . . . . . . . . . . . . . . . . . . . . . . $-0.7$ V to $+V_S$
$-V_S$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $-7$ V
Analog Output Current . . . . . . . . . . . . . . . . . . . . . . 30 mA
Control Amplifier Input Voltage Range . . . . . . . . 0 V to $-4$ V
Reference Input Voltage Range . . . . . . . . . . . . . . 0 V to $-V_S$
Maximum Junction Temperature . . . . . . . . . . . . . . . 150°C
Operating Temperature Range . . . . . . . . . . . $-40$°C to $+85$°C
Internal Reference Output Current . . . . . . . . . . . . . . 500 µA
Lead Temperature (10 sec Soldering) . . . . . . . . . . . . 300°C
Storage Temperature . . . . . . . . . . . . . . . . . . $-65$°C to $+165$°C
Control Amplifier Output Current . . . . . . . . . . . . $\pm2.5$ mA

*Stresses above those listed under Absolute Maximum Ratings may cause perma-
nent damage to the device. This is a stress rating only; functional operation of the
device at these or any other conditions above those indicated in the operational
sections of this specification is not implied. Exposure to absolute maximum rating
conditions for extended periods may affect device reliability.

## EXPLANATION OF TEST LEVELS

| Test Level | Definition |
|---|---|
| I | 100% production tested |
| II | The parameter is 100% production tested at 25°C; sampled at temperature production. |
| III | Sample tested only |
| IV | Parameter is guaranteed by design and characterization testing. |
| V | Parameter is a typical value only. |
| VI | All devices are 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range devices. |

## ORDERING GUIDE

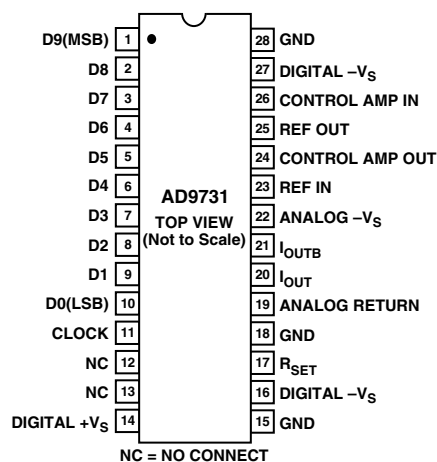| Model | Temperature Range | Package Description | Package Options |
|---|---|---|---|
| AD9731BR | $-40$°C to $+85$°C | 28-Lead Wide Body (SOIC) | R-28 |
| AD9731BR-REEL | $-40$°C to $+85$°C | 28-Lead Wide Body (SOIC) | R-28 |
| AD9731BRS | $-40$°C to $+85$°C | 28-Lead Shrink Small (SSOP) | RS-28 |
| AD9731BRS-REEL | $-40$°C to $+85$°C | 28-Lead Shrink Small (SSOP) | RS-28 |
| AD9731-PCB | 0°C to 70°C | PCB | |

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily
accumulate on the human body and test equipment and can discharge without detection. Although
the AD9731 features proprietary ESD protection circuitry, permanent damage may occur on
devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are
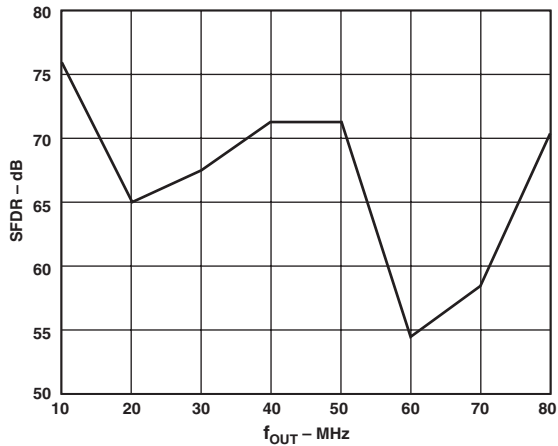recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

## PIN FUNCTION DESCRIPTIONS

| Pin No. | Mnemonic | Function |
|---|---|---|
| 1 | D9(MSB) | Most significant data bit of digital input word |
| 2–9 | D8–D1 | Eight bits of 10-bit digital input word |
| 10 | D0(LSB) | Least significant data bit of digital input word |
| 11 | CLOCK | TTL-compatible edge-triggered latch enable signal for on-board registers |
| 12, 13 | NC | No internal connection to this pin |
| 14 | DIGITAL $+V_S$ | 5 V supply voltage for digital circuitry |
| 15, 18, 28 | GND | Converter ground |
| 16 | DIGITAL $-V_S$ | –5.2 V supply voltage for digital circuitry |
| 17 | $R_{SET}$ | Connection for external reference set resistor; nominal 1.96 k$\Omega$. Full-scale output current = 32 (control amp in V/$R_{SET}$). |
| 19 | ANALOG RETURN | Analog return. This point and the reference side of the DAC load resistors should be connected to the same potential (nominally ground). |
| 20 | $I_{OUT}$ | Analog current output; full-scale current occurs with a digital word input of all "1s." With external load resistor, output voltage = $I_{OUT}$ ($R_{LOAD}\|R_{INTERNAL}$). $R_{INTERNAL}$ is nominally 240 $\Omega$. |
| 21 | $I_{OUTB}$ | Complementary analog current output; full-scale current occurs with a digital word input of all "0s." |
| 22 | ANALOG $-V_S$ | Negative analog supply, nominally –5.2 V |
| 23 | REF IN | Normally connected to CONTROL AMP OUT (Pin 24). Direct line to DAC current source network. Voltage changes (noise) at this point have a direct effect on the full-scale output current of the DAC. Full-scale current output = 32 (CONTROL AMP IN/$R_{SET}$) when using the internal amplifier. DAC load is virtual ground. |
| 24 | CONTROL AMP OUT | Normally connected to REF IN (Pin 23). Output of internal control amplifier that provides a reference for the current switch network. |
| 25 | REF OUT | Normally connected to CONTROL AMP IN (Pin 26). Internal voltage reference, nominally –1.25 V. |
| 26 | CONTROL AMP IN | Normally connected to REF Out (Pin 25) if not connected to external reference. |
| 27 | DIGITAL $-V_S$ | Negative digital supply, nominally –5.2 V. |

## PIN CONFIGURATION



```
D9(MSB)  1  •              28  GND
    D8   2                 27  DIGITAL –Vs
    D7   3                 26  CONTROL AMP IN
    D6   4                 25  REF OUT
    D5   5                 24  CONTROL AMP OUT
    D4   6      AD9731      23  REF IN
    D3   7     TOP VIEW     22  ANALOG –Vs
    D2   8  (Not to Scale)  21  IOUTB
    D1   9                 20  IOUT
 D0(LSB) 10                19  ANALOG RETURN
  CLOCK  11                18  GND
    NC   12                17  RSET
    NC   13                16  DIGITAL –Vs
DIGITAL +Vs 14             15  GND
```

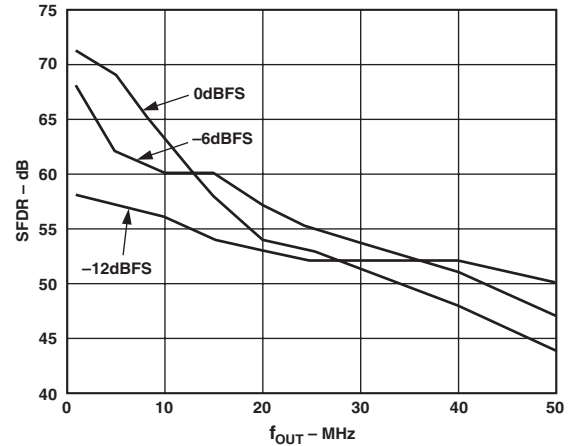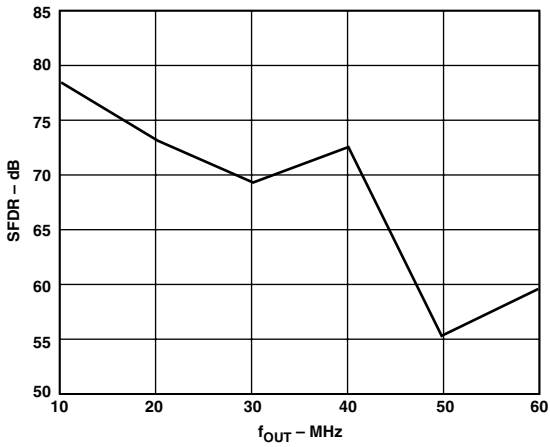NC = NO CONNECT

# AD9731–Typical Performance Characteristics



TPC 1. Narrowband SFDR (Clock = 170 MHz) vs. $f_{OUT}$ Frequency



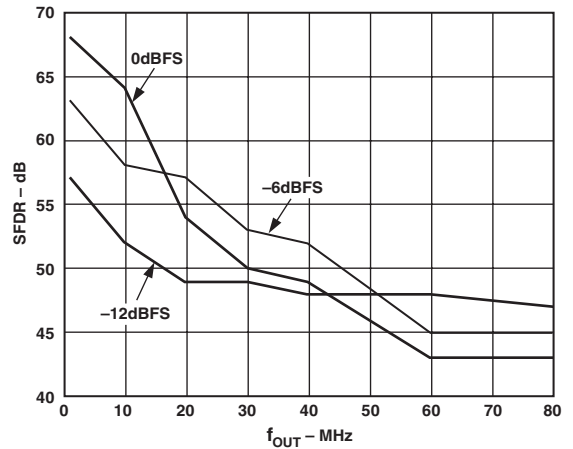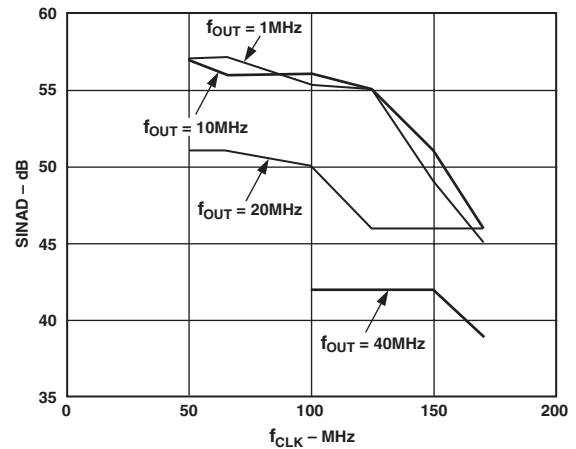TPC 2. Narrowband SFDR (Clock = 125 MHz) vs. $f_{OUT}$ Frequency
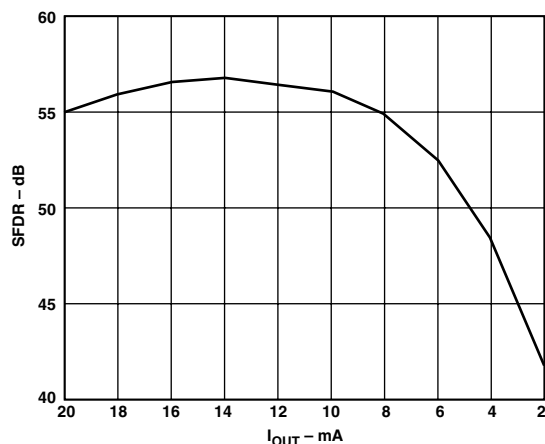


TPC 3. Wideband SFDR, $f_{CLK}$ = 50 MSPS



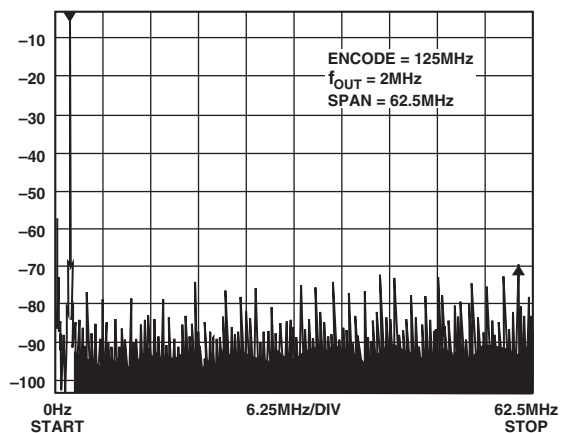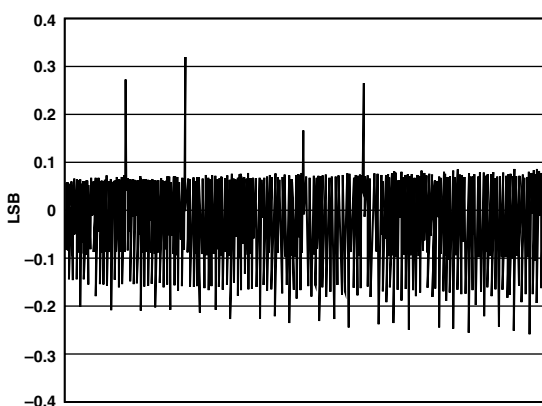TPC 4. Wideband SFDR, $f_{CLK}$ = 125 MSPS



TPC 5. Wideband SFDR, $f_{CLK}$ = 170 MSPS



TPC 6. SINAD, $A_{OUT}$ = 0 dBFS

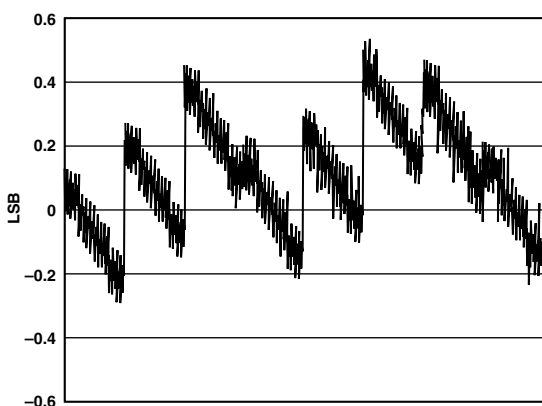TPC 7. SFDR vs. $I_{OUT}$ (Clock =125 MHz/$f_{OUT}$ = 40 MHz)



ENCODE = 125MHz
$f_{OUT}$ = 2MHz
SPAN = 62.5MHz

TPC 10. Wideband SFDR 2 MHz $f_{OUT}$; 125 MHz Clock



TPC 8. Typical Differential Nonlinearity Performance (DNL)



ENCODE = 125MHz
$f_{OUT}$ = 10MHz
SPAN = 62.5MHz
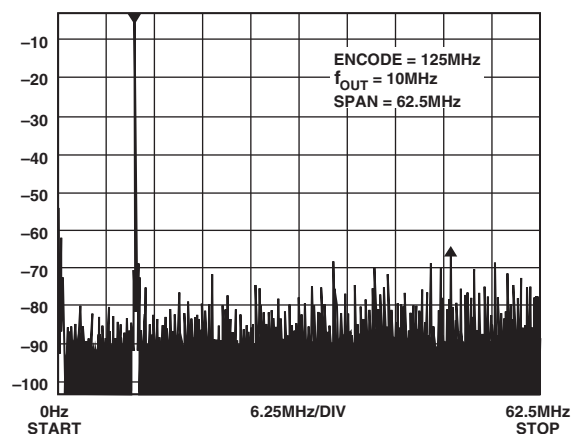
TPC 11. Wideband SFDR 10 MHz $f_{OUT}$; 125 MHz Clock



TPC 9. Typical Integral Nonlinearity Performance (INL)
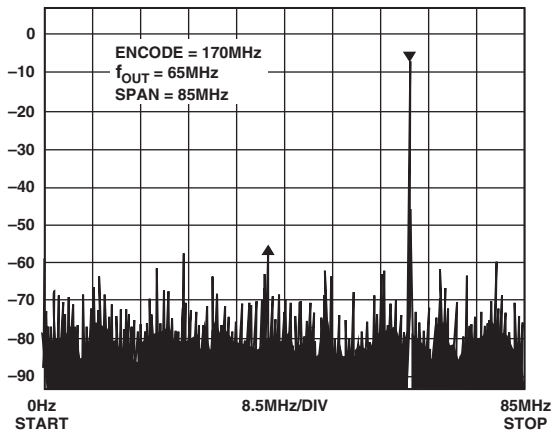


ENCODE = 125MHz
$f_{OUT}$ = 20MHz
SPAN = 62.5MHz
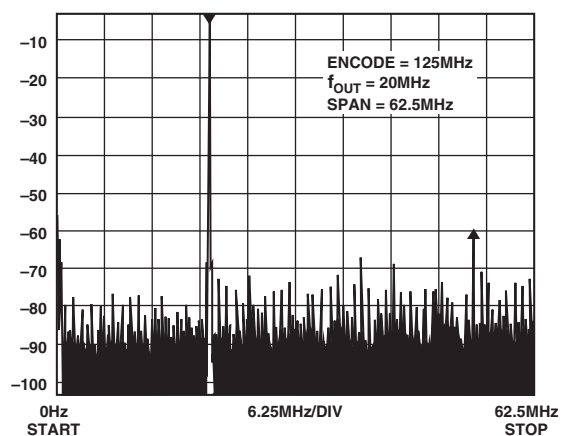
TPC 12. Wideband SFDR 20 MHz $f_{OUT}$; 125 MHz Clock

# AD9731
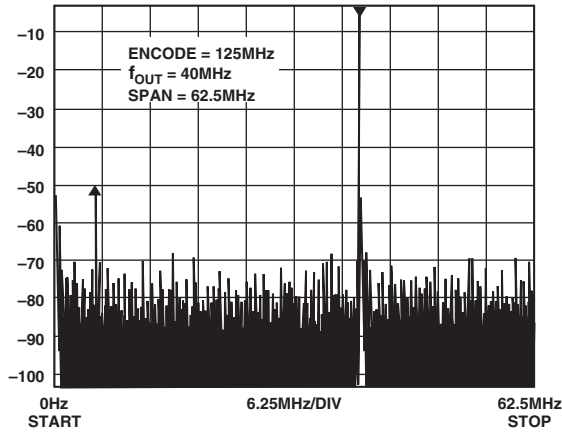


TPC 13. Wideband SFDR 40 MHz $f_{OUT}$; 125 MHz Clock



TPC 14. Wideband SFDR 65 MHz $f_{OUT}$; 170 MHz Clock
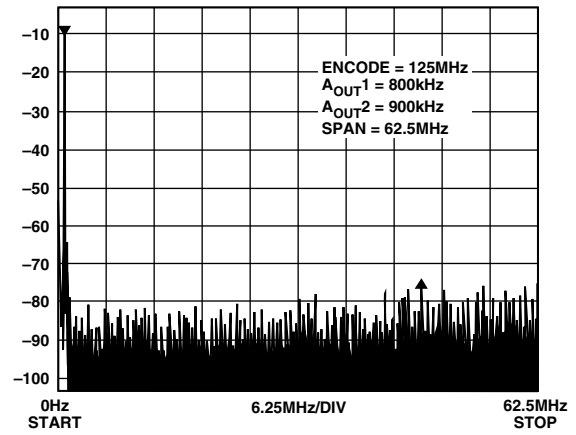


TPC 15. Wideband SFDR 70 MHz $f_{OUT}$; 170 MHz Clock
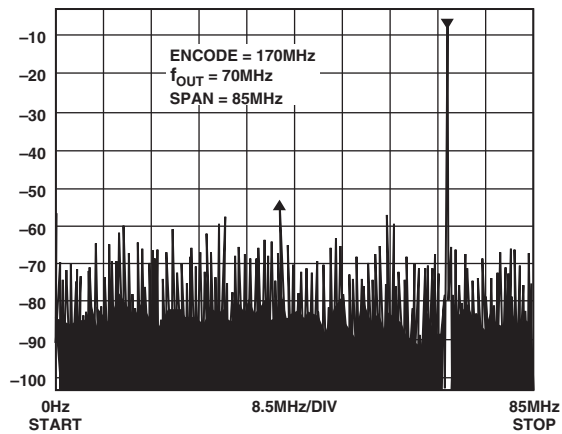


TPC 16. Wideband Intermodulation Distortion F1 = 800 kHz; F2 = 900 kHz; 125 MHz Clock; Span = 2 MHz



TPC 17. Wideband Intermodulation Distortion F1 = 800 kHz; F2 = 900 kHz; 125 MHz Clock; Span = 62.5 MHz

REV. B

**THEORY AND APPLICATIONS**
The AD9731 high speed digital-to-analog converter utilizes most significant bit decoding and segmentation techniques to reduce glitch impulse and deliver high dynamic performance on lower power consumption than previous bipolar DAC technologies.

The design is based on four main subsections: the decoder/driver circuits, the edge-triggered data register, the switch network, and the control amplifier. An internal band gap reference is included to allow operation of the device with minimum external support components.

**Digital Inputs/Timing**
The AD9731 has TTL/high speed CMOS-compatible single-ended inputs for data inputs and clock. The switching threshold is 1.5 V.

In the decoder/driver section, the three MSBs are decoded to seven "thermometer code" lines. An equalizing delay is included for the seven least significant bits and the clock signals. This delay minimizes data skew and data setup and hold times at the register inputs.

The on-board register is rising edge triggered and should be used to synchronize data to the current switches by applying a pulse with proper data setup and hold times as shown in the timing diagram. Although the AD9731 is designed to provide isolation of the digital inputs to the analog output, some coupling of digital transitions is inevitable. Digital feedthrough can be minimized by forming a low pass filter at the digital input by using a resistor in series with the capacitance of each digital input. This common high speed DAC application technique has the effect of isolating digital input noise from the analog output.

**Input Clock and Data Timing Relationship**
SINAD in a DAC is dependent on the relationship between the position of the clock edges and the point in time at which the input data changes. The AD9731 is rising edge triggered, and so exhibits SINAD sensitivity when the data transition is close to this edge. In general, the goal when applying the AD9731 is to make the data transition close to the falling clock edge. This becomes more important as the sample rate increases. Figure 2 shows the relationship of SINAD to clock placement from the AD9731 and a competitive part, both sampling at 125 MSPS. The AD9731 has excellent performance as far as the narrowness of the "window" in which it is sensitive to SINAD.
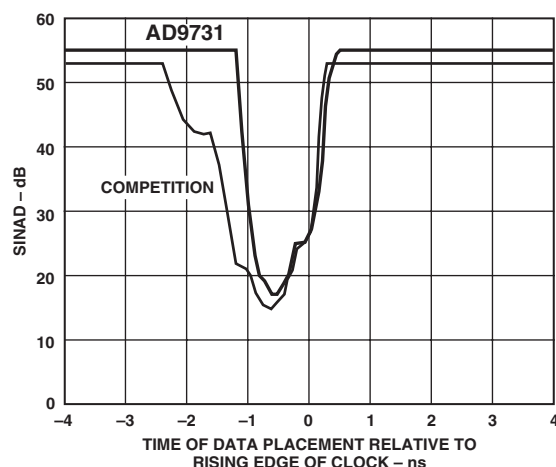


Figure 2.  SINAD vs. Clock Placement; $f_{CLK}$ = 125 MSPS, $f_{OUT}$ = 20 MHz

**References**
The internal band gap reference, control amplifier, and reference input are pinned out to provide maximum user flexibility in configuring the reference circuitry for the AD9731. When using the internal reference, REF OUT (Pin 25) should be connected to CONTROL AMP IN (Pin 26). CONTROL AMP OUT (Pin 24) should be connected to REF IN (Pin 23). A 0.1 μF ceramic capacitor connected from Pin 23 to Analog –$V_S$ (Pin 22) improves settling time by decoupling switching noise from the current sink baseline. A reference current cell provides feedback to the control amplifier by sinking current through $R_{SET}$ (Pin 17).

Full-scale current is determined by CONTROL AMP IN and $R_{SET}$ according to the following equation:

$$I_{OUT} \text{ (FS)} = 32(CONTROL\ AMP\ IN/R_{SET})$$

The internal reference is nominally –1.25 V with a tolerance of ±8% and typical drift over temperature of 100 ppm/°C. If greater accuracy or temperature stability is required, an external reference can be used. The AD589 reference features 10 ppm/°C drift over the 0°C to 70°C temperature range.

Two modes of multiplying operation are possible with the AD9731. Signals with bandwidths up to 2.5 MHz and input swings from –0.6 V to –1.2 V can be applied to the CONTROL AMP IN pin as shown in Figure 3. Because the control amplifier is internally compensated, the 0.1 μF capacitor discussed above can be reduced to maximize the multiplying bandwidth. However, it should be noted that output settling time, for changes in the digital word, will be degraded.
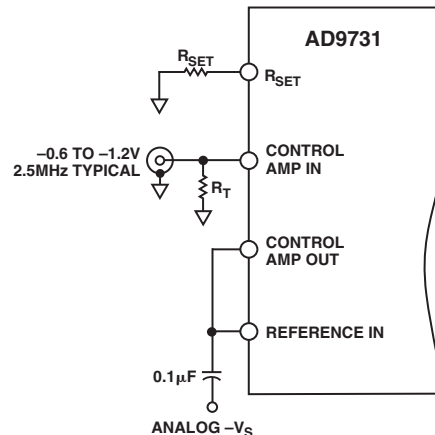


Figure 3.  Low Frequency Multiplying Circuit

# AD9731

The REFERENCE IN pin can also be driven directly for wider bandwidth multiplying operation. The analog signal for this mode of operation must have a signal swing in the range of –3.3 V to –4.25 V. This can be implemented by capacitively coupling into REFERENCE IN a signal with a dc bias of –3.3 V ($I_{OUT} \approx$ 22.5 mA) to –4.25 V ($I_{OUT} \approx$ 3 mA), as shown in Figure 4, or by dividing REFERENCE IN with a low impedance op amp whose signal swing is limited to the stated range.

NOTE: When using an external reference, the external reference voltage must be applied prior to applying $-V_S$.
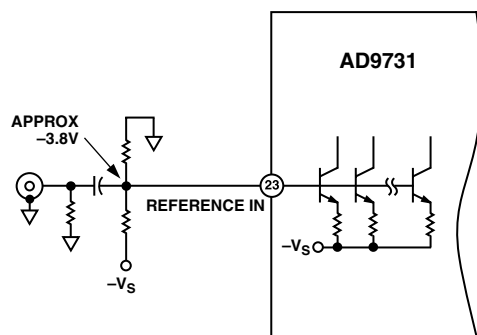


Figure 4.  Wideband Multiplying Circuit

**Analog Output**

The switch network provides complementary current outputs $I_{OUT}$ and $I_{OUTB}$. The design of the AD9731 is based on statistical current source matching, which provides a 10-bit linearity without trim. Current is steered to either $I_{OUT}$ or $I_{OUTB}$ in proportion to the digital input word. The sum of the two currents is always equal to the full-scale output current minus 1 LSB. The current can be converted to a voltage by resistive loading as shown in the block diagram. Both $I_{OUT}$ and $I_{OUTB}$ should be equally loaded for best overall performance. The voltage that is developed is the product of the output current and the value of the load resistor.

An operational amplifier can also be used to perform the I-to-V conversion of the DAC output. Figure 5 shows an example of a circuit that uses the AD9631, a high speed, current feedback amplifier. The resistor values in Figure 5 provide a 4.096 V swing, centered at ground, at the output of the AD9631 amplifier.
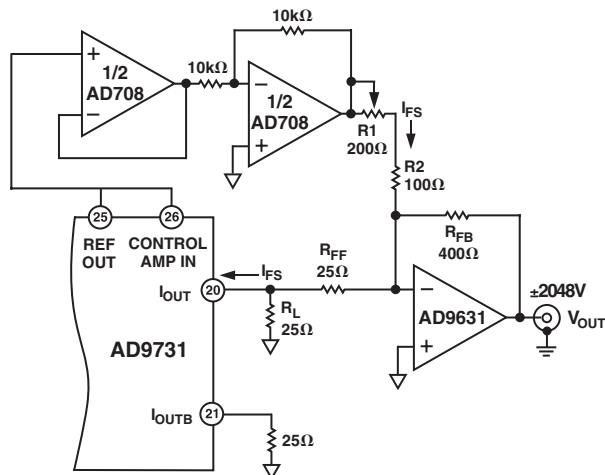


Figure 5.  I-to-V Conversion Using a Current Feedback Amplifier

**EVALUATION BOARD**

The performance characteristics of the AD9731 make it ideally suited for direct digital synthesis (DDS) and other waveform synthesis applications. The AD9731 evaluation board provides a platform for analyzing performance under optimum layout conditions. The AD9731 also provides a reference for high speed circuit board layout techniques.
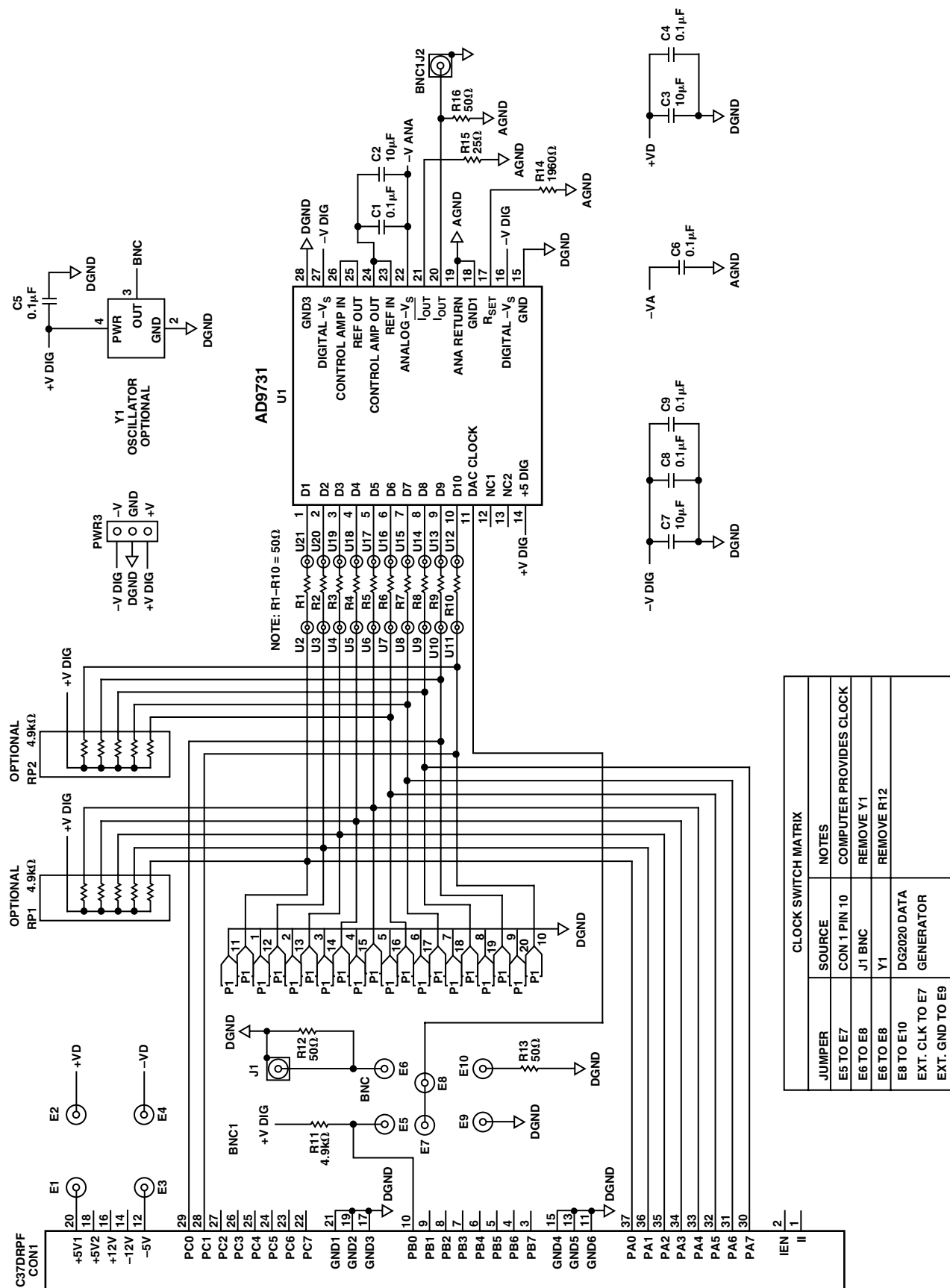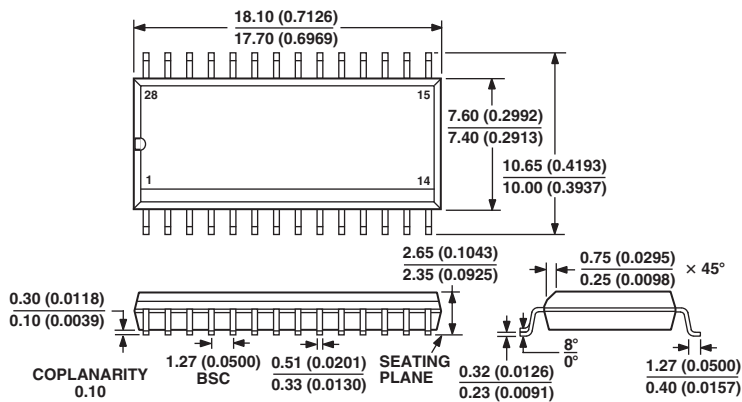
Figure 6. PCB Evaluation Board Schematic

# AD9731

## OUTLINE DIMENSIONS

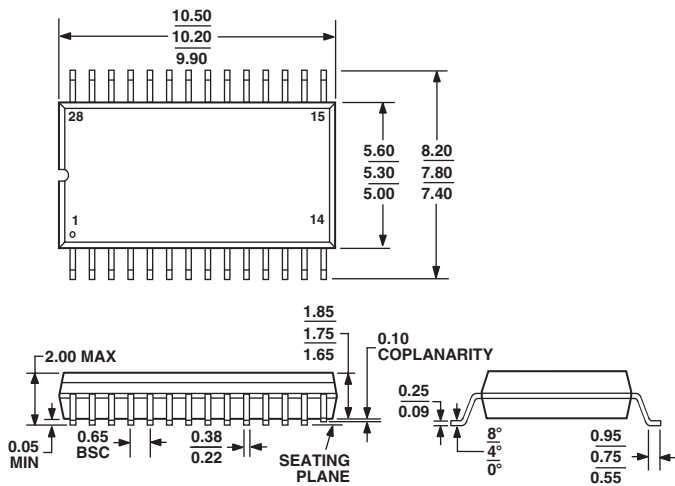### 28-Lead Standard Small Outline Package [SOIC]
### Wide Body
### (R-28)

Dimensions shown in millimeters and (inches)

18.10 (0.7126)
17.70 (0.6969)

28    15

7.60 (0.2992)
7.40 (0.2913)

10.65 (0.4193)
10.00 (0.3937)

1    14

2.65 (0.1043)
2.35 (0.0925)

0.75 (0.0295)
0.25 (0.0098)    × 45°

0.30 (0.0118)
0.10 (0.0039)

COPLANARITY
0.10

1.27 (0.0500)
BSC

0.51 (0.0201)
0.33 (0.0130)

SEATING
PLANE

0.32 (0.0126)
0.23 (0.0091)

8°
0°

1.27 (0.0500)
0.40 (0.0157)

**COMPLIANT TO JEDEC STANDARDS MS-013AE**
**CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS**
**(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR**
**REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN**

### 28-Lead Shrink Small Outline Package [SSOP]
### (RS-28)

Dimensions shown in millimeters

10.50
10.20
9.90

28    15

5.60
5.30
5.00

8.20
7.80
7.40

1    14

1.85
1.75
1.65

0.10
COPLANARITY

2.00 MAX

0.25
0.09

0.05
MIN

0.65
BSC

0.38
0.22

SEATING
PLANE

8°
4°
0°

0.95
0.75
0.55

**COMPLIANT TO JEDEC STANDARDS MO-150AH**

# Revision History