ANALOG DEVICES

12-Bit, 100 MSPS D/A Converters

AD9712/AD9713

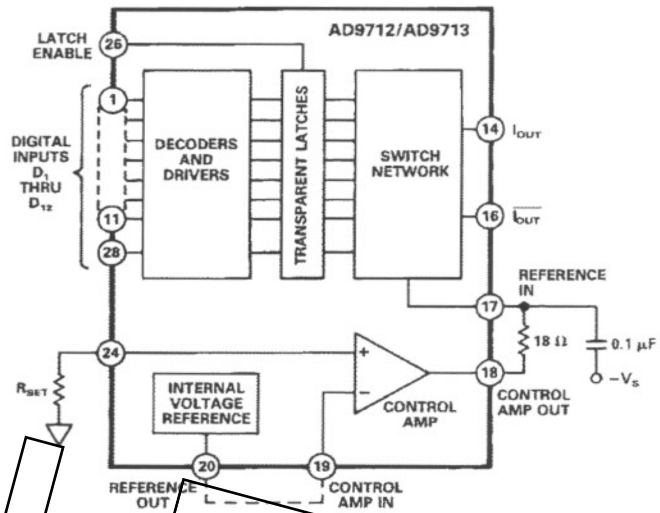
FEATURES

100 MSPS Update Rate
ECL/TTL Compatibility
Low Glitch Impulse: 100 pV–s
Fast Settling: 30 ns to ±1 LSB
Low Power: 700 mW

APPLICATIONS

ATE
Signal Reconstruction
Arbitrary Waveform Generators
Digital Synthesizers
Signal Generators

FUNCTIONAL BLOCK DIAGRAM

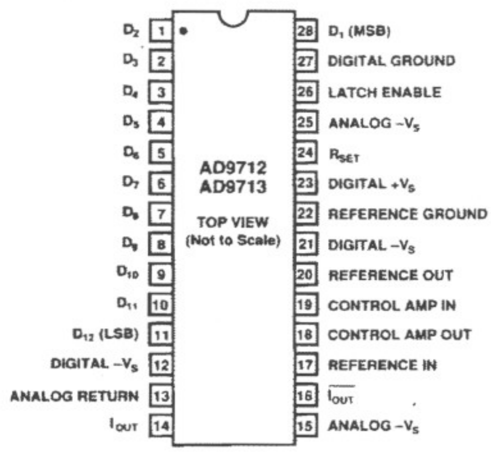


GENERAL DESCRIPTION

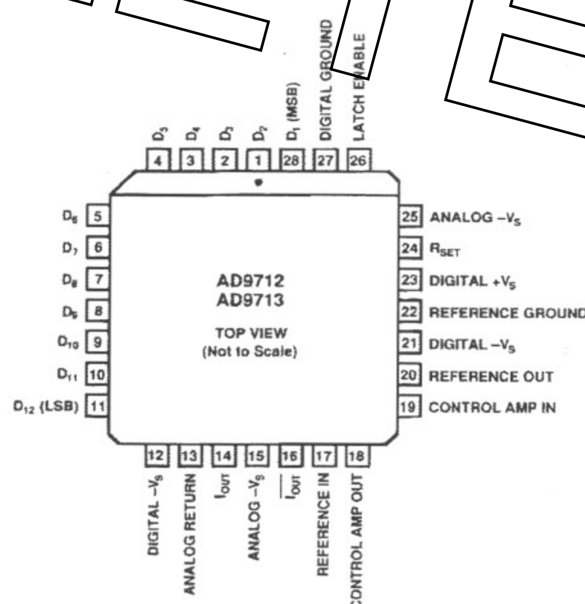
The AD9712 and AD9713 are 12-bit, high speed digital-to-analog converters constructed in an advanced oxide isolated bipolar process. The AD9712 is an ECL-compatible device featuring update rates of 100 MSPS minimum; the TTL-compatible AD9713 will update at 80 MSPS minimum.

Designed for direct digital synthesis, waveform reconstruction, and high resolution imaging applications, both devices feature low glitch impulse of 100 pV-s; and fast settling times of 30 ns to ±1 LSB. Both units are characterized for dynamic performance, and have excellent harmonic suppression.

The AD9712 and AD9713 are available in 28-pin plastic DIPs and PLCCs, with an operating temperature range of 0 to +70°C. Contact the factory for availability of military-grade devices.



Plastic DIP Pinout Designations (Top View)



PLCC Pinout Designations

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
West Coast 714/641-9391
Central 214/231-5094
Atlantic 215/643-7790

AD9712/AD9713—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) (AD9713 Only) . . . . +6 V
Negative Supply Voltage ($-V_S$)
 (AD9712 and AD9713) . . . . −7 V
DAC Outputs to ANALOG RETURN . . . . . . +0.5 V to −2 V
Digital Input Voltages (D_1–D_{12}, LATCH ENABLE)
 AD9712 . . . . 0 V to $-V_S$
 AD9713 . . . . 0 V to $+V_S$
Internal Reference Output Current . . . . . −20 µA to +500 µA
Control Amplifier Input Voltage Range . . . . 0 V to −4 V
Control Amplifier Output Current . . . . ±2.5 mA
REFERENCE IN Voltage Range . . . . −3.7 V to $-V_S$
Analog Output Current (I_{OUT} or $\overline{I_{OUT}}$) . . . . 30 mA
Operating Temperature Range
 AD9712JN/JP . . . . 0 to +70°C
 AD9713JN/JP . . . . 0 to +70°C
Maximum Junction Temperature[2] . . . . +150°C
Lead Temperature (Soldering, 10 seconds) . . . . +300°C
Storage Temperature Range . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS ($-V_S$ = −5.2 V; $+V_S$ = +5 V (AD9713 Only); CONTROL AMP IN = −1.2 V (external); R_{SET} = 7.5 kΩ, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9712JN/JP Min	Typ	Max	AD9713JN/JP Min	Typ	Max	Units
RESOLUTION			12			12			Bits
DC ACCURACY									
Differential Nonlinearity (J)	+25°C	I		1.2	2.0		1.2	2.0	LSB
	Full	VI			4.0			4.0	LSB
Integral Nonlinearity (J)	+25°C	I			3.0			3.0	LSB
("Best Fit" Straight Line)	Full	VI			4.0			4.0	LSB
INITIAL OFFSET ERROR									
Zero-Scale Offset Error	+25°C	I		0.5	1.5		0.5	1.5	µA
	Full	VI			5.0			5.0	µA
Full-Scale Gain Error[3]	+25°C	I		4.0	8.5		4.0	8.5	%
	Full	VI			11.0			11.0	%
Offset Drift Coefficient	+25°C	V		0.03			0.03		µA/°C
REFERENCE/CONTROL AMP									
Internal Reference Voltage	+25°C	I	−1.13	−1.26	−1.39	−1.13	−1.26	−1.39	V
	Full	I	−1.11		−1.41	−1.11		−1.41	V
Internal Reference Voltage Drift	Full	V		300			300		µV/°C
Amplifier Input Impedance	+25°C	V		50			50		kΩ
Amplifier Bandwidth	+25°C	V		300			300		kHz
REFERENCE INPUT[4]									
Reference Input Impedance	+25°C	V		3			3		kΩ
Reference Multiplying Bandwidth[5]	+25°C	V		40			40		MHz
OUTPUT PERFORMANCE									
Full-Scale Output Current[6]	+25°C	V		20.48			20.48		mA
Output Compliance Range	+25°C	IV	−1.2		+3	−1.2		+3	V
Output Resistance	+25°C	IV	2.0	2.5	3.0	2.0	2.5	3.0	kΩ
Output Capacitance	+25°C	V		30			30		pF
Output Update Rate[7]	+25°C	IV	100	110		80	90		MSPS
Output Settling Time (t_{ST})[8]									
Current Settling	+25°C	V		30			30		ns
Voltage Settling (R_L = 50 Ω)	+25°C	V		30			30		ns
Output Propagation Delay (t_{PD})[9]	+25°C	V		8			11		ns
Glitch Impulse[10]	+25°C	V		100			100		pV-s
Output Slew Rate[11]	+25°C	V		400			400		V/µs
Output Rise Time[11]	+25°C	V		3			3		ns
Output Fall Time[11]	+25°C	V		2			2		ns

Parameter (Conditions)	Temp	Test Level	AD9712JN/JP Min	Typ	Max	AD9713JN/JP Min	Typ	Max	Units
DIGITAL INPUTS									
Logic "1" Voltage	Full	VI	−1.0	−0.8		2.0			V
Logic "0" Voltage	Full	VI		−1.7	−1.5			0.8	V
Logic "1" Current	Full	VI			20			20	μA
Logic "0" Current	Full	VI			10			600	μA
Input Capacitance	+25°C	V		3			3		pF
Input Setup Time (t_S)[12]	+25°C	V		3			3		ns
Input Hold Time (t_H)[13]	+25°C	V		3			3		ns
Latch Pulse Width (t_{LPW}) (Transparent)	+25°C	V		2.5			4		ns
AC LINEARITY[14]									
Spurious-Free Dynamic Range	+25°C	V		−60			−55		dBc
POWER SUPPLY[15]									
Positive Supply Current (+5.0 V)	+25°C	I					10	20	mA
	Full	VI						23	mA
Negative Supply Current (−5.2 V)	+25°C	I		130	160		135	165	mA
	Full	VI			170			175	mA
Nominal Power Dissipation	+25°C	V		676			726		mW
Power Supply Rejection Ratio (PSRR)[16]	+25°C	I		50	350		50	350	μA/V

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: 28-pin plastic DIP θ_{JA} = 42°C/W; θ_{JC} = 7°C/W; 28-pin PLCC θ_{JA} = 48°C/W; θ_{JC} = 10°C/W.
[3]Measured as error of the ratio of full-scale current to current through R_{SET} (160 μA nominal); ratio is nominally 128.
[4]Full-scale variations among devices are more severe when driving REFERENCE IN directly.
[5]Frequency at which a 3 dB reduction in output of DAC is observed; R_L = 50 Ω; 50% modulation at midscale.
[6]Based on $I_{FS} = 128\ (V_{REF}/R_{SET})$ when using internal amplifier.
[7]Output settling to 0.1%.
[8]Measured at midscale transition, to ±0.024%.
[9]Measured from falling edge of LATCH ENABLE signal to 50% point of full-scale transition.
[10]Glitch impulse combines the absolute value of positive and negative transitions operating in latched mode.
[11]Measured with R_L = 50 Ω and DAC operating in latched mode.
[12]Data must remain stable prior to falling edge of LATCH ENABLE signal for specified time.
[13]Data must remain stable after rising edge of LATCH ENABLE signal for specified time.
[14]Update rate ≤50 MSPS; output frequency = 5 MHz.
[15]Supply voltages should remain stable within ±5% for normal operation.
[16]Measured at ±5% of $+V_S$ (AD9713 only) and $-V_S$ (AD9712 or AD9713) using external reference.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Level

- I – 100% production tested.
- II – 100% production tested at +25°C, and sample tested at specified temperatures.
- III – Sample tested only.
- IV – Parameter is guaranteed by design and characterization testing.
- V – Parameter is a typical value only.
- VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

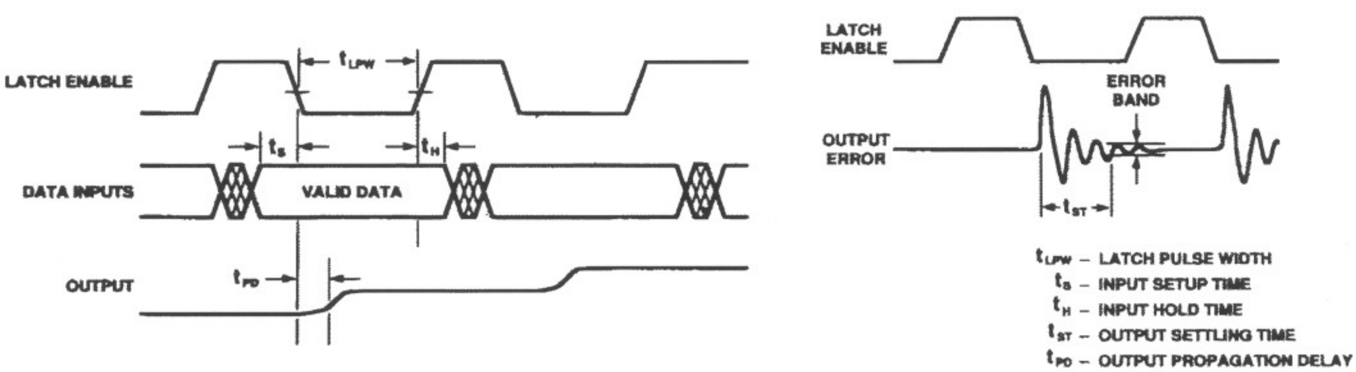
ORDERING GUIDE

Model	Description	Package Option*
AD9712JN	ECL-Compatible Plastic DIP	N-28
AD9712JP	ECL-Compatible PLCC	P-28A
AD9713JN	TTL-Compatible Plastic DIP	N-28
AD9713JP	TTL-Compatible PLCC	P-28A

*N = Plastic DIP; P = Plastic Leaded Chip Carrier.

AD9712/AD9713 PIN DESCRIPTIONS

Pin No.	Name	Function
1–10	D_2–D_{11}	Ten of twelve digital input bits.
11	D_{12} (LSB)	Least Significant Bit (LSB) of digital input word.
12	DIGITAL $-V_S$	One of two negative digital supply pins; nominally −5.2 V.
13	ANALOG RETURN	Analog ground return. This point and the reference side of the DAC load resistors should be connected to the same potential (nominally ground).
14	I_{OUT}	Analog current output; full-scale output occurs with digital inputs at all "1."
15	ANALOG $-V_S$	One of two negative analog supply pins; nominally −5.2 V.
16	$\overline{I_{OUT}}$	Complementary analog current output; zero scale output occurs with digital inputs at all "1."
17	REFERENCE IN	Normally connected to CONTROL AMP OUT (Pin 18). Direct line to DAC current switch network. Voltage changes at this point have a direct effect on the full-scale output. Full-scale current output = 128 (Reference voltage/R_{SET}) when using internal amplifier.
18	CONTROL AMP OUT	Normally connected to REFERENCE IN (Pin 17). Output of internal control amplifier, which provides a temperature compensated drive level to the current switch network.
19	CONTROL AMP IN	Normally connected to REFERENCE OUT (Pin 20) if not connected to external reference. Full-scale current out = 128 (Reference voltage/R_{SET}) when using internal amplifier.
20	REFERENCE OUT	Normally connected to CONTROL AMP IN (Pin 19). Internal voltage reference, nominally −1.26 V.
21	DIGITAL $-V_S$	One of two negative digital supply pins; nominally −5.2 V.
22	REFERENCE GROUND	Ground return for the internal voltage reference and amplifier.
23	DIGITAL $+V_S$	Positive digital supply pin; used only on the AD9713; nominally +5 V.
24	R_{SET}	Connection for external resistance reference. Full-scale current out = 128 (Reference voltage/R_{SET}) when using internal amplifier.
25	ANALOG $-V_S$	One of two negative analog supply pins; nominally −5.2 V.
26	LATCH ENABLE	Transparent latch control line.
27	DIGITAL GROUND	Digital ground return.
28	D_1 (MSB)	Most Significant Bit (MSB) of digital input word.



AD9712/AD9713 Timing Diagram

THEORY AND APPLICATIONS

The AD9712 and AD9713 high speed digital-to-analog converters utilize Most Significant Bit (MSB) decoding and segmentation techniques to reduce glitch impulse and maintain linearity without trimming.

As shown in the functional block diagram, the design is based on four main subsections: the Decoder/Driver circuits, the Transparent Latches, the Switch Network and the Control Amplifier. An internal band-gap reference is also included to allow operation with a minimum of external components.

Digital Inputs

The AD9712 employs single-ended ECL-compatible inputs for data inputs D_1–D_{12} and LATCH ENABLE. The internal ECL midpoint reference is designed to match 10K ECL device thresholds. On the AD9713, a TTL translator is added at each input; with this exception, the AD9712 and AD9713 are identical.

In the Decoder/Driver section, the four MSBs (D_1–D_4) are decoded to 15 "thermometer code" lines. An equalizing delay is included for the eight Least Significant Bits (LSBs) and LATCH ENABLE. This delay minimizes data skew, and data setup and hold times at the latch inputs; this is important when operating the latches in the transparent mode. Without the delay, skew caused by the decoding circuits would degrade glitch impulse.

The latches operate in their transparent mode when LATCH ENABLE (Pin 26) is at logic level "0." The latches can be used to synchronize data to the current switches by applying a narrow LATCH ENABLE pulse with proper data setup and hold times as shown in the timing diagram. With an external transparent latch at each data input clocked out of phase with the DAC, the AD9712/AD9713 operates in a master slave (edge-triggered) mode.

Although the AD9712/AD9713 chip is designed to provide isolation from digital inputs to the outputs, some coupling of digital transitions is inevitable, especially with TTL or CMOS inputs applied to the AD9713. Digital feedthrough can be reduced by forming a low-pass filter using a resistor in series with the capacitance of each digital input.

References

As shown in the functional block diagram, the internal band-gap reference, control amplifier and reference input are pinned out for maximum user flexibility when setting the reference.

When using the internal reference, REFERENCE OUT (Pin 20) should be connected to CONTROL AMP IN (Pin 19). CONTROL AMP OUT (Pin 18) should be connected to REFERENCE IN (Pin 17) through an 18 Ω resistor. A 0.1 µF ceramic capacitor from Pin 17 to $-V_S$ (Pin 15) improves settling by decoupling switching noise from the current sink base line. A reference current cell provides feedback to the control amp by sinking current through R_{SET} (Pin 24).

Full-scale output current is determined by the voltage at CONTROL AMP IN (V_{REF}) and R_{SET} according to the equation:

$$I_{OUT}\ (FS) = V_{REF}/R_{SET} \times 128.$$

The internal reference is nominally −1.26 V with a tolerance of ±10% and typical drift over temperature of 300 µV/°C. If greater accuracy or better temperature stability is required, an external reference can be utilized. The AD589 reference shown in Figure 1 features ±10 ppm/°C drift over temperatures from 0 to +70°C.

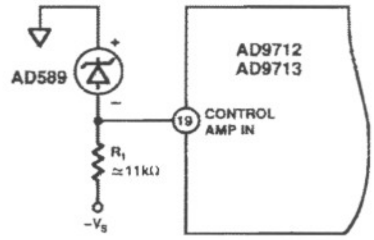


Figure 1. Use of AD589 as External Reference

Two modes of multiplying operation are possible with the AD9712/AD9713. Signals with bandwidths up to 400 kHz and input swings from −0.1 V to −1.2 V can be applied to the CONTROL AMP input as shown in Figure 2. Because the control amplifier is internally compensated, the 0.1 µF capacitor at Pin 17 can be eliminated to maximize the multiplying bandwidth. However, it should be noted that settling time for changes to the digital inputs will be degraded.

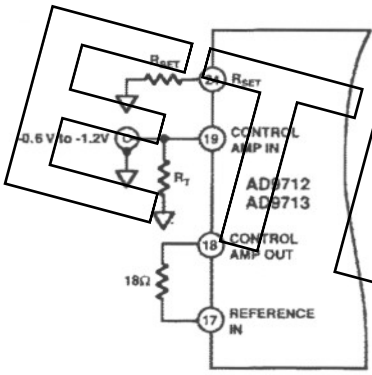


Figure 2. Low Frequency Multiplying Circuit

The REFERENCE IN pin can also be driven directly for wider bandwidth multiplying operation. The analog signal for this mode of operation must have a signal swing in the range of −4 V to −5.2 V. This can be implemented by capacitively coupling into REFERENCE IN an ac signal and establishing a dc bias of −4.0 V to −5.2 V, as shown in Figure 3; or by driving REFERENCE IN with a low impedance op amp whose signal swing is limited to the stated range.

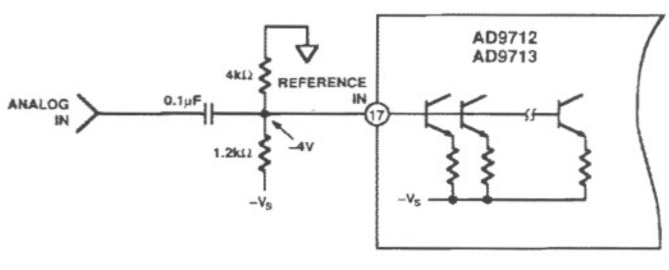


Figure 3. Wideband Multiplying Circuit

Outputs

The Switch Network controls complementary current outputs I_{OUT} and $\overline{I_{OUT}}$. As indicated earlier, D_1–D_4 are decoded into 15 "thermometer code" lines which drive matched current sources. D_5 and D_6 control weighted current sources; and D_7–D_{12} are applied to the R-2R network.

This segmentation reduces frequency domain errors due to glitch impulse. Current is steered to either I_{OUT} or $\overline{I_{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full-scale output current minus one LSB.

The current output can be converted to a voltage by resistive loading as shown in Figure 4. Both I_{OUT} and $\overline{I_{OUT}}$ should be loaded equally for best overall performance. The voltage which is developed is the product of the output current and the value of the load resistor.

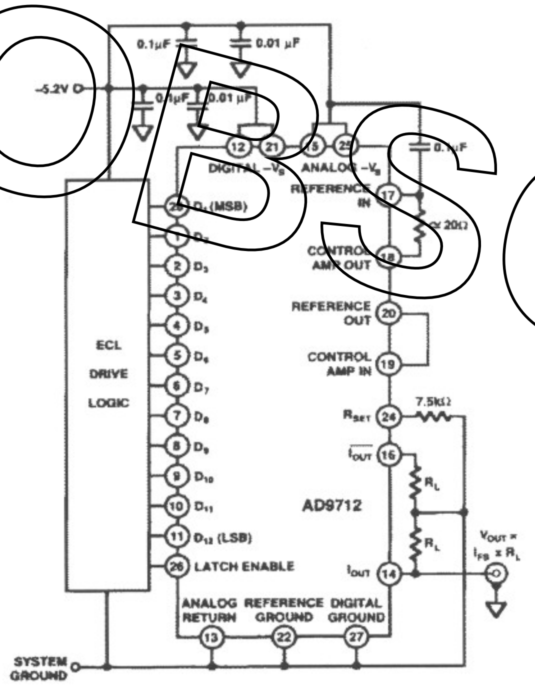


Figure 4. Typical Resistive Load Connection

When operating at the nominal full-scale current of 20.48 mA, the voltage swing will be from 0 to −1.024 V across 50 Ω resistors. Bipolar outputs are possible by sourcing a current equal to half the DAC full-scale current into the load resistor.

An alternate method of converting the current output to voltage is by driving the summing node of an operational amplifier directly with a feedback resistor selected according to the equation:

$$R_{FB} = V_{OUT}\,(FS)\,/\,I_{OUT}\,(FS)$$

A current feedback amplifier such as the AD9610 offers significantly faster settling and greater bandwidth than a conventional voltage feedback op amp. The feedback resistor for the AD9610 must be 1.5 kΩ or greater to maintain stability. This value for R_{FB}, along with the 20.48 mA full-scale output current, results in a full-scale output of 30 V, which exceeds the output range of the AD9610.

Full-scale output voltage can be reduced by either reducing the DAC's full-scale output current, or by using a current divider at the DAC output as shown in Figure 5. Reducing DAC full-scale output current degrades both linearity and settling time; therefore, the current divider method is preferable.

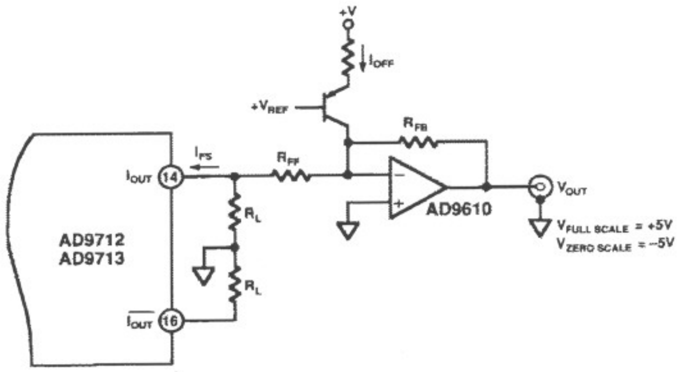


Figure 5. I/V Conversion Using Current Feedback Amp

The DAC output is not clamped at virtual ground in this configuration because of the series resistance R_{FF}. The value of R_{FF} is selected according to the equation:

$$R_{FF} = \frac{R_L I_{FS} - \left(\frac{V_{Full\ Scale}}{R_{FB}} + I_{OFF}\right) R_L}{\frac{V_{Full\ Scale}}{R_{FB}} + I_{OFF}}.$$

As an example, assume the following conditions:

$R_L = 50\ \Omega$

$R_{FB} = 1.5\ k\Omega$

$I_{FS} = 20.48\ mA$

$I_{OFF} = \frac{-V_{Zero\ Scale}}{R_{FB}} = 3.3\ mA$

Given these conditions, $R_{FF} = 103.6\ \Omega$

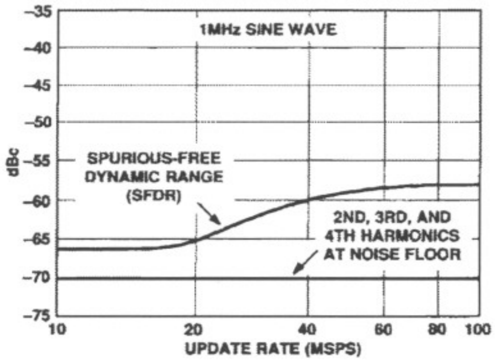
Power and Grounding

Maintaining low noise on power supplies and ground is critical for obtaining optimum results with the AD9712 or AD9713. DACs are most often used in circuits which are predominantly digital. To preserve 12-bit performance, especially at conversion speeds up to 100 MSPS, special precautions are necessary for power supplies and grounding.

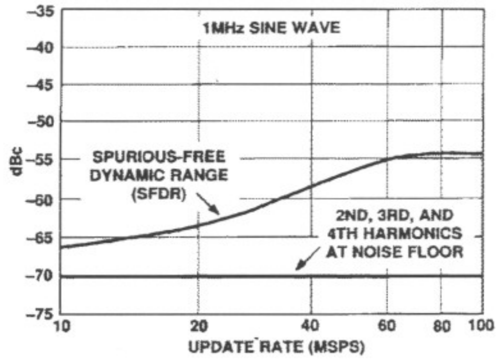
Ideally, the DAC should have a separate analog ground plane. All ground pins of the DAC, as well as reference and analog output components, should be tied directly to this analog ground plane. The DAC's ground plane should be connected to the system ground plane at a single point.

Ferrite beads, along with high frequency, low inductance decoupling capacitors, should be used for the supply connections to isolate digital switching currents from the DAC supply pins. Separate isolation networks for the digital and analog supply connections will further reduce supply noise coupling to the output.

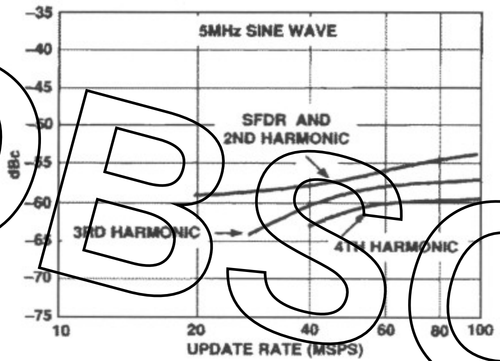
Molded socket assemblies should be avoided even when prototyping circuits with the AD9712 or AD9713. When the DAC cannot be directly soldered into the board, individual pin sockets such as AMP #6-330808-0 (knock-out end), or #60330808-3 (open end) should be used. These have much less effect on interlead capacitance than do molded assemblies.



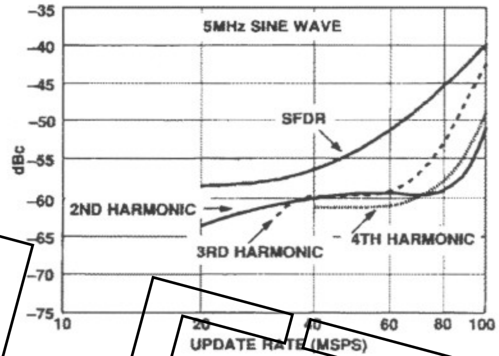
AD9712 Harmonic Distortion vs. Update Rate



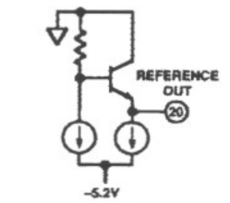
AD9713 Harmonic Distortion vs. Update Rate



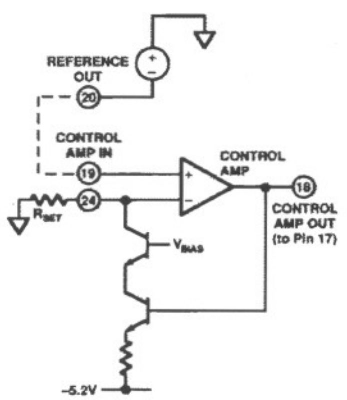
AD9712 Harmonic Distortion vs. Update Rate

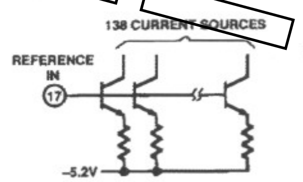


AD9713 Harmonic Distortion vs. Update Rate

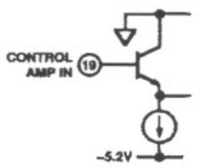


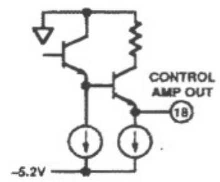
Reference Output

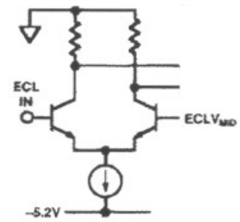




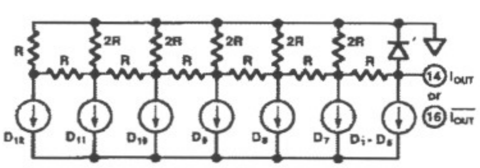
Reference Input



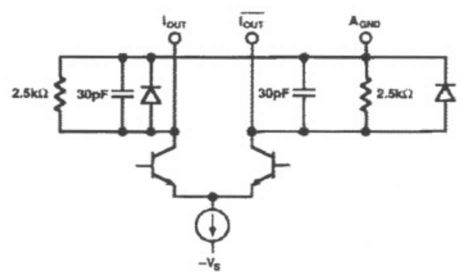


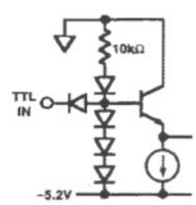


Control Amplifier Input *Full-Scale Current Control Loop* *Control Amplifier Output* *ECL Input Buffer*



R-2R DAC (for 6 LSBs)





TTL Input Buffer

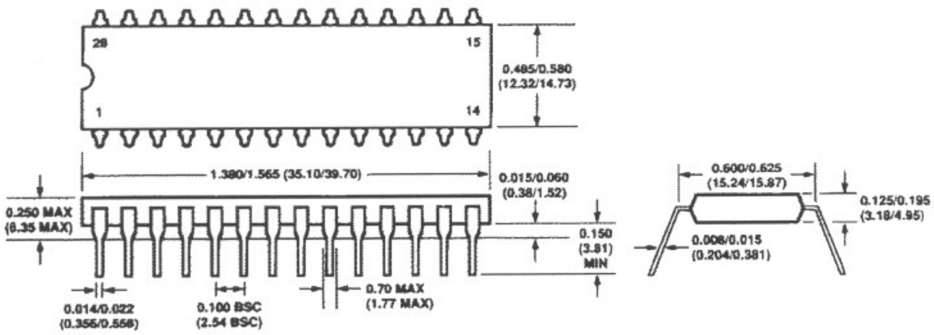
Output Circut

AD9712/AD9713 Equivalent Circuits

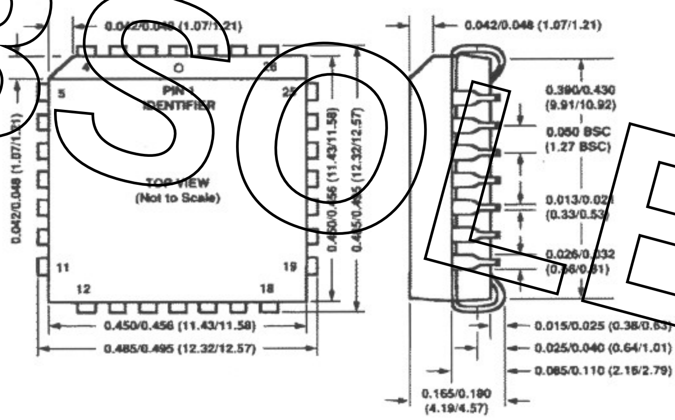
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

28-Pin Plastic DIP (Suffix N)



28-Pin Plastic Leaded Chip Carrier (Suffix P)



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