Audio/Video, 60 MHz, 16 × 8, Gain of +2 Crosspoint Switch

AD8112

FEATURES

- Low cost, 16 × 8, high speed, nonblocking switch array
  - Pin-compatible 16 × 16 version available (AD8113)
- Serial or parallel programming of switch array
- Serial data out allows daisy chaining control of multiple 16 × 8 arrays to create larger switch arrays
- Output disable allows connection of multiple devices without loading the output bus
- Complete solution
  - Buffered inputs
  - 8 output amplifiers
  - Operates on ±5 V or ±12 V supplies
  - Low supply current of 54 mA
- Excellent audio performance V_S = ±12 V
  - ±10 V output swing
  - 0.002% THD at 20 kHz maximum 20 V p-p (R_L = 600 Ω)
- Excellent video performance V_S = ±5 V
  - 0.1 dB gain flatness of 10 MHz
  - 0.1% differential gain error (R_L = 1 kΩ)
  - 0.1° differential phase error (R_L = 1 kΩ)
- Excellent ac performance
  - −3 dB bandwidth 60 MHz
- Low all-hostile crosstalk of −83 dB at 20 kHz
- Reset pin allows disabling of all outputs (connected to a capacitor to ground provides power-on reset capability)
- 100-lead LQFP (14 mm × 14 mm)

APPLICATIONS

- CCTV surveillance/DVR
- Analog/digital audio routers
- Video routers (NTSC, PAL, S-Video, SECAM)
- Multimedia systems
- Video conferencing

FUNCTIONAL BLOCK DIAGRAM

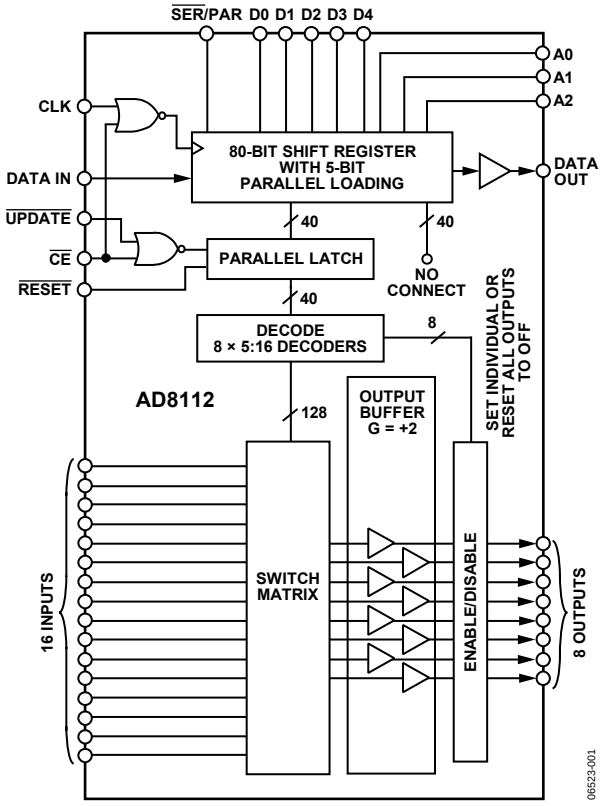

Figure 1.

GENERAL DESCRIPTION

The AD8112 is a low cost, fully buffered crosspoint switch matrix that operates on ±12 V for audio applications and ±5 V for video applications. It offers a −3 dB signal bandwidth greater than 60 MHz and channel switch times of less than 60 ns with 0.1% settling for use in both analog and digital audio. The AD8112 operated at 20 kHz has a crosstalk performance of −83 dB and isolation of 90 dB. In addition, ground/power pins surround all inputs and outputs to provide extra shielding for operation in the most demanding audio routing applications. With a differential gain and differential phase better than 0.1% and 0.1°, respectively, and a 0.1 dB flatness output of up to 10 MHz, the AD8112 is suitable for many video applications.

The AD8112 includes eight independent output buffers that can be placed into a disabled state for paralleling crosspoint outputs so that off channel loading is minimized. The AD8112 has a gain of +2. It operates on voltage supplies of ±5 V or ±12 V while consuming only 34 mA or 31 mA of current, respectively. The channel switching is performed via a serial digital control (which can accommodate the daisy chaining of several devices) or via a parallel control, allowing updating of an individual output without reprogramming the entire array.

The AD8112 is packaged in a 100-lead LQFP and is available over the commercial temperature range of 0°C to 70°C.

Rev. 0

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REVISION HISTORY

2/07—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = ±12 V, R_L = 600 Ω, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 200 mV p-p, R_L = 600 Ω, V_S = ±12 V	46	60		MHz
	V_{OUT} = 200 mV p-p, R_L = 150 Ω, V_S = ±5 V	41	60		MHz
	V_{OUT} = 8 V p-p, R_L = 600 Ω, V_S = ±12 V		10		MHz
	V_{OUT} = 2 V p-p, R_L = 150 Ω, V_S = ±5 V		25		MHz
Gain Flatness	0.1 dB, V_{OUT} = 200 mV p-p, R_L = 150 Ω, V_S = ±5 V		10		MHz
Propagation Delay	V_{OUT} = 2 V p-p, R_L = 150 Ω		20		ns
Settling Time	0.1%, 2 V Step, R_L = 150 Ω, V_S = ±5 V		23		ns
Slew Rate	2 V step, R_L = 150 Ω, V_S = ±5 V		100		V/µs
	20 V step, R_L = 600 Ω, V_S = ±12 V		120		V/µs
NOISE/DISTORTION PERFORMANCE					
Differential Gain Error	NTSC, R_L = 1 kΩ, V_S = ±5 V		0.1		%
Differential Phase Error	NTSC, R_L = 1 kΩ, V_S = ±5 V		0.1		Degrees
Total Harmonic Distortion	20 kHz, R_L = 600 Ω, 20 V p-p		0.002		%
Crosstalk, All Hostile	f = 5 MHz, R_L = 150 Ω, V_S = ±5 V		−67		dB
	f = 20 kHz		−83		dB
Off Isolation	f = 5 MHz, R_L = 150 Ω, V_S = ±5 V, one channel		−100		dB
	f = 20 kHz, one channel		−83		dB
Input Voltage Noise	20 kHz		14		nV/√Hz
	0.1 MHz to 10 MHz		12		nV/√Hz
DC PERFORMANCE					
Gain Error	No load, V_S = ±12 V, V_{OUT} = ±8 V		0.3	2.5	%
	R_L = 600 Ω, V_S = ±12 V		0.5		%
	R_L = 150 Ω, V_S = ±5 V		0.5		%
Gain Matching	No load, channel-to-channel		0.7	3.5	%
	R_L = 600 Ω, channel-to-channel		0.7		%
	R_L = 150 Ω, channel-to-channel		0.7		%
Gain Temperature Coefficient			20		ppm/°C
OUTPUT CHARACTERISTICS					
Output Resistance	Enabled		0.3		Ω
	Disabled	3.4	4		kΩ
Output Capacitance	Disabled		5		pF
Output Voltage Swing	V_S = ±5 V, no load	±3.2	±3.5		V
	V_S = ±12 V, no load	±10.3	±10.5		V
	I_{OUT} = 20 mA, V_S = ±5 V	±2.7	±3		V
	I_{OUT} = 20 mA, V_S = ±12 V	±9.8	±10		V
Short-Circuit Current	R_L = 0 Ω		55		mA
INPUT CHARACTERISTICS					
Input Offset Voltage	All configurations		±4.5	±8.5	mV
	Temperature coefficient		10		µV/°C
Input Voltage Range	No load, V_S = ±5 V		±1.5		V
	V_S = ±12 V		±5.0		V
Input Capacitance	Any switch configuration		4		pF
Input Resistance			50		MΩ
Input Bias Current	Any number of enabled inputs	+1	±1.6		µA

Parameter	Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS					
Enable On Time			80		ns
Switching Time, 2 V Step	50% update to 1% settling		50		ns
Switching Transient (Glitch)			20		mV p-p
POWER SUPPLIES					
Supply Current	AV_{CC} outputs enabled, no load, V_S = ±12 V		50	54	mA
	AV_{CC} outputs disabled, V_S = ±12 V		34	38	mA
	AV_{CC} outputs enabled, no load, V_S = ±5 V		45	50	mA
	AV_{CC} outputs disabled, V_S = ±5 V		31	35	mA
	AV_{EE} outputs enabled, no load, V_S = ±12 V		50	54	mA
	AV_{EE} outputs disabled, V_S = ±12 V		34	38	mA
	AV_{EE} outputs enabled, no load, V_S = ±5 V		45	50	mA
	AV_{EE} outputs disabled, V_S = ±5 V		31	35	mA
	DV_{CC} outputs enabled, no load		8	13	mA
DYNAMIC PERFORMANCE					
Supply Voltage Range	AV_{CC}	4.5		12.6	V
	AV_{EE}	−12.6		−4.5	V
	DV_{CC}	4.5		5.5	V
PSRR	DC	75	80		dB
	f = 100 kHz		60		dB
	f = 1 MHz		40		dB
OPERATING TEMPERATURE RANGE					
Temperature Range	Operating (still air)		0 to 70		°C
θ_{JA}	Operating (still air)		40		°C/W

TIMING CHARACTERISTICS (SERIAL)

Table 2.

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Serial Data Setup Time	t_1	20			ns
CLK Pulse Width	t_2	100			ns
Serial Data Hold Time	t_3	20			ns
CLK Pulse Separation, Serial Mode	t_4	100			ns
CLK to $\overline{\text{UPDATE}}$ Delay	t_5	0			ns
$\overline{\text{UPDATE}}$ Pulse Width	t_6	50			ns
CLK to DATA OUT Valid, Serial Mode	t_7			200	ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off				50	ns
Data Load Time, CLK = 5 MHz, Serial Mode			16		µs
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times				100	ns
$\overline{\text{RESET}}$ Time				200	ns

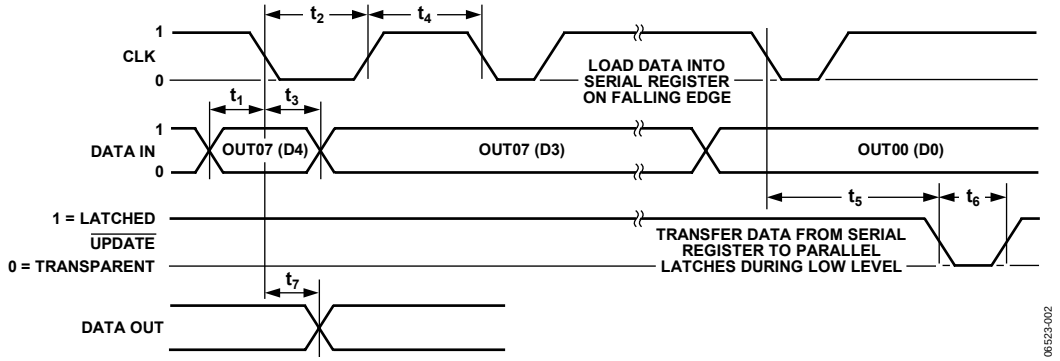


Figure 2. Timing Diagram, Serial Mode

Table 3. Logic Levels

Pins	V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR, CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	2.0 V min	0.8 V max			20 µA max	−400 µA min		
DATA OUT			2.7 V min	0.5 V max			−400 µA max	3.0 mA min

TIMING CHARACTERISTICS (PARALLEL)

Table 4.

Parameter	Symbol	Limit Min	Limit Max	Unit
Data Setup Time	t_1	20		ns
CLK Pulse Width	t_2	100		ns
Data Hold Time	t_3	20		ns
CLK Pulse Separation	t_4	100		ns
CLK to $\overline{\text{UPDATE}}$ Delay	t_5	0		ns
$\overline{\text{UPDATE}}$ Pulse Width	t_6	50		ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off			50	ns
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times			100	ns
$\overline{\text{RESET}}$ Time			200	ns

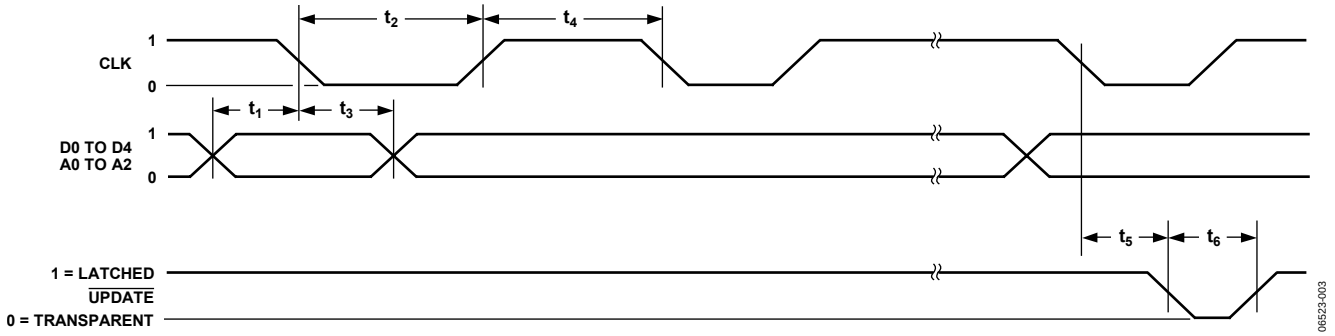


Figure 3. Timing Diagram, Parallel Mode

Table 5. Logic Levels

Pins	V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR, CLK, D0, D1, D2, D3, D4, A0, A1, A2, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	2.0 V min	0.8 V max			20 µA max	−400 µA min		
DATA OUT			2.7 V min	0.5 V max			−400 µA max	3.0 mA min

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Supply Voltage (AV_{CC} to AV_{EE})	26.0 V
Digital Supply Voltage (DV_{CC} to DGND)	6 V
Ground Potential Difference (AGND to DGND)	±0.5 V
Internal Power Dissipation[1]	3.1 W
Analog Input Voltage[2]	Maintain linear output
Digital Input Voltage	DV_{CC}
Output Voltage (Disabled Output)	(AV_{CC} − 1.5 V) to (AV_{EE} + 1.5 V)
Output Short-Circuit Duration	Momentary
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering 10 sec)	300°C

[1] Specification is for device in free air (T_A = 25°C): 100-lead plastic LQFP (ST): θ_{JA} = 40°C/W.
[2] To avoid differential input breakdown, ensure that one-half the output voltage (1/2 V_{OUT}) and any input voltage is less than 10 V of the potential differential. See Output Voltage Swing specification for linear output range.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

POWER DISSIPATION

The AD8112 is operated with ±5 V to ±12 V supplies and can drive loads down to 150 Ω (±5 V) or 600 Ω (±12 V), resulting in a large range of possible power dissipations. For this reason, extra care must be taken when derating the operating conditions based on ambient temperature.

Packaged in a 100-lead LQFP, the AD8112 junction-to-ambient thermal impedance (θ_{JA}) is 40°C/W. For long-term reliability, the maximum allowed junction temperature of the plastic encapsulated die should not exceed 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. The curve in Figure 4 shows the range of allowed power dissipations that meet these conditions over the commercial range of ambient temperatures.

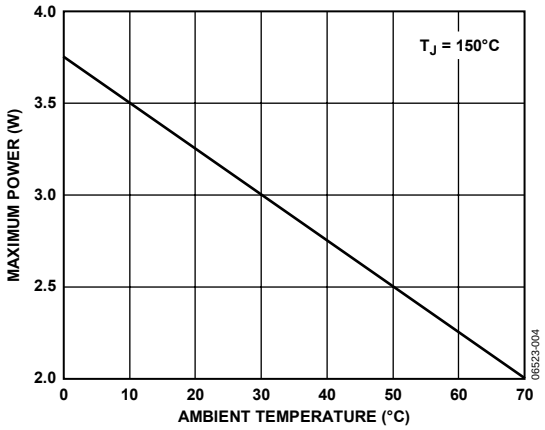


Figure 4. Maximum Power Dissipation vs. Ambient Temperature

Table 7. Operation Truth Table

$\overline{CE}$	$\overline{UPDATE}$	CLK	DATA IN	DATA OUT	$\overline{RESET}$	$\overline{SER}$/PAR	Operation/Comment
1	X	X	X	X	X	X	No change in logic.
0	1	↓	Data $_i$	Data $_{i-80}$	1	0	The data on the serial DATA IN line is loaded into serial register. The first bit clocked into the serial register appears at DATA OUT 80 clocks later.
0	1	↓	D0 ... D4, A0 ... A2	N/A in Parallel Mode	1	1	The data on the parallel data lines, D0 to D4, is loaded into the 80-bit serial shift register location addressed by A0 to A2.
0	0	X	X	X	1	X	Data in the 80-bit shift register transfers into the parallel latches that control the switch array. Latches are transparent.
X	X	X	X	X	0	X	Asynchronous operation. All outputs are disabled. Remainder of logic is unchanged.

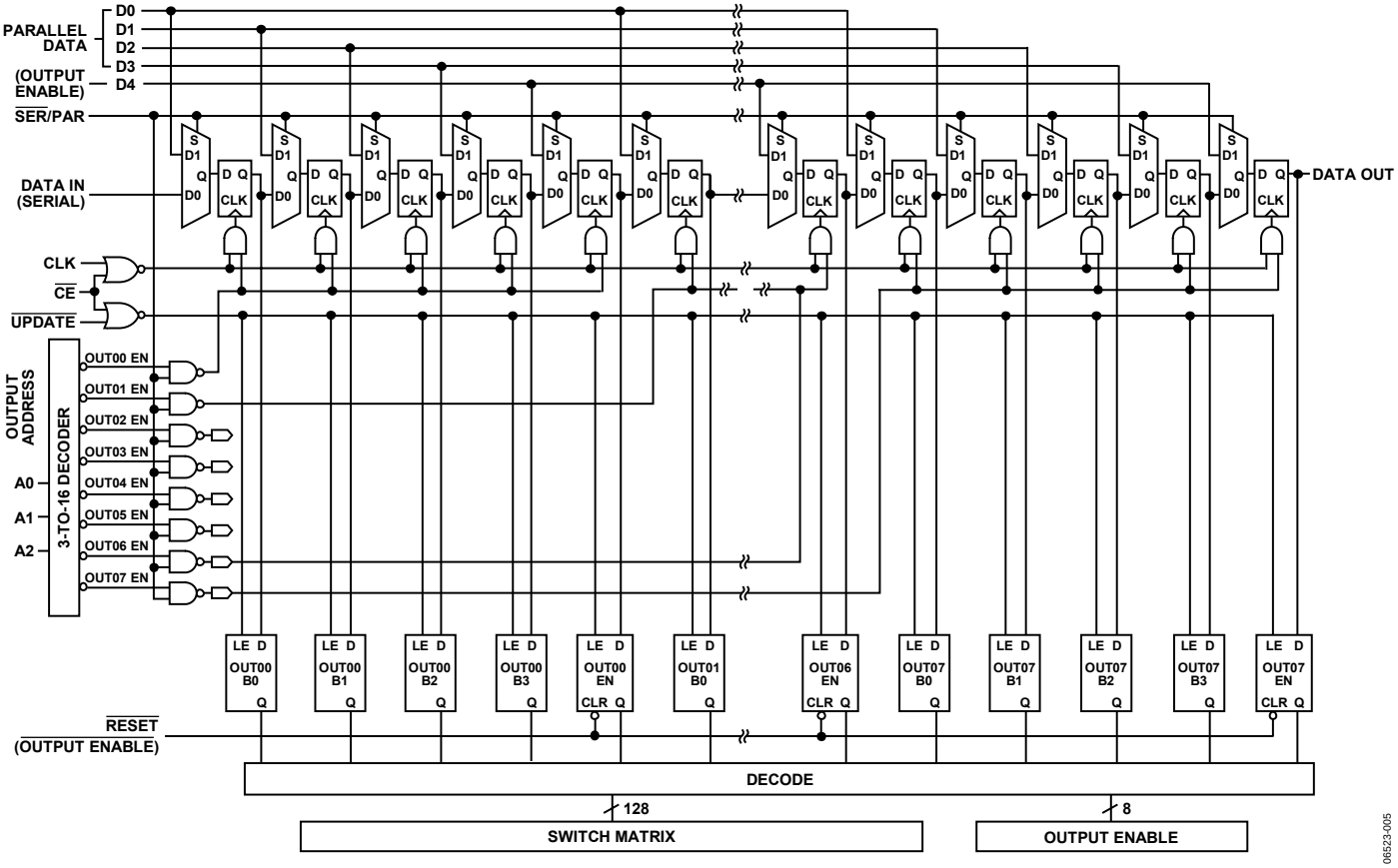


Figure 5. Logic Diagram

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

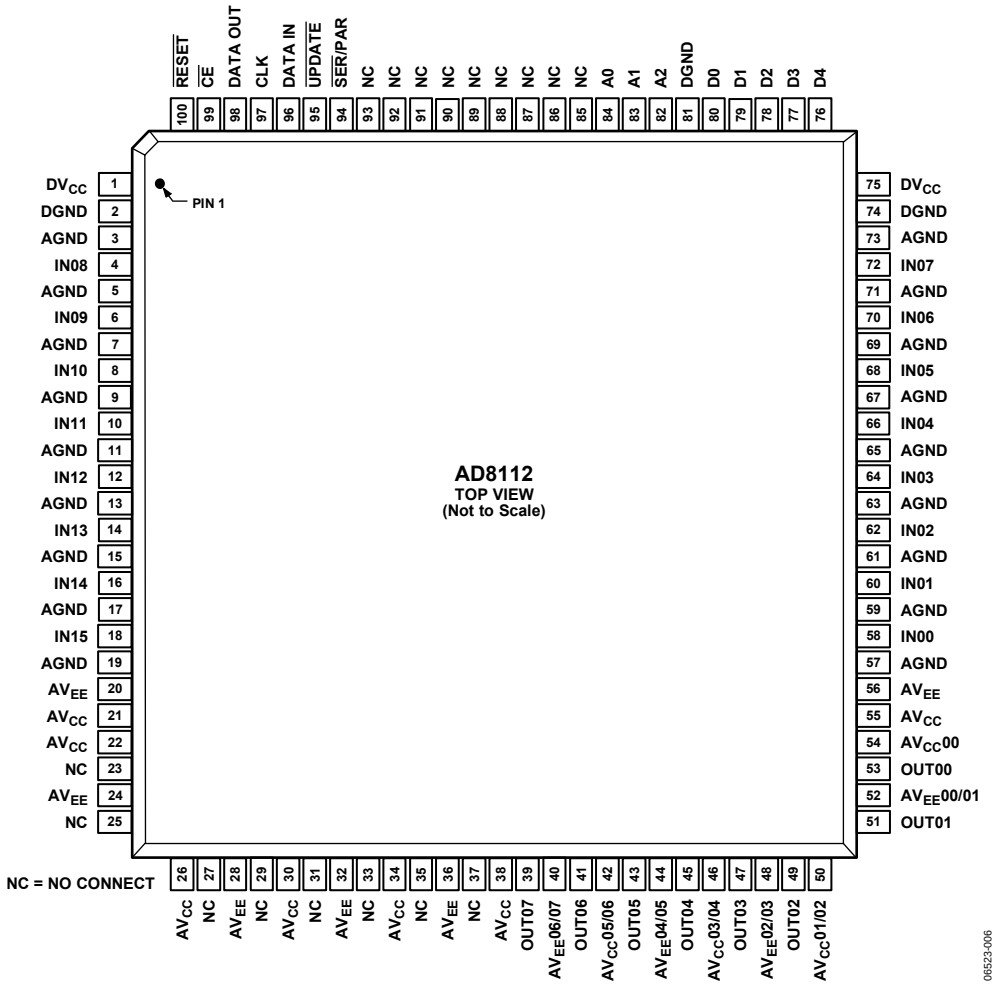


Figure 6. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
58, 60, 62, 64, 66, 68, 70, 72, 4, 6, 8, 10, 12, 14, 16, 18	IN00 to IN15[1]	Analog Inputs for Channel Numbers 00 through 15.
96	DATA IN	Serial Data Input, TTL-compatible.
97	CLK	Clock, TTL-compatible. Falling edge triggered.
98	DATA OUT	Serial Data Output, TTL-compatible.
95	$\overline{\text{UPDATE}}$	Enable (Transparent) Low. Allows serial register to connect directly to switch matrix. Data latched when high.
100	$\overline{\text{RESET}}$	Disable Outputs, Active Low.
99	$\overline{\text{CE}}$	Chip Enable, Enable Low. Must be low to clock in and latch data.
94	$\overline{\text{SER}}$/PAR	Serial Data/Parallel Data. When low, this pin selects serial data mode; when high, this pin selects parallel data mode, high. Must be connected.
53, 51, 49, 47, 45, 43, 41, 39	OUT00 to OUT07[1]	Analog Outputs for Channel Numbers 00 Through 07.
3, 5, 7, 9, 11, 13, 15, 17, 19, 57, 59, 61, 63, 65, 67, 69, 71, 73	AGND	Analog Ground for Inputs and Switch Matrix. Must be connected.
1, 75	DV_{CC}	5 V for Digital Circuitry.
2, 74, 81	DGND	Ground for Digital Circuitry.
20, 24, 28, 32, 36, 56	AV_{EE}	−5 V for Inputs and Switch Matrix.

Pin No.	Mnemonic	Description
21, 22, 26, 30, 34, 38, 55	AV_{CC}	5 V for Inputs and Switch Matrix.
54	AV_{CC}xx	5 V for Output Amplifier. This pin is shared by Channel Numbers xx and yy. Must be connected.
50, 46, 42	AV_{CC}xx/yy[1]	5 V for Output Amplifier. This pin is shared by Channel Numbers xx and yy. Must be connected.
52, 48, 44, 40	AV_{EE}xx/yy[1]	−5 V for Output Amplifier. This pin is shared by Channel Numbers xx and yy. Must be connected.
84	A0	Parallel Data Input, TTL-compatible (Output Select LSB).
83	A1	Parallel Data Input, TTL-compatible (Output Select).
82	A2	Parallel Data Input, TTL-compatible (Output Select).
80	D0	Parallel Data Input, TTL-compatible (Input Select LSB).
79	D1	Parallel Data Input, TTL-compatible (Input Select).
78	D2	Parallel Data Input, TTL-compatible (Input Select).
77	D3	Parallel Data Input, TTL-compatible (Input Select MSB).
76	D4	Parallel Data Input, TTL-compatible (Output Enable).
23, 25, 27, 29, 31, 33, 35, 37, 85 to 93	NC	No Connect.

[1] xx = Chanel numbers 00 through 15 for analog inputs; yy = channel numbers 00 through 07 for analog outputs.

I/O SCHEMATICS

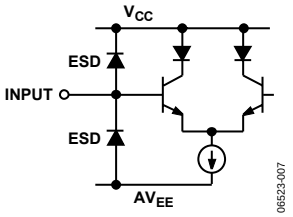


Figure 7. Analog Input

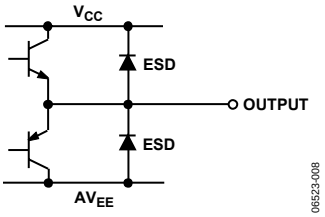


Figure 8. Analog Output

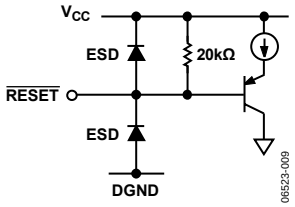


Figure 9. Reset Input

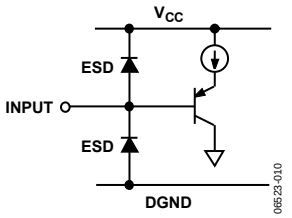


Figure 10. Logic Input

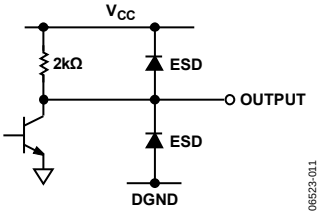


Figure 11. Logic Output

TYPICAL PERFORMANCE CHARACTERISTICS

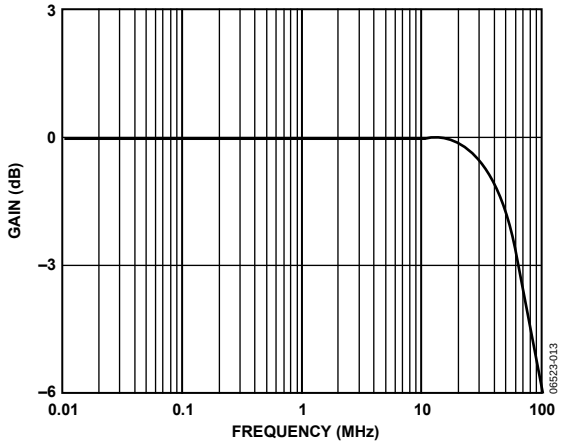


Figure 12. Small-Signal Bandwidth, $V_S = \pm 5$ V, $R_L = 150\ \Omega$, $V_{OUT} = 200$ mV p-p

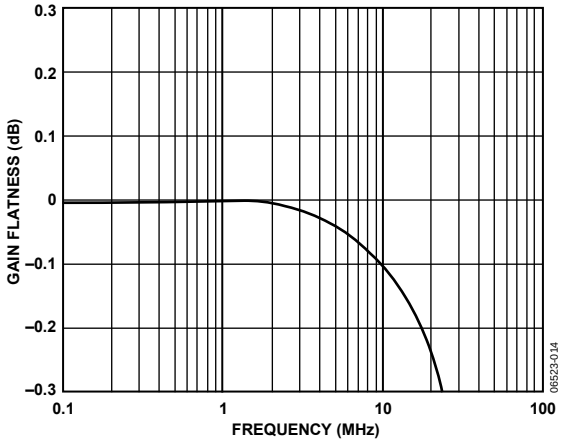


Figure 13. Small-Signal Gain Flatness, $V_S = \pm 5$ V, $R_L = 150\ \Omega$, $V_{OUT} = 200$ mV p-p

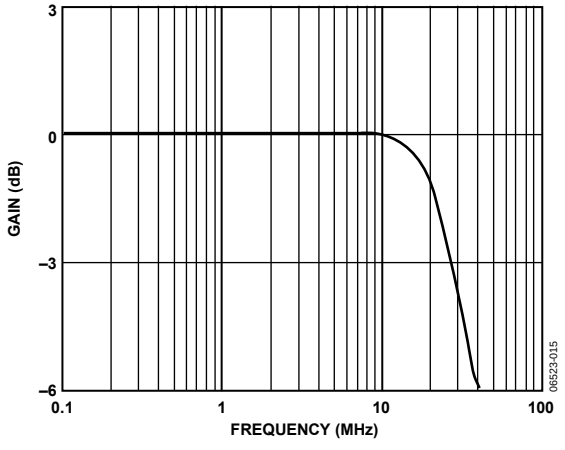


Figure 14. Large-Signal Bandwidth, $V_S = \pm 5$ V, $R_L = 150\ \Omega$, $V_{OUT} = 2$ V p-p

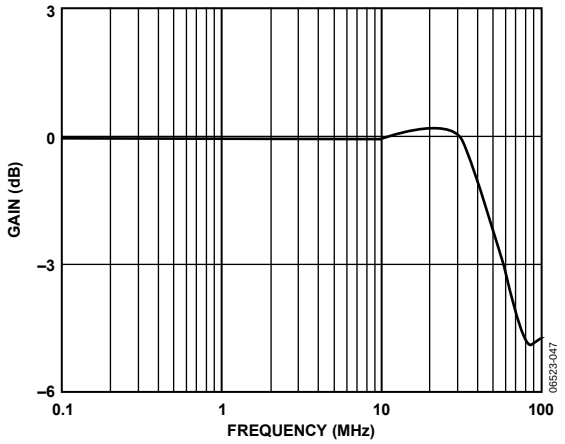


Figure 15. Small-Signal Bandwidth, $V_S = \pm 12$ V, $R_L = 600\ \Omega$, $V_{OUT} = 200$ mV p-p

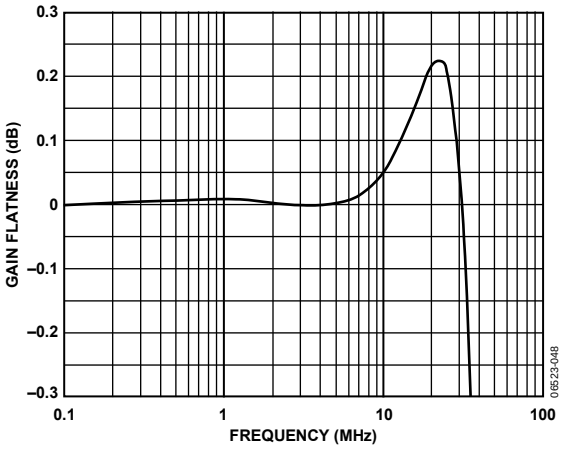


Figure 16. Small-Signal Gain Flatness, $V_S = \pm 12$ V, $R_L = 600\ \Omega$, $V_{OUT} = 200$ mV p-p

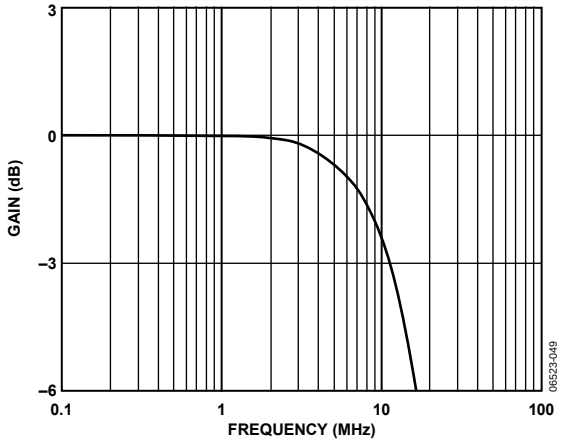


Figure 17. Large-Signal Bandwidth, $V_S = \pm 12$ V, $R_L = 600\ \Omega$, $V_{OUT} = 8$ V p-p

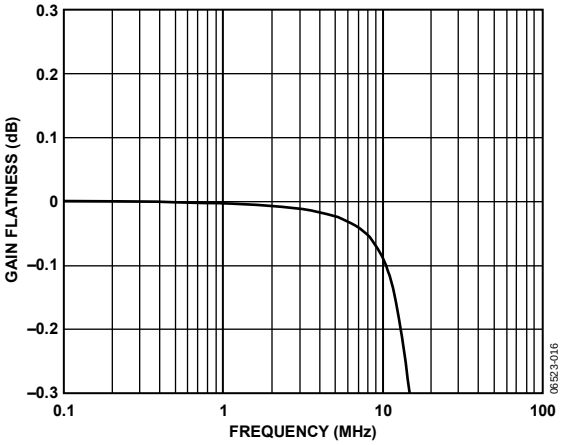


Figure 18. Large-Signal Gain Flatness, $V_S = \pm 5$ V, $R_L = 150\ \Omega$, $V_{OUT} = 2$ V p-p

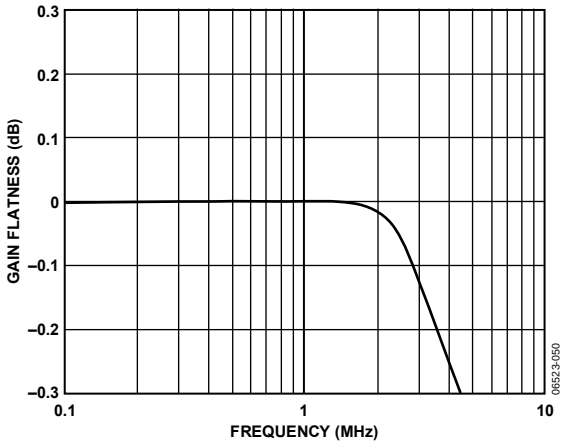


Figure 21. Large-Signal Gain Flatness, $V_S = \pm 12$ V, $R_L = 600\ \Omega$, $V_{OUT} = 8$ V p-p

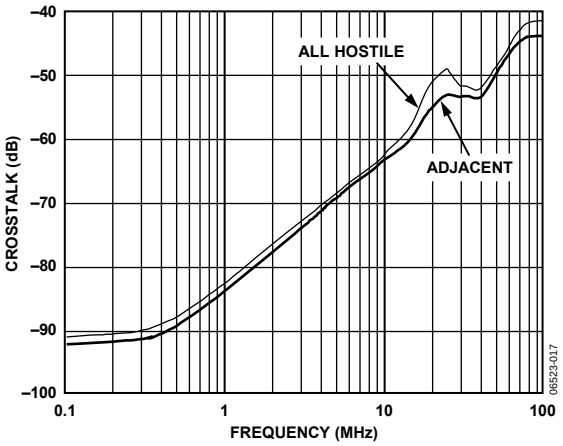


Figure 19. Crosstalk vs. Frequency, $V_S = \pm 5$ V, $R_L = 150\ \Omega$, $V_{OUT} = 2$ V p-p

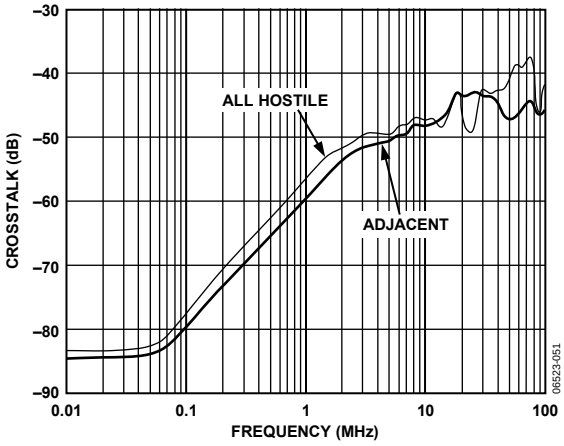


Figure 22. Crosstalk vs. Frequency, $V_S = \pm 12$ V, $R_L = 600\ \Omega$, $V_{OUT} = 20$ V p-p

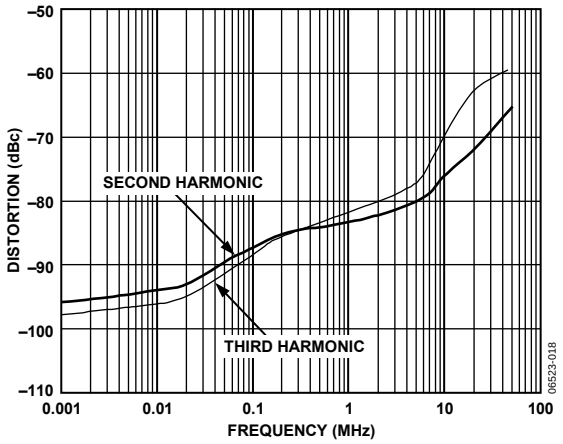


Figure 20. Distortion vs. Frequency, $V_S = \pm 5$ V, $R_L = 150\ \Omega$, $V_{OUT} = 2$ V p-p

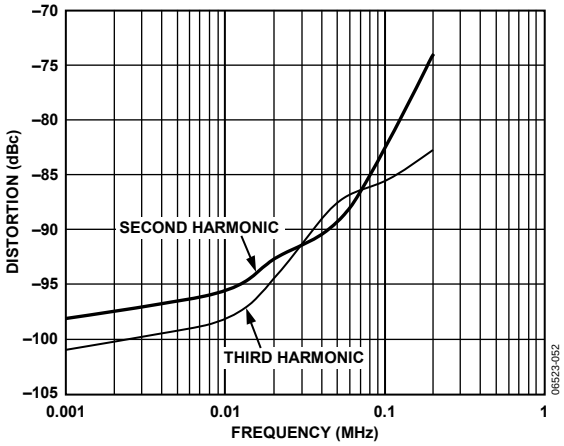


Figure 23. Distortion vs. Frequency, $V_S = \pm 12$ V, $R_L = 600\ \Omega$, $V_{OUT} = 20$ V p-p

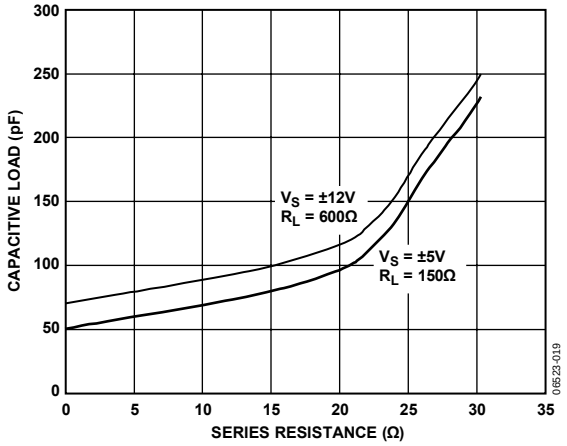


Figure 24. Capacitive Load vs. Series Resistance for Less than 30% Overshoot

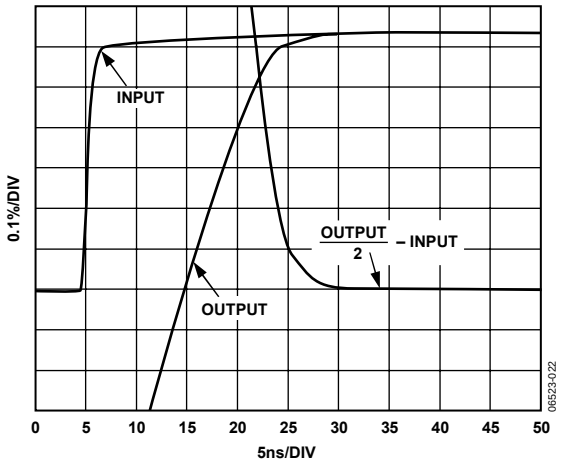


Figure 27. Settling Time to 0.1%, 2 V Step, V_S = ±5 V, R_L = 150 Ω

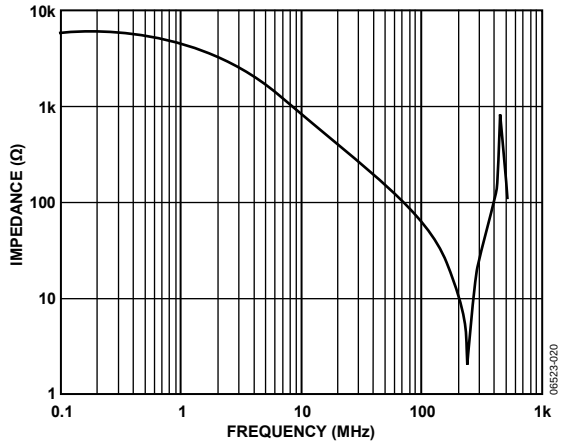


Figure 25. Disabled Output Impedance vs. Frequency, V_S = ±5 V

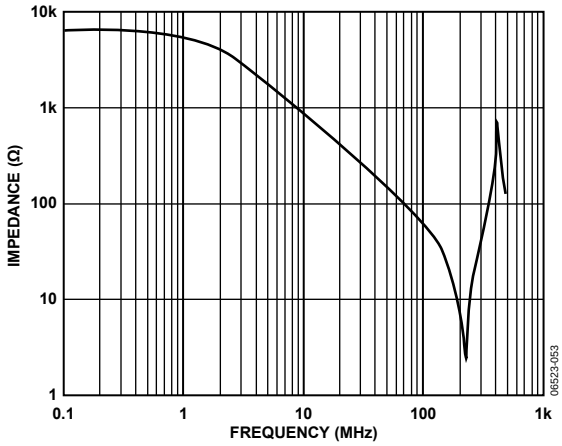


Figure 28. Disabled Output Impedance vs. Frequency, V_S = ±12 V

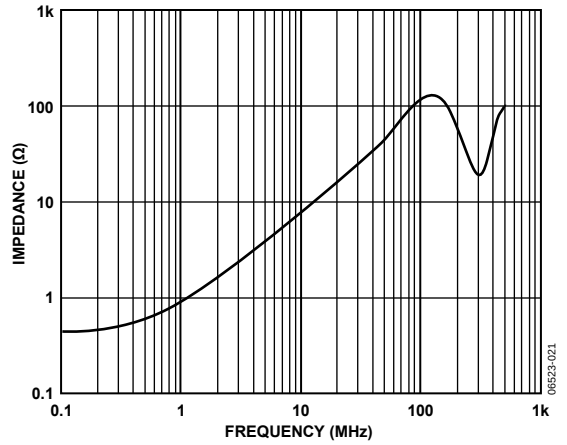


Figure 26. Enabled Output Impedance vs. Frequency, V_S = ±5 V

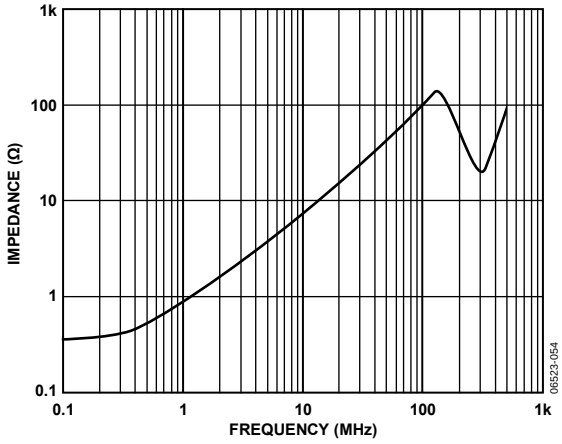


Figure 29. Enabled Output Impedance vs. Frequency, V_S = ±12 V

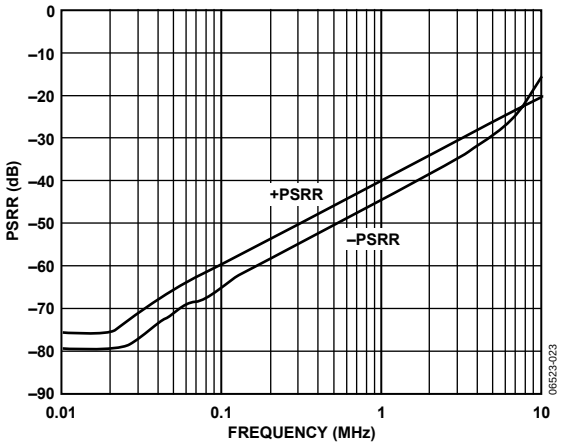


Figure 30. PSRR vs. Frequency, $V_S = \pm 5$ V

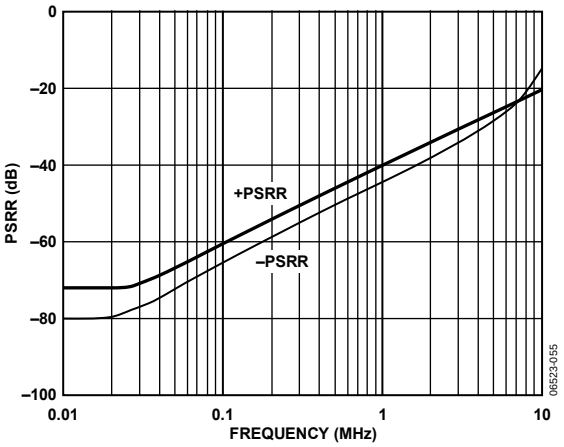


Figure 33. PSRR vs. Frequency, $V_S = \pm 12$ V

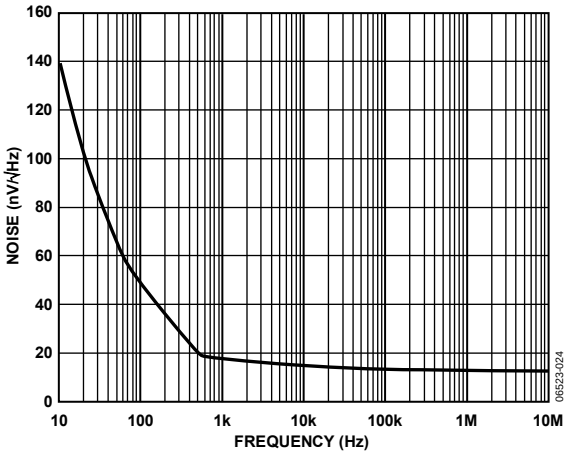


Figure 31. Noise vs. Frequency

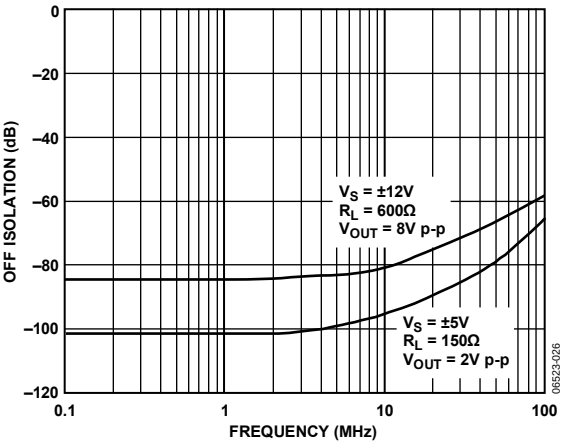


Figure 34. Off Isolation vs. Frequency

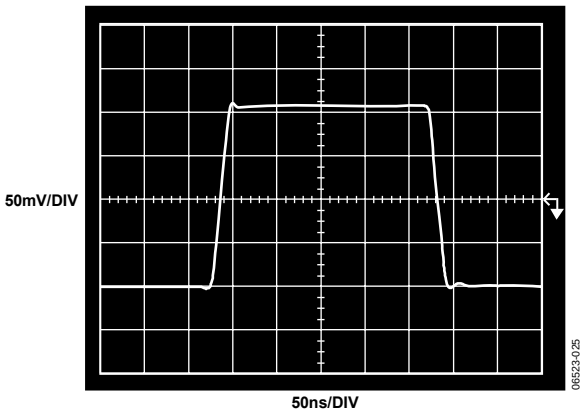


Figure 32. Small-Signal Pulse Response, $V_S = \pm 5$ V, $R_L = 150\ \Omega$

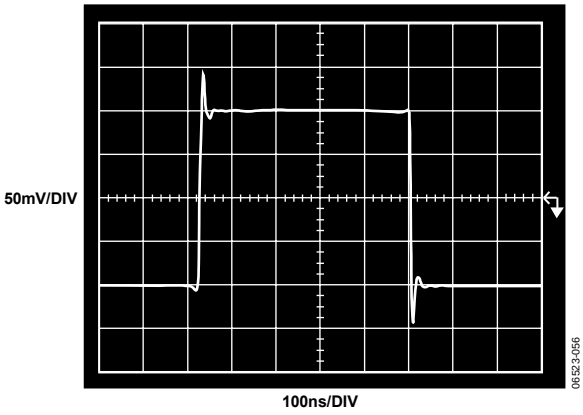


Figure 35. Small-Signal Pulse Response, $V_S = \pm 12$ V, $R_L = 600\ \Omega$

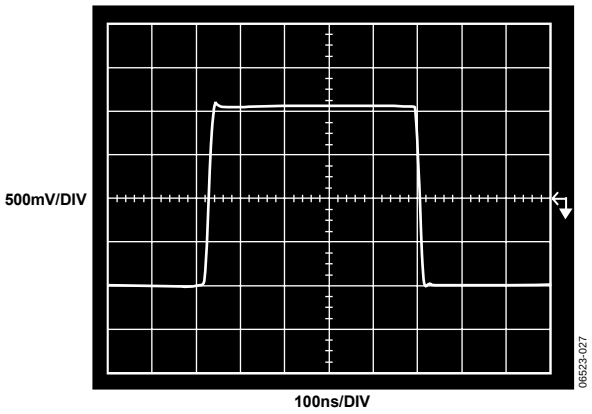


Figure 36. Large-Signal Pulse Response, $V_S = \pm 5$ V, $R_L = 150\ \Omega$

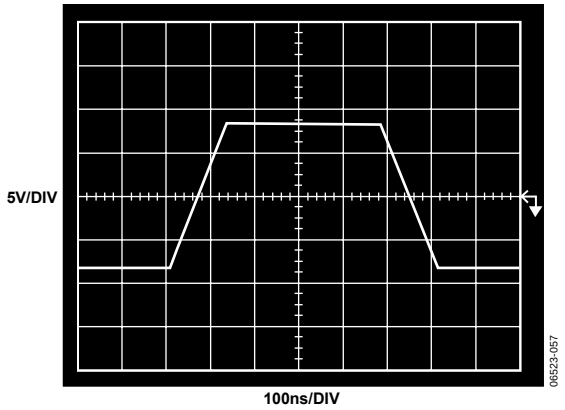


Figure 39. Large-Signal Pulse Response, $V_S = \pm 12$ V, $R_L = 600\ \Omega$

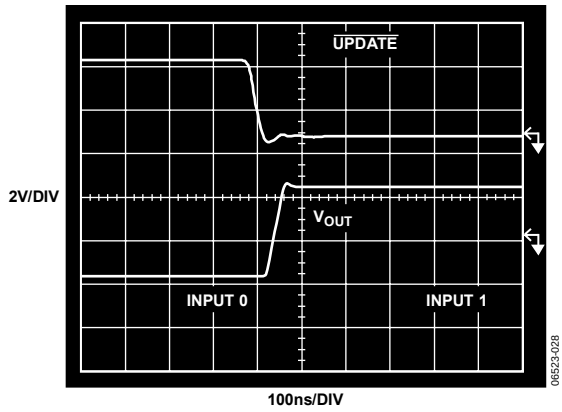


Figure 37. Switching Time, $V_S = \pm 5$ V, $R_L = 150\ \Omega$

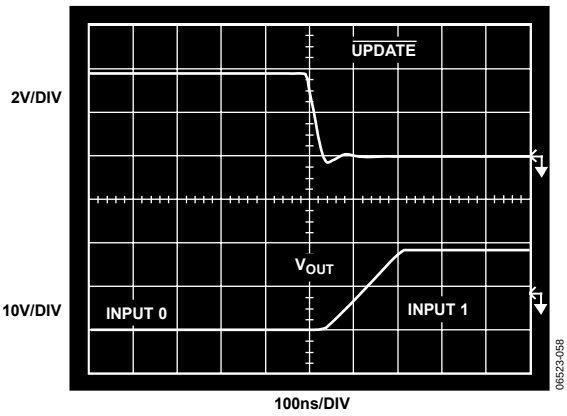


Figure 40. Switching Time, $V_S = \pm 12$ V, $R_L = 600\ \Omega$

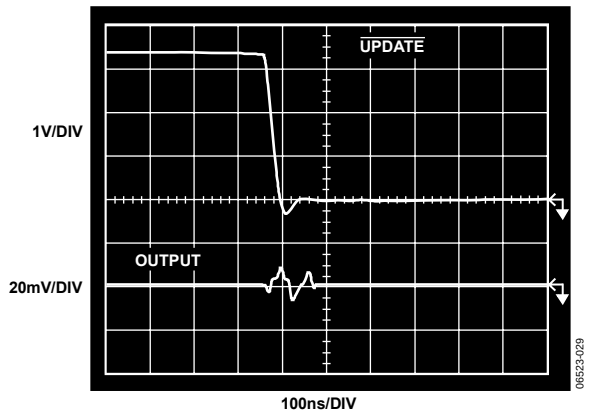


Figure 38. Switching Transient, $V_S = \pm 5$ V, $R_L = 150\ \Omega$

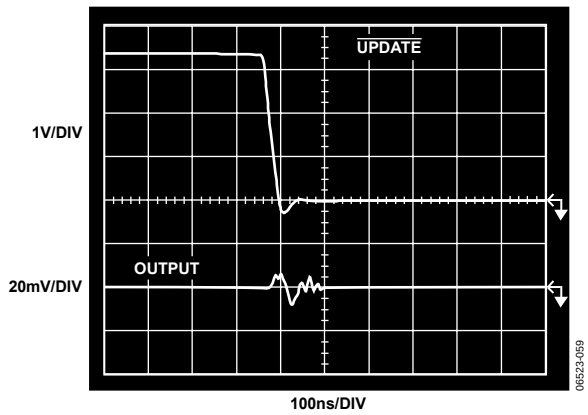


Figure 41. Switching Transient, $V_S = \pm 12$ V, $R_L = 600\ \Omega$

THEORY OF OPERATION

The AD8112 has a gain of +2 and is a crosspoint array with eight outputs, each of which can be connected to any one of 16 inputs. Organized by output row, 16 switchable transconductance stages are connected to each output buffer in the form of a 16-to-1 multiplexer. Each of the 16 rows of transconductance stages are wired in parallel to the 16 input pins, for a total array of 256 transconductance stages. Decoding logic for each output selects one (or none) of the transconductance stages to drive the output stage. The transconductance stages are NPN input differential pairs, sourcing current into the folded cascode output stage. The compensation networks and emitter follower output buffers are in the output stage. Voltage feedback sets the gain at +2.

When operated with ±12 V supplies, this architecture provides ±10 V drive for 600 Ω audio loads with extremely low distortion (<0.002%) at audio frequencies. Provided the supplies are lowered to ±5 V (to limit power consumption), the AD8112 can drive reverse-terminated video loads, swinging ±3.0 V into 150 Ω. Disabling unused outputs and transconductance stages minimizes on-chip power consumption.

Features of the AD8112 facilitate the construction of larger switch matrices. The unused outputs can be disabled, leaving only a feedback network resistance of 4 kΩ on the output. This allows multiple ICs to be bused together, provided the output load impedance is greater than the minimum allowed values. Because no additional input buffering is necessary, high input resistance and low input capacitance are easily achieved without additional signal degradation.

The AD8112 inputs have a unique bias current compensation scheme that overcomes a problem common to transconductance input array architectures. Typically, an input bias current increases as more transconductance stages connected to the same input are turned on. Anywhere from zero to 16 transconductance stages can share one input pin, so there is a varying amount of bias current supplied through the source impedance driving the input. For audio systems with larger source impedances, this has the potential of creating large offset voltages, audible as pops when switching between channels. The AD8112 samples and cancels the input bias current contributions from each transconductance stage so that the residual bias current is nominally zero regardless of the number of enabled inputs.

Due to the flexibility in allowed supply voltages, internal crosstalk isolation clamps have variable bias levels. These levels were chosen to allow for the necessary input range to accommodate the full output swing with a gain of +2. Overdriving the inputs beyond the device's linear range will eventually forward bias these clamps, increasing power dissipation. The valid input range for ±12 V supplies is ±5 V. The valid input range for ±5 V supplies is ±1.5 V. When outputs are disabled and being driven externally, the voltage applied to them should not exceed the valid output swing range for the AD8112. Exceeding ±10.5 V on the outputs of the AD8112 may apply a large differential voltage on the unused transconductance stages and should be avoided.

A flexible TTL-compatible logic interface simplifies the programming of the matrix. Either parallel or serial loading into a first rank of latches programs each output. A global latch simultaneously updates all outputs. In serial mode, a serial output pin allows devices to be daisy-chained together for single pin programming of multiple ICs. A power-on reset pin is available to avoid bus conflicts by disabling all outputs.

Regardless of the supply voltage applied to the AV_{CC} and AV_{EE} pins, the digital logic requires 5 V on the DV_{CC} pin with respect to DGND. In order for the digital-to-analog interface to work properly, DV_{CC} must be at least 7 V above AV_{EE}. Finally, internal ESD protection diodes require that the DGND and AGND pins be at the same potential.

CALCULATION OF POWER DISSIPATION

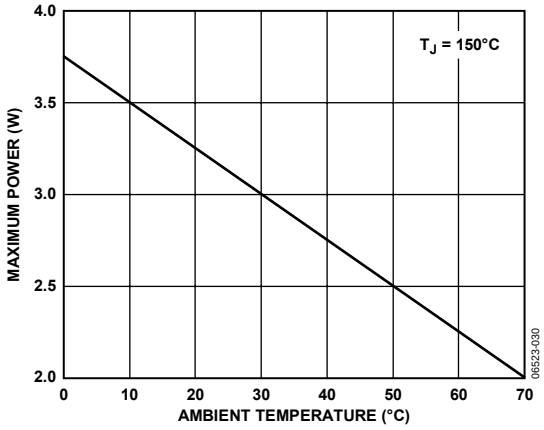


Figure 42. Maximum Power Dissipation vs. Ambient Temperature

The curve in Figure 42 was calculated from

$$P_{D,MAX} = \frac{\left(T_{JUNCTION,MAX} - T_{AMBIENT}\right)}{\theta_{JA}}$$

As an example, if the AD8112 is enclosed in an environment at 50°C (T_A), the total on-chip dissipation under all load and supply conditions must not be allowed to exceed 2.5 W.

When calculating on-chip power dissipation, it is necessary to include the rms current being delivered to the load multiplied by the rms voltage drop on the AD8112 output devices. The dissipation of the on-chip, 4 kΩ feedback resistor network must also be included. For a sinusoidal output, the on-chip power dissipation due to the load and feedback network can be approximated by

$$P_{D,\,MAX} = \left(AV_{CC} - V_{OUTPUT,\,RMS}\right) \times I_{OUTPUT,\,RMS} + \left(\frac{V_{OUTPUT,\,RMS}^{\ 2}}{4\ \text{k}\Omega}\right)$$

For nonsinusoidal output, the power dissipation is calculated by integrating the on-chip voltage drop multiplied by the load current over one period.

The user can subtract the quiescent current for the Class AB output stage when calculating the loaded power dissipation. For each output stage driving a load, subtract a quiescent power according to

$$P_{D,\,OUTPUT} = (AV_{CC} - AV_{EE}) \times I_{O,\,QUIESCENT}$$

where:
$I_{O,\,QUIESCENT}$ = 0.67 mA.

For each disabled output, the quiescent power supply current in AV_{CC} and AV_{EE} drops by approximately 1.25 mA, although there is a power dissipation in the on-chip feedback resistors if the disabled output is being driven from an external source.

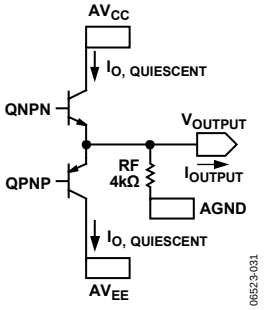


Figure 43. Simplified Output Stage

Example

The power supplies of the AD8112 with an ambient temperature of 70°C and all eight outputs driving 6 V rms into 600 Ω loads are ±12 V.

1. Calculate the power dissipation of the AD8112 using quiescent currents (see the Specifications section).

   $P_{D,\,QUIESCENT} = (AV_{CC} + I_{AVCC}) + (AV_{EE} \times I_{AVEE}) + (DV_{CC} \times I_{DVCC})$

   $P_{D,\,QUIESCENT} = (12\ \text{V} \times 54\ \text{mA}) + (-12\ \text{V} \times -54\ \text{mA}) + (5\ \text{V} \times 13\ \text{mA}) = 1.3\ \text{W}$

2. Calculate the power dissipation from the loads.

   $P_{D,\,OUTPUT} = (AV_{CC} - V_{OUTPUT,\,RMS}) \times I_{OUTPUT,\,RMS} + V_{OUTPUT}^{2}/4\ \text{k}\Omega$

   $P_{D,\,OUTPUT} = (12\ \text{V} - 6\ \text{V}) \times 6\ \text{V}/600\ \Omega + (6\ \text{V})^2/4\ \text{k}\Omega = 69\ \text{mW}$

   There are eight outputs, thus

   $nP_{D,\,OUTPUT} = 8 \times 69\ \text{mW} = 0.55\ \text{W}$

3. Subtract quiescent output current for number of loads (assumes output voltage >> 0.5 V).

   $P_{DQ,\,OUTPUT} = (AV_{CC} - AV_{EE}) \times I_{O,\,QUIESCENT}$

   $P_{DQ,\,OUTPUT} = (12\ \text{V} - (-12\ \text{V})) \times 0.67\ \text{mA} = 16\ \text{mW}$

   There are eight outputs, thus

   $nP_{DQ,\,OUTPUT} = 8 \times 16\ \text{mW} = 0.13\ \text{W}$

4. Verify that power dissipation does not exceed the maximum allowed value.

   $P_{D,\,ON\text{-}CHIP} = P_{D,\,QUIESCENT} + nP_{D,\,OUTPUT} - nP_{DQ,\,OUTPUT}$

   $P_{D,\,ON\text{-}CHIP} = 1.3\ \text{W} + 0.55\ \text{W} - 0.13\ \text{W} = 1.7\ \text{W}$

This power dissipation is below the maximum allowed dissipation for all ambient temperatures approaching 70°C.

It can be shown that for a dual supply of ±*a*, a Class AB output stage dissipates maximum power into a grounded load when the output voltage is a/2. Therefore, for a ±12 V supply, the previous example demonstrates the worst-case power dissipation into 600 Ω. It can be seen from this example that the minimum load resistance for ±12 V operation is 600 Ω for full rated operating temperature range. For larger safety margins when the output signal is unknown, loads of 1 kΩ and greater are recommended. When operating with ±5 V supplies, this load resistance can be lowered to 150 Ω.

SHORT-CIRCUIT OUTPUT CONDITIONS

Although there is short-circuit current protection on the AD8112 outputs, the output current can reach values of 55 mA into a grounded output. Sustained operation with even one shorted output will exceed the maximum die temperature and may result in device failure (see the Absolute Maximum Ratings section).

APPLICATION NOTES

The AD8112 has two options for changing the programming of the crosspoint matrix. In the first option, a serial word of 80 bits is provided to update the entire matrix. The serial data needs to be prefixed with 40 zeros because there are 40 unconnected bits. The second option allows for changing a single output's programming via a parallel interface. The serial option requires fewer signals but more time (clock cycles) for changing the programming, whereas the parallel programming technique requires more signals but can change outputs individually and requires fewer clock cycles to complete programming.

SERIAL PROGRAMMING

The serial programming mode uses the device pins: $\overline{CE}$, CLK, DATA IN, $\overline{UPDATE}$, and $\overline{SER}$/PAR. The first step is to assert a low on $\overline{SER}$/PAR to enable the serial programming mode. The $\overline{CE}$ pin for the chip must be low to allow data to be clocked into the device. The $\overline{CE}$ signal can be used to address an individual device when devices are connected in parallel.

The $\overline{UPDATE}$ signal should be high during the time that data is shifted into the device's serial port. Although the data shifts in when $\overline{UPDATE}$ is low, the transparent asynchronous latches allow the shifting data to reach the matrix. This causes the matrix to try to update to every intermediate state as defined by the shifting data.

The data at DATA IN is clocked in upon each falling edge of CLK. A total of 80 bits must be shifted in to complete the programming because there are 40 unconnected bits. For each of the eight outputs, there are four bits (D0 to D3) that determine the source of the input followed by one bit (D4) that determines the enabled state of the output. If D4 is low (output disabled), the four associated bits (D0 to D3) do not matter, because no input will be switched to that output.

The most significant output address data is shifted in first, and then followed in sequence until the least significant output address data is shifted in. At this point $\overline{UPDATE}$ can be taken low, which programs the device with the data that was just shifted in. The $\overline{UPDATE}$ registers are asynchronous, and when $\overline{UPDATE}$ is low (and $\overline{CE}$ is low), they are transparent.

If more than one AD8112 device is to be serially programmed in a system, the DATA OUT signal from one device can be connected to the DATA IN of the next device to form a serial chain. All of the CLK, $\overline{CE}$, $\overline{UPDATE}$, and $\overline{SER}$/PAR pins should be connected in parallel and operated as described previously. The serial data is input into the DATA IN pin of the first device of the chain, and it ripples through to the last device. Therefore, the data for the last device in the chain should come at the beginning of the programming sequence. The length of the programming sequence is 80 bits times the number of devices in the chain.

PARALLEL PROGRAMMING

When using the parallel programming mode, it is not necessary to reprogram the entire device when making changes to the matrix. In fact, parallel programming allows the modification of a single output. Because this requires only one CLK/$\overline{UPDATE}$ cycle, significant time is saved by using parallel programming.

One important consideration when using parallel programming is that the $\overline{RESET}$ signal does not reset all registers in the AD8112. When taken low, the $\overline{RESET}$ signal only sets each output to the disabled state. This is helpful during power-up to ensure that two parallel outputs will not be active at the same time.

After initial power-up, the internal registers in the device generally have random data, even though the $\overline{RESET}$ signal has been asserted. If parallel programming is used to program one output, then that output is properly programmed, but the rest of the device has a random program state depending on the internal register content at power-up. Therefore, when using parallel programming, it is essential that all outputs be programmed to a desired state after power-up to ensure that the programming matrix is always in a known state. Then, parallel programming can be used to modify a single output or multiple outputs.

Similarly, if both $\overline{CE}$ and $\overline{UPDATE}$ are taken low after initial power-up, the random power-up data in the shift register is programmed into the matrix. Therefore, to prevent the crosspoint from being programmed into an unknown state, do not apply low logic levels to both $\overline{CE}$ and $\overline{UPDATE}$ after power is initially applied. Programming the full shift register one time to a desired state, by either serial or parallel programming after initial power-up, eliminates the possibility of programming the matrix to an unknown state.

To change an output programming via parallel programming, $\overline{SER}$/PAR and $\overline{UPDATE}$ should be taken high and $\overline{CE}$ should be taken low. The CLK signal should be in the high state. The 3-bit address of the output to be programmed should be put on A0 to A2. The first four data bits (D0 to D3) should contain the information identifying the input that is programmed to the addressed output. The fifth data bit (D4) determines the enabled state of the output. If D4 is low (output disabled), the data on D0 to D3 does not matter.

After the desired address and data signals have been established, the data can be latched into the shift register by a high to low transition of the CLK signal. The matrix will not be programmed, however, until the $\overline{UPDATE}$ signal is taken low. It is therefore possible to latch in new data for several or all outputs via successive negative transitions of CLK while $\overline{UPDATE}$ is held high, and then for the new data to take effect when $\overline{UPDATE}$ goes

low. This technique should be used when programming the device for the first time after power-up when using parallel programming.

POWER-ON RESET

When powering up the AD8112, it is usually desirable to have the outputs in the disabled state. The $\overline{\text{RESET}}$ pin, when taken low, causes all outputs to be in the disabled state. However, the $\overline{\text{RESET}}$ signal does not reset all registers in the AD8112. This is important when operating in the parallel programming mode. (Please refer to the Parallel Programming section for information about programming internal registers after power-up.) Serial programming updates the entire matrix, therefore no special considerations apply.

Because the data in the shift register is random after power-up, it should not be used to program the matrix; otherwise the matrix can enter an unknown state. To prevent this, do not apply logic low signals to both $\overline{\text{CE}}$ and $\overline{\text{UPDATE}}$ immediately after power-up. The shift register should first be loaded with the desired data, and then $\overline{\text{UPDATE}}$ can be taken low to program the device.

The $\overline{\text{RESET}}$ pin has a 20 kΩ pull-up resistor to DV_{CC} that can be used to create a simple power-up reset circuit. A capacitor from $\overline{\text{RESET}}$ to ground holds $\overline{\text{RESET}}$ low until the device stabilizes. The low condition causes all the outputs to be disabled. The capacitor then charges through the pull-up resistor to the high state, thus allowing full programming capability of the device.

SPECIFYING AUDIO LEVELS

Several methods are used to specify audio levels. A level is actually a power measurement, which requires not just a voltage measurement, but also a reference impedance. Traditionally both 150 Ω and 600 Ω have been used as references for audio level measurements.

The typical reference power level is 1 mW. Power levels that are measured relative to this reference level are given the designation dBm. However, it is necessary to be sure of the reference impedance used for such measurements. This can be either explicit (for example, 0 dBm (600 Ω)) or implicit (if there is an agreement on what the reference impedance is).

Because modern voltmeters have high input impedances, measurements can be made that do not terminate the signal. Therefore, it is not proper to consider this type of measurement a dBm, or power measurement. However, a measurement scale that is designated dBu is used to measure unterminated voltages. This scale has a voltage reference for 0 dBu that is the same as the voltage required to produce 0 dBm (600 Ω).

Because $P = V^2/R$, the voltage required to create 1 mW into 600 Ω is 0.775 V rms. This is the voltage reference (0 dB) used for dBu measurements without regard to the impedance.

The AD8112 operates as a voltage-in/voltage-out device. Therefore, all parameters are specified in volts, but users can convert the values to other power units or decibel-type measurements as required by a particular application.

CREATING UNITY-GAIN CHANNELS

The channels in the AD8112 each have a gain of +2. This gain is necessary, as opposed to a gain of unity, to restrict the voltage on internal nodes to less than the breakdown voltage. If it is desired to create channels with an overall gain of unity, a resistive divider can be used at the input to divide the signals by 2. After passing through any input/output channel combination of the AD8112, the overall gain of unity is achieved.

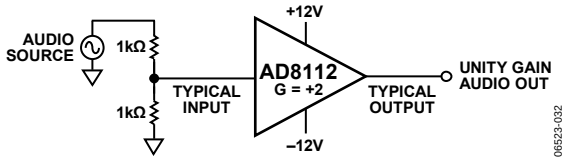


Figure 44. Input Divide Circuit

Figure 44 shows a typical input with a divide-by-2 input divider that creates a unity gain channel. The circuit uses 1 kΩ resistors to form the divider. These resistors need to be high enough so they do not overload the drive circuit. But if they are too high, they generate an offset voltage due to the input bias current that flows through them. Larger resistors also increase the thermal noise of the channel.

The circuit shown in Figure 44 can handle inputs that swing up to ±10 V when the AD8112 operates on analog supplies of ±12 V. After passing through the divider, the maximum voltage is ±5 V at the input. This maximum input amplitude is ±10 V at the output after the gain of +2 of the channels.

VIDEO SIGNALS

Unlike audio signals, which have lower bandwidths and longer wavelengths, video signals often use controlled-impedance transmission lines that are terminated in their characteristic impedance. Although this is not always the case, there are some considerations when using the AD8112 to route video signals with controlled-impedance transmission lines. Figure 45 shows a schematic of an input and output treatment of a typical video channel.

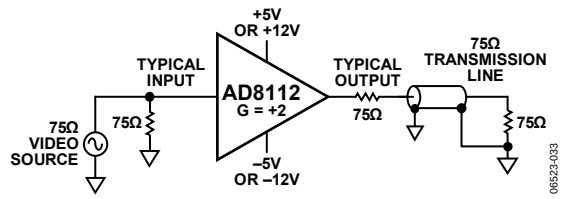


Figure 45. Video Signal Circuit

Video signals usually use 75 Ω transmission lines that need to be terminated with this value of resistance at each end. When such a source is delivered to one of the AD8112 inputs, the high input impedance does not properly terminate these signals. Therefore, the line should be terminated with a 75 Ω shunt resistor to ground. Because video signals are limited in their peak-to-peak amplitude, there is no need to attenuate video signals before they pass through the AD8112.

The AD8112 outputs are very low impedance and do not properly terminate the source end of a 75 Ω transmission line. In these cases, a series 75 Ω resistor should be inserted at an output that drives a video signal. Then the transmission line should be terminated with 75 Ω at its far end. This overall termination scheme divides the amplitude of the AD8112 output by 2. An overall unity gain channel is produced as a result of the AD8112's channel gain of +2.

CREATING LARGER CROSSPOINT ARRAYS

The AD8112 is a high density building block for creating crosspoint arrays of dimensions larger than 16 × 8. Various features, such as output disable and chip enable, are useful for creating larger arrays.

The first consideration in constructing a larger crosspoint is to determine the minimum number of devices required. The 16 × 8 architecture of the AD8112 contains 128 points, which is a factor of 32 greater than a 4 × 1 crosspoint (or multiplexer). The PC board area, power consumption, and design effort savings are readily apparent when compared with using these smaller devices.

For a nonblocking crosspoint, the number of points required is the product of the number of inputs multiplied by the number of outputs. Nonblocking requires that the programming of a given input to one or more outputs does not restrict the availability of that input to be a source for any other outputs.

Some nonblocking crosspoint architectures require more than this minimum as previously calculated. Also, there are blocking architectures that can be constructed with fewer devices than this minimum. These systems have connectivity available on a statistical basis that is determined when designing the overall system.

The basic concept in constructing larger crosspoint arrays is to connect inputs in parallel in a horizontal direction and to wire-OR the outputs together in the vertical direction. The meaning of horizontal and vertical can best be understood by looking at Figure 46, which illustrates this concept for a 32 × 16 crosspoint array that uses four AD8112s.

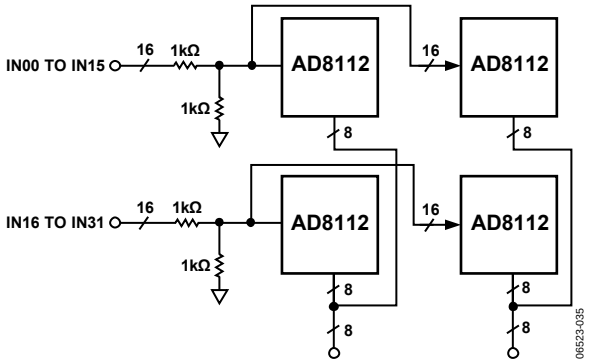


Figure 46. 32 x 16 Audio Crosspoint Array Using Four AD8112s

The inputs are individually assigned to each of the 32 inputs of the two devices and a divider is used to normalize the channel gain. The outputs are wire-OR'ed together in pairs. The output from only one wire-OR'ed pair should be enabled at any given time. The device programming software must be properly written to for this to happen.

Using additional crosspoint devices in the design can lower the number of outputs that must be wire-OR'ed together. Figure 47 shows a block diagram of a system using ten AD8112s to create a nonblocking, gain of +2, 128 × 8 crosspoint that restricts the wire-OR'ing at the output to only four outputs.

Additionally, by using the lower eight outputs from each of the two Rank 2 AD8112s, a blocking 128 × 16 crosspoint array can be realized. There are, however, some drawbacks to this technique. The offset voltages of the various cascaded devices accumulate, and the bandwidth limitations of the devices compound. In addition, the extra devices consume more current and take up more board space. Consider the overall system design specifications when using the various trade-offs.

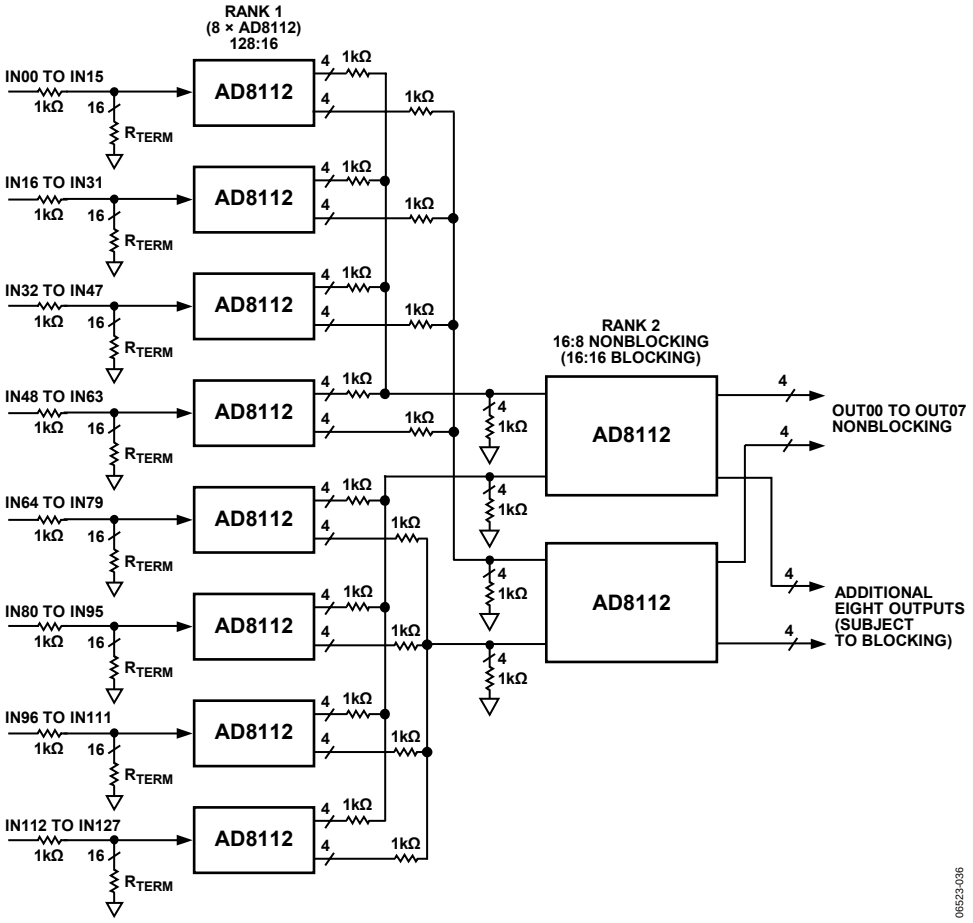


Figure 47. Nonblocking 128 × 8 Audio Array (128 × 16 Blocking)

MULTICHANNEL VIDEO AND AUDIO

The video specifications of the AD8112 make it an ideal candidate for creating composite video crosspoint switches. These can be made quite dense by taking advantage of the AD8112's high level of integration and the fact that composite video requires only one crosspoint channel per system video channel. There are, however, other video formats that can be routed with the AD8112, requiring more than one crosspoint channel per video channel.

Some systems use twisted pair cables to carry video or audio signals. These systems utilize differential signals and can lower costs because they use lower cost cables, connectors, and termination methods. They also have the ability to lower crosstalk and reject common-mode signals, which can be important for equipment that operates in noisy environments, or where common-mode voltages are present between transmitting and receiving equipment.

In such systems, the audio or video signals are differential; there are positive and negative (or inverted) versions of the signals. These complementary signals are transmitted through each of the two cables of the twisted pair, yielding a first-order zero common-mode voltage. At the receive end, the signals are differentially received and converted back into a single-ended signal.

When switching these differential signals, two channels are required in the switching element to handle the two differential signals that compose the video or audio channel. Thus, one differential video or audio channel is assigned to a pair of crosspoint channels, both input and output. For a single AD8112, eight differential video or audio channels can be assigned to the 16 inputs, and four differential video or audio channels can be assigned to the eight outputs. This effectively forms an 8×4 differential crosspoint switch.

Programming such a device requires that inputs and outputs be programmed in pairs. This information can be deduced through inspection of the programming format of the AD8112 and the requirements of the system.

There are other analog video formats requiring more than one analog circuit per video channel. One two-circuit format that is commonly being used in systems such as satellite TV, digital cable boxes, and higher quality VCRs is called S-video or Y/C video. This format carries the brightness (luminance or Y) portion of the video signal on one channel and the color (chrominance, chroma, or C) portion on a second channel.

Because S-video also uses two separate circuits for one video channel, creating a crosspoint system requires assigning one video channel to two crosspoint channels, as in the case of a differential video system. Aside from the nature of the video format, other aspects of these two systems are the same. Stereo audio can also be routed in a paired-channel arrangement similar to a two-channel video system.

There are yet other video formats using three channels to carry the video information. Video cameras produce RGB (red, green, blue) directly from the image sensors. RGB is also the usual format used internally by computers for graphics. RGB can also be converted to Y, R–Y, B–Y format, sometimes called YUV format. These three-circuit video standards are referred to as component analog video.

The component video standards require three crosspoint channels per video channel to handle the switching function. Similar to the two-circuit video formats, the inputs and outputs are assigned in groups of three, and the appropriate logic programming is performed to route the video signals.

CROSSTALK

Many systems, such as studio audio or broadcast video, that handle numerous analog signal channels have strict requirements for keeping the various signals from influencing other signals in the system. Crosstalk is the term used to describe the coupling of the signals of other nearby channels to a given channel.

When there are many signals in close proximity in a system, as undoubtedly is the case in a system that uses the AD8112, the crosstalk issues can be quite complex. A good understanding of the nature of crosstalk and some definition of terms is required in order to specify a system that uses one or more AD8112s.

Types of Crosstalk

Crosstalk can be propagated by one of three methods. These fall into the categories of electric field, magnetic field, and sharing of common impedances. This section explains these effects.

Every conductor can be both a radiator of electric fields and a receiver of electric fields. The electric field crosstalk mechanism occurs when the electric field created by the transmitter propagates across a stray capacitance (for example, free space) and then couples with the receiver and induces a voltage. This voltage is an unwanted crosstalk signal in any channel that receives it.

Currents flowing in conductors create magnetic fields that circulate around the currents. These magnetic fields then generate voltages in any other conductor whose paths is linked. The undesired induced voltages in these other channels are crosstalk signals. The channels with crosstalk have a mutual inductance that couples signals from one channel to another.

The power supplies, grounds, and other signal return paths of a multichannel system are generally shared by the various channels. When a current from one channel flows into one of these paths, a voltage that is developed across the impedance becomes an input crosstalk signal for other channels that share the common impedance.

All these sources of crosstalk are vector quantities; therefore the magnitudes cannot simply be added together to obtain the total crosstalk. In fact, there are conditions where driving additional circuits in parallel in a given configuration can reduce the crosstalk.

Areas of Crosstalk

A practical AD8112 circuit must be mounted to some sort of circuit board to connect it to power supplies and measurement equipment. Great care has been taken to create a characterization board (also available as an evaluation board) that adds minimum crosstalk to the intrinsic device. This, however, raises the issue that the crosstalk of a system is a combination of the intrinsic crosstalk of both the devices and the circuit board to which they are mounted. It is important to try to separate these two areas when attempting to minimize the effect of crosstalk.

In addition, crosstalk can occur among the inputs as well as the outputs of a cross-point. It can also occur from input to output. The following sections describe techniques for measuring and identifying the source of crosstalk.

Measuring Crosstalk

Crosstalk is measured by applying a signal to one or more channels and measuring the relative strength of that signal on a desired selected channel. The measurement is usually expressed as decibels down from the magnitude of the test signal. The crosstalk is expressed by

$$|XT| = 20\log_{10}\left(Asel(s)/Atest(s)\right)$$

where:
$s = jw$ is the Laplace transform variable.
Asel(s) = the amplitude of the crosstalk induced signal in the selected channel.
Atest(s) = the amplitude of the test signal.

It can be seen that crosstalk is a function of frequency, but not a function of the magnitude of the test signal (to first order). In addition, the crosstalk signal has a phase relative to the test signal associated with it.

A network analyzer is most commonly used to measure crosstalk over a frequency range of interest. It can provide both magnitude and phase information about the crosstalk signal.

As a crosspoint system or device grows larger, the number of theoretical crosstalk combinations and permutations can become extremely large. For example, in the case of the 16 × 8 matrix of the AD8112, consider the number of possible sources of crosstalk terms for a single channel, for example the IN00 input. IN00 is programmed to connect to one of the AD8112 outputs where crosstalk can be measured.

To measure this crosstalk, use one of the following two methods. In the first method, the crosstalk terms associated with driving a test signal into each of the other 15 inputs is measured one at a time, while applying no signal to IN00. In the second method, the crosstalk terms associated with driving a parallel test signal into all 15 other inputs is measured two at a time in all possible combinations, then three at a time, and so on, until, finally, there is only one way to drive a test signal into all 15 other inputs in parallel.

Each combination is legitimately different from the others and might yield a unique value, depending on the resolution of the measurement system. It is not practical to measure and then specify all these terms. Furthermore, this describes the crosstalk matrix for just one input channel. A similar crosstalk matrix can be proposed for every other input. In addition, if the possible combinations and permutations for connecting inputs to the other outputs (not used for measurement) are taken into consideration, the numbers of possibilities quickly grows to astronomical proportions. If a larger crosspoint array of multiple AD8112s is constructed, the numbers grow larger still.

Obviously, a subset of all these cases must be selected to be used as a guide for a practical measure of crosstalk. One common method is to measure all hostile crosstalk; this means that the crosstalk to the selected channel is measured while all other system channels are driven in parallel. In general, this yields the worst crosstalk number, but this is not always the case, due to the vector nature of the crosstalk signal.

Other useful crosstalk measurements are those created by the nearest neighbor or by the two nearest neighbors on either side. These crosstalk measurements are generally higher than those of more distant channels, and therefore can serve as a worst-case measure for any other 1-channel or 2-channel crosstalk measurements.

Input and Output Crosstalk

The flexible programming capability of the AD8112 can be used to diagnose whether crosstalk is greater on the input side or the output side. For example, to identify the source of crosstalk, the IN07 input channel can be programmed to drive OUT07, with the input to IN07 terminated to ground (via 50 Ω or 75 Ω) and no signal applied.

All the other inputs are driven in parallel with the same test signal (practically provided by a distribution amplifier), with all other outputs except OUT07 disabled. Because grounded IN07 is programmed to drive OUT07, no signal should be present. Any signal that is present can be attributed to the other 15 hostile input signals, because no other outputs are driven (they are all disabled). Therefore, this method measures the all-hostile input contribution to crosstalk into IN07. This method can be used for other input channels and combinations of hostile inputs.

For output crosstalk measurement, a single input channel is driven (IN00, for example) and all outputs other than a given output (IN07 in the middle) are programmed to connect to IN00. OUT07 is programmed to connect to IN15 (not in close proximity to IN00), which is terminated to ground. Therefore, OUT07 should not have a signal present because it is listening to a quiet input. Any signal measured at the OUT07 can be attributed to the output crosstalk of the other seven hostile outputs. Again, this method can be modified to measure other channels and other crosspoint matrix combinations.

Effect of Impedances on Crosstalk

The input side crosstalk can be influenced by the output impedance of the sources that drive the inputs. The lower the impedance of the drive source, the lower the magnitude of the crosstalk. The dominant crosstalk mechanism on the input side is capacitive coupling. The high impedance inputs do not have significant current flow to create magnetically induced crosstalk. However, significant current can flow through the input termination resistors and the loops that drive them. Therefore, the PC board on the input side can contribute to magnetically coupled crosstalk.

From a circuit standpoint, the input crosstalk mechanism looks like a capacitor coupling to a resistive load. For low frequencies the magnitude of the crosstalk is given by

$$|XT| = 20 \log_{10}[(R_S C_M) \times s]$$

where:
R_S is the source resistance.
C_M is the mutual capacitance between the test signal circuit and the selected circuit.
s is the Laplace transform variable.

From the equation, it can be observed that this crosstalk mechanism has a high-pass nature. It can also be minimized by reducing the coupling capacitance of the input circuits and lowering the output impedance of the drivers. If the input is driven from a 75 Ω terminated cable, the input crosstalk can be reduced by buffering this signal with a low output impedance buffer.

On the output side, the crosstalk can be reduced by driving a lighter load. Although the AD8112 is specified with excellent differential gain and phase when driving a standard 150 Ω video load, the crosstalk is higher than the minimum obtainable crosstalk due to the high output currents. These currents induce crosstalk via the mutual inductance of the output pins and bond wires of the AD8112.

From a circuit standpoint, this output crosstalk mechanism looks like a transformer with a mutual inductance between the windings that drive a load resistor. For low frequencies, the magnitude of the crosstalk is given by

$$|XT| = 20 \log_{10}\left(Mxy \times s / R_L\right)$$

where:
Mxy is the mutual inductance of output x to output y.
R_L is the load resistance on the measured output.

This crosstalk mechanism can be minimized by keeping the mutual inductance low and increasing R_L. The mutual inductance can be kept low by increasing the spacing of the conductors and minimizing their parallel length.

PCB LAYOUT

Extreme care must be exercised to minimize additional crosstalk generated by the system circuit board(s). The areas that must be carefully designed are grounding, shielding, signal routing, and supply bypassing.

The packaging of the AD8112 is designed to help minimize crosstalk. Each input is separated from each other input by an analog ground pin. All of these AGNDs should be directly connected to the ground plane of the circuit board. These ground pins provide shielding, low impedance return paths, and physical separation for the inputs. All of these help to reduce crosstalk.

Each output is separated from its two neighboring outputs by an analog supply pin of one polarity or the other. Each of these analog supply pins provides power to the output stages of only the two nearest outputs. These supply pins provide shielding, physical separation, and a low impedance supply for the outputs. Individual bypassing of each of these supply pins with a 0.01 µF chip capacitor connected directly to the ground plane minimizes high frequency output crosstalk via the mechanism of sharing common impedances.

In addition, each output has an on-chip compensation capacitor that is individually tied to the nearby analog ground pins (AGND00 through AGND07). This technique reduces crosstalk by preventing the currents that flow in these paths from sharing a common impedance on the IC and in the package pins. These AGNDxx signals should all be connected directly to the ground plane.

The input and output signals have minimum crosstalk if they are located between ground planes on layers above and below, and separated by ground in between. Vias should be located as close to the IC as possible to carry the inputs and outputs to the inner layer. The input and output signals surface at the input termination resistors and at the output series back-termination resistors. To the extent possible, these signals should also be separated as soon as they emerge from the IC package.

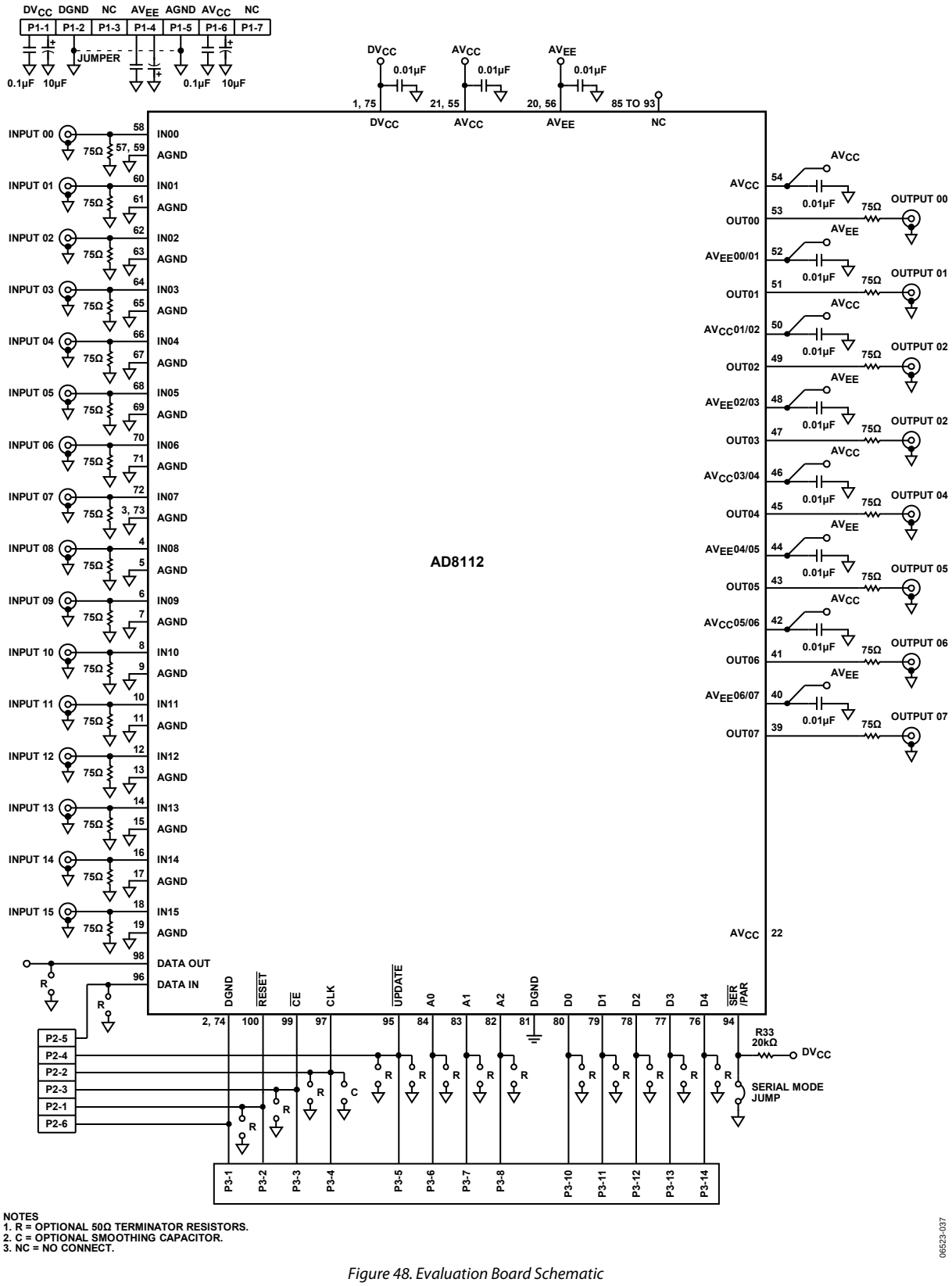
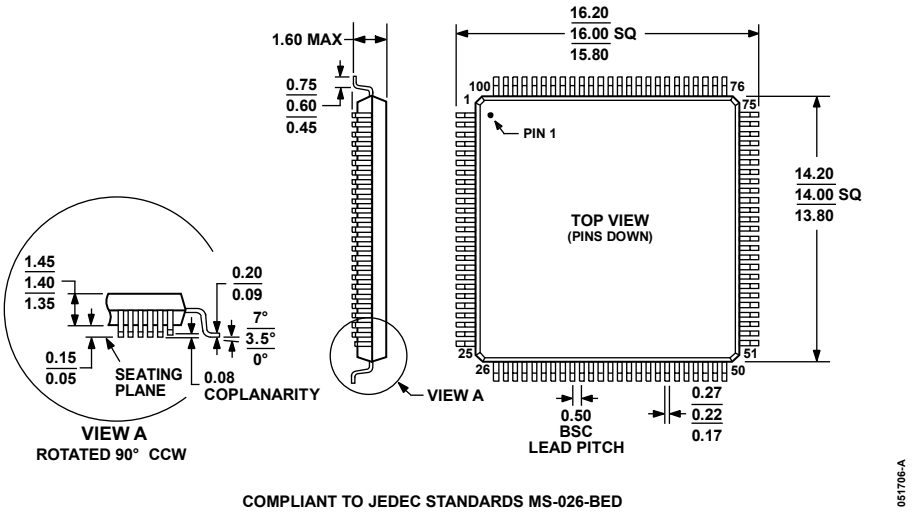


Figure 48. Evaluation Board Schematic

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BED

Figure 49. 100-Lead Low Profile Quad Flat Package [LQFP]
(ST-100)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8112JSTZ[1]	0°C to 70°C	100-Lead Plastic LQFP	ST-100
AD8112-EVALZ[1]		Evaluation Board	

[1] Z = Pb-free part.

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