2x7W Stereo / 1x10W Mono Class-D Audio Amplifier With Built-in Step-up Converter

Features

- Input voltage 2.6V~5.5V
- Adjustable boost converter output up to 9V
- Adjustable over current protection: 0.5A~4.5A
- Loudspeaker power from 9V supply @V_{CC}=5V
  Stereo: 5W/CH into 8Ω @ <10% THD+N
  Stereo: 7W/CH into 4Ω @ <0.1% THD+N
  Mono (PBTL): 10W/CH into 4Ω @THD+N=10%
- Loudspeaker power from 8V supply @V_{CC}=3.6V
  Stereo: 4W/CH into 8Ω @ <10% THD+N
  Mono (PBTL): 9W/CH into 4Ω @ THD+N=10%
- Differential inputs signal
- Four selectable, fixed gain settings
- Internal oscillator
- Short-Circuit protection with auto recovery option
- Under-Voltage detection
- Over-Voltage protection
- Pop noise and click noise reduction
- Adjustable power limit function for speaker protection
- Output DC detection for speaker protection
- Filter-Free operation
- Over temperature protection with auto recovery
- Superior EMC performance

Applications

- Blue-tooth Box
- Portable Media
- Audio Docking System
- Tablet Personal PC
- Consumer Audio Equipment

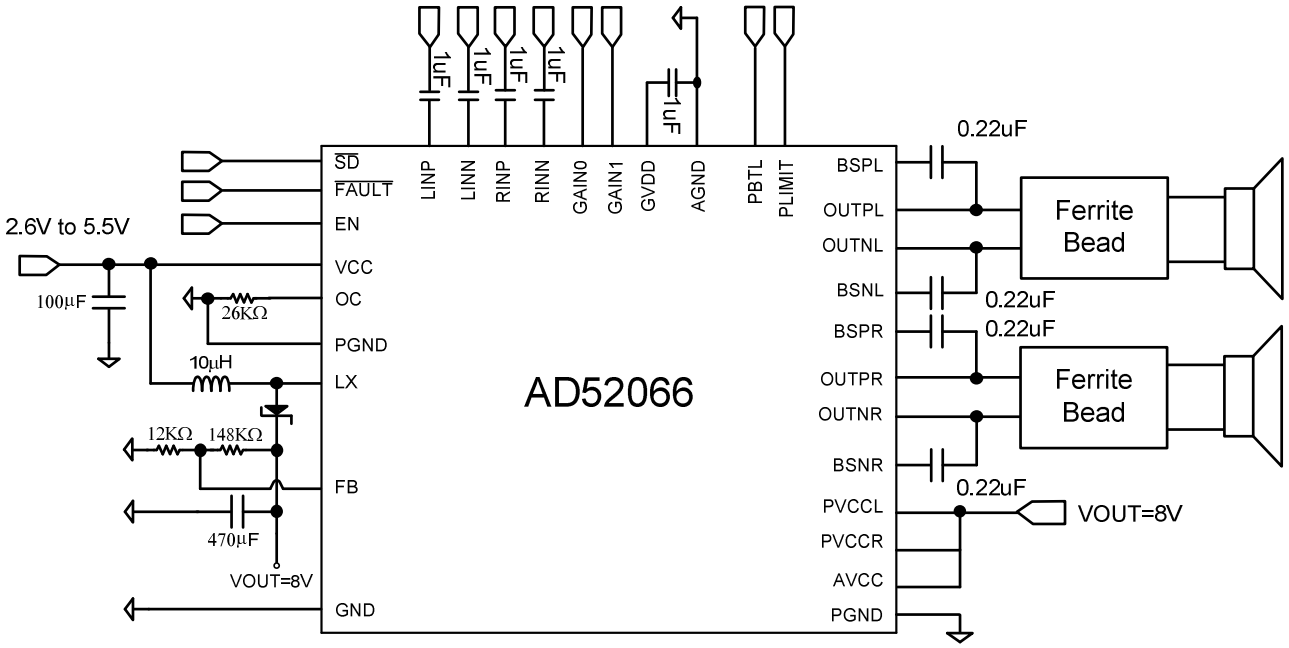
Description

The AD52066 is a high efficiency stereo class-D audio amplifier with built-in boost DC-DC converter. The loudspeaker driver can deliver 7W/CH output power into 4Ω loudspeaker under 0.1% THD+N at 5V supply voltage; driver 4W/CHx2 output power into 8Ω loudspeaker within 10% THD+N at Li-ion battery (3.6V).

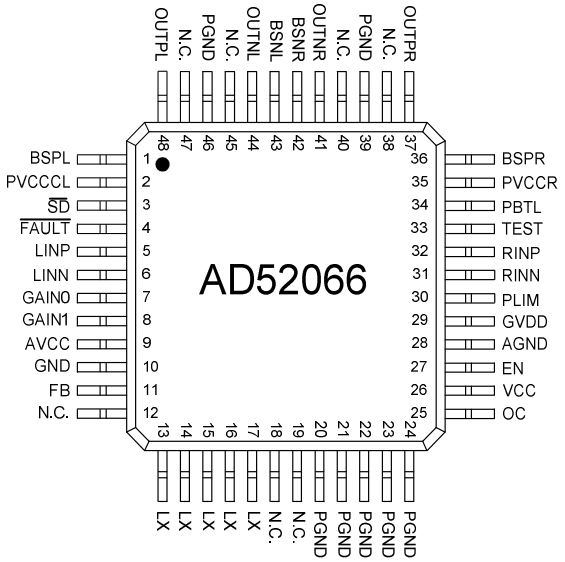
AD52066 provides parallel BTL (Mono) application also, and it can deliver 10W into 4Ω loudspeaker at 5V supply voltage. The adjustable power limit function allows user to set a voltage rail lower than half of 5V to limit the amount of current through the speaker.

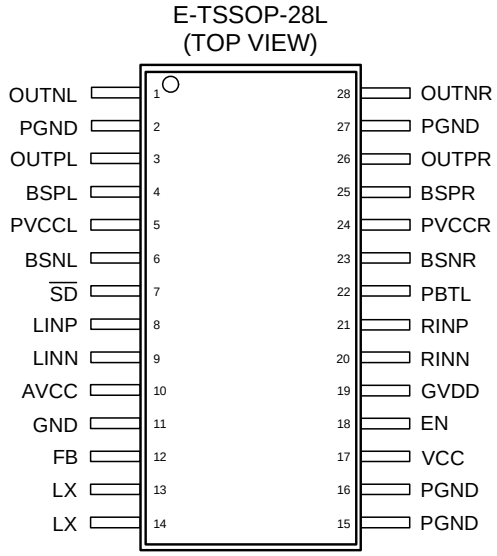
Output DC detection prevents speaker damage from long-time current stress. AD52066 provides superior EMC performance for filter-free application. The output short circuit and over temperature protection include auto-recovery feature.

Simplified Application Circuit



Pin Assignments





Pin Description

NAME	E-LQFP-48L	E-TSSOP-28L	TYP	DESCRIPTION
BSPL	1	4	I	Bootstrap I/O for left channel, positive high side FET.
PVCCL	2	5	P	High-voltage power supply for left-channel. Right channel and left channel power supply inputs are connect internal.
$\overline{SD}$	3	7	I	Shutdown signal for IC (low = disabled, high = operational). Voltage compliance to AVCC.
$\overline{FAULT}$	4	N/A	O	Open drain output used to display short circuit or dc detect fault. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting FAULTB pin to $\overline{SD}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling AVCC.
LINP	5	8	I	Positive audio input for left channel. Biased at 2.5V.
LINN	6	9	I	Negative audio input for left channel. Biased at 2.5V.
GAIN0	7	N/A	I	Gain select least significant bit. Voltage compliance to AVCC.
GAIN1	8	N/A	I	Gain select least significant bit. Voltage compliance to AVCC.
AVCC	9	10	P	Analog supply.
GND	10	11	P	Boost ground pin
FB	11	12	I	Receives the feedback voltage from an external resistive divider across the output.
N.C.	12	N/A		Not connected.
LX	13,14,15,16,17	13,14	O	Must be connected an Inductor from VCC pin to LX pin for boost and rectifying switches.
N.C.	18,19	N/A		Not connected.
PGND	20,21,22,23,24	2,15,16,27	P	Power Switch Ground Pin.

OC	25	N/A	I	OC adjustable via a resister from OC pin to GND (floating available).
VCC	26	17	P	Must be closely decoupled to GND pin with 470uF*1or greater ceramic capacitor.
EN	27	18	I	Boost enable pin (high=Enable; low=Disable).
AGND	28	N/A	P	Analog signal ground. Connect to the thermal pad.
GVDD	29	19	P	5V regulated output, also used as supply for PLIMIT function.
PLIM	30	N/A	O	Power limit level adjustment. Connect a resistor divider from GVDD to GND to set power limit. Give V(PLIMIT) <2.4V to set power limit level. Connect to GVDD (>2.4V) or GND to disable power limit function.
RINN	31	20	I	Negative audio input for right channel. Biased at 2.5V.
RINP	32	21	I	Positive audio input for right channel. Biased at 2.5V.
TEST	33	N/A	I	Test mode pin.
PBTL	34	22	I	Parallel BTL mode switch, high for parallel BTL output. Voltage compliance to AVCC.
PVCCR	35	24	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
BSPR	36	25	I	Bootstrap I/O for right channel, positive high side FET.
OUTPR	37	26	O	Class-D H-bridge positive output for right channel.
N.C.	38	N/A		Not connected.
PGND	39	N/A	P	Power ground for the H-bridges.
N.C.	40	N/A		Not connected.
OUTNR	41	28	O	Class-D H-bridge negative output for right channel.
BSNR	42	23	I	Bootstrap I/O for right channel, negative high side FET.
BSNL	43	6	I	Bootstrap I/O for left channel, negative high side FET.
OUTNL	44	1	O	Class-D H-bridge negative output for left channel.
N.C.	45	N/A		Not connected.
PGND	46	N/A	P	Power ground for the H-bridges.
N.C.	47	N/A		Not connected.
OUTPL	48	3	O	Class-D H-bridge positive output for left channel.
Thermal Pad			P	Must be soldered to PCB's ground plane.

Note:

P: Power or ground pins; I: Input pins; O: Output pins; I/O: The bidirectional pins

Ordering Information

Product ID	Package	Packing Code	Packing / MPQ	Comments
AD52066-LG48NR	E-LQFP 48L (7mmX7mm)	Y	250Units / Tube 2.5K Units / Box(10 Tray)	Green
AD52066-QG28NR	E-TSSOP 28L	T	50 Units / Tube 100 Tubes / Small Box	Green

Available Package

Package Type	Device No.	θ_{ja}(℃/W)	θ_{jt} (℃/W)	Ψ_{jt} (℃/W)	Exposed Thermal Pad
E-LQFP-48L 7X7	AD52066	22.9	34.9	1.64	Yes (Note1)
E-TSSOP 28L		28	27.1	1.33	Yes (Note 1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja} is measured on a room temperature (T_A=25 ℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.

Note 1.3: θ_{jt} represents the heat resistance for the heat flow between the chip and the package's top surface. (The junction-to-top thermal resistance is obtained by simulating a cold plate test on the top of the package).

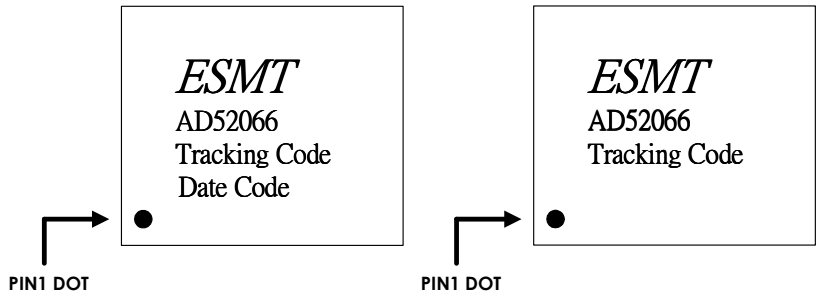
Note 1.4: Ψ_{jt} represents the heat resistance for the heat flow between the chip and the exposed pad center. (The junction-to-top characterization parameter is extracted from the simulation data to obtain θ_{ja}).

Marking Information

AD52066

- Marking Information

Line 1：LOGO
Line 2：Product No
Line 3：Tracking Code
Line 4：Date Code



E-LQFP 48L E-TSSOP 28L