2x15W Stereo Class-D Audio Amplifier with Power Limit

Features

- Single supply voltage
  4.5V ~ 14.4V for loudspeaker driver
  Built-in LDO output 5.5V for others
- Loudspeaker power from 12V supply
  BTL Mode: 8W/CH into 8Ω @1% THD+N
  BTL Mode: 10W/CH into 6Ω @<1% THD+N
  BTL Mode: 12W/CH into 4Ω @<1% THD+N
  PBTL Mode: 16W/CH into 4Ω @1% THD+N
- Loudspeaker power from 12V supply
  BTL Mode: 10W/CH into 8Ω @10% THD+N
  BTL Mode: 13W/CH into 6Ω @10% THD+N
  BTL Mode: 15W/CH into 4Ω@10% THD+N
  PBTL Mode: 20W/CH into 4Ω @10% THD+N
- 93% efficient Class-D operation eliminates need for heat sink
- Differential inputs
- Internal oscillator
- Short-Circuit protection with auto recovery option
- Under-Voltage detection
- Over-Voltage protection
- Pop noise and click noise reduction
- Adjustable power limit function for speaker protection
- Output DC detection for speaker protection
- Filter-Free operation
- Over temperature protection with auto recovery
- Superior EMC performance

Applications

- TV audio
- Boom-Box
- Powered speaker
- Monitors
- Consumer Audio Equipment

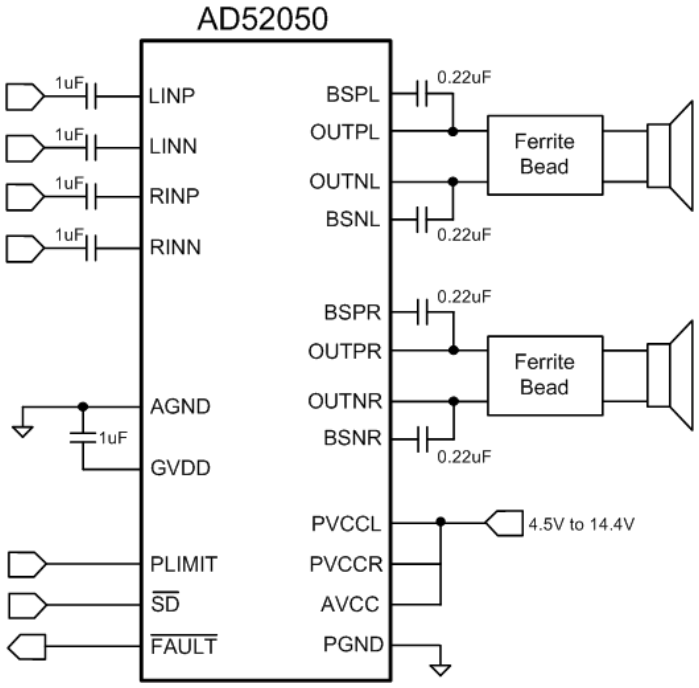
Description

The AD52050 is a high efficiency stereo class-D audio amplifier with adjustable power limit function. The loudspeaker driver operates from 4.5V~14.4V supply voltage. It can deliver 15W/CH output power into 4Ω loudspeaker within 10% THD+N at 12V supply voltage and without external heat sink when playing music.

The adjustable power limit function allows user to set a voltage rail lower than half of 5.5V to limit the amount of current through the speaker.

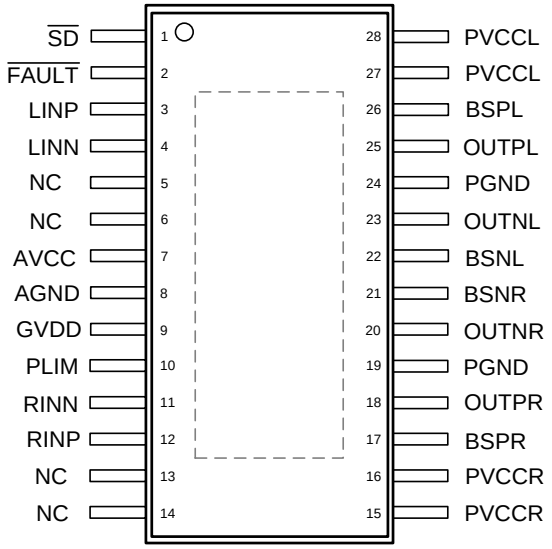
Output DC detection prevents speaker damage from long-time current stress. AD52050 provides superior EMC performance for filter-free application. The output short circuit and over temperature protection include auto-recovery feature.

Simplified Application Circuit

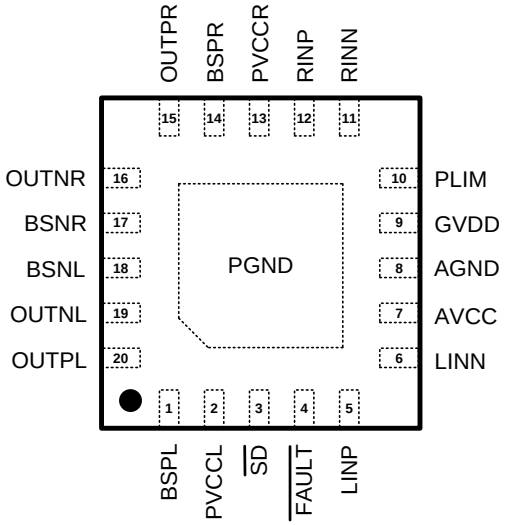


Pin Assignments

E-TSSOP-28L
(TOP VIEW)



TQFN 20L (4mmx4mm)
(Top VIEW)



Pin Description

NAME	E-TSSOP 28L	TQFN 20L	TYP	DESCRIPTION
$\overline{SD}$	1	3	I	Shutdown signal for IC (low = disabled, high = operational). Voltage compliance to AVCC.
$\overline{FAULT}$	2	4	O	Open drain output used to display short circuit or dc detect fault. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{FAULT}$ pin to $\overline{SD}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling AVCC.
LINP	3	5	I	Positive audio input for left channel.
LINN	4	6	I	Negative audio input for left channel.
NC	5	N/A	N/A	NC pin
NC	6	N/A	N/A	NC pin
AVCC	7	7	P	Analog supply.
AGND	8	8	P	Analog signal ground. Connect to the thermal pad.
GVDD	9	9	O	5.5V regulated output, also used as supply for PLIMIT function.
PLIMIT	10	10	I	Power limit level adjustment. Connect a resistor divider from GVDD to GND to set power limit. Give V(PLIMIT) <2.4V to set power limit level. Connect to GVDD (>2.4V) or GND to disable power limit function.
RINN	11	11	I	Negative audio input for right channel.
RINP	12	12	I	Positive audio input for right channel.
NC	13	N/A	N/A	NC pin

NC	14	N/A	N/A	NC pin
PVCCR	15,16	13	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
BSPR	17	14	I	Bootstrap I/O for right channel, positive high side FET.
OUTPR	18	15	O	Class-D H-bridge positive output for right channel.
PGND	19	Exposed pad	P	Power ground for the H-bridges.
OUTNR	20	16	O	Class-D H-bridge negative output for right channel.
BSNR	21	17	I	Bootstrap I/O for right channel, negative high side FET.
BSNL	22	18	I	Bootstrap I/O for left channel, negative high side FET.
OUTNL	23	19	O	Class-D H-bridge negative output for left channel.
PGND	24	Exposed pad	P	Power ground for the H-bridges.
OUTPL	25	20	O	Class-D H-bridge positive output for left channel.
BSPL	26	1	I	Bootstrap I/O for left channel, positive high side FET.
PVCCL	27,28	2	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
Thermal Pad		PGND	P	Must be soldered to PCB's ground plane.

Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD52050-26QG28NRR	E-TSSOP 28L	2500 Units / Reel 2500 Units / Small Box	Green
AD52050-26HI20NRR	TQFN 20L (4mm x 4mm)	3000 Units / Reel 6000 Units / Small Box	Green

Available Package

Package Type	Device No.	θ_{JA}(℃/W)	θ_{JT}(℃/W)	Ψ_{JT}(℃/W)	Exposed Thermal Pad
E-TSSOP 28L	AD52050	28	27.1	1.33	Yes (Note 1)
TQFN 20L		46	52.8	1.3	

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is necessary.

Note 1.2: θ_{JA} is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is simulated using the JEDEC51-5 thermal measurement standard.

Note 1.3: θ_{JT} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.

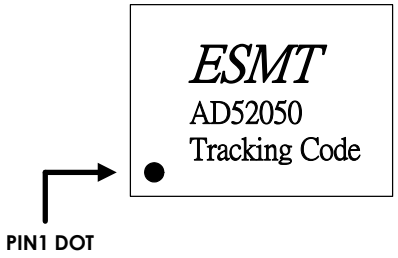
Note 1.4: Ψ_{JT} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtainingθ_{JA}, using a procedure described in JESD51-5.

Marking Information

AD52050

- Marking Information

Line 1：LOGO
Line 2：Product No
Line 3：Tracking Code



Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
PVCC	Supply voltage	PVCCL, PVCCR, AVCC	-0.3	16	V
V_I	Interface pin voltage	$\overline{SD}$, $\overline{FAULT}$	-0.3	16	V
		PLIM	-0.3	5.5	
T_A	Operating free-air temperature range		-40	85	°C
T_J	Operating junction temperature range		-40	150	°C
T_{stg}	Storage temperature range		-65	150	°C
R_L	Minimum Load Resistance		3.2		Ω

Recommended Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
PVCC	Supply voltage	PVCCL, PVCCR, AVCC	4.5	14.4	V
V_I	Signal input level voltage	LINP, LINN, RINP, RINN		2	Vrms
V_{IH}	High-level input voltage	$\overline{SD}$	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$		0.8	V
V_{OL}	Low-level output voltage	$\overline{FAULT}$, $R_{PULL-UP}$=100k, V_{CC}=16V		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, VI=2V, PVCC=12V		50	uA
I_{IL}	Low-level input current	$\overline{SD}$, V_I=0.8V, PVCC=12V		5	uA
I_{OH}	High-level output current	V_I=2V, PVCC=12V		50	uA
I_{OL}	Low-level output current	V_I=0.8V, PVCC=12V		50	uA
T_A	Operating free-air		-40	85	°C

General Electrical Characteristics

- PVCC=12V, R_L=8Ω, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
$I_{CC(q)}$	Quiescent supply current	SD=2V, no load, PVCC=12V		8	12	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SD=0.8V, no load, PVCC=12V		< 12	25	uA
$R_{DS(on)}$	Drain-source on-state resistance-High side NMOS	PVCC=12V, Id=500mA, T_J=25 °C		220		mΩ
	Drain-source on-state resistance-Low side NMOS			220		mΩ
$\|V_{OS}\|$	Class-D output offset voltage (measured differential)	PVCC=12V V_I=0V, Gain=26dB		1.5	10	mV
t_{ON}	Turn-on time	SD=2V		90		ms
t_{OFF}	Turn-off time	SD=0.8V		2		μs
GVDD	Regulator output	I_{GVDD}=0.1mA	5.225	5.5	5.775	V
G	Gain	PVCC=12V, SD=2V	25	26	27	dB

Electrical Characteristics and Specifications of Loudspeaker Driver (BTL , Stereo)

- PVCC=12V, R_L=8Ω, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
P_O	Output power	THD+N=10%, f=1kHz, 8Ω		10		W
		THD+N=10%, f=1kHz, 6Ω		13		
		THD+N=10%, f=1kHz, 4Ω		15		
THD+N	Total harmonic distortion plus noise	PVCC=12V, R_L=8Ω, f=1kHz, P_O=5W (half-power)		0.03		%
		PVCC=12V, R_L=6Ω, f=1kHz, P_O=6.5W (half-power)		0.03		
		PVCC=12V, R_L=4Ω, f=1kHz, P_O=7.5W (half-power)		0.03		
SNR	Signal to noise ratio	Maximum output at THD+N<1%, f=1kHz, Gain=26dB, a-weighted		100		dB
V_n	Output integrated noise	F=20Hz ~ 20kHz, Gain=26dB, a-weighted filter, R_L=8Ω		90		μV
K_{SVR}	Power Supply Rejection Ratio	V_{ripple}=200mVpp at 1kHz, Gain=26dB, inputs ac-grounded		-70		dB
Crosstalk	Crosstalk	F=1kHz, V_O=1Vrms, Gain=26dB		-95		dB
f_{OSC}	Oscillator frequency		250	310	370	kHz
T_{SENSOR}	Thermal trip point			150		°C
	Thermal hysteresis			25		°C

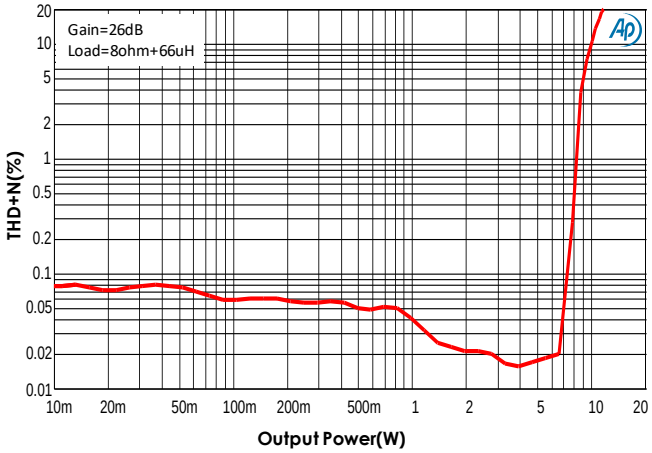
Electrical Characteristics and Specifications of Loudspeaker Driver (PBTL , Mono)

- PVCC=12V, R_L=4Ω, T_A=25°C (unless otherwise noted)

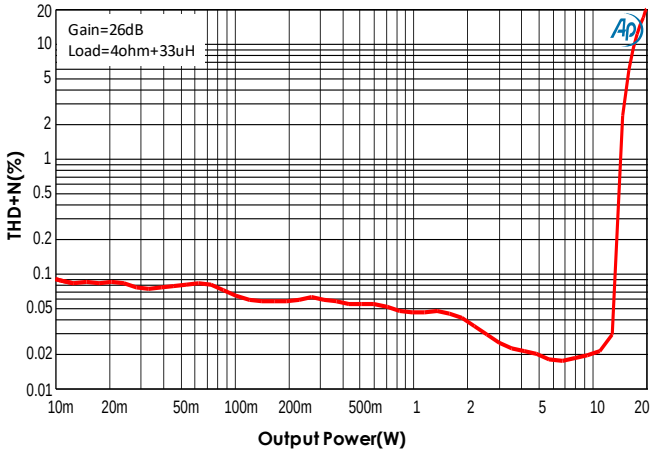
P_O	Output power	THD+N=1%, f=1kHz, 4Ω		16		W
		THD+N=10%, f=1kHz, 4Ω		20		
THD+N	Total harmonic distortion plus noise	PVCC=12V, R_L=4Ω, f=1kHz, P_O=10W		0.02		%
SNR	Signal to noise ratio	Maximum output at THD+N<1%, f=1kHz, Gain=26dB, a-weighted		96		dB
V_n	Output integrated noise	F=20Hz ~ 20kHz, Gain=26dB, a-weighted filter, R_L=8Ω		90		μV
K_{SVR}	Power Supply Rejection Ratio	V_{ripple}=200mVpp at 1kHz, Gain=26dB, inputs ac-grounded		-70		dB

Typical Characteristics

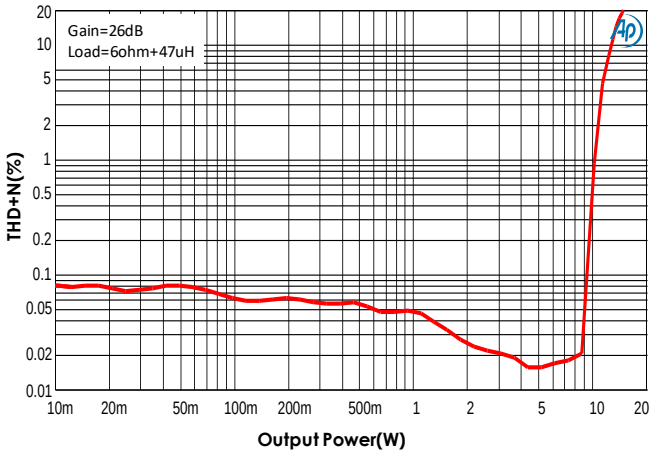
THD+N vs. Output Power, 8Ω load (Stereo)



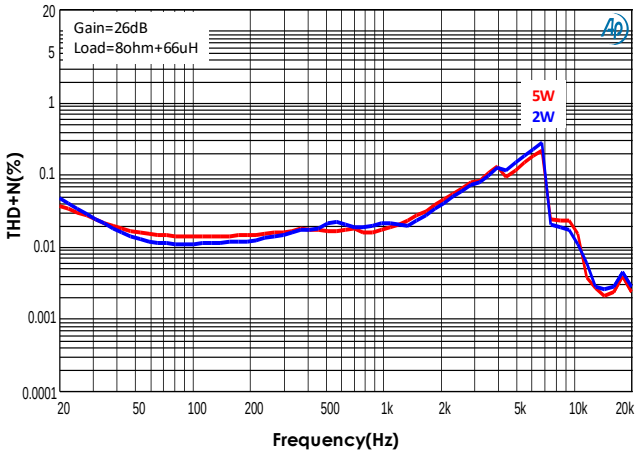
THD+N vs. Output Power, 4Ω load (Stereo)



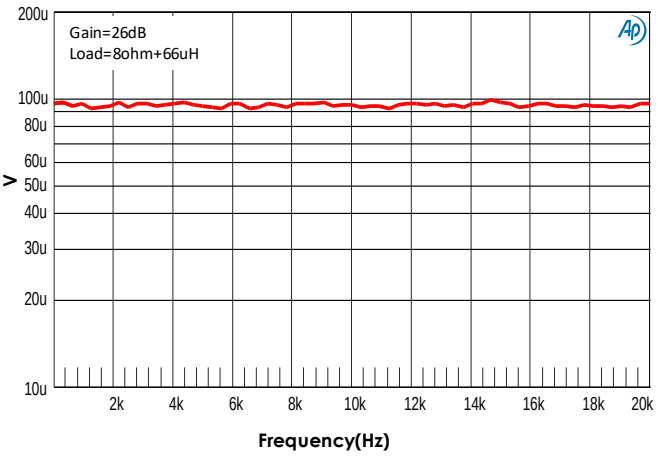
THD+N vs. Output Power, 6Ω load (Stereo)



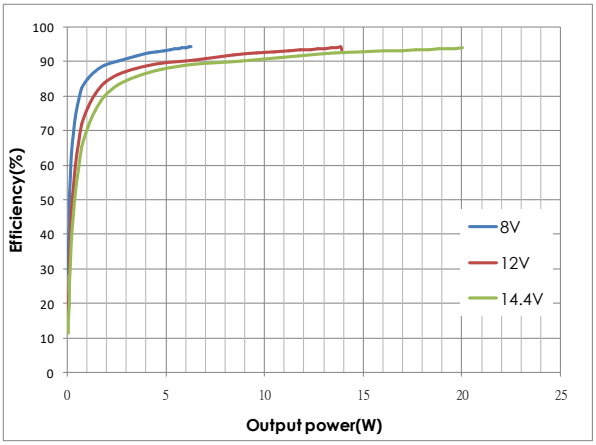
THD + N (%) vs. Frequency, 8Ω load (Stereo)



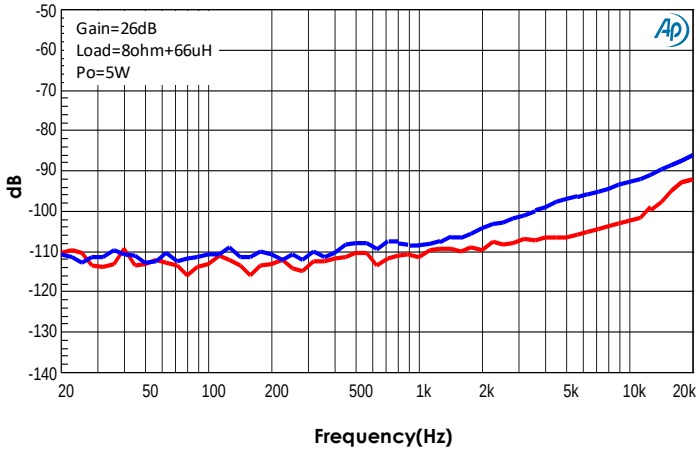
Noise, 8Ω load (Stereo)



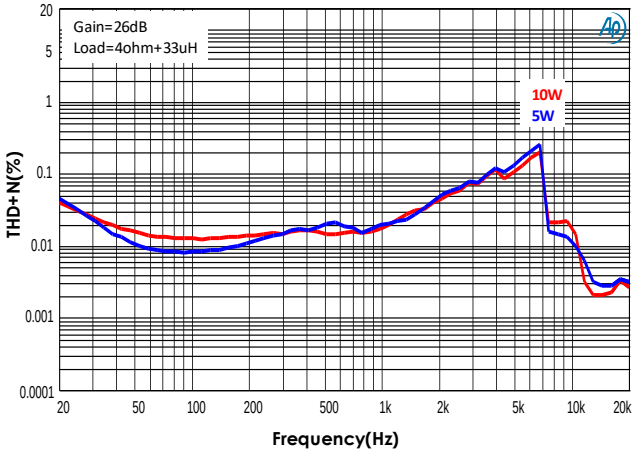
Efficiency (Stereo 8Ω load) / 2ch



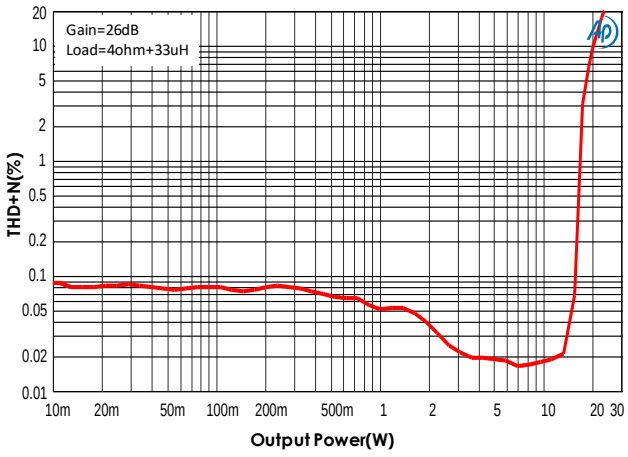
Cross-Talk ,8Ω load (Stereo)



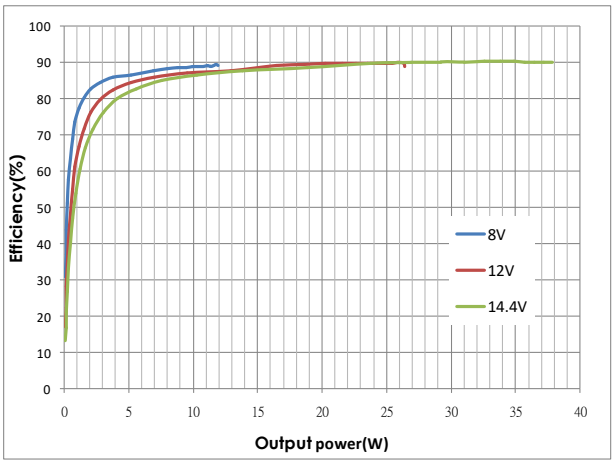
THD + N (%) vs. Frequency, 4Ω load (Mono)



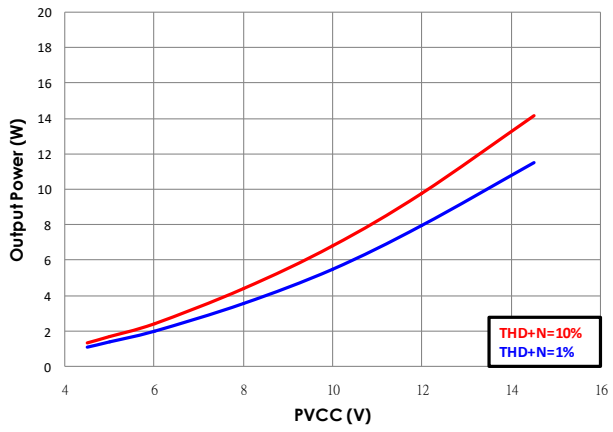
THD+N vs. Output Power, 4Ω load (Mono)



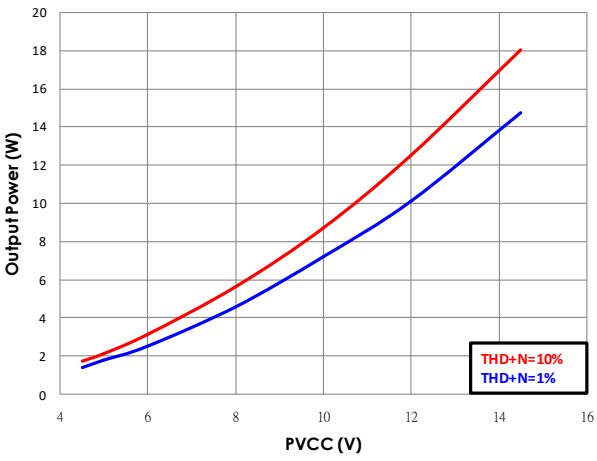
Efficiency (Mono 4Ω load)



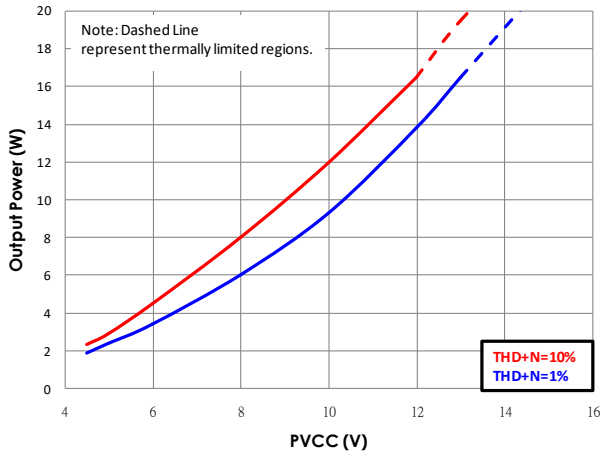
Supply voltage vs. Output Power, 8Ω load (Stereo)



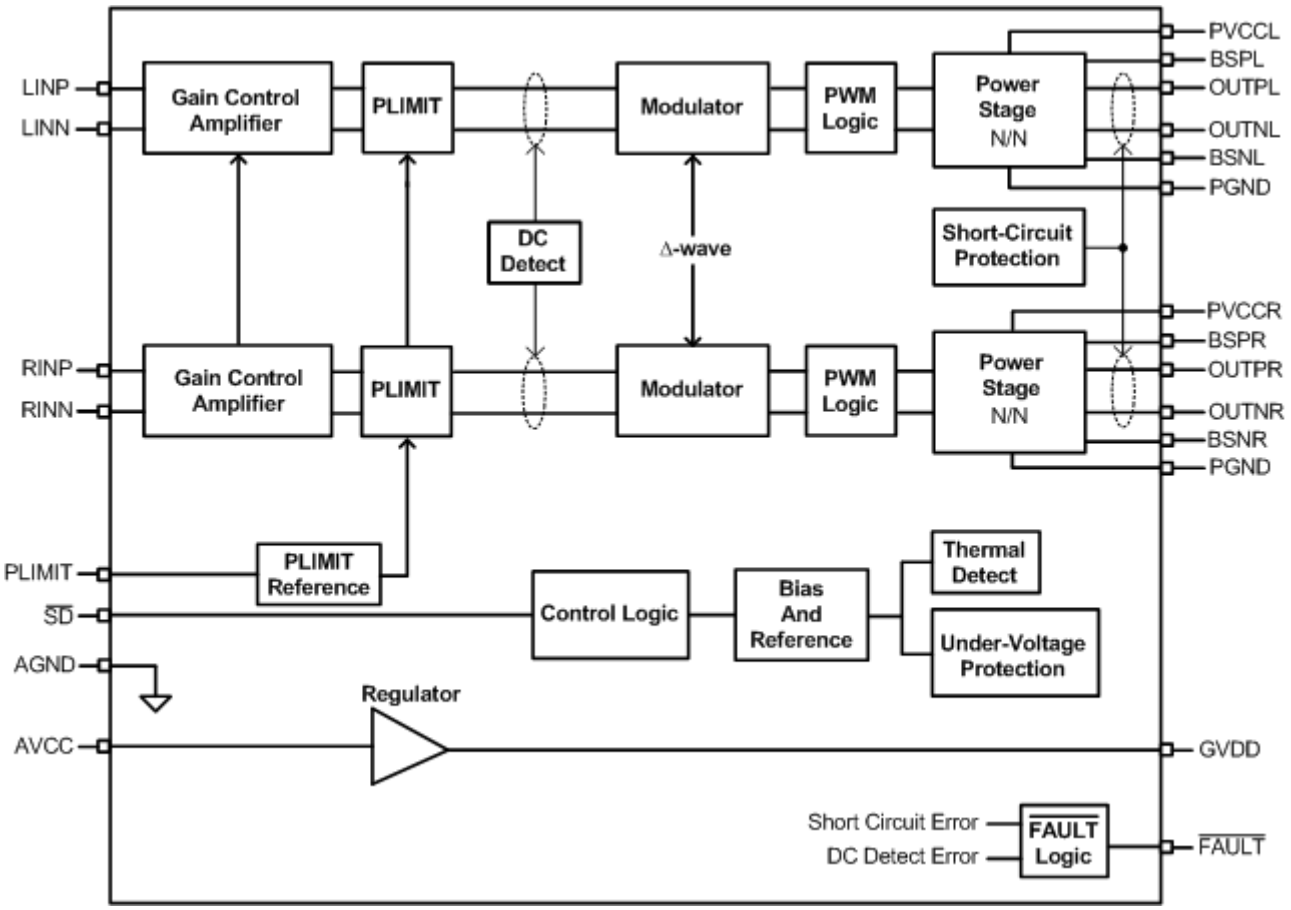
Supply voltage vs. Output Power, 6Ω load (Stereo)



Supply voltage vs. Output Power, 4Ω load (Stereo)



Functional Block Diagram



Operation Descriptions

- **Shutdown ($\overline{SD}$) control**

  Pulling $\overline{SD}$ pin low will let AD52050 operate in low-current state for power conservation. The AD52050 outputs will enter mute once $\overline{SD}$ pin is pulled low, and regulator will also disable to save power. If let $\overline{SD}$ pin floating, the chip will enter shutdown mode because of the internal pull low resistor. For the best power-off performance, place the chip in the shutdown mode in advance of removing the power supply.

- **DC detection**

  AD52050 has dc detection circuit to protect the speakers from DC current which might be occurred as input capacitor defect or inputs short on printed circuit board. The detection circuit detects first volume amplifier stage output, when both differential outputs' voltage become higher than a determined voltage or lower than a determined voltage for more than 420ms, the dc detect error will occur and report to $\overline{FAULT}$ pin. At the same time, loudspeaker drivers of right/left channel will disable and enter Hi-Z. This fault can not be cleared by cycling $\overline{SD}$, it is necessary to cycle the PVCC supply.

  The minimum differential input voltages required to trigger the DC detect function are shown in table1. The input voltage must keep above the voltage listed in the table for more than 420msec to trigger the DC detect fault. The equivalent class-D output duty of the DC detect threshold is listed in table2.

Table 1. DC Detect Threshold

AV (dB)	Vin (mV, differential)
26	125

Table 2. Output DC Detect Duty (for Either Channel)

PVCC (V)	Output Duty Exceeds
8	20.8%
12	20.8%

- **Thermal protection**

  If the internal junction temperature is higher than 150°C, the outputs of loudspeaker drivers will be disabled and at low state. The temperature for AD52050 returning to normal operation is about 125°C. The variation of protected temperature is about 10%. Thermal protection faults are NOT reported on the $\overline{\text{FAULT}}$ pin.

- **Short-circuit protection**

  To protect loudspeaker drivers from over-current damage, AD52050 has built-in short-circuit protection circuit. When the wires connected to loudspeakers are shorted to each other or shorted to VSS or to PVCC, overload detectors may activate. Once one of right and left channel overload detectors are active, the amplifier outputs will enter a Hi-Z state and the protection latch is engaged. The short protection fault is reported on $\overline{\text{FAULT}}$ pin as a low state. The latch can be cleared by reset $\overline{\text{SD}}$ or power supply cycling.

  The short circuit protection latch can have auto-recovery function by connect the $\overline{\text{FAULT}}$ pin directly to $\overline{\text{SD}}$ pin. The latch state will be released after 420msec, and the short protection latch will re-cycle if output overload is detected again.

- **Under-voltage detection**

  When the GVDD voltage is lower than 2.8V or the AVCC voltage is lower than 4V, loudspeaker drivers of right/left channel will be disabled and kept at low state. Otherwise, AD52050 return to normal operation.

- **PBTL (Mono) function**

  AD52050 provides the application of parallel BTL operation with two outputs of each channel connected directly. If connect INPL and INNL directly to Ground (without capacitors) this sets the device in Mono mode during power up. Connect OUTPR and OUTNR together for the positive speaker terminal and OUTNL and OUTPL together for the negative pin. Analog input signal is applied to INPR and INNR.

- **Over-voltage protection**

  When the PVCC voltage is higher than 15.5V, loudspeaker will be disabled kept at low state. The protection status will be released as PVCC lower than 15V.

- **Power limit function**
  - The voltage at PLIMIT pin can used to limit the power of first gain control amplifier output. Add a resistor divider from GVDD to ground to set the voltage V_{PLIMIT} at the PLIMIT pin. The voltage V_{PLIMIT} sets a limit on the output peak-to-peak voltage. PLIMIT is adjustable from 1.46V~2.75V.

For normal BTL operation (Stereo) operation:

$$Po@1\% = \frac{\left[\frac{2.75V - P_{LIMIT}}{2.1V + 0.89 \times P_{LIMIT}} \times 2 \times PVDD \times (1.23 - 0.0076 \times PVDD)\right]^2}{2 \times R_L}$$

$$Po@10\% = (Po@1\%) \times (1.2 + 0.02 \times PVDD)$$

Connect PLIMIT pin to ground or GVDD to disable power limit function. The output variation during power limit feature enable may have +-20% variation due to process window.

Table 3. BTL PLIMIT Typical Operation Ⅰ

Test Conditions	Output P_O (W)	V_{PLIMIT} (V) @ THD+N=10%
PVCC=12V RL=8Ω	3	1.941
	5	1.752
	8	1.55
	9	1.495

Table 3.1 PBTL PLIMIT Typical Operation Ⅱ

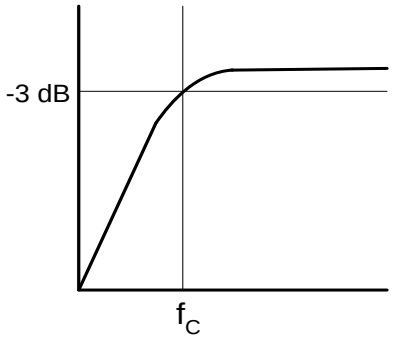
Test Conditions	Output P_O (W)	V_{PLIMIT} (V) @ THD+N=10%
PVCC=12V RL=4Ω	6	1.941
	10	1.752
	12	1.676
	16	1.55

Application information

- **Input capacitors (C_{in})**

  The performance at low frequency (bass) is affected by the corner frequency (f_c) of the high-pass filter composed of input resistor (R_{in}) and input capacitor (C_{in}), determined in equation (2). Typically, a 0.1μF or 1μF ceramic capacitor is suggested for C_{in}. The resistance of input resistors is 30kΩ at gain +26dB setting in AD52050. However, there is 20% variation in input resistance from production variation.

$$f_c = \frac{1}{2\pi R_{in} C_{in}} \ (\text{Hz}) \quad \cdots\cdots\cdots (2)$$



- **Ferrite Bead selection**

  If the traces from the AD52050 to speaker are short, the ferrite bead filters can reduce the high frequency emissions to meet FCC requirements. A ferrite bead that has very low impedance at low frequency and high impedance at high frequency (above 1MHz) is recommended. The impedance of the ferrite bead can be used along with a small capacitor with a value around 1000pF to reduce the frequency spectrum of the signal to an acceptable level.

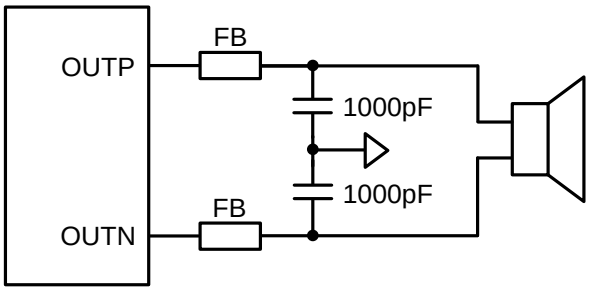


Figure 2. Typical Ferrite Bead Filter

- **Output LC Filter**

  If the traces from the AD52050 to speaker are not short, it is recommended to add the output LC filter to eliminate the high frequency emissions. Figure 3 shows the typical output filter for 8Ω speaker with a cut-off frequency of 27 kHz and Figure 4 shows the typical output filter for 4Ω speaker with a cut-off frequency of 27 kHz.

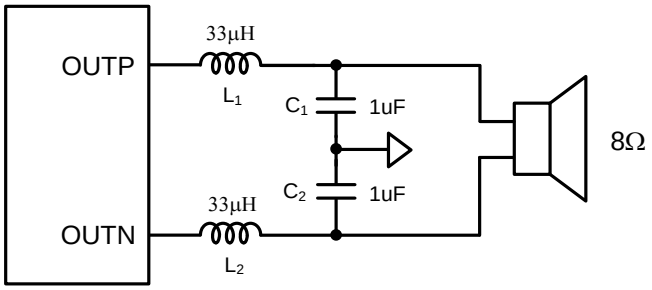


Figure 3. Typical LC Output Filter for 8Ω Speaker

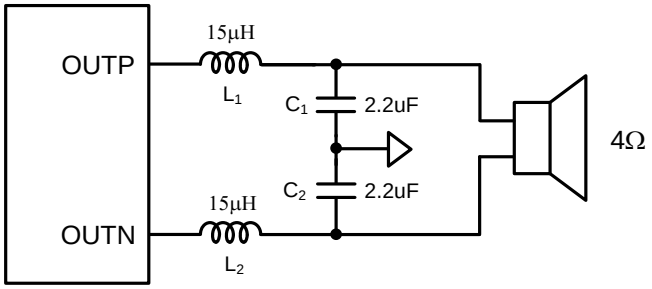


Figure 4. Typical LC Output Filter for 4Ω Speaker

- **Power supply decoupling capacitor (Cs)**

  Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to PVCC and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1000pF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1μF or 1μF as close as possible to the device PVCC leads works best. For low frequency noise filtering, a 100μF or greater capacitor (tantalum or electrolytic type) is suggested.

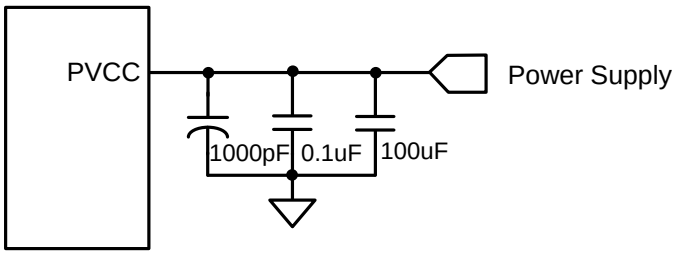
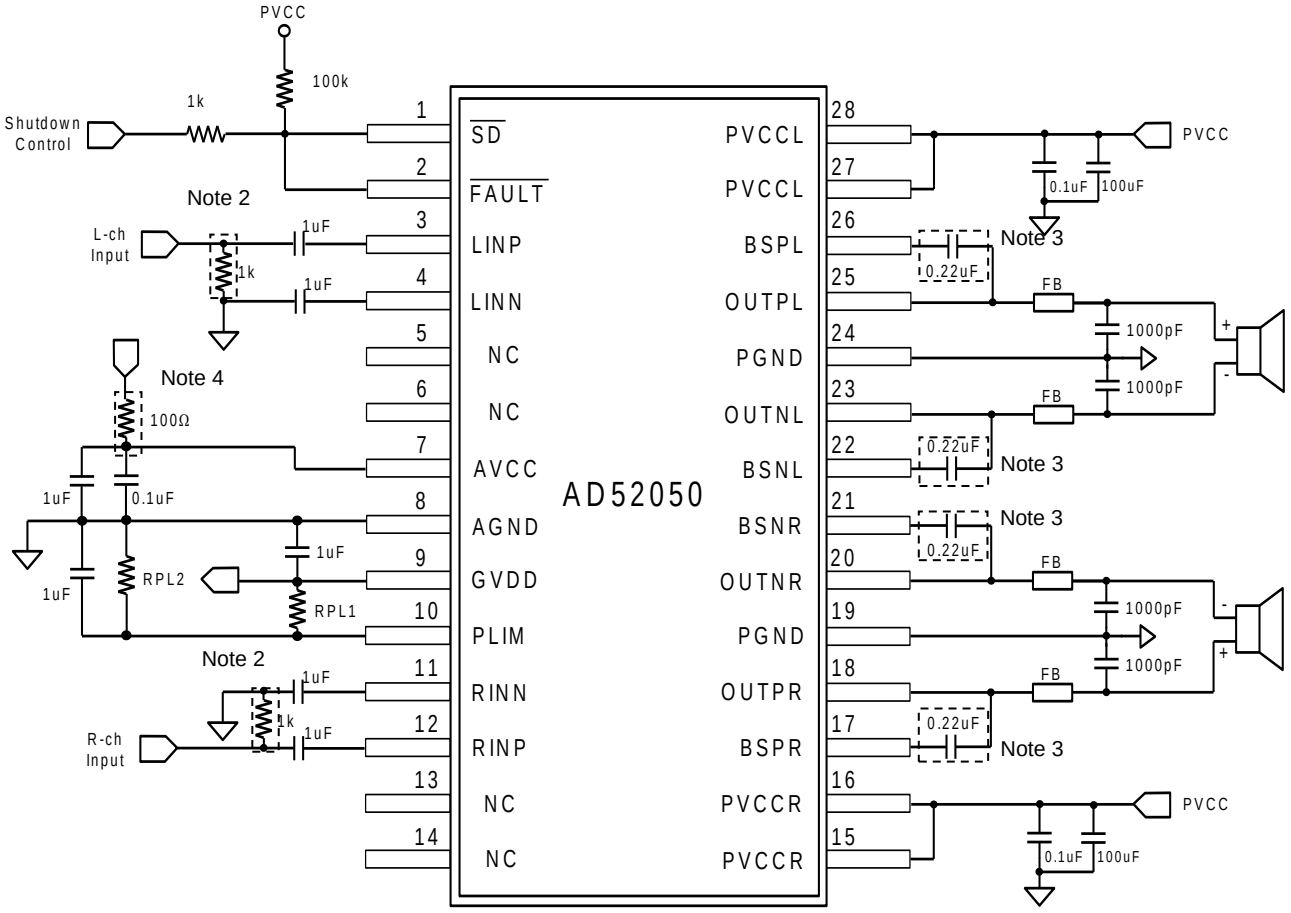


Figure 5. Recommended Power Supply Decoupling Capacitors.

Application Circuit Example

- Application circuit for BTL (Stereo) mode configuration and Single-Ended Input



Note : These resistances must be connected to ground, resistance=1Kohm

Note 2: These resistances must be connected to ground, resistance=1Kohm.

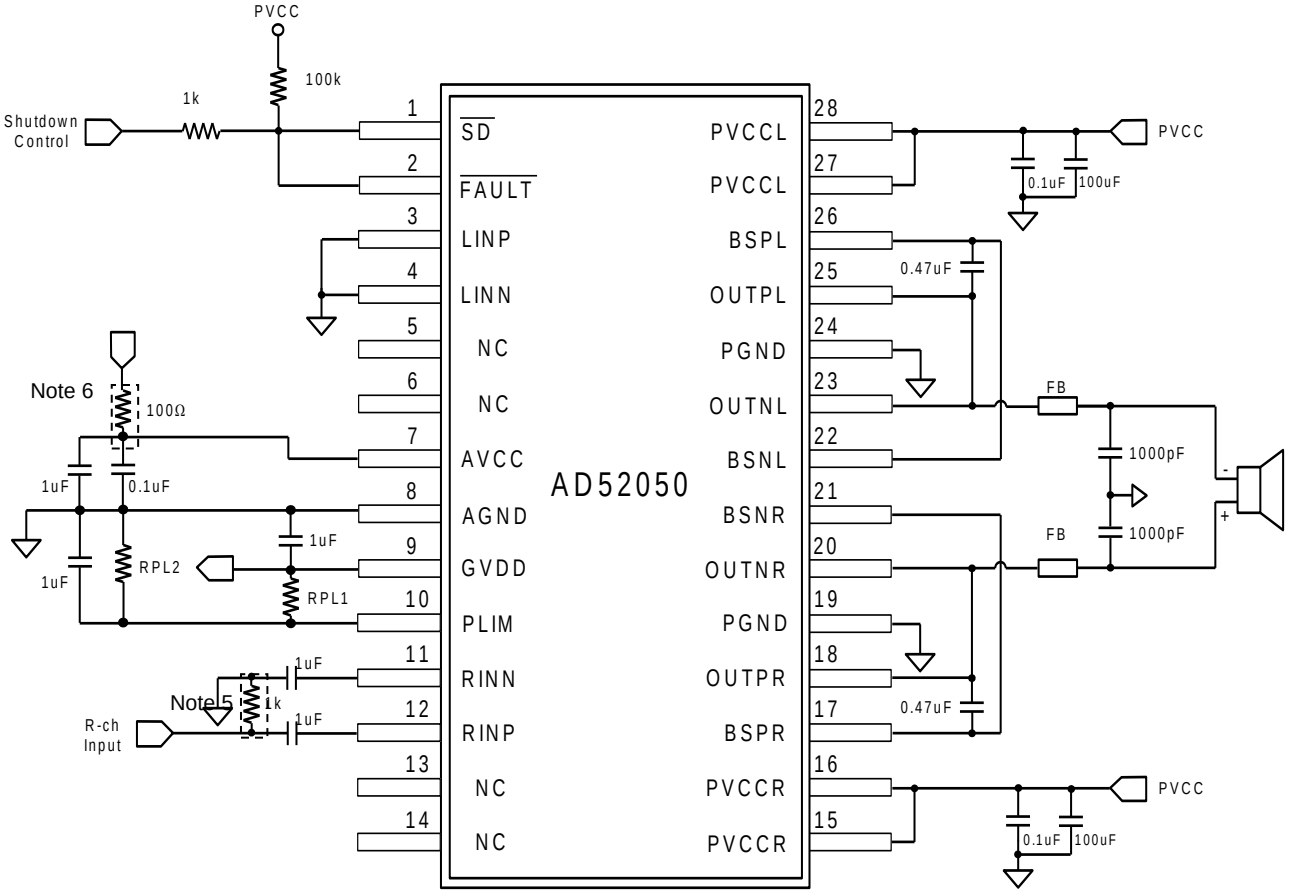
Note 3: These capacitors should be change to 0.47uF, while the PVCC<=5V.

Note 4: The under-voltage threshold for AVCC could be adjusted by R_{AVCC}, the formula will be followed

$R_{AVCC} \leq \frac{AVCC-4}{30} \ (K\Omega)$, R_{AVCC}=100ohm minimum is requirement in AD52050.

Application Circuit Example

- Application circuit for parallel BTL (Mono) mode configuration and Single-Ended Input



Note. Be noted that input should be applied on R-Channel only for Mono application.

Note 5: These resistances must be connected to ground, resistance=1Kohm.

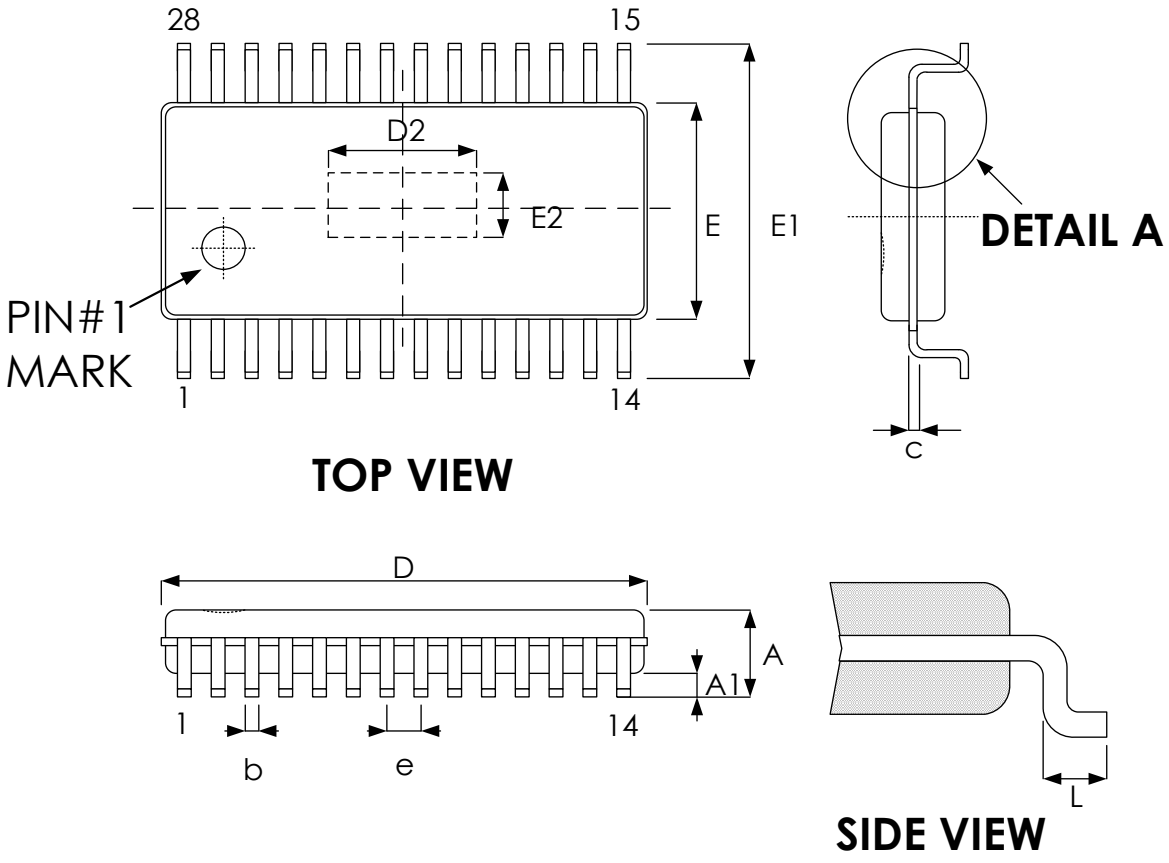
Note 6: The under-voltage threshold for AVCC could be adjusted by R_{AVCC}, the formula will be followed

$R_{AVCC} \leq \frac{AVCC-4}{30} \ (K\Omega)$, R_{AVCC}=100ohm minimum is requirement in AD52050.

Note 7: Be noted that input should be applied on R-channel only for Mono application

Package Dimensions

- **E-TSSOP 28L (173 mil)**



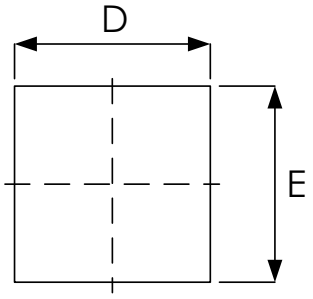
Symbol	Dimension in mm	
	Min	Max
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

Exposed pad

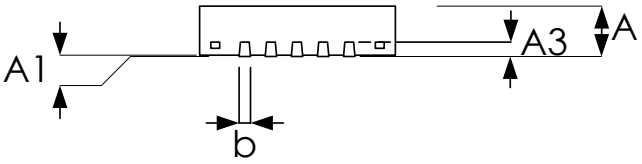
	Dimension in mm	
	Min	Max
D2	5.00	6.40
E2	2.50	2.90

Package Dimensions

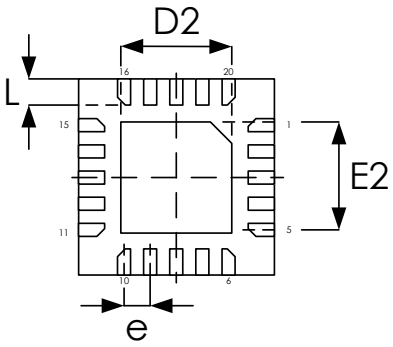
- **TQFN-20L (4mm x 4mm)**



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimension in mm	
	Min	Max
A	0.70	0.85
A1	0.00	0.05
A3	0.18	0.03
b	0.18	0.30
D	3.90	4.10
E	3.90	4.10
e	0.50 BSC	
L	0.30	0.50

	Dimention in mm	
	Min	Max
D2	1.90	2.05
E2	1.90	2.05

Revision History

Revision	Date	Description
0.1	2017.12.29	Initial version.
0.2	2018.07.24	Added TQFN 20L package option into.
0.3	2018.09.13	Update typical characteristics.
1.0	2019.03.21	1.Remove “Preliminary” reversion to 1.0, modify Package Dimensions 2.Modify gain spec & order information
1.1	2020.01.09	Update operation descriptions for under-voltage detection. Update application circuit.
1.2	2020.12.07	Update application information. Update application circuit (added R_{AVCC} node).

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