Quad Channel, 256-Position, SPI, Nonvolatile Digital Potentiometer

Enhanced Product

AD5144-EP

FEATURES

- 10 kΩ resistance option
- Resistor tolerance: 8% maximum
- Maximum continuous current: ±6 mA at R_{AB} = 10 kΩ
- Low resistance temperature coefficient: 35 ppm/°C typical
- Wide bandwidth: 3 MHz at R_{AB} = 10 kΩ
- Fast start-up time: 75 µs
- Linear gain setting mode
- Single- and dual-supply operation
- Independent V_{LOGIC}: 1.8 V to 5.5 V

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Product change notification
- Qualification data available on request

APPLICATIONS

- Missiles and munitions
- Avionics and unmanned systems
- Programmable filters, delays, and time constants
- Programmable power supplies

FUNCTIONAL BLOCK DIAGRAM

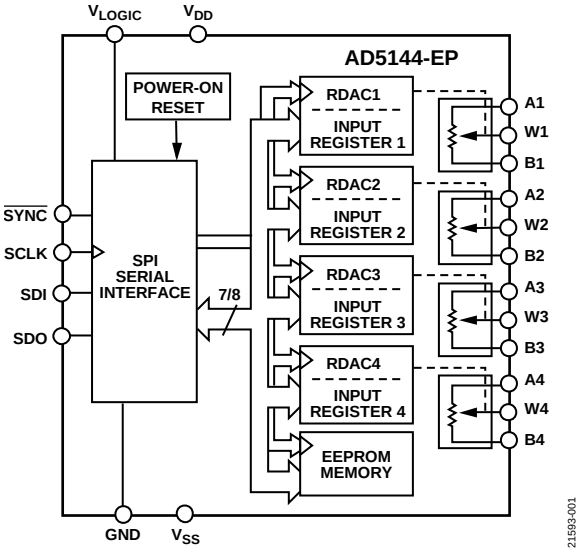

Figure 1.

GENERAL DESCRIPTION

The AD5144-EP potentiometer provides a nonvolatile solution for 256-position adjustment applications, offering guaranteed low resistor tolerance errors of ±8% and up to ±6 mA current density in the Ax, Bx, and Wx pins.

The low resistor tolerance and low nominal temperature coefficient simplify open-loop applications as well as applications requiring tolerance matching.

The linear gain setting mode allows independent programming of the resistance between the digital potentiometer terminals, through the Terminal A to Terminal W (R_{AW}) and the Terminal W to Terminal B (R_{WB}) string resistors, allowing accurate resistor matching.

The high bandwidth and low total harmonic distortion (THD) ensure optimal performance for ac signals, making this device suitable for filter design.

The low wiper resistance of 40 Ω at the ends of the resistor array allow for pin-to-pin connection.

The wiper values can be set through a serial peripheral interface (SPI) digital interface that is also used to read back the wiper register and electronically erasable programmable read-only memory (EEPROM) contents.

The AD5144-EP is available in a 20-lead TSSOP. The device is guaranteed to operate over the −55°C to +125°C temperature range.

Additional application and technical information can be found in the AD5144 data sheet.

Rev. A
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

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REVISION HISTORY

10/2019—Rev. 0 to Rev. A

Changes to Table 1 4

9/2019—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = 2.3 V to 5.5 V and V_{SS} = 0 V for the single-supply range, V_{DD} = 2.25 V to 2.75 V and V_{SS} = −2.25 V to −2.75 V for the dual-supply range, V_{LOGIC} = 1.8 V to 5.5 V, and −55°C < T_A < +125°C, unless otherwise noted. See the AD5144 data sheet for the test circuits that define the test conditions used in the Specifications section.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE (ALL RESISTIVE DIGITAL-TO-ANALOG CONVERTERS (RDACs))						
Resolution	N		8			Bits
Resistor Integral Nonlinearity[2]	R-INL	Terminal A and Terminal B resistor (R_{AB}) = 10 kΩ				
		V_{DD} ≥ 2.7 V	−2	±0.2	+2	LSB
		V_{DD} < 2.7 V	−5	±1.5	+5	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−0.5	±0.2	+0.5	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$		−8	±1	+8	%
Resistance Temperature Coefficient[3]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale		35		ppm/°C
Wiper Resistance[3]	R_W	Code = zero scale, R_{AB} = 10 kΩ		55	125	Ω
Bottom Scale or Top Scale	R_{BS} or R_{TS}	R_{AB} = 10 kΩ		40	80	Ω
Nominal Resistance Match	R_{AB1}/R_{AB2}	Code = 0xFF	−1	±0.2	+1	%
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (ALL RDACs)						
Integral Nonlinearity[4]	INL	R_{AB} = 10 kΩ	−1	±0.2	+1	LSB
Differential Nonlinearity[4]	DNL		−0.5	±0.2	+0.5	LSB
Full-Scale Error	V_{WFSE}	R_{AB} = 10 kΩ	−2.5	−0.1		LSB
Zero-Scale Error	V_{WZSE}	R_{AB} = 10 kΩ		1.2	3	LSB
Voltage Divider Temperature Coefficient[3]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		±5		ppm/°C
RESISTOR TERMINALS						
Maximum Continuous Current	I_A, I_B, and I_W					
		R_{AB} = 10 kΩ	−6		+6	mA
Terminal Voltage Range[5]			V_{SS}		V_{DD}	V
Capacitance A, Capacitance B[3]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale, R_{AB} = 10 kΩ		25		pF
Capacitance W[3]	C_W	f = 1 MHz, measured to GND, code = half scale, R_{AB} = 10 kΩ		12		pF
Common-Mode Leakage Current[3]		Terminal A voltage (V_A) = wiper terminal voltage (V_W) = Terminal B voltage (V_B)	−500	±15	+500	nA
DIGITAL INPUTS						
Input Logic[3]						
High	V_{INH}	V_{LOGIC} = 1.8 V to 2.3 V	0.8 × V_{LOGIC}			V
		V_{LOGIC} = 2.3 V to 5.5 V	0.7 × V_{LOGIC}			V
Low	V_{INL}				0.2 × V_{LOGIC}	V
Input Hysteresis[3]	V_{HYST}		0.1 × V_{LOGIC}			V
Input Current[3]	I_{IN}				±1	µA
Input Capacitance[3]	C_{IN}			5		pF

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DIGITAL OUTPUTS						
Output High Voltage[3]	V_{OH}	Pull-up resistor ($R_{PULL-UP}$) = 2.2 kΩ to V_{LOGIC}		V_{LOGIC}		V
Output Low Voltage[3]	V_{OL}	Sink current (I_{SINK}) = 3 mA			0.4	V
		I_{SINK} = 6 mA, V_{LOGIC} > 2.3 V			0.6	V
Three-State Leakage Current			−1		+1	μA
Three-State Output Capacitance				2		pF
POWER SUPPLIES						
Single-Supply Range		V_{SS} = GND	2.3		5.5	V
Dual-Supply Range			±2.25		±2.75	V
Logic Supply Range		Single supply, V_{SS} = GND	1.8		V_{DD}	V
		Dual supply, V_{SS} < GND	2.25		V_{DD}	V
Positive Supply Current	I_{DD}	V_{INH} = V_{LOGIC} or V_{INL} = GND				
		V_{DD} = 5.5 V		0.7	5.5	μA
		V_{DD} = 2.3 V		400		nA
Negative Supply Current	I_{SS}	V_{INH} = V_{LOGIC} or V_{INL} = GND	−5.5	−0.7		μA
EEPROM Store Current[3, 6]	$I_{DD\_EEPROM\_STORE}$	V_{INH} = V_{LOGIC} or V_{INL} = GND		2		mA
EEPROM Read Current[3, 7]	$I_{DD\_EEPROM\_READ}$	V_{INH} = V_{LOGIC} or V_{INL} = GND		320		μA
Logic Supply Current	I_{LOGIC}	V_{INH} = V_{LOGIC} or V_{INL} = GND		0.05	1.4	μA
Power Dissipation[8]	P_{DISS}	V_{INH} = V_{LOGIC} or V_{INL} = GND		3.5		μW
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD}/\Delta V_{SS}$ = V_{DD} ± 10%, code = full scale		−66	−60	dB
DYNAMIC CHARACTERISTICS[9]						
Bandwidth	BW	−3 dB, R_{AB} = 10 kΩ		3		MHz
Total Harmonic Distortion	THD	V_{DD}/V_{SS} = ±2.5 V, V_A = 1 V rms, V_B = 0 V, f = 1 kHz		−80		dB
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, f = 10 kHz, R_{AB} = 10 kΩ		7		nV/√Hz
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, from zero scale to full scale, ±0.5 LSB error band, R_{AB} = 10 kΩ		2		μs
Crosstalk (C_{W1}/C_{W2})	C_T	R_{AB} = 10 kΩ		10		nV-sec
Analog Crosstalk	C_{TA}			−90		dB
Endurance[10]		T_A = 25°C		1		Mcycles
		−40°C < T_A < +125°C	100			kcycles
Data Retention[11, 12]				50		Years

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V, V_{SS} = 0 V, and V_{LOGIC} = 5 V.
[2] Resistor integral nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. The maximum wiper current is limited to (0.7 × V_{DD})/R_{AB}.
[3] Guaranteed by design and characterization, not subject to production test.
[4] INL and DNL are measured across the Terminal W and Terminal B voltage (V_{WB}) with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment.
[6] $I_{DD\_EEPROM\_STORE}$ is different from the operating current. Supply current for EEPROM program lasts approximately 30 ms.
[7] $I_{DD\_EEPROM\_READ}$ is different from the operating current. Supply current for EEPROM read lasts approximately 20 μs.
[8] P_{DISS} is calculated from (I_{DD} × V_{DD}) + (I_{LOGIC} × V_{LOGIC}).
[9] All dynamic characteristics use V_{DD}/V_{SS} = ±2.5 V, and V_{LOGIC} = 2.5 V.
[10] Endurance is qualified per JEDEC Standard 22, Method A117 to 100,000 cycles measured at −40°C to +125°C.
[11] Retention lifetime equivalent at junction temperature (T_J) = 125°C per JEDEC Standard 22, Method A117. Retention lifetime based on an activation energy of 1 eV, derates with junction temperature in the Flash/EE memory.
[12] 50 years apply to an endurance of 1000 cycles. An endurance of 100,000 cycles has an equivalent retention lifetime of 5 years.

INTERFACE TIMING SPECIFICATIONS

V_{LOGIC} = 1.8 V to 5.5 V, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2. SPI Interface

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit	Description
t_1	V_{LOGIC} > 1.8 V	20			ns	SCLK cycle time
	V_{LOGIC} = 1.8 V	30			ns	
t_2	V_{LOGIC} > 1.8 V	10			ns	SCLK high time
	V_{LOGIC} = 1.8 V	15			ns	
t_3	V_{LOGIC} > 1.8 V	10			ns	SCLK low time
	V_{LOGIC} = 1.8 V	15			ns	
t_4		10			ns	$\overline{SYNC}$ to SCLK falling edge setup time
t_5		5			ns	Data setup time
t_6		5			ns	Data hold time
t_7		10			ns	$\overline{SYNC}$ rising edge to next SCLK fall ignored
t_8[2]		20			ns	Minimum $\overline{SYNC}$ high time
t_9[3]			50		ns	SCLK rising edge to SDO valid
t_{10}				500	ns	$\overline{SYNC}$ rising edge to SDO pin disable
$t_{POWER-UP}$				75	µs	Start-up time (not shown in Figure 3 and Figure 4)

[1] All input signals are specified with rising time (t_R) = falling time (t_F) = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[2] Refer to $t_{EEPROM\_PROGRAM}$ and $t_{EEPROM\_READBACK}$ for memory command operations (see the control pins table in the AD5144 data sheet for additional information).
[3] The pull-up resistance (R_{PULL_UP}) = 2.2 kΩ to V_{DD} with a capacitance load of 168 pF.

SHIFT REGISTER AND TIMING DIAGRAMS

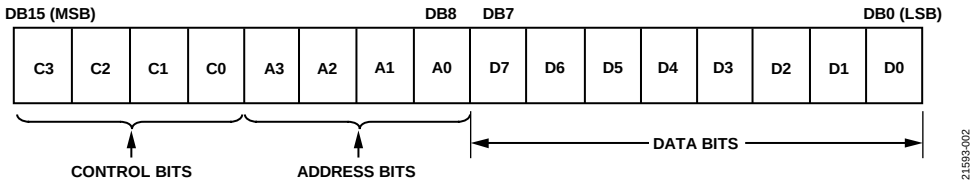

Figure 2. Input Shift Register Contents

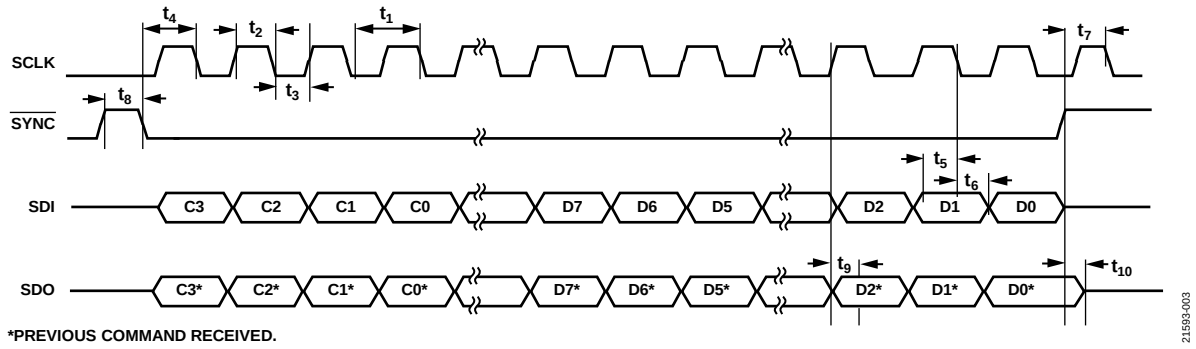

Figure 3. SPI Serial Interface Timing Diagram, CPOL = 0, CPHA = 1

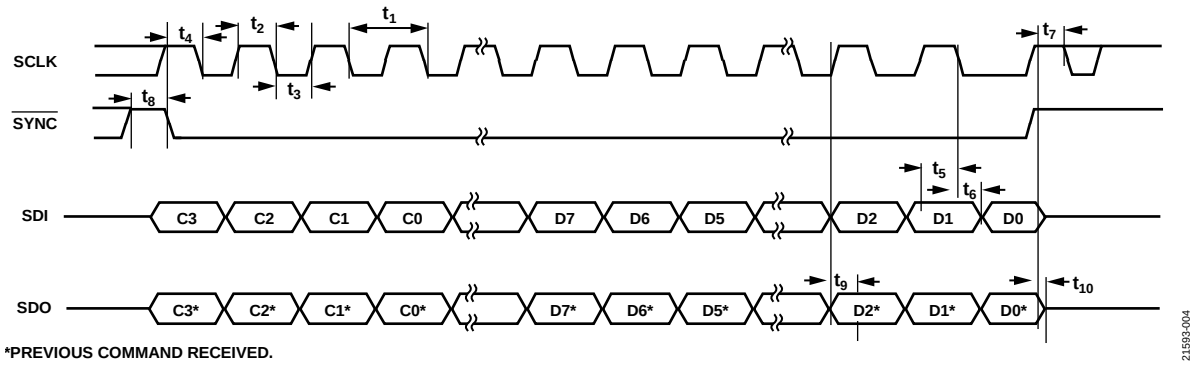

Figure 4. SPI Serial Interface Timing Diagram, CPOL = 1, CPHA = 0

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7.0 V
V_{SS} to GND	+0.3 V to −7.0 V
V_{DD} to V_{SS}	7 V
V_{LOGIC} to GND	−0.3 V to V_{DD} + 0.3 V or +7.0 V (whichever is less)
V_A, V_W, V_B to GND	V_{SS} − 0.3 V, V_{DD} + 0.3 V
I_A, I_W, I_B	
Pulsed[1], R_{AW} = 10 kΩ	
Frequency > 10 kHz	±6 mA/d[2]
Frequency ≤ 10 kHz	±6 mA/√d[2]
Digital Inputs	−0.3 V to V_{LOGIC} + 0.3 V or +7 V (whichever is less)
Operating Temperature Range, T_A[3]	−55°C to +125°C
Maximum Junction Temperature, T_J Maximum	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	(T_J max − T_A)/θ_{JA}
Field Induced Charged Device Model (FICDM)	1.5 kV

[1] The maximum terminal current is bounded by the maximum current handling of the switches, the maximum power dissipation of the package, and the maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] d = pulse duty factor.
[3] T_A includes programming of EEPROM memory.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure, and θ_{JC} is the junction to case thermal resistance measured at package top.

Table 4. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
RU-20	143	45	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board, still air (0 m/sec airflow). See JEDEC JESD-51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

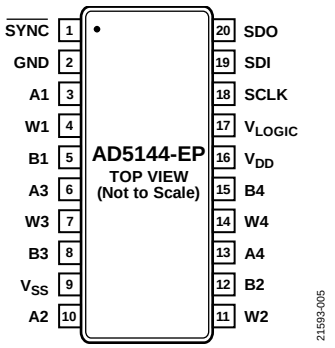

Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{SYNC}}$	Synchronization Data Input, Active Low. When $\overline{\text{SYNC}}$ returns high, data is loaded into the input shift register.
2	GND	Ground Pin, Logic Ground Reference.
3	A1	Terminal A of RDAC 1. $V_{SS} \le V_A \le V_{DD}$.
4	W1	Wiper Terminal of RDAC 1. $V_{SS} \le V_W \le V_{DD}$.
5	B1	Terminal B of RDAC 1. $V_{SS} \le V_B \le V_{DD}$.
6	A3	Terminal A of RDAC 3. $V_{SS} \le V_A \le V_{DD}$.
7	W3	Wiper Terminal of RDAC 3. $V_{SS} \le V_W \le V_{DD}$.
8	B3	Terminal B of RDAC 3. $V_{SS} \le V_B \le V_{DD}$.
9	V_{SS}	Negative Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
10	A2	Terminal A of RDAC 2. $V_{SS} \le V_A \le V_{DD}$.
11	W2	Wiper Terminal of RDAC 2. $V_{SS} \le V_W \le V_{DD}$.
12	B2	Terminal B of RDAC 2. $V_{SS} \le V_B \le V_{DD}$.
13	A4	Terminal A of RDAC 4. $V_{SS} \le V_A \le V_{DD}$.
14	W4	Wiper Terminal of RDAC 4. $V_{SS} \le V_W \le V_{DD}$.
15	B4	Terminal B of RDAC 4. $V_{SS} \le V_B \le V_{DD}$.
16	V_{DD}	Positive Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
17	V_{LOGIC}	Logic Power Supply, 1.8 V to V_{DD}. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
18	SCLK	Serial Clock Line. Data is clocked in at the logic low transition.
19	SDI	Serial Data Input.
20	SDO	Serial Data Output. SDO is an open-drain output pin that must have an external pull-up resistor.

TYPICAL PERFORMANCE CHARACTERISTICS

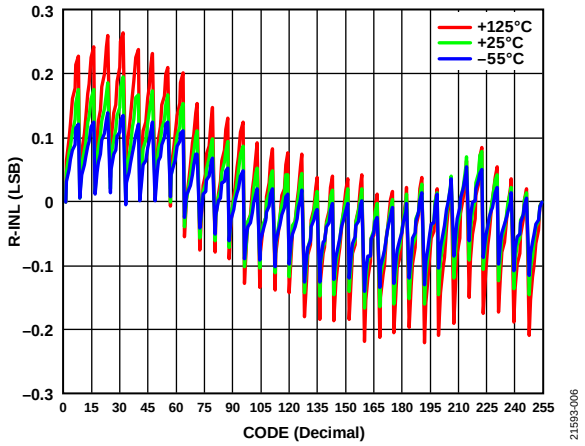

Figure 6. R-INL vs. Code for Various Temperatures

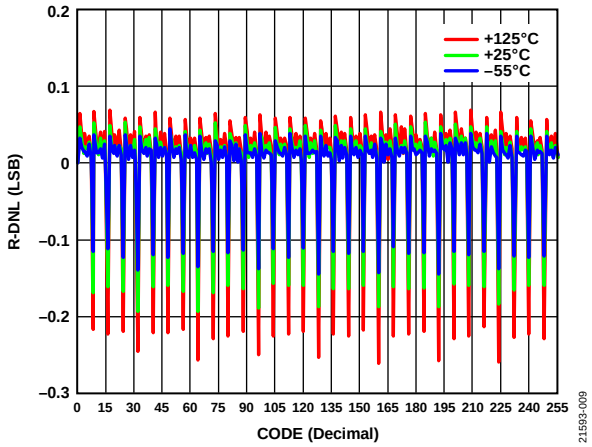

Figure 9. R-DNL vs. Code for Various Temperatures

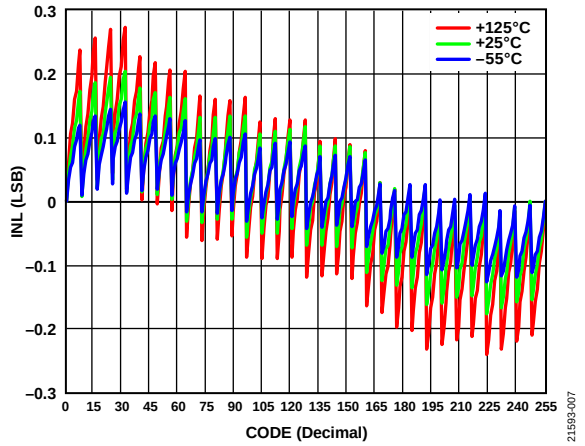

Figure 7. INL vs. Code for Various Temperatures

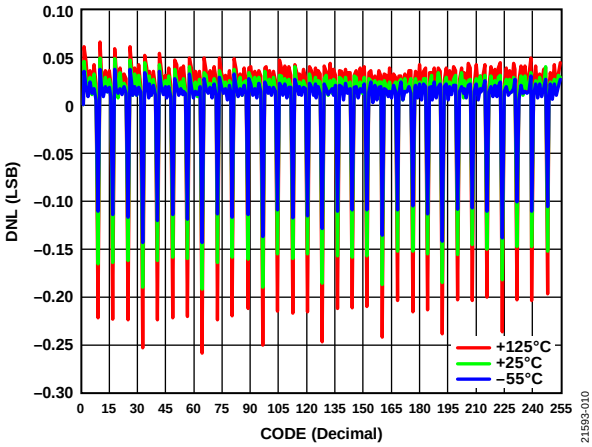

Figure 10. DNL vs. Code for Various Temperatures

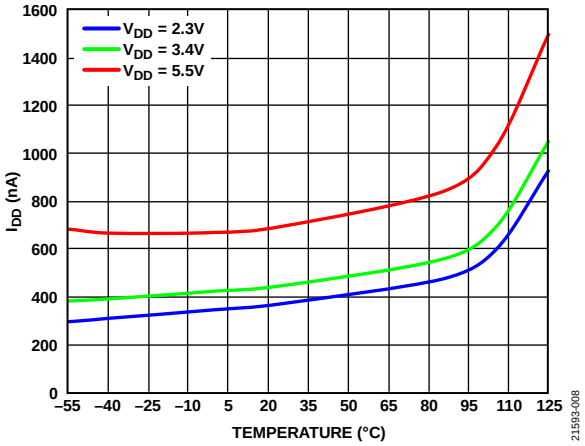

Figure 8. Supply Current (I_{DD}) vs. Temperature for Various Power Supplies

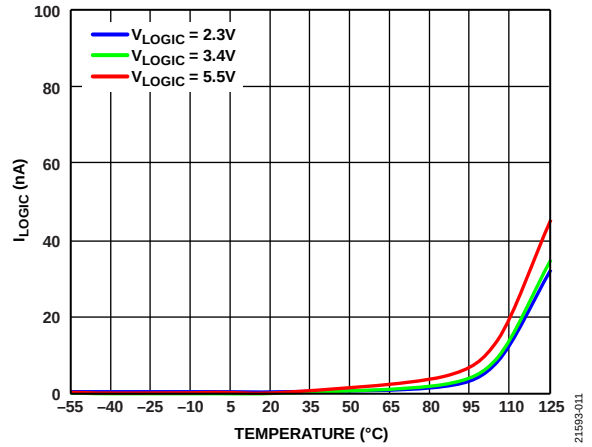

Figure 11. I_{LOGIC} vs Temperature for Various Logic Voltages

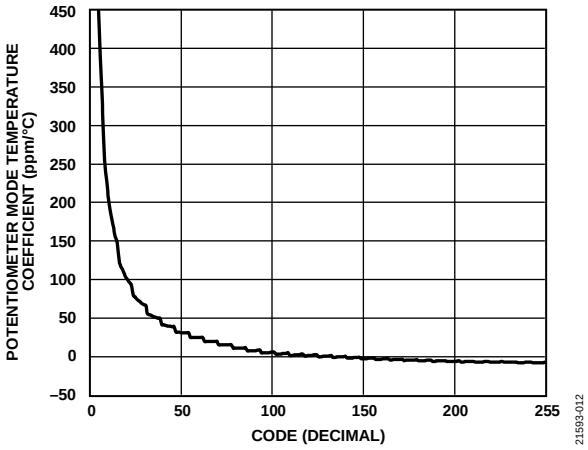

Figure 12. Potentiometer Mode Temperature Coefficient ($(\Delta V_W/V_W)/\Delta T \times 106$) vs. Code

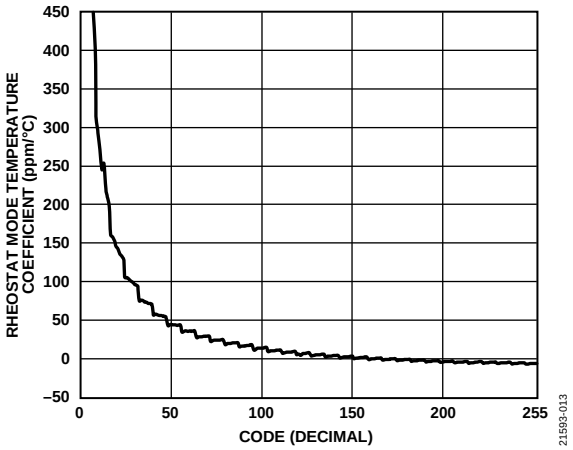

Figure 13. Rheostat Mode Temperature Coefficient ($(\Delta R_{WB}/R_{WB})/\Delta T \times 106$) vs. Code

OUTLINE DIMENSIONS

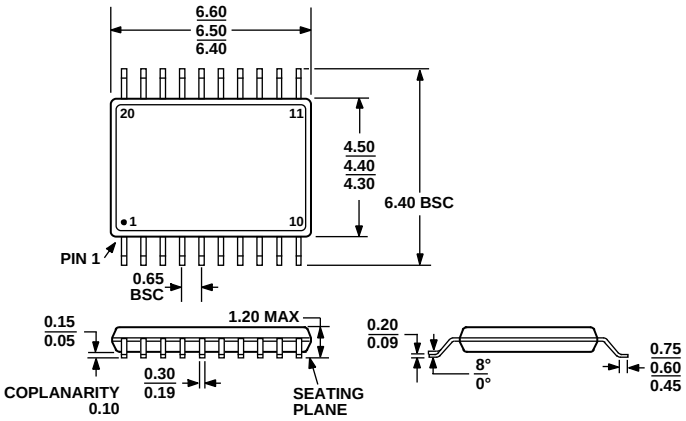

Figure 14. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	R_{AB} (kΩ)	Resolution	Interface	Temperature Range	Package Description	Package Option
AD5144TRUZ10-EP	10	256	SPI	−55°C to +125°C	20-Lead TSSOP	RU-20
AD5144TRUZ10-EP-R7	10	256	SPI	−55°C to +125°C	20-Lead TSSOP	RU-20

[1] Z = RoHS Compliant Part.