

IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

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Thank you for your cooperation and understanding,

WeEn Semiconductors



ACTT10X-800C

AC Thyristor Triac power switch

21 July 2014

Product data sheet

1. General description

Planar passivated AC Thyristor Triac power switch in a SOT186A (TO-220F) "full pack" plastic package with self-protective capabilities against low and high energy transients.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- Full cycle AC conduction
- Isolated mounting base package
- Less sensitive gate for high noise immunity
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Safe clamping capability for low energy over-voltage transients
- Self-protective turn-on during high energy voltage transients
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls
- Applications subject to high temperature

4. Quick reference data

Table 1. Quick reference data

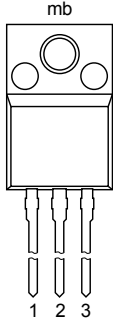

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	90	A
T_j	junction temperature		-	-	125	$^{\circ}\text{C}$
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 63\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	10	A



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PP}	peak pulse voltage	$T_j = 25\text{ }^{\circ}\text{C}$; non-repetitive, off-state; Fig. 6	-	-	2	kV
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 8	-	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 8	-	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD- G-; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 8	-	-	35	mA
V_{CL}	clamping voltage	$I_{CL} = 0.1\text{ mA}$; $t_p = 1\text{ ms}$; $T_j = 25\text{ }^{\circ}\text{C}$	850	-	-	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 125\text{ }^{\circ}\text{C}$; exponential waveform; gate open circuit	2000	-	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 125\text{ }^{\circ}\text{C}$; $I_{T(RMS)} = 10\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit	20	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>TO-220F (SOT186A)</p>	 <p>sym051</p>
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
ACTT10X-800C	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Marking

Table 4. Marking codes

Type number	Marking code
ACTT10X-800C	ACTT10X-800C

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_h \leq 63^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	10	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{j(init)}} = 25^\circ\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	90	A
		full sine wave; $T_{\text{j(init)}} = 25^\circ\text{C}$; $t_p = 16.7\text{ ms}$	-	99	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	40	A^2s
di_{T}/dt	rate of rise of on-state current	$I_{\text{T}} = 15\text{ A}$; $I_{\text{G}} = 0.2\text{ A}$; $di_{\text{G}}/dt = 0.2\text{ A}/\mu\text{s}$	-	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current	$t = 20\text{ }\mu\text{s}$	-	2	A
P_{GM}	peak gate power		-	5	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	$^\circ\text{C}$
T_{j}	junction temperature		-	125	$^\circ\text{C}$
V_{PP}	peak pulse voltage	$T_{\text{j}} = 25^\circ\text{C}$; non-repetitive, off-state; Fig. 6	-	2	kV

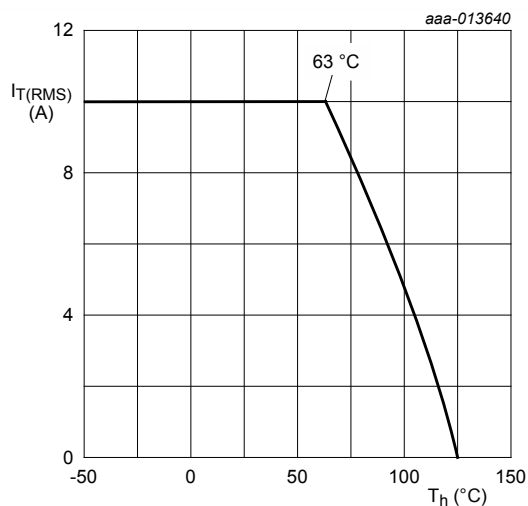
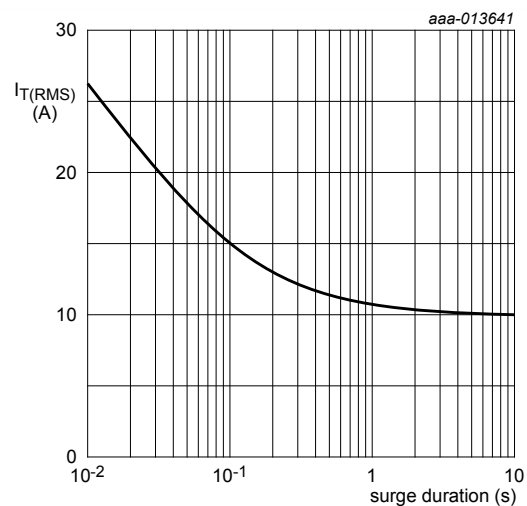


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values



$f = 50\text{ Hz}$; $T_h = 63^\circ\text{C}$

Fig. 2. RMS on-state current as a function of surge duration; maximum values

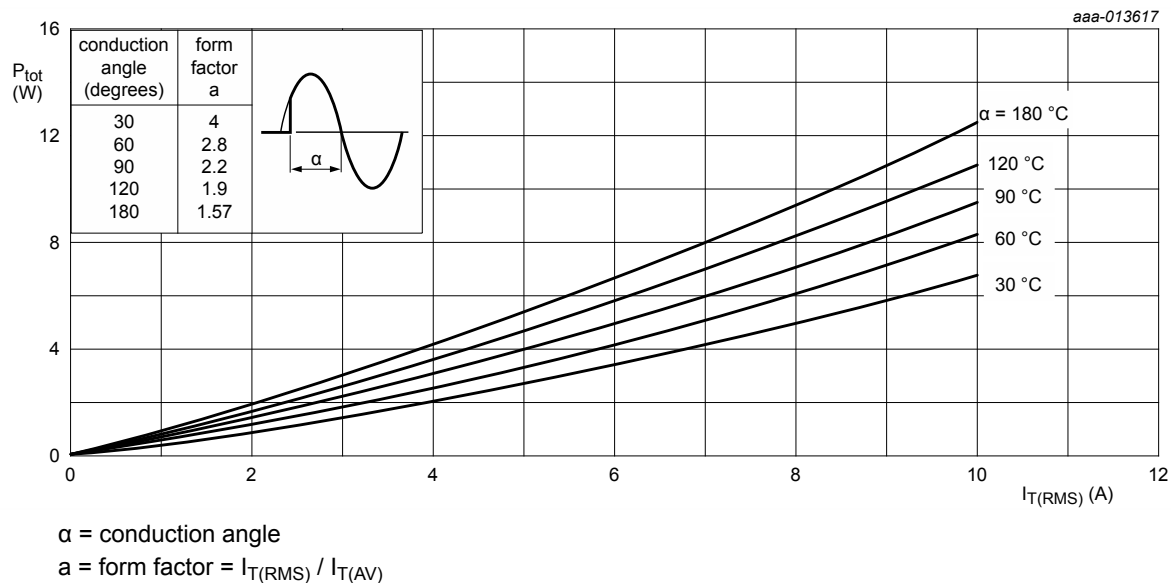


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

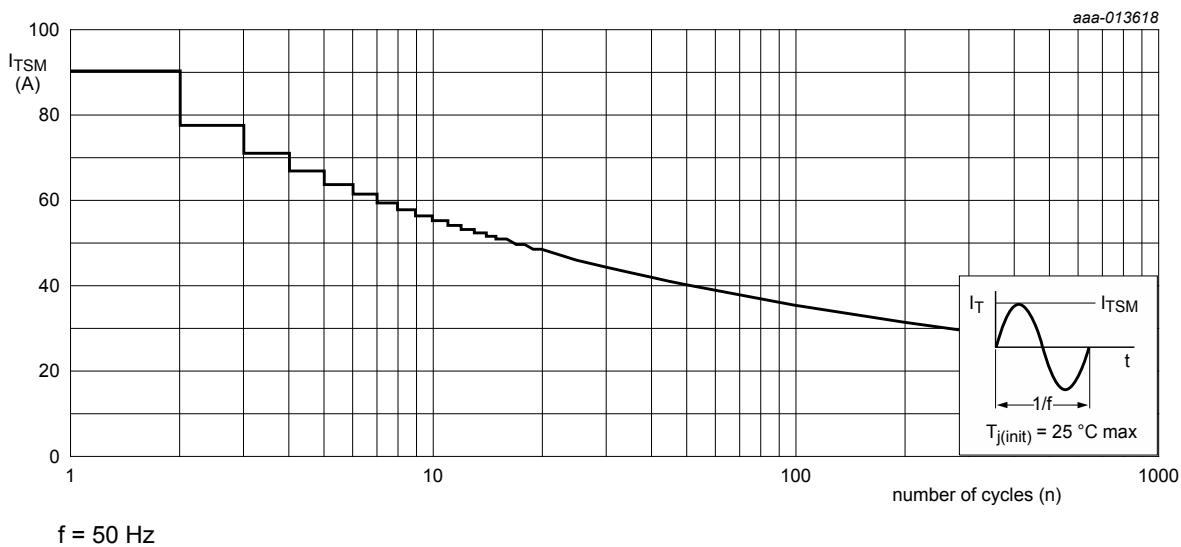


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

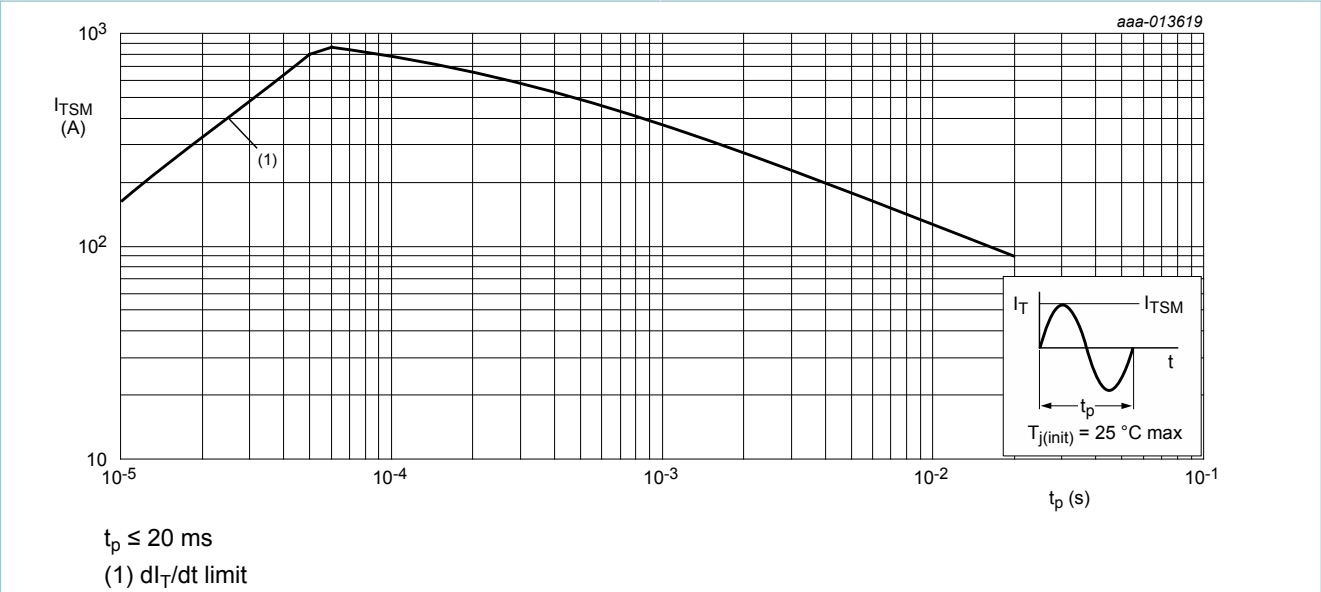


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

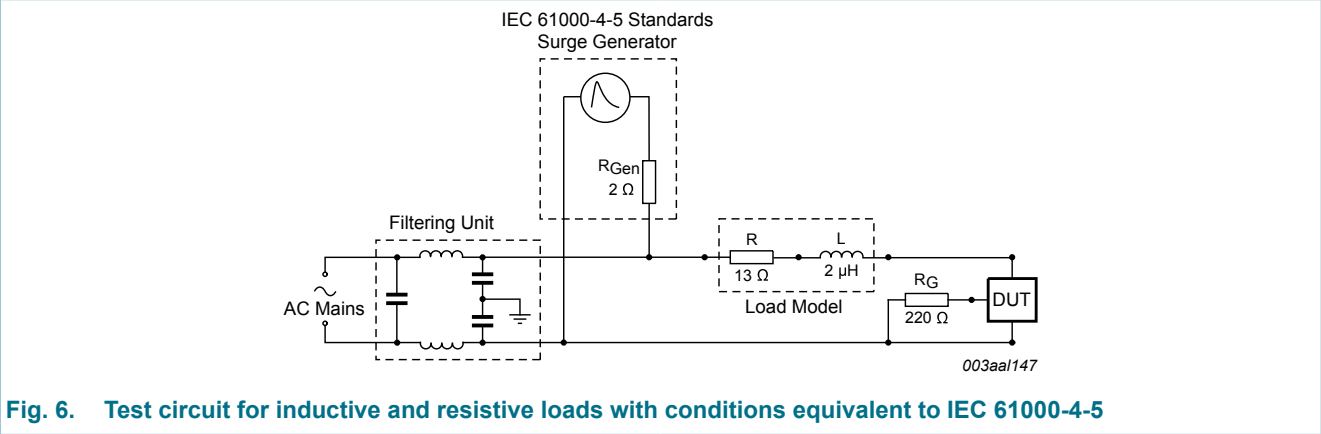
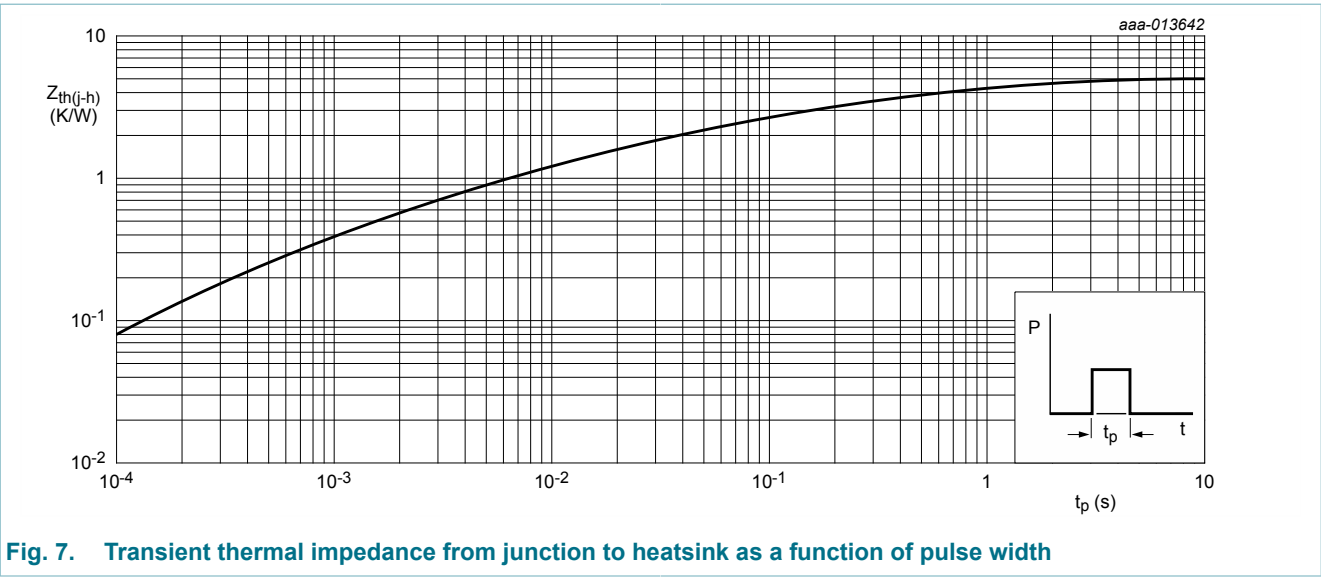


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full cycle; with heatsink compound; Fig. 7	-	-	5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	55	-	K/W



10. Isolation characteristics

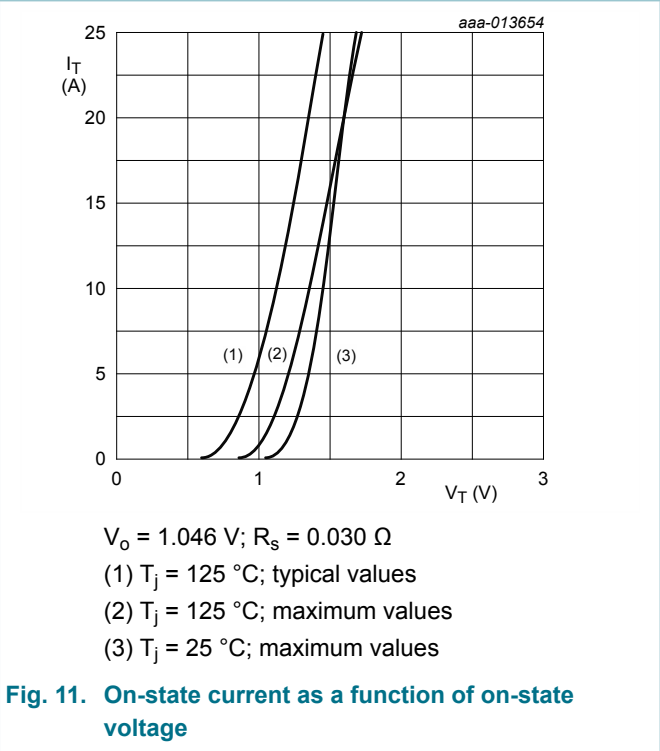
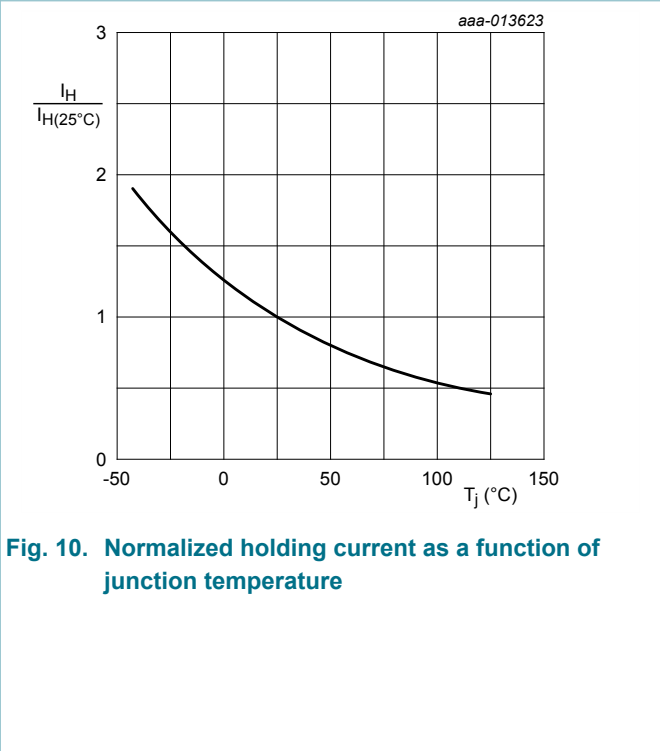
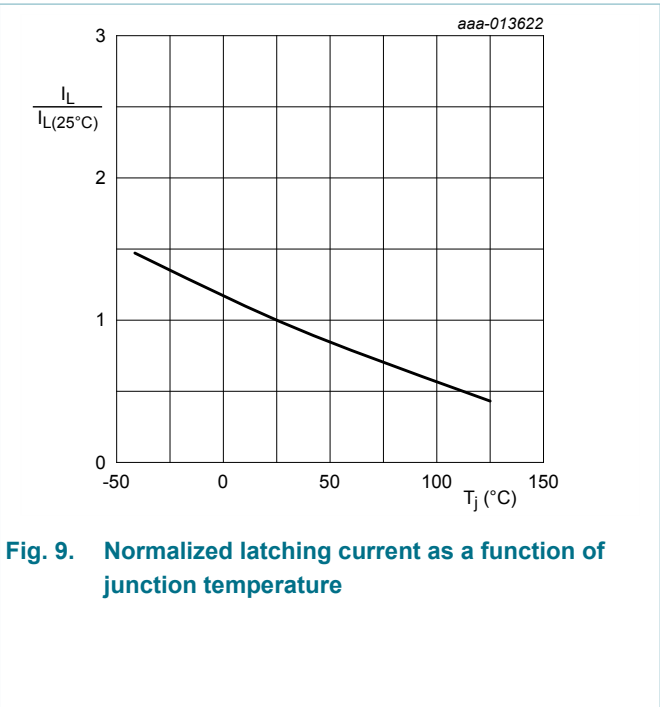
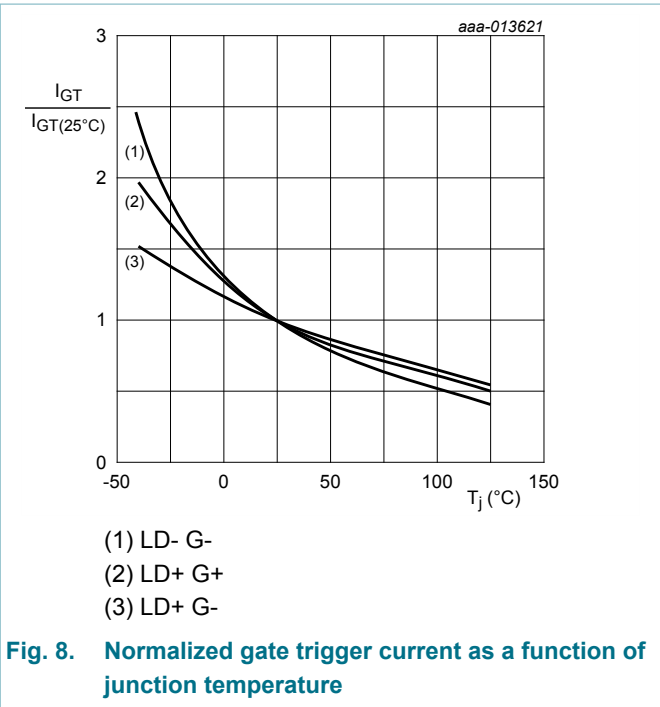
Table 7. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	50 Hz ≤ f ≤ 60 Hz; RH ≤ 65% RH; T _h = 25 °C; from all terminals to external heatsink; sinusoidal waveform; clean and dust free	-	-	2500	V
C_{isol}	isolation capacitance	f = 1 MHz; T _h = 25 °C; from main terminal 2 to external heatsink	-	10	-	pF

11. Characteristics

Table 8. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8		-	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8		-	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8		-	-	35	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9		-	-	70	mA
		$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9		-	-	70	mA
		$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9		-	-	70	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10		-	-	55	mA
V_T	on-state voltage	$I_T = 14.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11		-	1.3	1.5	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 12		-	1	1.2	V
		$V_D = 400\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 125\text{ }^\circ\text{C}$		0.2	0.45	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		-	-	10	μA
		$V_D = 800\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$		-	-	0.5	mA
V_{CL}	clamping voltage	$I_{CL} = 0.1\text{ mA}$; $t_p = 1\text{ ms}$; $T_j = 25\text{ }^\circ\text{C}$		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; exponential waveform; gate open circuit		2000	-	-	V/ μs
di_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 10\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit		20	-	-	A/ms



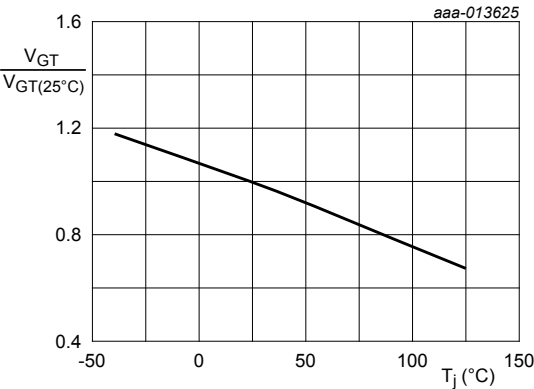


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

12. Package outline

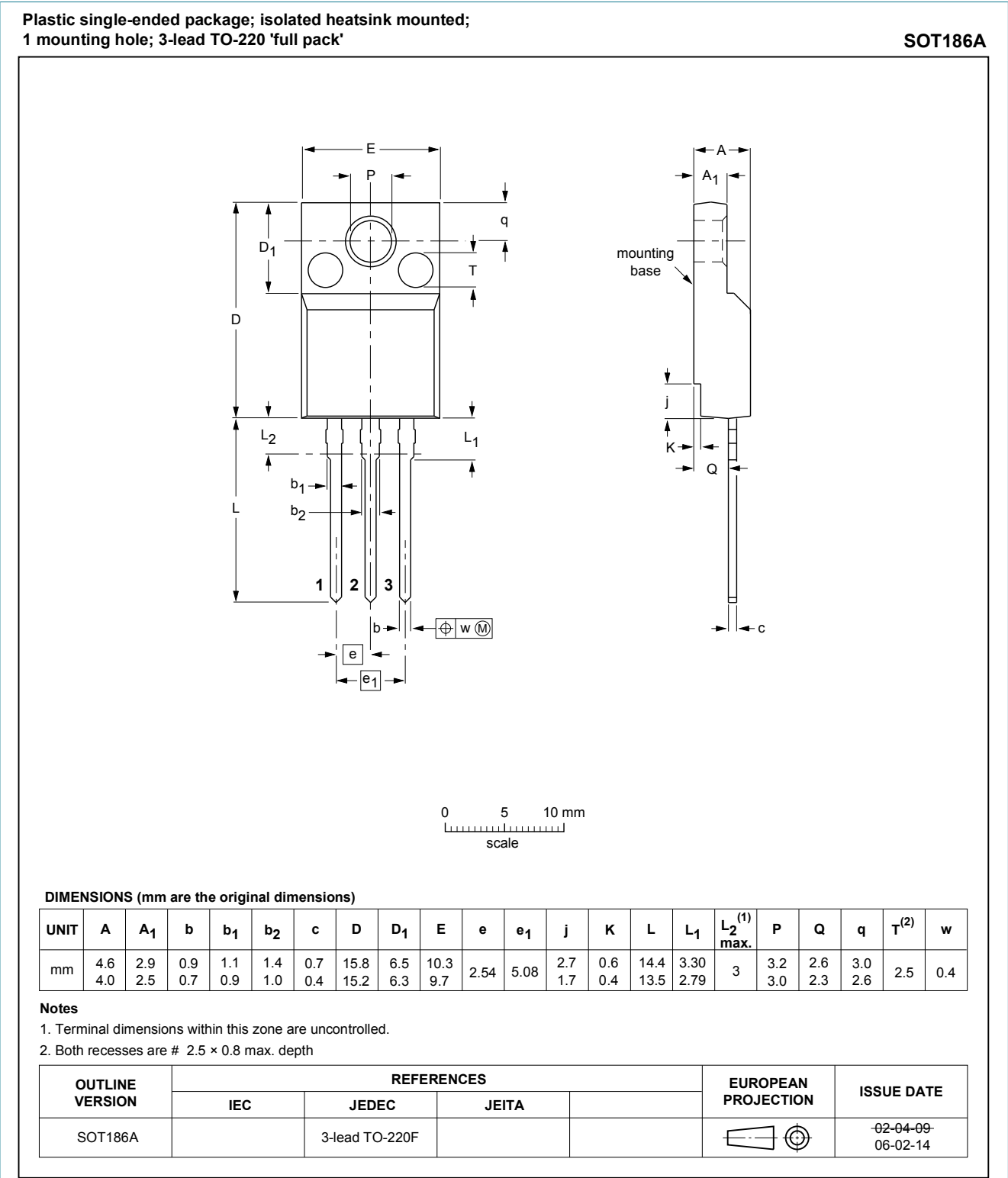


Fig. 13. Package outline TO-220F (SOT186A)

13. Legal information

13.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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14. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	3
8	Limiting values	4
9	Thermal characteristics	7
10	Isolation characteristics	7
11	Characteristics	8
12	Package outline	11
13	Legal information	12
13.1	Data sheet status	12
13.2	Definitions	12
13.3	Disclaimers	12
13.4	Trademarks	13

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