ACPM-7311
UMTS800 4x4 Power Amplifier Module (824-849MHz)
Data Sheet

Description

The ACPM-7311, a Wide-band Code Division Multiple Access(WCDMA) Power Amplifier (PA), is a fully matched 10-pin surface mount module developed for WCDMA handset applications. This power amplifier module operates in the 824-849MHz bandwidth. The ACPM-7311 meets the stringent WCDMA linearity requirements for output power of up to 28dBm.

The ACPM-7311 is also developed to meets HSDPA specs. Mode Control pins are provided for high efficiency improvement of the low output power range.
The ACPM-7311 is self contained, incorporating 50ohm input and output matching networks.

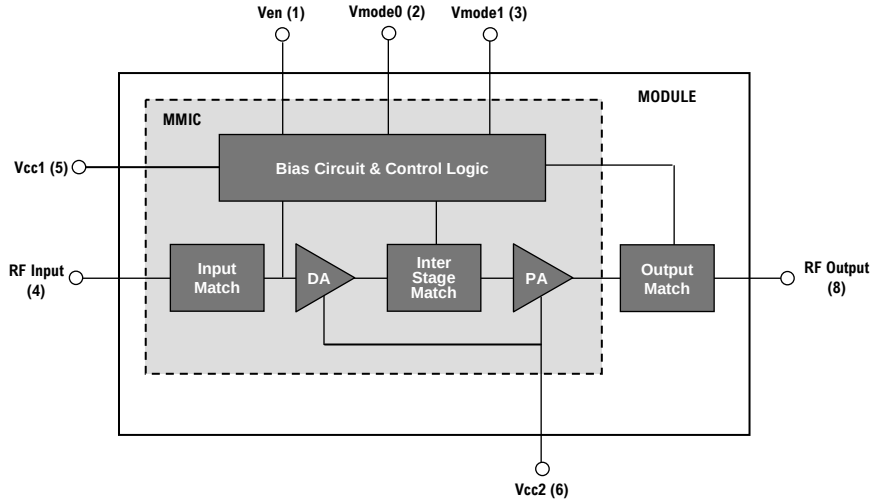
Features

- **Excellent linearity**
- **Low quiescent current**
- **High Efficiency**
  - **42% at Pout=28dBm**
  - **18% at Pout=16dBm**
  - **5.5% at Pout=8dBm**
  - **(without DCDC Converter)**
- **10-pin surface mounting package (4 mm x 4 mm x 1.1 mm)**
- **Internal 50 ohm matching networks for both RF input & output**

Applications

- **WCDMA handset (HSDPA)**

Functional Block Diagram



ACPM-7311
Revision Date: May 30, 2006
Revision Number: DS 0.08
Preliminary Data Sheet

Table 1. Absolute Maximum Ratings [1]

Parameter	Symbol	Min.	Normal	Max.	Unit
RF Input Power	Pin	-	-	10.0	dBm
DC Supply Voltage	Vcc	0	3.4	5.0	V
Enable Voltage	Ven	0	2.6	3.3	V
Mode Control Voltage	Vmode0	0	2.6	3.3	V
	Vmode1	0	2.6	3.3	V
Storage Temperature	Tstg	-55	-	+125	℃

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min.	Normal	Max.	Unit
DC Supply Voltage	Vcc	3.2	3.4	4.2	V
PA Enable	Ven	2.1	2.6	2.9	V
Mode Control Voltage					
- High Power Mode	Vmode0	0	0	0.5	V
	Vmode1	0	0	0.5	V
- Mid Power Mode	Vmode0	2.1	2.6	2.9	V
	Vmode1	0	0	0.5	V
- Low Power Mode	Vmode0	2.1	2.6	2.9	V
	Vmode1	2.1	2.6	2.9	V
Operating Frequency	Fo	824		849	MHz
Case Operating Temperature	To	-20	25	90	℃

Table 3. Power Range Truth Table[2]

Power Mode	Symbol	Ven	Vmode0	Vmode1	Range
High Power Mode	PR3	High	Low	Low	~ 28dBm
Mid Power Mode	PR2	High	High	Low	~ 16dBm
Low Power Mode	PR1	High	High	High	~ 8dBm
Shut Down Mode	-	Low	-	-	-

Notes:

1. No damage assuming only one parameter is set at limit at a time with all other parameters set at or below nominal value.
2. High (2.1 - 2.9V), Low (0.0V - 0.5V).

Table 4. Electrical Characteristics for WCDMA Mode (Vcc=3.4V, Ven=2.6V, T=25℃) [1]

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Frequency Range	F		824	-	849	MHz
Gain	Gain_hi	High Power Mode, Pout=28.0 dBm	24	26.5		dB
	Gain_mid	Mid Power Mode, Pout=16.0 dBm	12	16		dB
	Gain_low	Low Power Mode, Pout=8.0 dBm	11	14.5		dB
Power Added Efficiency	PAE_hi	High Power Mode, Pout=28.0 dBm	38.5	42		%
	PAE_mid	Mid Power Mode, Pout=16.0 dBm	14.5	18		%
	PAE_low	Low Power Mode, Pout=8.0 dBm	4.5	5.5		%
Total Supply Current	Icc_hi	High Power Mode, Pout=28.0 dBm		440	480	mA
	Icc_mid	Mid Power Mode, Pout=16.0 dBm		60	75	mA
	Icc_low	Low Power Mode, Pout=8.0 dBm		25	32	mA
Quiescent Current	Iq_hi	High Power Mode		96	105	mA
	Iq_mid	Mid Power Mode		15	20	mA
	Iq_low	Low Power Mode		11	13	mA
Enable Current	Ien_hi	High Power Mode		0.18	1	mA
	Ien_mid	Mid Power Mode		0.18	1	mA
	Ien_low	Low Power Mode		0.18	1	mA
Control Current	Imode0_mid	Mid Power Mode		0.15	1	mA
	Imode1_low	Low Power Mode		0.15	1	mA
	Imode0_low	Low Power Mode		0.15	1	mA
Total Current in Power-down mode	Ipd	Ven=0V		0.2	5	μA
ACLR in High power mode [2] 5 MHz offset 10 MHz offset	ACLR1_hi ACLR2_hi	High Power Mode, Pout=28.0 dBm		-42 -54	-37 -46	dBc dBc
ACLR in Mid power mode [2] 5 MHz offset 10 MHz offset	ACLR1_mid ACLR2_mid	Mid Power Mode, Pout=16.0 dBm		-42 -56	-37 -46	dBc dBc
ACLR in Low power mode [2] 5 MHz offset 10 MHz offset	ACLR1_low ACLR2_low	Low Power Mode, Pout=8.0 dBm		-42 -56	-37 -46	dBc dBc
Harmonic Suppression Second Third	2f0 3f0	High Power Mode, Pout=28.0 dBm		-39 -60	-30 -40	dBc dBc
Input VSWR	VSWR			2:1	2.5:1	
Stability (Spurious Output)	S	VSWR 6:1, All phase			-60	dBc
Noise Power in Rx Band	RxBN	High Power Mode, Pout=28.0 dBm		-135		dBm/Hz
Ruggedness	Ru	Pout<28.0dBm, Pin<10dBm, All phase High Power Mode			10:1	VSWR
Phase discontinuity	Ph mid_hi	Mid <-> Hi at Pout=16.0dBm		12		Degree
	Ph low_mid	Low <-> Mid at Pout=8.0dBm		12		Degree

Notes:
1. Electrical characteristics are specified under WCDMA modulated(3GPP Uplink DPCCH + 1DPDCH) signal
2. ACP is expressed as a ratio of total adjacent power to signal power, both with 3.84MHz bandwidth at specified offsets.

Table 5. Electrical Characteristics for HSDPA Mode (Vcc=3.4V, Ven=2.6V, T=25℃) [1]

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Frequency Range	F		824	-	849	MHz
Gain	Gain_hih	High Power Mode, Pout=27.5 dBm	24	26.5		dB
	Gain_midh	Mid Power Mode, Pout=16.0 dBm	12	16		dB
	Gain_lowh	Low Power Mode, Pout=8.0 dBm	11	14.5		dB
Power Added Efficiency	PAE_hih	High Power Mode, Pout=27.5 dBm	33.5	37		%
	PAE_midh	Mid Power Mode, Pout=16.0 dBm	14.5	18		%
	PAE_lowh	Low Power Mode, Pout=8.0 dBm	4.5	5.5		%
Total Supply Current	Icc_hih	High Power Mode, Pout=27.5 dBm		400	440	mA
	Icc_midh	Mid Power Mode, Pout=16.0 dBm		60	75	mA
	Icc_lowh	Low Power Mode, Pout=8.0 dBm		25	32	mA
ACLR in High power mode [2] 5 MHz offset	ACLR1_hih	High Power Mode, Pout=27.5 dBm	-	-42	-37	dBc
10 MHz offset	ACLR2_hih			-56	-46	dBc
ACLR in Mid power mode [2] 5 MHz offset	ACLR1_midh	Mid Power Mode, Pout=16.0 dBm	-	-42	-37	dBc
10 MHz offset	ACLR2_midh			-56	-46	dBc
ACLR in Low power mode [2] 5 MHz offset	ACLR1_lowh	Low Power Mode, Pout=8.0 dBm	-	-42	-37	dBc
10 MHz offset	ACLR2_lowh			-56	-46	dBc

Notes:
1. Electrical characteristics are specified under HSDPA modulated Up-Link signal (DPCCH/DPDCH=12/15, HS-DPCCH/DPDCH=15/15)
2. ACP is expressed as a ratio of total adjacent power to signal power, both with 3.84MHz bandwidth at specified offsets

Evaluation Board Description

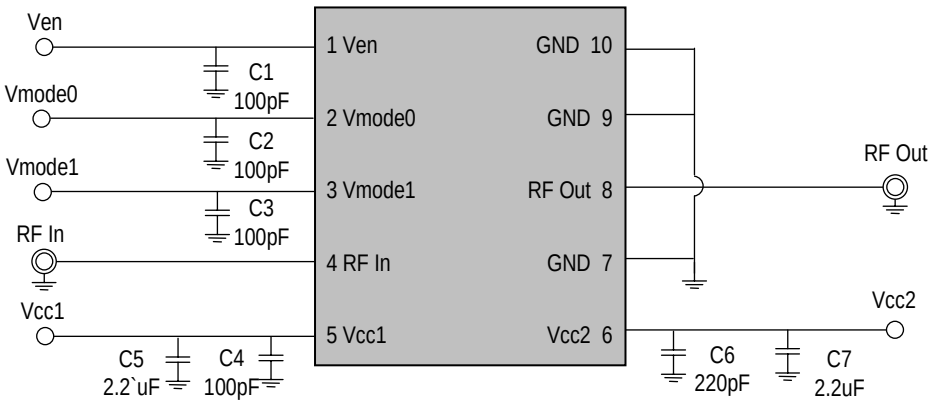


Figure 1. Evaluation Board Schematic

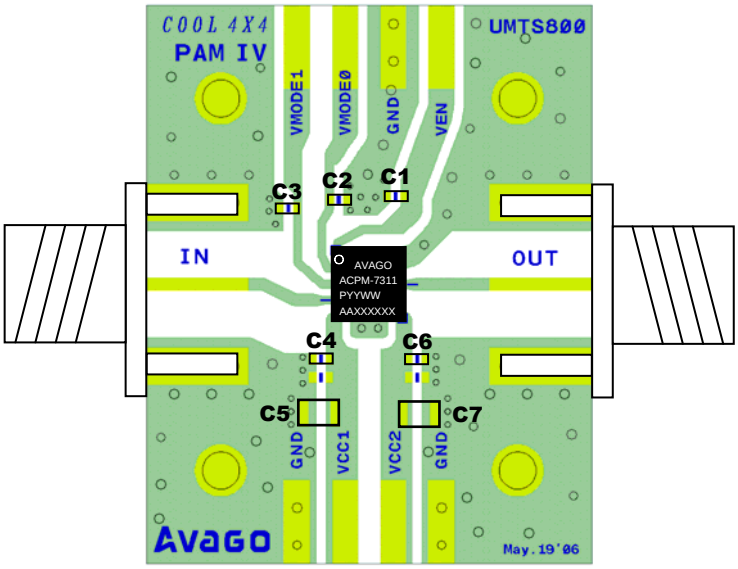
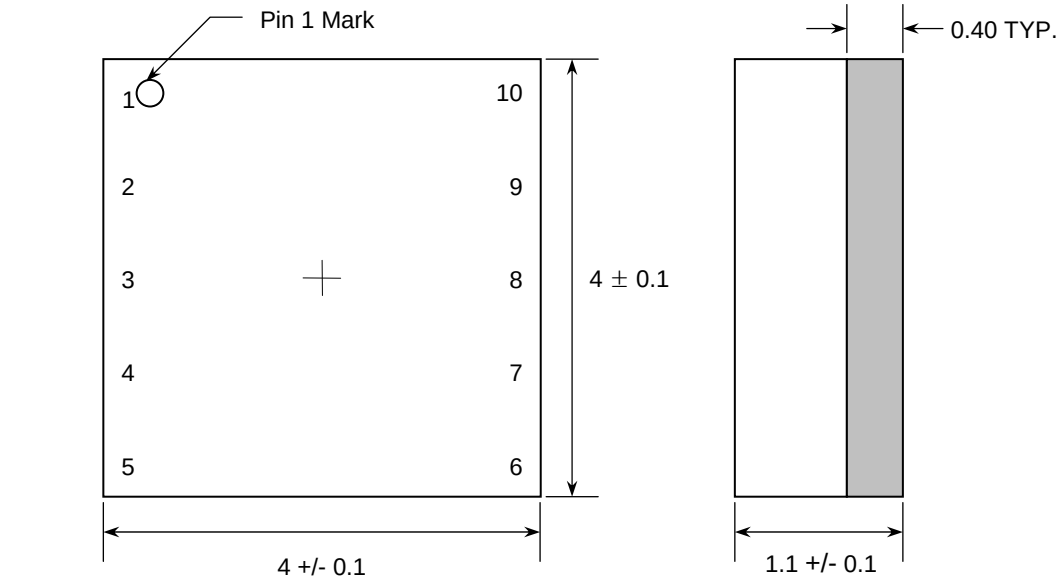
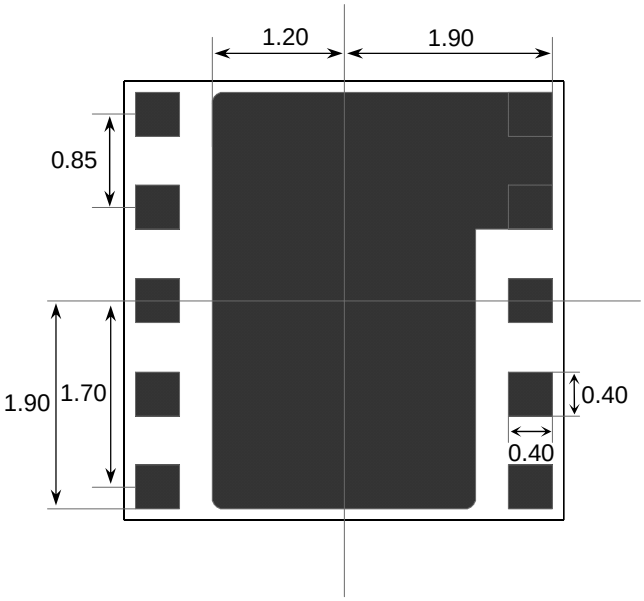


Figure 2. Evaluation Board Assembly Diagram

Package Dimensions and Pin Descriptions





X-RAY BOTTOM VIEW

Pin #	Name	Description
1	Ven	Enable Voltage
2	Vmode0	Control Voltage
3	Vmode1	Control Voltage
4	RF In	RF Input
5	Vcc1	Supply Voltage
6	Vcc2	Supply Voltage
7	GND	Ground
8	RF Out	RF Output
9	GND	Ground
10	GND	Ground

PIN DESCRIPTIONS

Figure 3. Package Dimensional Drawing and Pin Descriptions.

Notes:
1. All dimensions are in millimeters
2. Dimensions without tolerance: .XX → +/-0.05mm

Package Dimensions and Pin Descriptions, continued

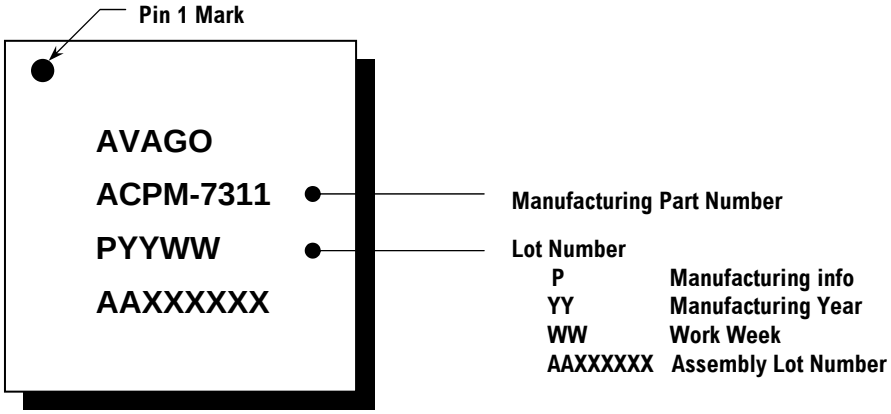


Figure 4. Marking Specifications.

PCB Design Guidelines

The recommended ACPM-7311 PCB Land pattern is shown in Figure 5 and Figure 6. The substrate is coated with solder mask between the I/O and conductive paddle to protect the gold pads from short circuit that is caused by solder bleeding/bridging.

Stencil Design Guidelines

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads.
The recommended stencil layout is shown in Figure 7. Reducing the stencil opening can potentially generate more voids. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads or conductive paddle to adjacent I/O pads.Considering the fact that solder paste thickness will directly affect the quality of the solder joint,a good choice is to use laser cut stencil composed of 0.100mm(4mils)or 0.127mm(5mils) thick stainless steel which is capable of producing the required fine stencil outline.

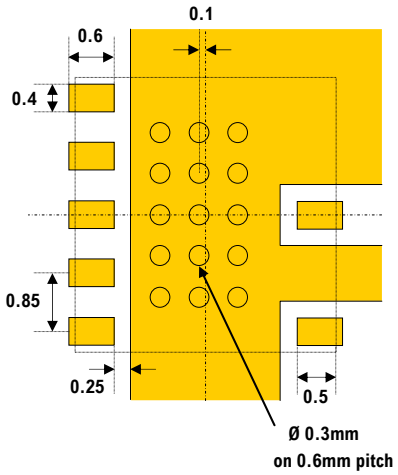


Figure 5. Metallization

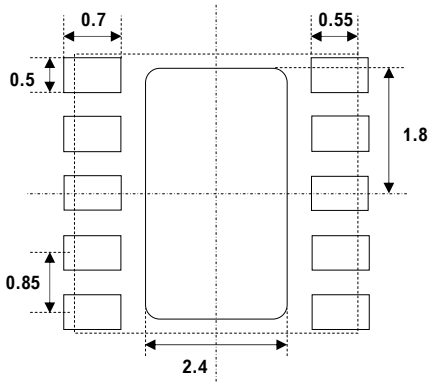


Figure 6. Solder Mask Opening

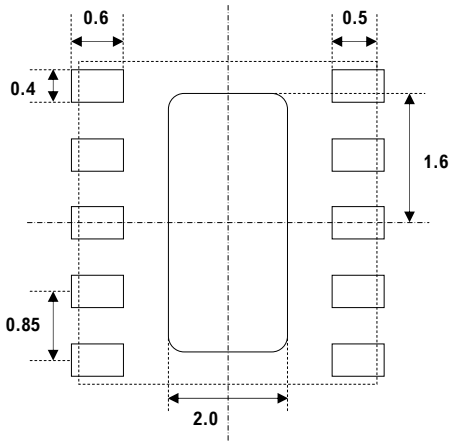
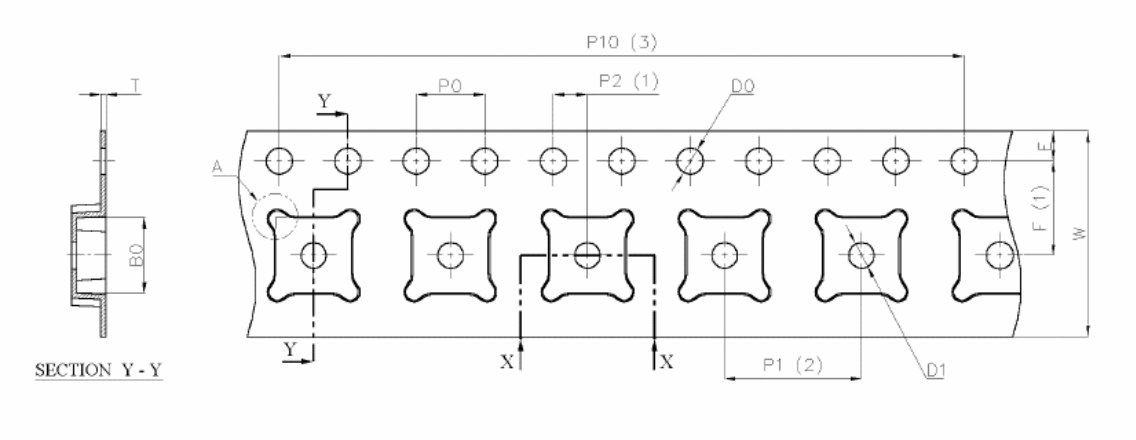
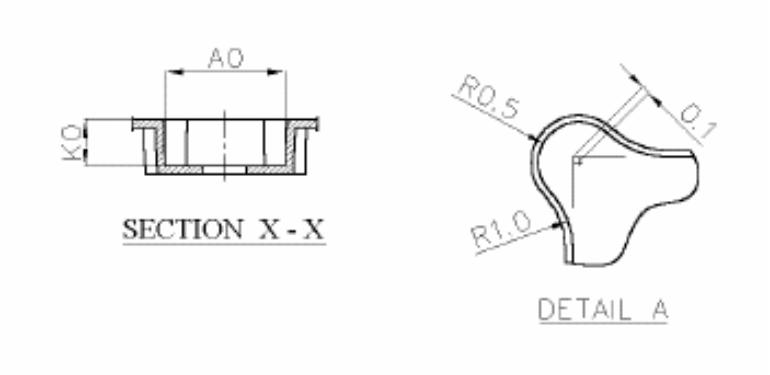
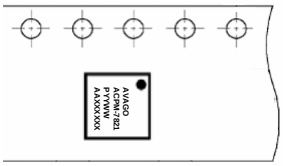


Figure 7. Solder Paste Stencil Aperture

Tape and Reel Information







Dimension List

Annote	Milimeter	Annote	Milimeter
A0	4.40±0.10	P2	2.00±0.05
B0	4.40±0.10	P10	40.00±0.20
K0	1.70±0.10	E	1.75±0.10
D0	1.55±0.05	F	5.50±0.05
D1	1.60±0.10	W	12.00±0.30
P0	4.00±0.10	T	0.30±0.05
P1	8.00±0.10		

Figure 8. Tape and Reel Format – 4 mm x 4 mm.

Reel Drawing

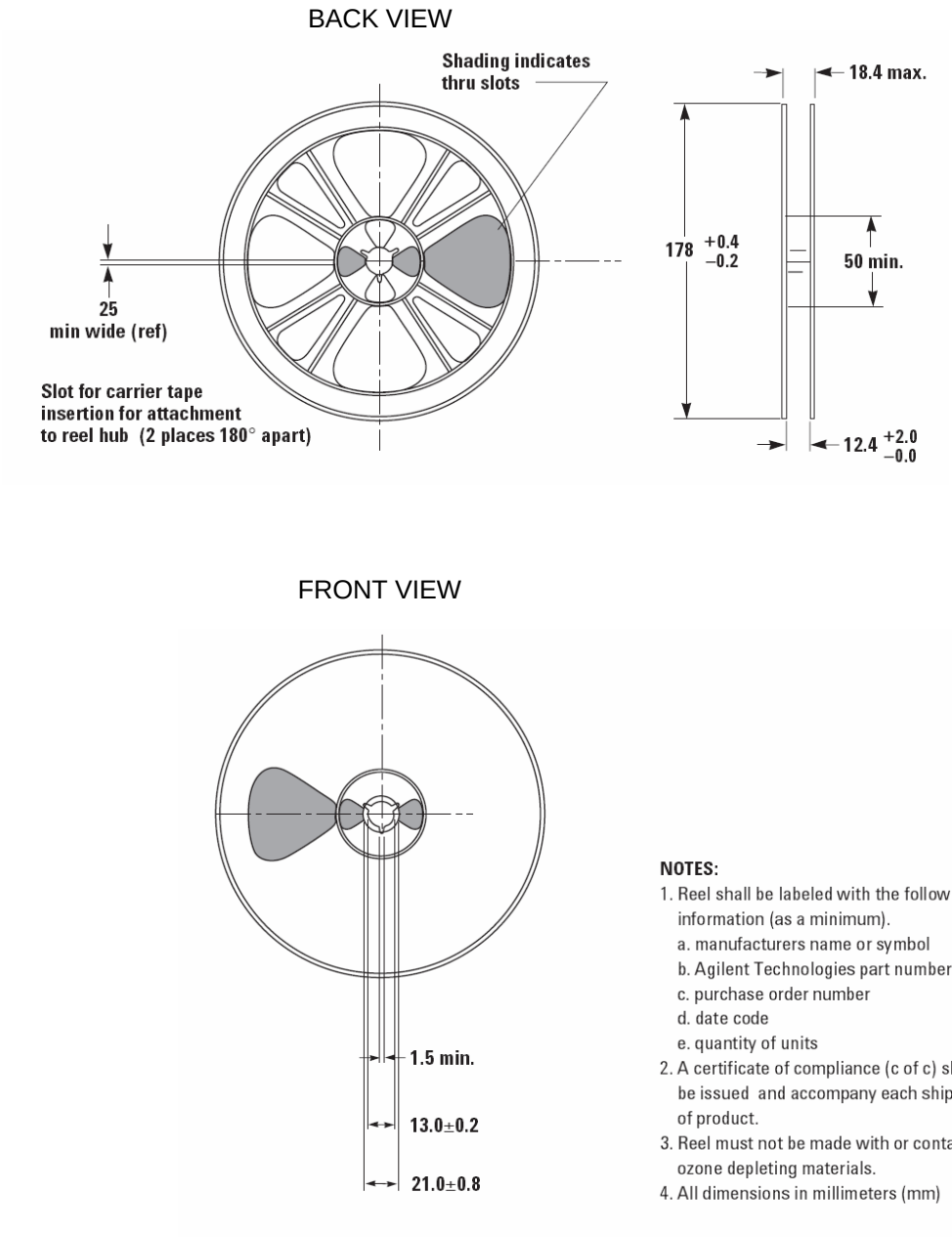


Figure 9. Plastic Reel Format (all dimensions are in millimeters)

Handling and Storage

ESD (Electrostatic Discharge)

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlet of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

MSL (Moisture Sensitivity Level)

Plastic encapsulated surface mount package is sensitive to damage induced by absorbed moisture and temperature. Avago Technologies follows JEDEC Standard J-STD 020B. Each component and package type is classified for moisture sensitivity by soaking a known dry package at various temperatures and relative humidity, and times. After soak, the components are subjected to three consecutive simulated reflows.

The out of bag exposure time maximum limits are determined by the classification test describe below which corresponds to a MSL classification level 6 to 1 according to the JEDEC standard IPC/JEDEC J-STD-020B and J-STD-033.

ACPM-7311 is MSL3. Thus, according to the J-STD-033 p.11 the maximum Manufacturers Exposure Time (MET) for this part is 168 hours. After this time period, the part would need to be removed from the reel, de-taped and then re-baked.

MSL classification reflow temperature for the ACPM-7311 is targeted at 260℃ +0/-5℃. Figure 10 and Table 8 show typical SMT profile for maximum temperature of 260 +0/-5℃.

Table 6. ESD Classification

Pin #	Name	Description	HBM	CDM	Classification
1	Ven	Supply Voltage	± 2000V	± 200V	Class 2
2	Vmode0	RF Input	± 2000V	± 200V	Class 2
3	Vmode1	Ground	± 2000V	± 200V	Class 2
4	RF In	Control Voltage	± 2000V	± 200V	Class 2
5	Vcc1	Enable Voltage	± 2000V	± 200V	Class 2
6	Vcc2	Ground	± 2000V	± 200V	Class 2
7	GND	Ground	± 2000V	± 200V	Class 2
8	RF Out	RF Output	± 2000V	± 200V	Class 2
9	GND	Ground	± 2000V	± 200V	Class 2
10	GND	Supply Voltage	± 2000V	± 200V	Class 2

Note :
1. Module products should be considered extremely ESD sensitive

Table 7. Moisture Classification Level and Floor Life

MSL Level	Floor Life (out of bag) at factory ambient =< 30oC/60% RH or as stated
1	Unlimited at =< 30oC/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

Note :
1. The MSL Level is marked on the MSL Label on each shipping bag.

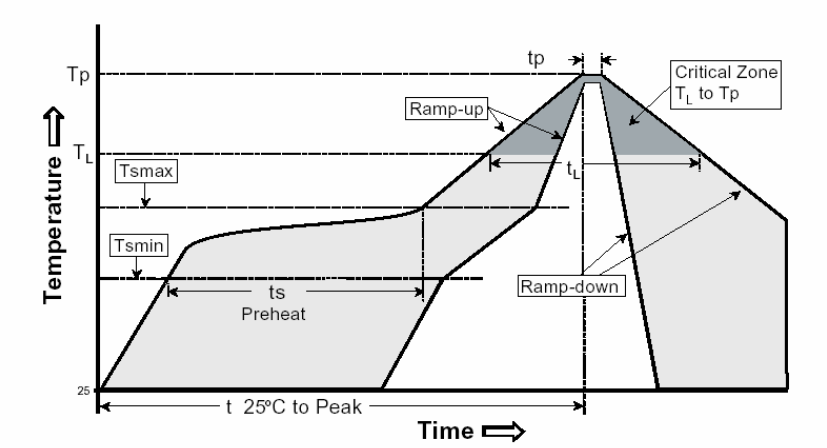


Figure 10. Typical SMT Reflow Profile for Maximum Temperature = 260 +0/-5°C

Table 8. Typical SMT Reflow Profile for Maximum Temperature = 260+0 / -5℃

Profile Feature	Sn-Pb Solder	Pb-Free Solder
Average ramp-up rate (TL to TP)	3℃/sec max	3℃ /sec max
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	 100℃ 150℃ 60-120 sec	 100℃ 150℃ 60-180 sec
Tsmax to TL - Ramp-up Rate		3℃ /sec max
Time maintained above: - Temperature (TL) - Time (TL)	 183℃ 60-150 sec	 217℃ 60-150 sec
Peak temperature (Tp)	240 +0/-5℃	260 +0/-5℃
Time within 5℃ of actual Peak Temperature (tp)	10-30 sec	10-30 sec
Ramp-down Rate	6℃ /sec max	6℃ /sec max
Time 25℃ to Peak Temperature	6 min max.	8 min max.

Storage Condition

Packages described in this document must be stored in sealed moisture barrier, anti-static bags. Shelf life in a sealed moisture barrier bag is 12 months at <40℃ and 90% relative humidity (RH) J-STD-033 p.7.

Out-of-Bag Time Duration

After unpacking the device must be soldered to the PCB within 168 hours as listed in the J-STD-020B p.11 with factory conditions <30℃ and 60% RH.

Baking

It is not necessary to re-bake the part if both conditions (storage conditions and out-of bag conditions) have been satisfied. Baking must be done if at least one of the conditions above have not been satisfied. The baking conditions are 125℃ for 12 hours J-STD-033 p.8.

CAUTION: Tape and reel materials typically cannot be baked at the temperature described above. If out-of-bag exposure time is exceeded, parts must be baked for a longer time at low temperatures, or the parts must be de-reeled, de-taped, re-baked and then put back on tape and reel. (See moisture sensitive warning label on each shipping bag for information of baking).

Board Rework

Component Removal, Rework and Remount

If a component is to be removed from the board, it is recommended that localized heating be used and the maximum body temperatures of any surface mount component on the board not exceed 200℃. This method will minimize moisture related component damage. If any component temperature exceeds 200℃, the board must be baked dry per 4-2 prior to rework and/or component removal. Component temperatures shall be measured at the top center of the package body. Any SMD packages that have not exceeded their floor life can be exposed to a maximum body temperature as high as their specified maximum reflow temperature.

Removal for Failure Analysis

Not following the above requirements may cause moisture/reflow damage that could hinder or completely prevent the determination of the original failure mechanism.

Baking of Populated Boards

Some SMD packages and board materials are not able to withstand long duration bakes at 125℃. Examples of this are some FR-4 materials, which cannot withstand a 24 hr bake at 125℃. Batteries and electrolytic capacitors are also temperature sensitive. With component and board temperature restrictions in mind, choose a bake temperature from Table 4-1 in J-STD 033; then determine the appropriate bake duration based on the component to be removed. For additional considerations see IPC-7711 and IPC-7721.

Derating due to Factory Environmental Conditions

Factory floor life exposures for SMD packages removed from the dry bags will be a function of the ambient environmental conditions. A safe, yet conservative, handling approach is to expose the SMD packages only up to the maximum time limits for each moisture sensitivity level as shown in Table 7. This approach, however, does not work if the factory humidity or temperature are greater than the testing conditions of 30℃/60% RH. A solutions for addressing this problem is to derate the exposure times based on the knowledge of moisture diffusion in the component package materials (ref. JESD22-A120). Recommended equivalent total floor life exposures can be estimated for a range of humidities and temperatures based on the nominal plastic thickness for each device. Table 9 lists equivalent derated floor lives for humidities ranging from 20-90% RH for three temperature, 20℃,25℃, and 30℃. This table is applicable to SMDs molded with novolac, biphenyl or multifunctional epoxy mold compounds. The following assumptions were used in calculating Table 9:

1. Activation Energy for diffusion = 0.35eV (smallest known value).
2. For ≤60% RH, use Diffusivity = 0.121exp (-0.35eV/kT) mm2/s (this used smallest known Diffusivity @ 30℃).
3. For >60% RH, use Diffusivity = 1.320exp (-0.35eV/kT) mm2/s (this used largest known Diffusivity @ 30℃).

Table 9. Recommended Equivalent Total Floor Life (days) @ 20℃, 25 ℃ & 30 ℃ For ICs with Novolac, Biphenyl and Multifunctional Epoxies (Reflow at same temperature at which the component was classified)

Maximum Percent Relative Humidity												
Package Type and Body Thickness	Moisture Sensitivity Level	5%	10%	20%	30%	40%	50%	60%	70%	80%	90%	
Body Thickness ≥3.1 mm Including PQFPs >84 pin, PLCCs (square) All MQFPs or All BGAs ≥1 mm	Level 2a	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	60 78 103	41 53 69	33 42 57	28 36 47	10 14 19	7 10 13	6 8 10	30℃ 25℃ 20℃
	Level 3	∞ ∞ ∞	∞ ∞ ∞	10 13 17	9 11 14	8 10 13	7 9 12	7 9 12	5 7 10	4 6 8	4 5 7	30℃ 25℃ 20℃
	Level 4	∞ ∞ ∞	5 6 8	4 5 7	4 5 7	4 5 7	3 5 7	3 4 6	3 3 5	2 3 4	2 3 4	30℃ 25℃ 20℃
	Level 5	∞ ∞ ∞	4 5 7	3 5 7	3 4 6	2 4 5	2 3 5	2 3 4	2 2 3	1 2 2	1 2 3	30℃ 25℃ 20℃
	Level 5a	∞ ∞ ∞	2 3 5	1 2 4	1 2 3	1 2 3	1 2 3	1 2 2	1 1 2	1 1 2	1 1 2	30℃ 25℃ 20℃
Body 2.1 mm ≤ Thickness <3.1 mm including PLCCs (rectangular) 18-32 pin SOICs (wide body) SOICs ≥20 pins, PQFPs ≤80 pins	Level 2a	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	86 148 ∞	39 51 69	28 37 49	4 6 8	3 4 5	2 3 4	30℃ 25℃ 20℃
	Level 3	∞ ∞ ∞	∞ ∞ ∞	19 25 32	12 15 19	9 12 15	8 10 13	7 9 12	3 5 7	2 3 5	2 3 4	30℃ 25℃ 20℃
	Level 4	∞ ∞ ∞	7 9 11	5 7 9	4 5 7	4 5 6	3 4 6	3 4 5	2 3 4	2 2 3	1 2 3	30℃ 25℃ 20℃
	Level 5	∞ ∞ ∞	4 5 6	3 4 5	3 3 5	2 3 4	2 3 4	2 3 4	1 2 3	1 1 3	1 1 2	30℃ 25℃ 20℃
	Level 5a	∞ ∞ ∞	2 2 3	1 2 2	1 2 2	1 2 2	1 2 2	1 2 2	1 1 2	0.5 1 2	0.5 1 1	30℃ 25℃ 20℃
Body Thickness <2.1 mm including SOICs <18 pin All TQFPs, TSOPs or All BGAs <1 mm body thickness	Level 2a	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	28 ∞ ∞	1 2 2	1 1 2	1 1 1	30℃ 25℃ 20℃
	Level 3	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	11 14 20	7 10 13	1 2 2	1 1 2	1 1 1	30℃ 25℃ 20℃
	Level 4	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	9 12 17	5 7 9	4 5 7	3 4 6	1 2 2	1 1 2	1 1 1	30℃ 25℃ 20℃
	Level 5	∞ ∞ ∞	∞ ∞ ∞	13 18 26	5 6 8	3 4 6	2 3 5	2 3 4	1 2 2	1 1 2	1 1 1	30℃ 25℃ 20℃
	Level 5a	∞ ∞ ∞	10 13 18	3 5 6	2 3 4	1 2 3	1 2 2	1 2 2	1 1 2	1 1 2	0.5 1 1	30℃ 25℃ 20℃

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