DESCRIPTION

The A93C66 provides 4096 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 256 words of 16 bits each, when the ORG pin is connected to V_{CC} and 512 words of 8 bits each when it is tied to ground.

The A93C66 is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate erase cycle is required before write. The Write cycle is only enabled when it is in the Erase/Write Enable state. When CS is brought “high” following the initiation of a write cycle, the DO pin outputs the Ready/Busy status.

The A93C66 is available in SOP8 and TSSOP8 Package.

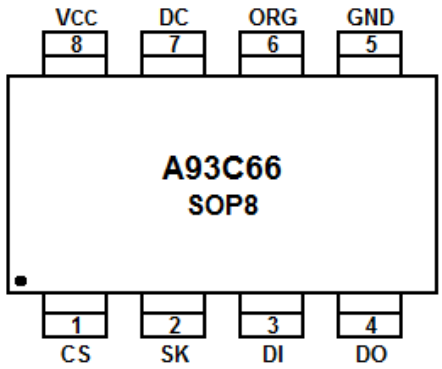
FEATURES

- Three-wire Serial Interface
- V_{CC} = 1.8V to 5.5V
- Sequential Read Operation
- 2 MHz Clock Rate (5V) Compatibility
- Self-timed Write Cycle (5 ms max)
- 1 Million Write Cycles guaranteed
- Data Retention > 100 Years
- Available in SOP8 and TSSOP8 Package

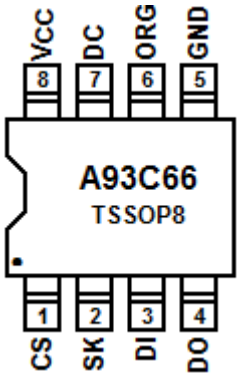
ORDERING INFORMATION

Package Type	Part Number	
SOP8	M8	A93C66M8R
		A93C66M8U
		A93C66M8VR
		A93C66M8VU
TSSOP8	TMX8	A93C66TMX8R
		A93C66TMX8U
		A93C66TMX8VR
		A93C66TMX8VU
Note	R: Tape & Reel U: Tube V: Halogen free Package	
AiT provides all RoHS products suffix “ V “ means Halogen free Package		

PIN DESCRIPTION



Top View



Top View

Pin #		Symbol	Functions
SOP8	TSSOP8		
1	1	CS	Chip Select
2	2	SK	Serial Data Clock
3	3	DI	Serial Data Input
4	4	DO	Serial Data Output
5	5	GND	Ground
6	6	ORG	Internal Organization
7	7	DC	Don't Connect
8	8	V_{CC}	Power Supply

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	-0.3V ~ +6.5V
Input/ Output Voltage	GND-0.3V ~ V_{CC} +0.3V
Operating Ambient Temperature	-40℃ ~ +85℃
Storage Temperature	-65℃ ~ +150℃

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

PIN CAPACITANCE

T_A=25℃, f=1.0MHz, V_{CC}=+1.8V (Unless otherwise specified)

PARAMETER	SYMBOL	MAX	UNIT	CONDITION
Output Capacitance (DO)	C_{OUT}	5	pF	V_{OUT}=0V
Input Capacitance (CS, SK, DI)	C_{IN}	5	pF	V_{IN}=0V

DC ELECTRICAL CHARACTERISTICS

T_A=-40℃ to +85℃, V_{CC}=+1.8V to +5.5V (Unless otherwise specified)

Parameter	Symbo	Condition		MIN	TYP	MAX	Unit
Supply Voltage	V_{CC1}			1.8	-	5.5	V
Supply Voltage	V_{CC2}			2.7	-	5.5	V
Supply Voltage	V_{CC3}			4.5	-	5.5	V
Supply Current	I_{CC}	V_{CC}=5.0V	Read at 1.0MHz	-	0.2	2.0	mA
			Write at 1.0MHz	-	0.9	3.0	
Standby Current	I_{SB1}	V_{CC}=1.8V	CS=0V	-	-	1.0	μA
Standby Current	I_{SB2}	V_{CC}=2.7V,		-	-	1.0	
Standby Current	I_{SB3}	V_{CC}=5.0V		-	-	1.0	
Input Leakage NOTE1	I_{IL}	V_{IN}=0V to V_{CC}		-	0.1	1.0	μA
Input Leakage NOTE2	I_{IL}	V_{IN}=0V to V_{CC}		-	2.0	3.0	μA
Output Leakage	I_{OL}	V_{IN}=0V to V_{CC}		-	0.1	1.0	uA
Input Low VoltageNOTE3	V_{IL1}	2.7V ≤ V_{CC} ≤ 5.5V		-0.3	-	0.8	V
Input High VoltageNOTE3	V_{IH1}			2.0	-	V_{CC}+0.3	
Input Low VoltageNOTE3	V_{IL2}	1.8V ≤ V_{CC} ≤ 2.7V		-0.5	-	V_{CC}+0.3	V
Input High VoltageNOTE3	V_{IH2}			V_{CC}x0.7	-	V_{CC}+0.3	
Output Low Voltage	V_{OL1}	2.7V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1mA	-	-	0.4	V
Output High Voltage	V_{OH1}		I_{OH} = -0.4mA	2.4	-	-	
Output Low Voltage	V_{OL2}	1.8V ≤ V_{CC} ≤ 2.7V	I_{OL}=0.15mA	-	-	0.2	V
Output High Voltage	V_{OH2}		I_{OH}=-100uA	V_{CC}-0.2	-	-	

NOTE1: DI、CS、SK input pin

NOTE2: ORG input pin

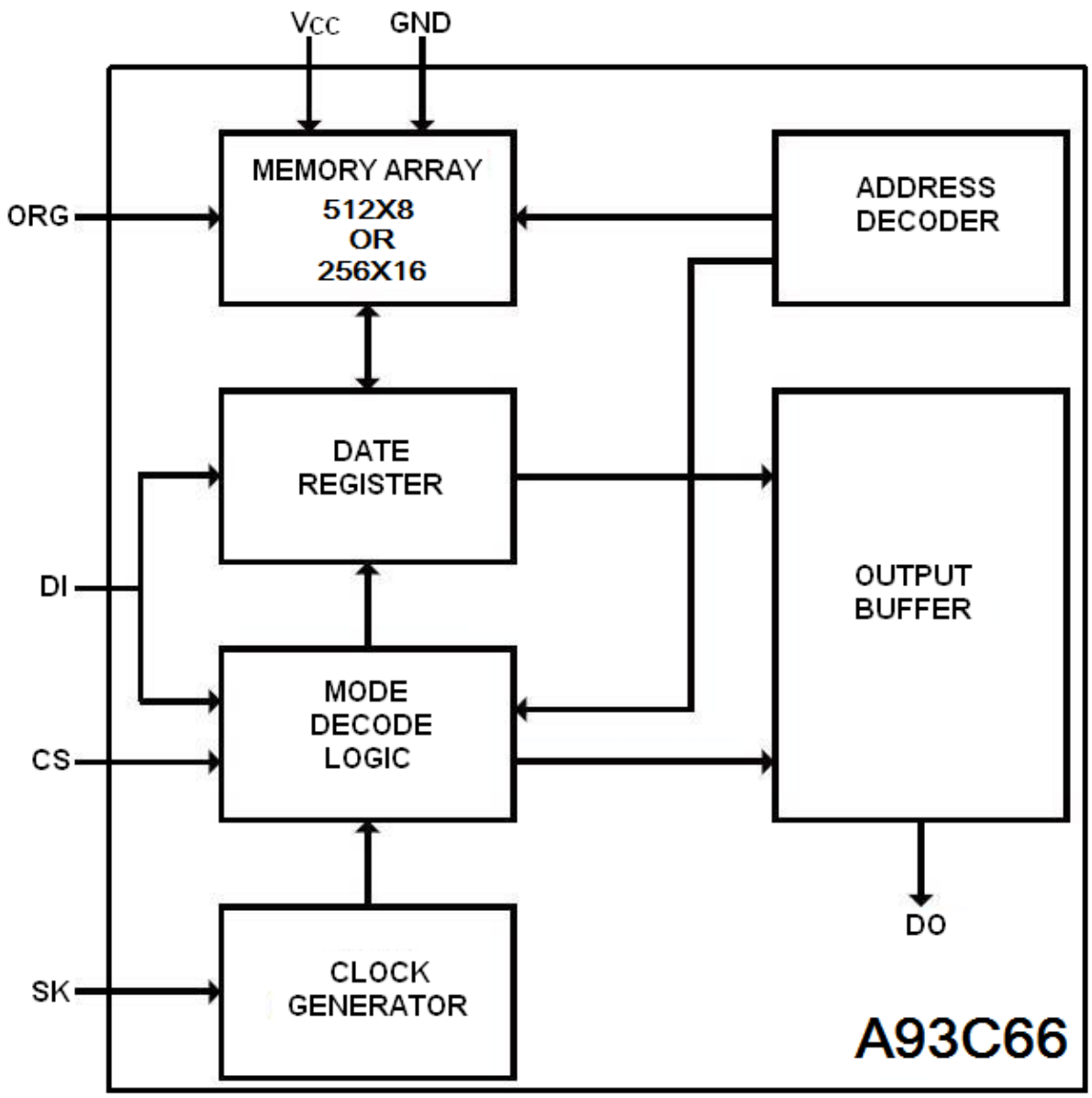
NOTE3: V_{IL} min and V_{IH} max are reference only and are not tested.

AC ELECTRICAL CHARACTERISTICS

T_A=-40℃ to +85℃, V_{CC}=+1.8V to +5.5V, C_L=1 TTL Gate and 100pF, unless otherwise specified.

Parameter	Symbol	Condition		MIN	TYP	MAX	Unit
SK Clock Frequency	f_{SK}	1.8V ≤ V_{CC} ≤ 5.5V		0	-	0.25	MHz
		2.7V ≤ V_{CC} ≤ 5.5V		0	-	1	
		4.5V ≤ V_{CC} ≤ 5.5V		0	-	2	
SK High Time	t_{SKH}	1.8V ≤ V_{CC} ≤ 5.5V		1000	-	-	ns
		2.7V ≤ V_{CC} ≤ 5.5V		250	-	-	
		4.5V ≤ V_{CC} ≤ 5.5V		250	-	-	
SK Low Time	t_{SKL}	1.8V ≤ V_{CC} ≤ 5.5V		1000	-	-	ns
		2.7V ≤ V_{CC} ≤ 5.5V		250	-	-	
		4.5V ≤ V_{CC} ≤ 5.5V		250	-	-	
Minimum CS Low Time	t_{CS}	1.8V ≤ V_{CC} ≤ 5.5V		1000	-	-	ns
		2.7V ≤ V_{CC} ≤ 5.5V		250	-	-	
		4.5V ≤ V_{CC} ≤ 5.5V		250	-	-	
CS Setup Time	t_{CSS}	Relative to SK					ns
		1.8V ≤ V_{CC} ≤ 5.5V		200	-	-	
		2.7V ≤ V_{CC} ≤ 5.5V		50	-	-	
		4.5V ≤ V_{CC} ≤ 5.5V		50	-	-	
DI Setup Time	t_{DIS}	Relative to SK					ns
		1.8V ≤ V_{CC} ≤ 5.5V		400	-	-	
		2.7V ≤ V_{CC} ≤ 5.5V		100	-	-	
		4.5V ≤ V_{CC} ≤ 5.5V		100	-	-	
CS Hold Time	t_{CSH}	Relative to SK		0	-	-	ns
DI Hold Time	t_{DIH}	Relative to SK					ns
		1.8V ≤ V_{CC} ≤ 5.5V		400	-	-	
		2.7V ≤ V_{CC} ≤ 5.5V		100	-	-	
		4.5V ≤ V_{CC} ≤ 5.5V		100	-	-	
Output Delay to “1”	t_{PD1}	AC Test	1.8V ≤ V_{CC} ≤ 5.5V	-	-	1000	ns
			2.7V ≤ V_{CC} ≤ 5.5V	-	-	250	
			4.5V ≤ V_{CC} ≤ 5.5V	-	-	250	
Output Delay to “0”	t_{PD0}	AC Test	1.8V ≤ V_{CC} ≤ 5.5V	-	-	1000	ns
			2.7V ≤ V_{CC} ≤ 5.5V	-	-	250	
			4.5V ≤ V_{CC} ≤ 5.5V	-	-	250	
CS to Status Valid	t_{SV}	AC Test	1.8V ≤ V_{CC} ≤ 5.5V	-	-	1000	ns
			2.7V ≤ V_{CC} ≤ 5.5V	-	-	250	
			4.5V ≤ V_{CC} ≤ 5.5V	-	-	250	
CS to DO in High Impedance	t_{DF}	AC Test C_S = V_{IL}					ns
		1.8V ≤ V_{CC} ≤ 5.5V		-	-	400	
		2.7V ≤ V_{CC} ≤ 5.5V		-	-	100	
		4.5V ≤ V_{CC} ≤ 5.5V		-	-	100	
Write Cycle Time	t_{WP}			-	1.5	5	ms
5.0V, 25℃	Endurance			1M	-	-	Write Cycles

BLOCK DIAGRAM



When the ORG pin is connected to V_{CC}, the “x16” organization is selected. When it is connected to ground, the “x8” organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1 Meg ohm pull-up, then “x16“organization is selected.

DETAILED INFORMATION

The A93C66 is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a start bit (logic"1") followed by the appropriate OP Code and the desired memory address location.

Instruction Set of A93C66

Instruction	SB	OP Code	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A_8 - A_0	A_7 - A_0			Reads data stored in memory, at specified address
EWEN	1	00	11XXXXXXX	11XXXXXX			Write enable must precede all programming modes
ERASE	1	11	A_8 - A_0	A_7 - A_0			Erase memory location An - A_0
WRITE	1	01	A_8 - A_0	A_7 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location An - A_0
ERAL	1	00	10XXXXXXX	10XXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V
WRAL	1	00	01XXXXXXX	01XXXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V
EWDS	1	00	00XXXXXXX	00XXXXXX			Disables all programming instructions

The X's in the address field represent don't care values and must be clocked.

READ (READ)

The Read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic "0") precedes the 8- or 16-bit data output string. The A93C66 supports sequential read operations. The device will automatically increment the internal address pointer and clock out the next memory location as long as Chip Select (CS) is held high .In this case, the dummy bit (logic "0") will not be clocked out between memory locations, thus allowing for a continuous steam of data to be read.

ERASE/WRITE (EWEN):

To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or V_{CC} power is removed from the part.

ERASE (ERASE)

The Erase (ERASE) instruction programs all bits in the specified memory location to the logical “1”state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (T_{CS}). A logic “1” at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE)

The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (T_{CS}). A logic “0” at DO indicates that programming is still in progress. A logic “1” indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A Ready/Busy status cannot be obtained if the CS is brought high after the end of the self timed programming cycle, TWP.

ERASE ALL (ERAL)

The Erase All (ERAL) instruction programs every bit in the memory array to the logic “1” state and is primarily used for testing purposes. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (T_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

WRITE ALL (WRAL)

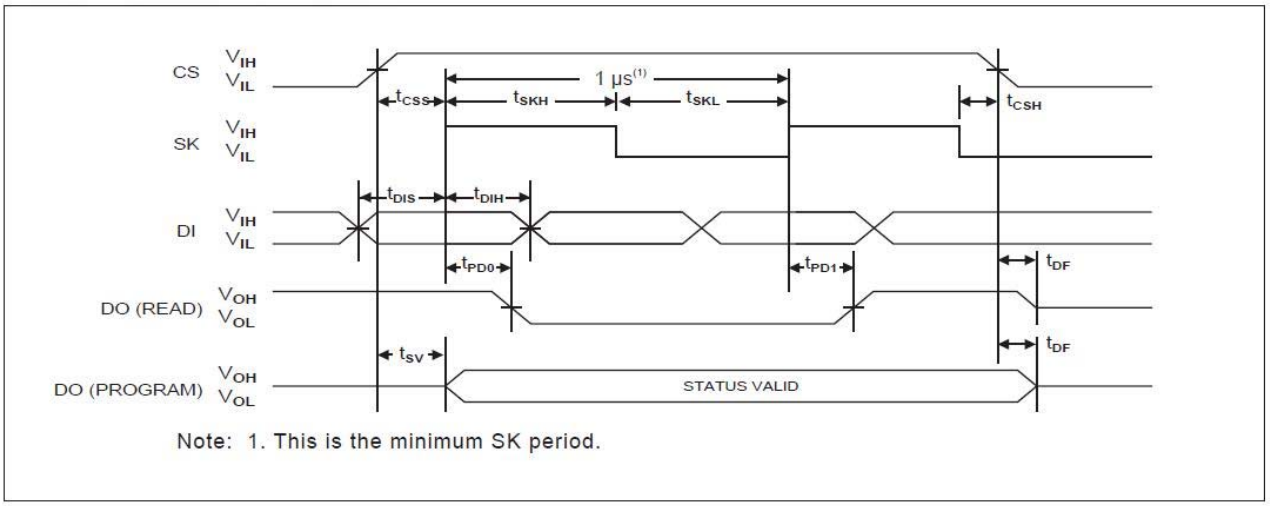
The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (T_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS)

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

TIMING DIAGRAMS

Fig1. Synchronous Data Timing



Organization Key for Timing Diagrams

I/O	A93C66(4K)	
	X 8	X 16
AN	A8	A7
DN	D7	D15

Fig2. READ Timing

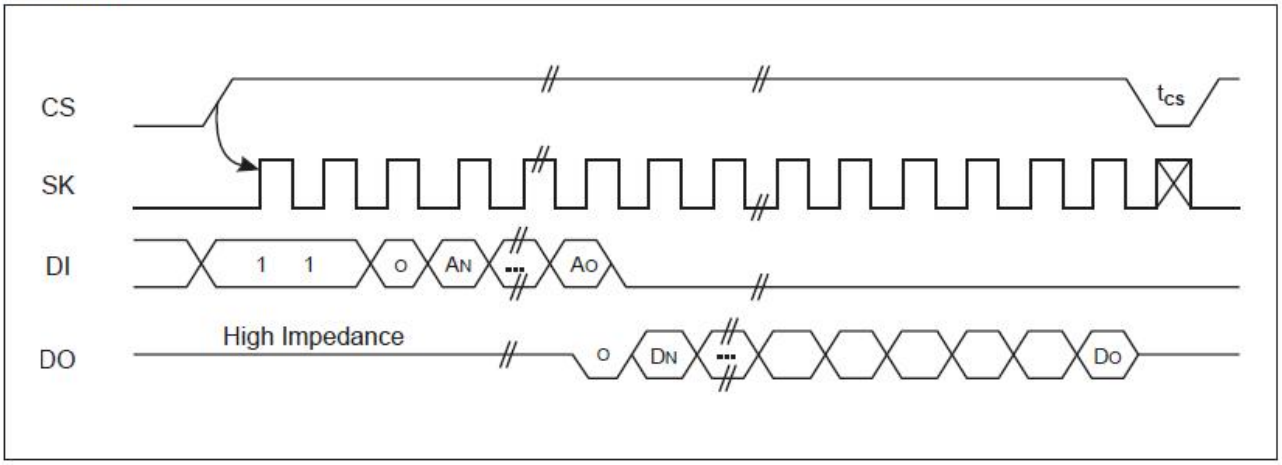


Fig3. EWEN Timing

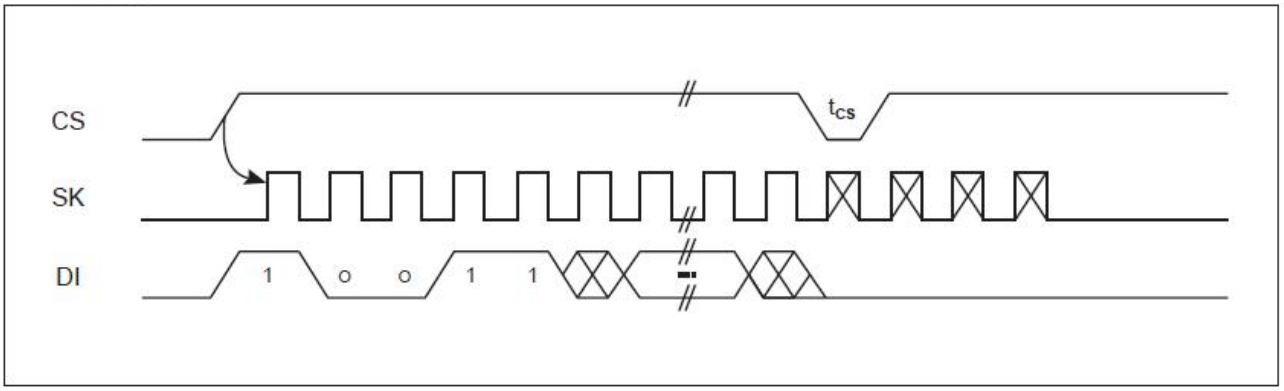


Fig4. EWDS Timing

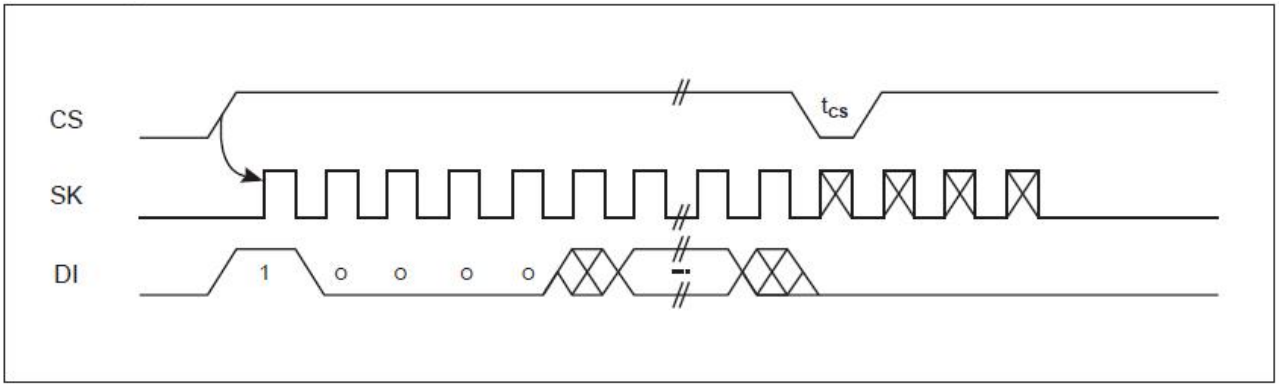


Fig5. WRITE Timing

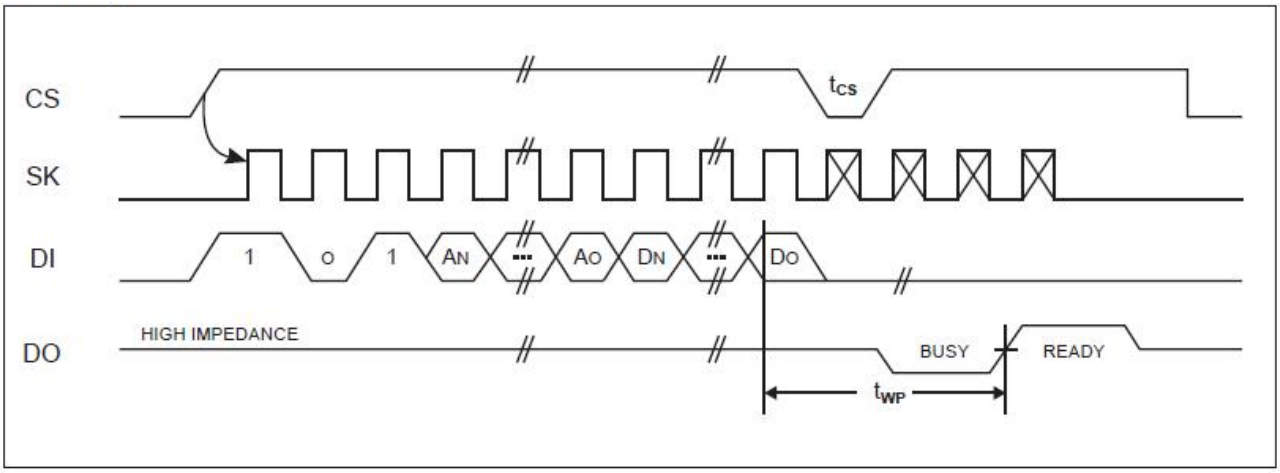


Fig6. WRAL Timing (Valid only at V_{CC}=4.5V to 5.5V)

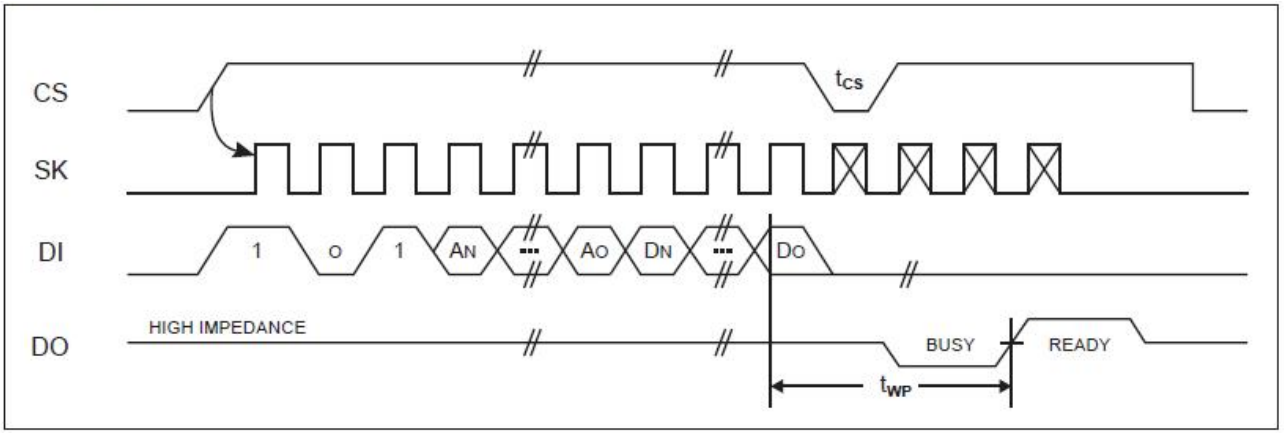


Fig7. ERASE Timing

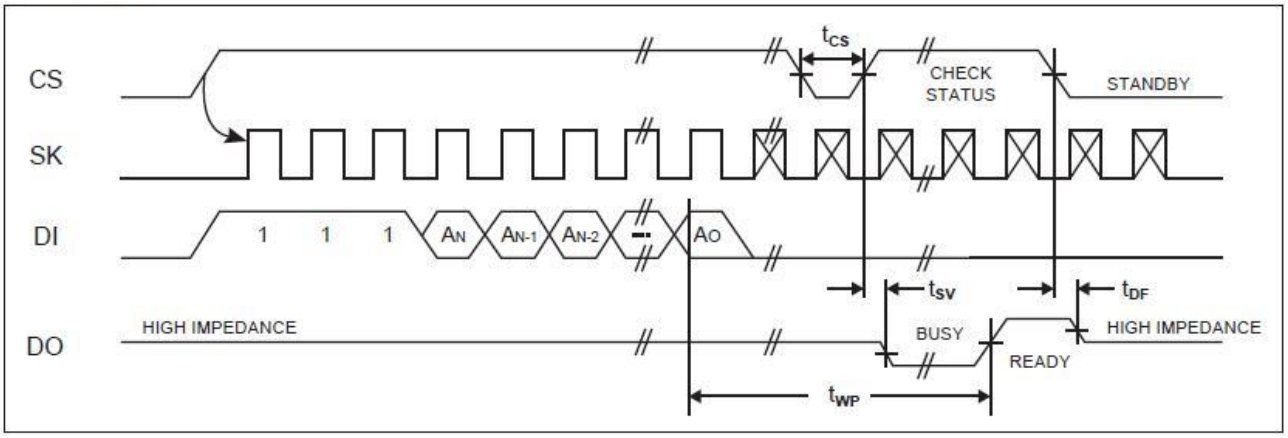
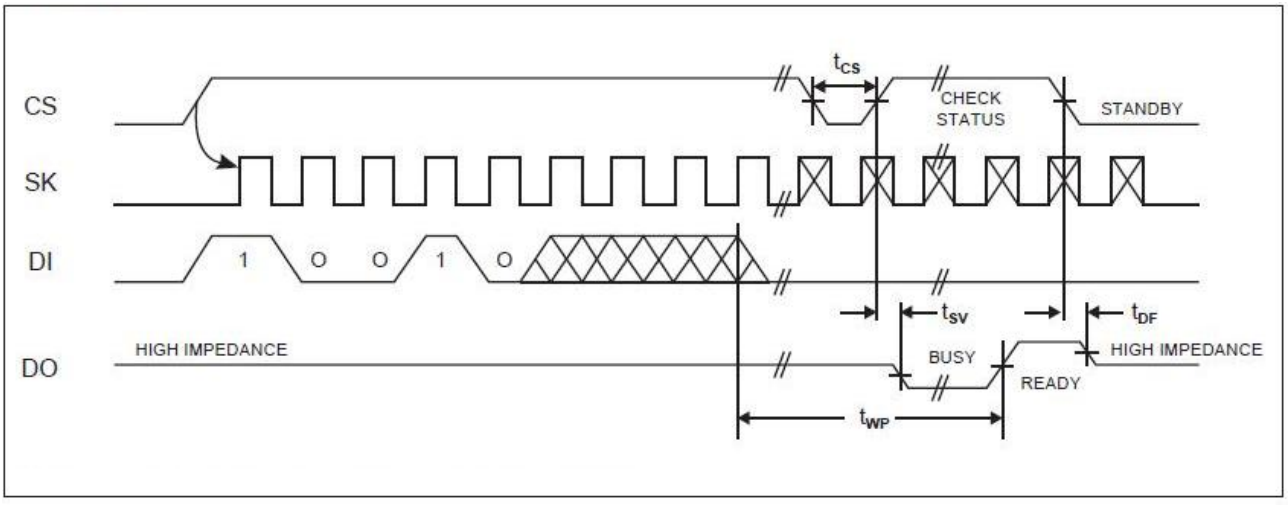
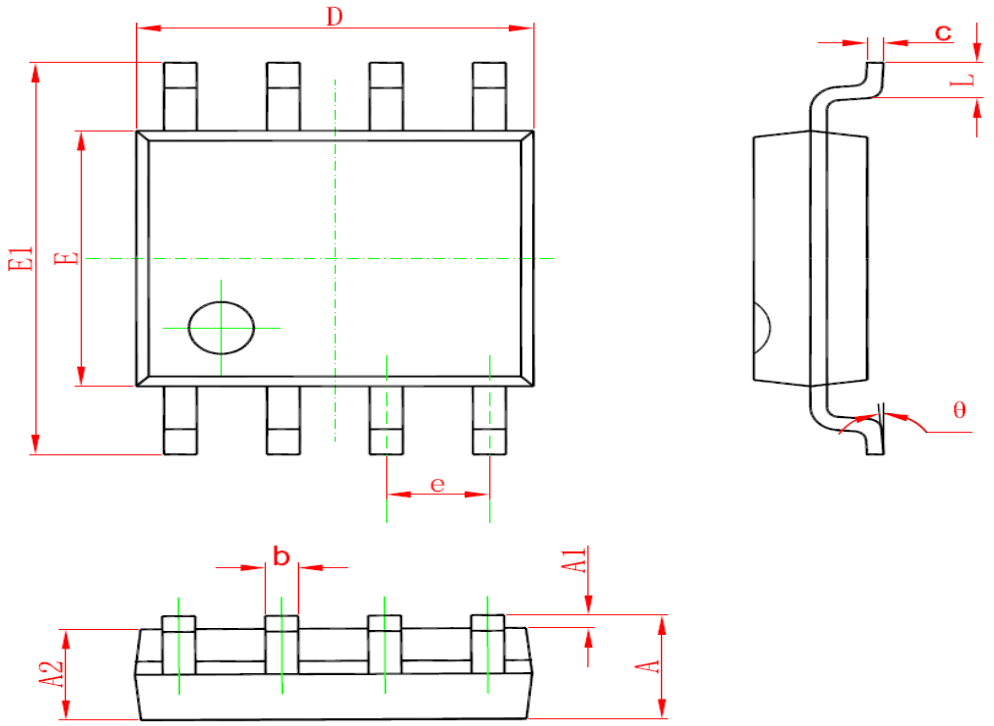


Fig8. ERAL Timing (Valid only at V_{CC}=4.5V to 5.5V)



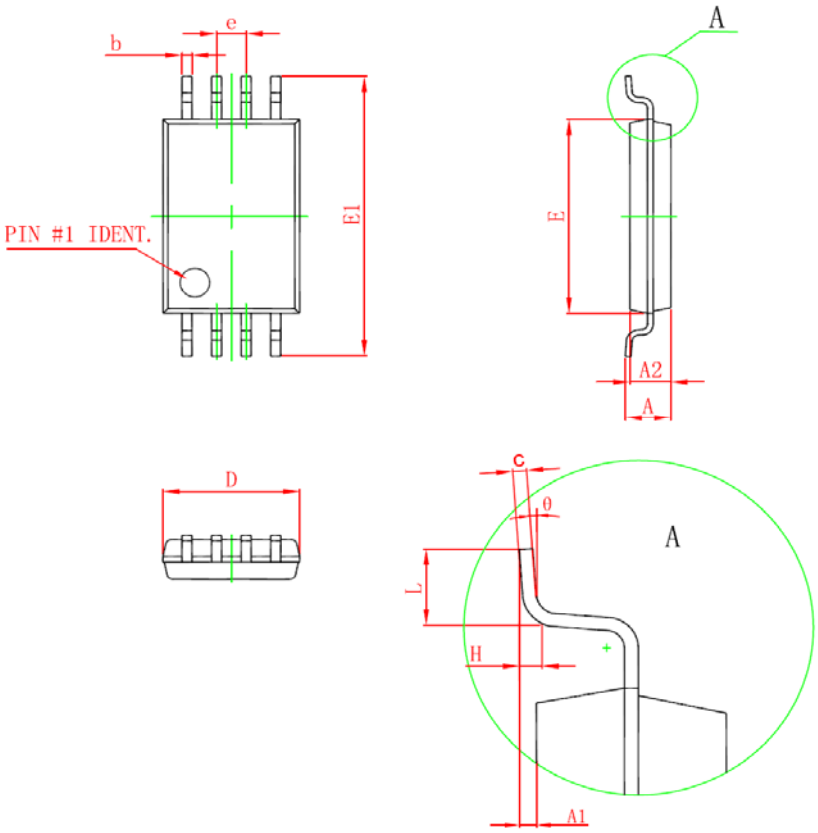
PACKAGE INFORMATION

Dimension in SOP8 (Unit: mm)



Symbol	Min	Max
A	-	1.770
A1	0.080	0.280
A2	-	1.770
b	0.440	0.530
c	0.210	0.260
D	4.700	5.100
E	3.700	4.100
E1	5.800	6.200
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

Dimension in TSSOP8 (Unit: mm)



Symbol	Min	Max
D	2.830	3.030
E	4.300	4.500
b	0.200	0.280
c	0.090	0.200
E1	6.200	6.600
A	-	1.200
A2	0.900	1.050
A1	0.050	0.150
e	0.65 (BSC)	
L	0.450	0.750
H	0.25(TYP)	
θ	0°	8°

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