Document Title

A9129 Data Sheet, sub1GHz SoC

Revision History

Rev. No.	History	Issue Date	Remark
0.1	Initial issue.	Feb., 2014	Objective
0.2	Update pin definition, registers and application circuit	Sep., 2014	Preliminary
0.3	Update pin definition, registers and application circuit	Dec., 2014	Preliminary
0.4	Update interference data, add AES/CCM description, correct the power management table 19.1, update RSSI curve	Feb., 2015	Preliminary
0.5	Add RX sensitivity value for 433MHz/915MHz. Delete output power range. Add maximum output power, RF power control range. Fix typo. in chapter 8.	Dec., 2015	Preliminary
0.6	Add 13.4 serial baud rate for SBRG_EN. Remove “open drain”. Modify recommended VTH in 9.2.4.1. Add note for BODF bit setting in 10.5. Revise electrical spec in chapter 3 & 8.	Mar., 2016	Preliminary
0.7	Correct error in 9.2.64, 9.2.68~9.2.70, 9.2.160.	Jun., 2016	Preliminary
0.8	Correct error in 9.2.18, 9.2.19. Add note for CKO bit setting in 9.2.45.	Aug., 2016	Preliminary
0.9	Update WOR1 register	Nov., 2016	Preliminary

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1. General Description

A9129 is a high performance and low cost Sub1GHz ISM band system-on-chip (SoC) wireless transceiver. This device integrates high speed pipeline 8051 MCU, 16KBytes In-system programmable flash memory, 4KB SRAM, various powerful functions and excellent performance of Sub1GHz GFSK/FSK transceiver. A9129 has various operating modes, making it highly suited for systems where ultra-low power consumption is required. A9129 has an 8bit ADC for RSSI and 8 channel 12bit ADC for general purpose. Three kinds of serial communication port (SPI, I^2C and UART) can interact with other device(s).

A9129 is one of AMICCOM sub1GHz family. It integrates AMICCOM sub1GHz transceiver well and offers a low cost solution with advanced radio features such as high output power amplifier up to 10 dBm (433MHz band, excluding LPF and HPF) and low noise receiver (-110dBm @50Kbps). Therefore, A9129 is very suitable for long LOS (line-of-sight) applications without the need to add an external LNA or PA.

The on-chip data rate divider supports programmable on-air data rates from 2K to 250Kbps to satisfy different system requirements. For a battery powered system, A9129 supports fast settling time to reduce average power consumption.

2. Typical Applications

- Wireless sensor networks
- Industrial monitoring and control
- Wireless alarm and security system
- Wireless ISM band data communication
- Remote control
- Home and building automation

3. Features

- Small Package size (QFN6 X6, 48 pins).
- High performance pipeline complicated 8051
- Operation clock: 1, 1/2, 1/4, 1/8, 1/16, 1/32 of crystal oscillator.
- 16KB Flash memory, 4KB SRAM
- UART, I^2C, SPI serial communication
- Three 16/8-bit counter/timers
- Two channel PWM
- Watchdog timer
- Sleep timer
- In-Circuit Debugger
- In-System programming/ In-Application programming
- 32 GPIO
- 8 channel 12bit SAR ADC
- One channel 8 bit ADC for RSSI and battery detect
- Programmable threshold of carrier detect.
- Frequency band: 315/433/470/868/915 MHz.
- FSK and GFSK modulation.
- Programmable data rate from 2Kbps to 250Kbps.
- RX Current consumption (AGC Off) 868MHz: 7.9mA.
- TX Current consumption 868MHz: 25mA @ 10dBm.
- PM3 mode without Sleep timer (1.6 uA).
- On chip regulator, support input voltage 2.0 ~ 3.6 V.
- High RX sensitivity 868MHz.
  - -109dBm at 50Kbps on-air data rate.
  - -106dBm at 100Kbps on-air data rate.
  - -105dBm at 150Kbps on-air data rate.
  - -102dBm at 250Kbps on-air data rate.
- Support low cost crystal (12.8 MHz /16 MHz /19.2MHz).
- Support RTC clock 32.768KHz
- Fast PLL settling time (120 us).
- 9-bits Digital RSSI and Auto RSSI measurement
- Auto Calibrations.
- Auto CRC and Filtering
- HW AES128 to support CCM* security.
- On-chip full range VCO and Fractional-N PLL synthesizer.

- On-chip low power RC oscillator for WOR (Wake on RX) function.
- AFC (Auto Frequency Compensation) for frequency drift due to Xtal aging.
- Separated 64 bytes FIFO for RX and TX.
- Built-in Battery Detect, Thermal Sensor and Crystal load capacitors.

4. Pin Configurations

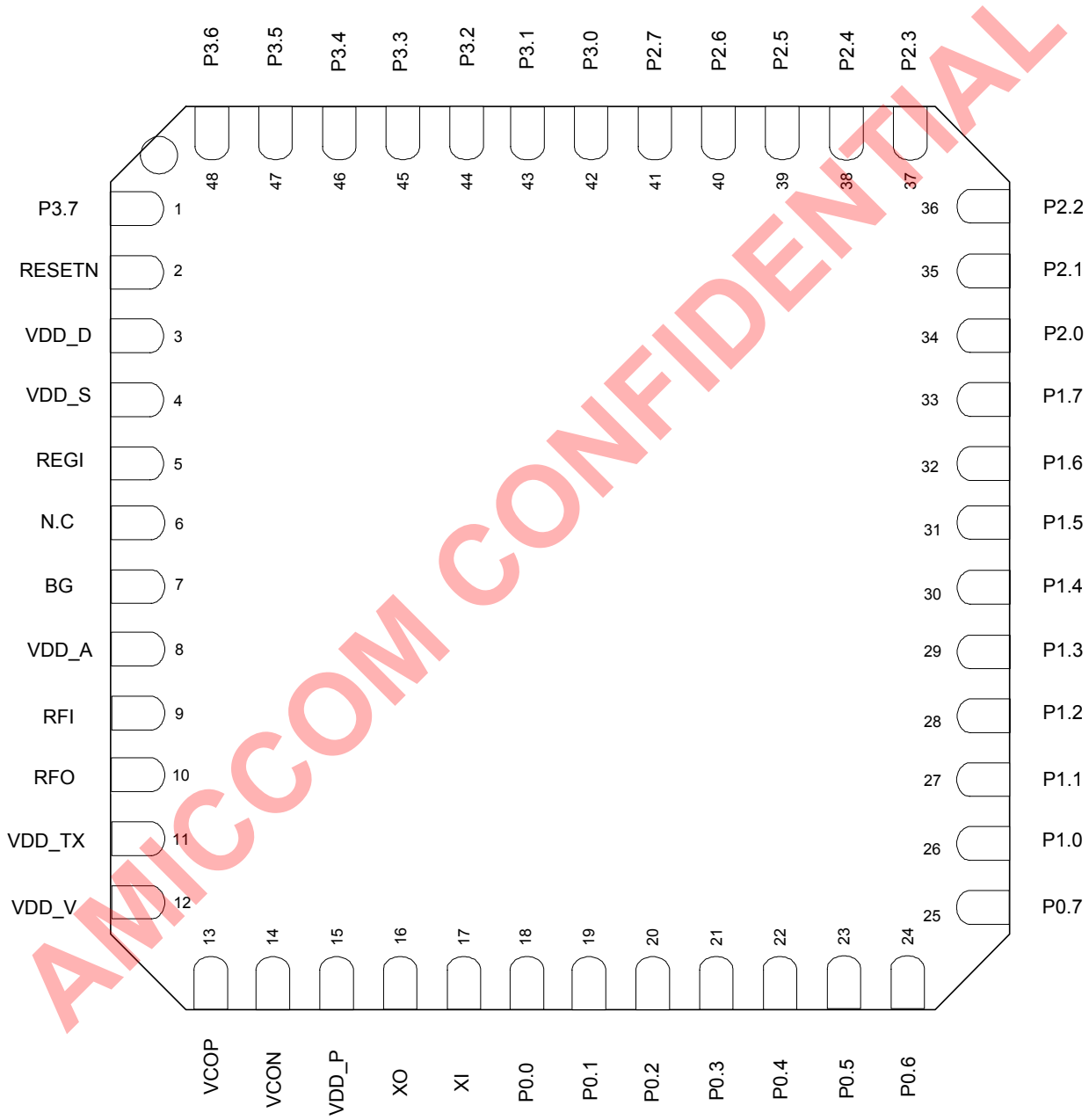


Figure 4.1 A9129 QFN 6x6 Package Top View

5. Pin Descriptions (I: input; O: output, I/O: input or output)

Pin No.	Symbol	I/O	Function Description
1	P3.7	DIO	RTC_O
2	RESETN	I	RESETN input
3	VDD_D	O	VDD_D supply voltage output
4	VDD_S	O	VDD_S supply voltage output
5	REGI	I	Regulator input
6	N.C		
7	BG	O	Band gap output
8	VDD_A	O	VDD_A supply voltage output
9	RFI	I	RF input
10	RFO	O	RF output
11	VDD_TX	O	TX supply voltage output.
12	VDD_V	I	VCO supply voltage input.
13	VCOP	O	VCO tank positive pin.
14	VCON	O	VCO tank negative pin.
15	VDD_P	I	PLL supply voltage output
16	XO	O	Crystal oscillator output.
17	XI	I	Crystal oscillator input.
18	P0.0	DIO	SPI_SCLK
19	P0.1	DIO	SPI_MOSI
20	P0.2	DIO	SPI_MISO
21	P0.3	DIO	SPI_SSEL
22	P0.4	DIO	GPIO/ ICE mode
23	P0.5	DIO	I2C_SCL
24	P0.6	DIO	I2C_SDA
25	P0.7	DIO	INT2 /GIO1
26	P1.0	DIO	Timer2_T2/IN1
27	P1.1	DIO	Timer2_T2EX/CS1
28	P1.2	DIO	INT3 /GIO2/RS1
29	P1.3	DIO	INT4/ CKO/RT1
30	P1.4	DIO	TTAG_TTDIO
31	P1.5	DIO	TTAG_TTCK
32	P1.6	DIO	PWM0
33	P1.7	DIO	PWM1
34	P2.0	DIO/AI	ADC4
35	P2.1	DIO/AI	ADC5
36	P2.2	DIO/AI	ADC6
37	P2.3	DIO/AI	ADC7
38	P2.4	DIO	
39	P2.5	DIO	
40	P2.6	DIO	
41	P2.7	DIO	
42	P3.0	DIO	UART0_RX
43	P3.1	DIO	UART0_TX
44	P3.2	DIO	INT0/ADC0
45	P3.3	DIO	INT1/ADC1
46	P3.4	DIO	Timer0_T0/ADC2
47	P3.5	DIO	Timer1_T1/ADC3
48	P3.6	DIO	RTC_I
	Back side plate	G	Ground. Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.

6. Chip Block Diagram

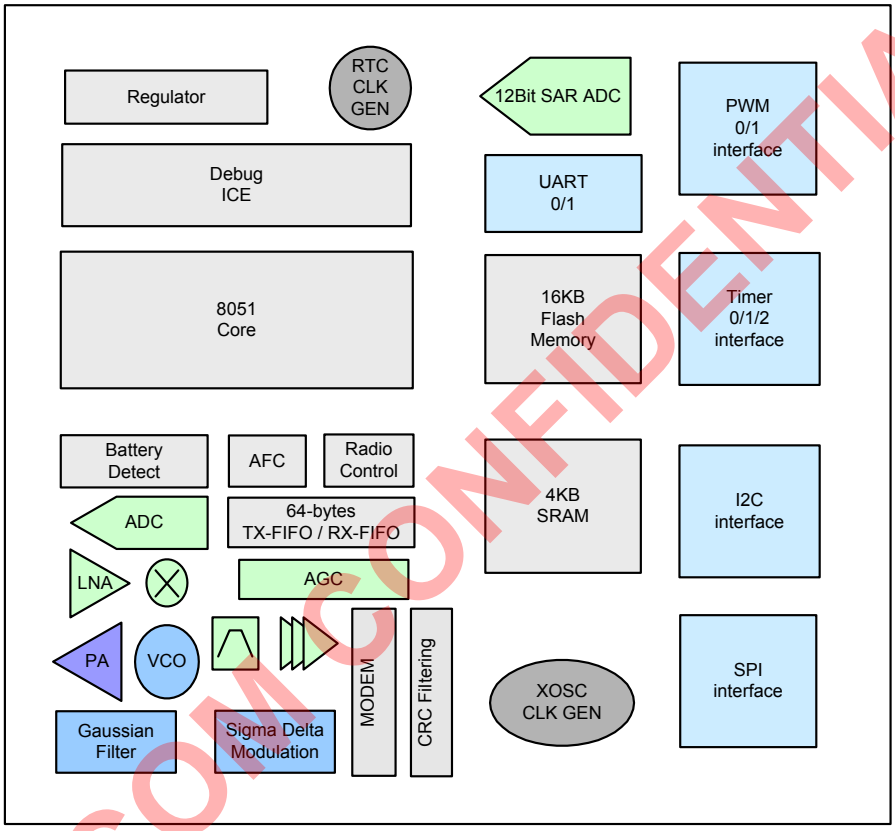


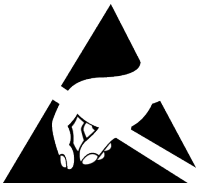
Figure 6.1 A9129 Block Diagram

7. Absolute Maximum Ratings

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD)	GND	-0.3 ~ 3.6	V
Digital IO pins range	GND	-0.3 ~ VDD+0.3	V
Voltage on the analog pins range	GND	-0.3 ~ 2.1	V
Input RF level		14	dBm
Storage Temperature range		-55 ~ 125	°C
ESD Rating	HBM	± 2K	V
	MM	± 200	V

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.
*VCOP、VCON pins pass HBM +/- 1KV. RFO pin passes MM <-25V.
*Device is Moisture Sensitivity Level III (MSL 3).



8. Electrical Specification

(Ta=25℃, VDD=3.3V, data rate= 100Kbps, F_{XTAL} =12.8MHz, On Chip Regulator = 1.8V, PN9 pattern, with matching network and low pass filter, unless otherwise noted.)

Parameter	Description	Min.	Typ.	Max.	Unit
General					
Operating Temperature		-40		85	℃
Supply Voltage (VDD)	Regulator supply input	2.0	3.3	3.6	V
Current Consumption (MCU in stop mode and RF in sleep mode)	PM2 mode with Sleep timer		4.1		μA
	PM3 mode with Sleep timer		2.1		μA
	PM3 mode without Sleep timer		1.6		μA
Current Consumption (MCU in normal mode) 433MHz band MCU Clock @ 12.8MHz	Sleep Mode		3.2		mA
	Standby Mode		3.35		mA
	PLL Mode(CG off)		4.9		mA
	RX Mode (AGC Off)		7.1		mA
	RX Mode (AGC ON)		7.3		mA
	TX 10.5dBm (TBG=48, TDC=2, PAC=0)		22		mA
Current Consumption (MCU in normal mode) 433MHz band MCU Clock @ 0.8MHz	Sleep Mode		1.0		mA
	Standby Mode		1.15		mA
	PLL Mode(CG off)		2.7		mA
	RX Mode (AGC Off)		4.9		mA
	RX Mode (AGC ON)		5.1		mA
	TX 10.5dBm (TBG=48, TDC=2, PAC=0)		19.5		mA
Current Consumption (MCU in normal mode) 868MHz band MCU Clock @ 12.8MHz	PLL Mode(CG off)		5.5		mA
	RX Mode (AGC Off)		7.9		mA
	RX Mode (AGC ON)		8.1		mA
	TX 10dBm (TBG=48, TDC=2, PAC=0)		25		mA
Synthesizer block					
Crystal settling time	Idle to standby (XTAL 49US)		0.5		ms
Crystal frequency	General case		12.8/16/19.2		MHz
	Data rate = 250Kbps		16		MHz
	Data rate = 32.768K or 16.384Kbps		12.582912		MHz
	Data rate = 38.4Kbps		19.6608		MHz
Crystal tolerance			±20		ppm
Crystal Load Capacitance			20		pF
Crystal ESR				100	ohm
PLL settling time @settle to 25kHz	Standby to PLL		120		μs
Transmitter					
Maximum Output Power	433MHz (excluding LPF and HPF)		10		dBm
	868MHz (excluding LPF and HPF)		10		dBm
RF Power Control Range	433MHz (excluding LPF and HPF)		40		dB
	868MHz (excluding LPF and HPF)		40		dB
Out Band Spurious Emission 1. Pout = 12 dBm 2. With LPF and HPF	f < 1GHz (RBW =100kHz)			-36	dBm
	47MHz< f <74MHz 87.5MHz< f <118MHz 174MHz< f <230MHz 470MHz< f <862MHz (RBW =100kHz)			-54	dBm

	Above 1GHz (RBW = 1MHz)			-30	dBm
	2nd Harmonic			-30	dBm
	3rd Harmonic			-30	dBm
TX settling time	PLL to TX		80		μs
Receiver					
433MHz RX Sensitivity @BER=0.1% high gain mode	50kbps (Fdev = 18.75KHz)		-110		dBm
	100kbps (Fdev = 37.5KHz)		-108		
	150kbps (Fdev = 56.25KHz)		-106		
	250kbps (Fdev = 93.75KHz) ,16MHz Xtal		-102		
868MHz RX Sensitivity @BER=0.1% high gain mode	50kbps (Fdev = 18.75KHz)		-109		dBm
	100kbps (Fdev = 37.5KHz)		-106		
	150kbps (Fdev = 56.25KHz)		-105		
	250kbps (Fdev = 93.75KHz),16MHz Xtal		-102		
915MHz RX Sensitivity @BER=0.1% high gain mode	50kbps (Fdev = 18.75KHz)		-108		dBm
	100kbps (Fdev = 37.5KHz)		-105		
	150kbps (Fdev = 56.25KHz)		-103		
	250kbps (Fdev = 93.75KHz),16MHz Xtal		-101		
IF Filter bandwidth	50K Mode (10 ppm Xtal needed)		50		KHz
	100K Mode		100		
	150K Mode		150		
	250K Mode		250		
IF center frequency	50K Mode		100		KHz
	100K Mode		200		
	150K Mode		300		
	250K Mode		500		
Interference (915MHz, 100Kbps)	Co-channel (C/I)		14		dB
	ACR1 (C/I_{ch1})		-21		dB
	ACR2 (C/I_{ch2})		-37		dB
	Offset ± 10MHz		-50		dB
Maximum Operating Input Power	@ RF input (BER = 0.1%)			10	dBm
RX Spurious Emission	25MHz ~ 1GHz			-57	dBm
	Above 1GHz			-47	dBm
RSSI Range	AGC on	-110		-30	dBm
RX Settling Time	PLL to RX		30		μs
	Standby to RX		250		μs
12Bit SAR ADC					
Input voltage range		0		1.8	V
External reference voltage			1.8		V
Input capacitor			25		pF
Bandwidth			200		KHz
EOB, effective number of bits			10		Bit
INL			-/+ 2		LSB
DNL			-/+ 1		LSB
Conversion time		8		128	μs
Current consumption			0.4		mA
Regulator					
Regulator settling time	Pin 7 connected to 1nF		350		μs
Band-gap reference voltage			0.6		V
Regulator output voltage(VDDA)		1.8	1.8	2.1	V

Digital IO DC characteristics					
High Level Input Voltage (V_{IH})		0.7*VDD		VDD	V
Low Level Input Voltage (V_{IL})		0		0.3*VDD	V
High Level Output Voltage (V_{OH})	@I_{OH}= -0.5mA	VDD-0.4		VDD	V
Low Level Output Voltage (V_{OL})	@I_{OL}= 0.5mA	0		0.4	V

Power on Reset Electrical Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		REGI	Condition				
V_{POR}	REGI Start Voltage to ensure Power-on Reset	—	—	—	—	100	mV
$R_{POR\ AC}$	REGI Raising Rate to ensure Power-on Reset	—	—	0.04	—	—	V/ms
t_{POR}	Minimum Time for REGI to remain at V_{POR} to ensure Power-on Reset	—	—	3	—	—	ms

9. SFR & RFR(Radio Frequency Register)

A9129 contains standard 8051 SFRs(special function registers) and RFR (RF control registers). A9129's SFR location is almost the same as the standard 8052 SFR location. RFR is Radio Frequency Registers are located in XDATA spaces and located in 0x0800 ~ 0x08FF. For more detail information, please reference Section 9.2.

9.1 SFR Overview

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	EIP	OSCCON						
0xF0	B	I2CSADR	I2CSCR	I2CSBUF	I2CMSA	I2CMCR	I2CMBUF	I2CMTP
0xE8	EIE				SPCR	SPSR	SPDR	SSCR
0xE0	ACC	P3OE	P3PUN	P3WUN	SPCR1	SPSR1	SPDR1	SSCR1
0xD8	WDCON	P1OE	P1PUN	P1WUN				
0xD0	PSW	P0OE	P0PUN	P0WUN				
0xC8	T2CON	T2IF	RLDL	RLDH	TL2	TH2		DEVICR
0xC0								
0xB8	IP	PCONE	RSFLAG	IOSEL				
0xB0	P3	PWM1CON	PWM1H	PWM1L				
0xA8	IE	PWM0CON	PWM0H	PWM0L				
0xA0	P2							
0x98	SOCN0	SBUF0	FLSHCTRL	FLSHTMR	FLSHTPG	FLSHTER		
0x90	P1	EIF					DPS1DPH	DPS1DPL
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	DPS1PL
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON

Table 9.1 A9129 Special Function Registers (SFRs) table

: It means bit-addressable
: It means reserved.

Following are description of SFRs related to the operation of A9129 System Controller. Detailed descriptions of the remaining SFRs are including the sections of the datasheet associated with their corresponding system function. The arithmetic section of the processor performs extensive data manipulation and is comprised of the 8-bit arithmetic logic unit (ALU), an ACC(0xE0) register, B(0xF0) register and PSW(0xD0) register.

PSW (Address: D0h)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D0h PSW	R/W	CY	AC	F0	RS1	RS2	OV	F1	P
Reset		0	0	0	0	0	0	0	0

Program Status Word register

The ALU performs typical arithmetic operations as: addition, subtraction, multiplication, division and additional operations such as: increment, decrement, BCD-decimal-add-adjust and compare. Within logic unit are performance: AND, OR, Exclusive OR, complement and rotation. The Boolean processor performance the bit operations as: set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry.

CY - Carry flag
AC - Auxiliary carry
F0 - General purpose flag 0
RS[1:0] - Register bank select bits

RS[1:0]	Function description
00	- Bank 0, data address 0x00-0x07
01	- Bank 1, data address 0x08-0x0F
10	- Bank 2, data address 0x10-0x17
11	- Bank 3, data address 0x18-0x1F

OV - Overflow flag
F1 - General purpose flag 1
P - Parity flag
The PSW contains several bits that reflect the current state of the CPU.

ACC (Address: E0h)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E0h ACC	R/W								
Reset		0	0	0	0	0	0	0	0

Accumulator ACC Register

B (Address: F0h)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F0h B	R/W								
Reset		0	0	0	0	0	0	0	0

B Register

The B register is used during multiply and divide operations. In other cases may be used as normal SFR.

9.2 RFR Overview

Control Register Table

Address / Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1000h RSTCTL	W	RESETN	FWPRN	FRPRN	ADC12RN	FIFORN	BFCRN	--	--
	R	PWR	FECF	CRCF	CER	XER	PLLER	TRSR	TRER
0x1001h MODEC1	W	STRB7	STRB6	STRB5	STRB4	STRB3	STRB2	STRB1	STRB0
	R	ARCWTR	P_CKO	P_IRQ1O	P_IRQ2O	FPF	FSYNC	ENC_FLAG	--
0x1002h MODEC2	W/R	XEC	CCE	FMS	WOR_EN	FMT	--	HBS	ADCM
0x1003h MODEC3	W/R	FIFOREV	MSCD	VBS	SWT	VCC	VBC	FBC	RSSCR
0x1004h CAL1	W	MSCRC	VTL2	VTL1	VTL0	VTH2	VTH1	VTH0	MVBS
	R	FCD4	FCD3	FCD2	FCD1	FCD0	VB2	VB1	VB0
0x1005h	W	MVB2	MVB1	MVB0	MFBS	MFB3	MFB2	MFB1	MFB0

CAL2	R	DVT1	DVT0	VBCF	FBCF	FB3	FB2	FB1	FB0
0x1006h FIFO1	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
0x1007h FIFO2	W	FPM1	FPM0	TPSA5	TPSA4	TPSA3	TPSA2	TPSA1	TPSA0
0x1008h RCOSC1	W	RCOT2	RCOT1	RCOT0	MVS1	MVS0	MCALS	MAN	ENCAL
	R	NUMLH11	NUMLH10	NUMLH9	NUMLH8	VBD	RCOC9	RCOC8	ENCAL
0x1009h RCOSC2	W	--	--	--	--	RCTPUN	SLPO	MRCT9	MRCT8
	R	NUMLH7	NUMLH6	NUMLH5	NUMLH4	NUMLH3	NUMLH2	NUMLH1	NUMLH0
0x100Ah RCOSC3	W	MRCT7	MRCT6	MRCT5	MRCT4	MRCT3	MRCT2	MRCT1	MRCT0
0x100Bh RCOSC4	W	RCTS	XCC32K	XCP32K1	XCP32K0	TGNUM11	TGNUM10	TGNUM9	TGNUM8
0x100Ch RCOSC5	W	TGNUM7	TGNUM6	TGNUM5	TGNUM4	TGNUM3	TGNUM2	TGNUM1	TGNUM0
0x100Dh SYCK1	W/R	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
0x100Eh SYCK2	W/R	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS
0x100Fh PLL1	W	IP8	CRCINV	CHF2I	CHI2I	CHF1	CHF0	CHI1	CHI0
0x1010h PLL2	W	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
0x1011h PLL3	W	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8
0x1012h PLL4	W	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
0x1013h PLL5	W	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8
	R	AFC	FC[14:8]						
0x1014h PLL6	W	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0
	R	FC[7:0]							
0x1015h PLL7	W	CPS	XCC	CKX2	INTLP	PDLY2	PDLY1	PDLY0	MD0
0x1016h PLL8	W	ADCR	VCI	TXDBG	ISDIV	SDPW1	SDPW0	NSDO	EDI
0x1017h PLL9	W	VICMP	IA14	IA13	IA12	IA11	IA10	IA9	IA8
0x1018h PLL10	W	IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0
0x1019h PLL11	W	RFC3	RFC2	RFC1	RFC0	RIC11	RIC10	RIC9	RIC8
0x101Ah PLL12	W	RIC7	RIC6	RIC5	RIC4	RIC3	RIC2	RIC1	RIC0
0x101Bh CLOCK	W	HFB	EDIVS	XCP1	XCP0	INTXC	RBS	CGS	XS
	R	--	--	--	--	--	--	CGS	XS
0x101Ch TX1	W	TXDI	TDC1	TDC0	TME	GS	FDP2	FDP1	FDP0

0x101Dh TX2	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
0x101Eh TX3	W	MCNTR	DPRY2	DPRY1	DPRY0	BT1	BT0	TDLY1	TDLY0
0x101Fh TX4	W	PAC1	PAC0	TBG5	TBG4	TDC0	TBG2	TBG1	TBG0
0x1020h WOR1	W	WRDLY9	WRDLY8	WRDLY5	WRDLY4	WRDLY3	WRDLY2	WORDLY1	WORDLY0
0x1021h WOR2	W	WORDLY7	WORDLY6	WORDLY5	WORDLY4	WORDLY3	WORDLY2	WORDLY1	WORDLY0
0x1022h WOR3	W	LFIFOREV	WOR_SEL	RS_DLY2	RS_DLY1	RS_DLY0	AGC_DLY1	AGC_DLY0	WOR_CD
0x1023h WOR4	W	WORS3	WORS2	WORS1	WORS0	WOR_S	TMRE	TSEL	TWOR
0x1024h RFI1	W	CDSEL1	CDSEL0	PRRC1	PRRC0	RSM1	RSM0	RMP1	RMP0
	R	RHM[7:0]							
0x1025h RFI2	W	QCLIM	TRT2	TRT1	TRT0	ASMV2	ASMV1	ASMV0	AMVS
	R	RLM[7:0]							
0x1026h PM1	W	RC_DLY2	RC_DLY1	RC_DLY0	CELS	RGC1	RGC0	STS	QDP
0x1027h PM2	W	SPSS	RGV1	RGV0	BVT2	BVT1	BVT0	PRE_S	BDS
	R	--	--	--	--	--	--	VBD	BODF
0x1028h RTH1	W	IRTH7	IRTH6	IRTH5	IRTH4	IRTH3	IRTH2	IRTH1	IRTH0
0x1029h RTH2	W	IRTL7	IRTL6	IRTL5	IRTL4	IRTL3	IRTL2	IRTL1	IRTL0
0x102Ah AGC1	W	EXTL	VRSEL	MS	MSCL4	MSCL3	MSCL2	MSCL1	MSCL0
	R	--	--	LGC1	LGC0	MGC1	MGC0	IGC1	IGC0
0x102Bh AGC2	W	HDM	AGCE	ERSSM	EXRSI	LGM1	LGM0	MGM1	MGM0
0x102Ch AGC3	W	RGVA1	RGVA0	RGVT1	RGVT0	LHM1	LHM0	MHM1	MHM0
	R	--	--	--	--	LHM1	LHM0	MHM1	MHM0
0x102Dh AGC4	W	IGM1	IGM0	CA1	CA0	RSAGC1	RSAGC0	TXIB1	TXIB0
0x102Eh CKO1	W	XCL4	XCL3	XCL2	XCL1	XCL0	WSEL2	WSEL1	WSEL0
0x102Fh CKO2	W		CKOSM3	CKOSM2	CKOSM1	CKOSM0	CKOIM	CKOEM	SCT
0x1030h GPIO1	W	WRCKS	STRR	IRQ1SM3	IRQ1SM2	IRQ1SM1	IRQ1SM0	IRQ1IM	IRQ1OEM
0x1031h GPIO2	W	MCNT1	MCNT0	IRQ2SM3	IRQ2SM2	IRQ2SM1	IRQ2SM0	IRQ2IM	IRQ2OEM
0x1032h PIN1	W	RFT2	RFT1	RFT0	PRS	SCMDS	WMODE	INFS	SCKI
0x1033h PIN2	W	IRQI	IRQS1	IRQS0	IRQOE	CKOIK	CKOSK1	CKOSK0	CKOEK
0x1034h	W	CDTM1	CDTM0	FEP13	FEP12	FEP11	FEP10	FEP9	FEP8

VCB1	R	--	--	--	VCCF	VCBR[3:0]			
0x1035h VCB2	W	PKT1	PKT0	PKS	RVCOC3	RVCOC2	RVCOC1	RVCOC0	MVCS
0x1036h CHG1	W/R	CBG2	CBG1	CBG0	QDTX	FPL3	FPL2	FPL1	FPL0
0x1037h CHG2	W/R	IPL7	IPL6	IPL5	IPL4	IPL3	IPL2	IPL1	IPL0
0x1038h CHG3	W/R	CSLP1	CSLP0	MSLP	RSLP	FPH3	FPH2	FPH1	FPH0
0x1039h CHG4	W/R	IPH7	IPH6	IPH5	IPH4	IPH3	IPH2	IPH1	IPH0
0x103Ah IF1	W	AIF	IFOA14	IFOA13	IFOA12	IFOA11	IFOA10	IFOA9	IFOA8
0x103Bh IF2	W	IFOA7	IFOA6	IFOA5	IFOA4	IFOA3	IFOA2	IFOA1	IFOA0
0x103Ch IF3	W	FPA15	FPA14	FPA13	FPA12	FPA11	FPA10	FPA9	FPA8
0x103Dh IF4	W	FPA7	FPA6	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0
0x103Eh ACK1	W	MRCKS	RNUM3	RNUM2	RNUM1	RNUM0	CDRS1	CDRS0	SYNCS
	R	-	--	ARTEF	VPOAKF	RCR[3:0]			
0x103Fh ACK2	W/R	VKM	VKP	ARTMS	ARC3	ARC2	ARC1	ARC0	EARKS
0x1040h ART1	W/R	RND7	RND6	RND5	RND4	RND3	RND2	RND1	RND0
0x1041h ART2	W/R	ARD7	ARD6	ARD5	ARD4	ARD3	ARD2	ARD1	ARD0
0x1042h SYN1	W	CST	WHT9	CRC16	CRCSW1	CRCDNP1	-	EACKF	DC_SEL
	R	FC1BTX[7:0]							
0x1043h SYN2	W	FCL	EDRL	RNUM12	RNUM11	RNUM10	RCK_sel	dbuf_sel1	dbuf_sel0
	R	FC1BRX[7:0]							
0x1044h AFEP1	W	ACKFEP7	ACKFEP6	ACKFEP5	ACKFEP4	ACKFEP3	ACKFEP2	ACKFEP1	ACKFEP0
	R	--	LENFIFO[13:8]						
0x1045h AFEP2	W	WRDLY8	WRDLY7	WRDLY6	TX_1DLY4	TX_1DLY3	TX_1DLY2	TX_1DLY1	TX_1DLY0
	R	LENFIFO[7:0]							
0x1046h DC	W	-	-	-	-	-	-	-	-
	R	DCOUT[7:0]							
0x1047h LPS	W	-	-	-	-	INTLPS	INTLP_MAN	CAL_VBS	--
0x1048h AUX	W	HBHC	-	-	-	-	-	-	-
0x1049h WCK	W	WCKSEL1	WCKSEL0	B315	--	--	SYCKG	WOR_RST	WOR_HOLD
0x104Ch CDET1	W	CDTH17	CDTH16	CDTH15	CDTH14	CDTH13	CDTH12	CDTH11	CDTH10

0x104Dh CDET2		RGS	ADCCS	--	EXADVR	RCHC			CD_SEL
0x104Fh RX1	W	MLP1	MLP0	SLF2	SLF1	SLF0	ETH2	ETH1	ETH0
	R	--	--	--	--	--	--	--	ADCO[8]
0x1050h RX2	W	DMT	DMOS	DMG1	DMG0	BW1	BW0	ULS	RXDI
	R	ADCO[7:0]]							
0x1051h RX3		DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0
0x1052h RX4		PMD2	PMD1	PMD0	DCL2	DCL1	DCL0	DCM1	DCM0
0x1053h CODE1	W	WS6	WS5	WS4	WS3	WS2	WS1	WS0	MCS
0x1054h CODE2	W	WHTS	FECS	CRCS	PML2	PML1	PML0	IDL1	IDL0
0x1055h ADC1	W	ARSSI	RADC	AVS1	AVS0	MVSEL1	MVSEL0	XADSR	CDM
0x1056h ADC2	W	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
	R	ADC[7:0]							
0x1057h ID0	W/R	IDR[63:56]							
0x1058h ID1	W/R	IDR[55:48]							
0x1059h ID2	W/R	IDR[47:40]							
0x105Ah ID3	W/R	IDR[39:32]							
0x105Bh ID4	W/R	IDR[31:24]							
0x105Ch ID5	W/R	IDR[23:16]							
0x105Dh ID6	W/R	IDR[15:8]							
0x105Eh ID7	W/R	IDR[7:0]							
0x105Fh DID0	R	DID[31:24]							
0x1060h DID1	R	DID[23:16]							
0x1061h DID2	R	DID[15:8]							
0x1062h DID3	R	DID[7:0]							
0x1063h NONCE0	W/R	NONCE[135:128]							
0x1064h NONCE1	W/R	NONCE[127:120]							
0x1065h NONCE2	W/R	NONCE[119:112]							
0x1066h NONCE3	W/R	NONCE[111:104]							
0x1067h NONCE4	W/R	NONCE[103:96]							

0x1068h NONCE5	W/R	NONCE[95:88]
0x1069h NONCE6	W/R	NONCE[87:80]
0x106Ah NONCE7	W/R	NONCE[79:72]
0x106Bh NONCE8	W/R	NONCE[71:64]
0x106Ch NONCE9	W/R	NONCE[63:56]
0x106Dh NONCE10	W/R	NONCE[55:48]
0x106Eh NONCE11	W/R	NONCE[47:40]
0x106Fh NONCE12	W/R	NONCE[39:32]
0x1070h NONCE13	W/R	NONCE[31:24]
0x1071h NONCE14	W/R	NONCE[23:16]
0x1072h NONCE15	W/R	NONCE[15:8]
0x1073h NONCE16	W/R	NONCE[7:0]
0x1074h AESK0	W/R	AES_KEY[127:120]
0x1075h AESK1	W/R	AES_KEY [119:112]
0x1076h AESK2	W/R	AES_KEY [111:104]
0x1077h AESK3	W/R	AES_KEY [103:96]
0x1078h AESK4	W/R	AES_KEY [95:88]
0x1079h AESK5	W/R	AES_KEY [87:80]
0x107Ah AESK6	W/R	AES_KEY [79:72]
0x107Bh AESK7	W/R	AES_KEY [71:64]
0x107Ch AESK8	W/R	AES_KEY [63:56]
0x107Dh AESK9	W/R	AES_KEY [55:48]
0x107Eh AESK10	W/R	AES_KEY [47:40]
0x107Fh AESK11	W/R	AES_KEY [39:32]
0x1080h AESK12	W/R	AES_KEY [31:24]
0x1081h AESK13	W/R	AES_KEY [23:16]
0x1082h AESK14	W/R	AES_KEY [15:8]
0x1083h AESK15	W/R	AES_KEY [7:0]
0x1084h	W	AES_DIN [127:120]

AESD0	R	AES_DOUT[127:120]
0x1085h AESD1	W	AES_DIN [119:112]
	R	AES_DOUT[119:112]
0x1086h AESD2	W	AES_DIN [111:104]
	R	AES_DOUT[111:104]
0x1087h AESD3	W	AES_DIN [103:96]
	R	AES_DOUT[103:96]
0x1088h AESD4	W	AES_DIN [95:88]
	R	AES_DOUT[95:88]
0x1089h AESD5	W	AES_DIN [87:80]
	R	AES_DOUT[87:80]
0x108Ah AESD6	W	AES_DIN [79:72]
	R	AES_DOUT[79:72]
0x108Bh AESD7	W	AES_DIN [71:64]
	R	AES_DOUT[71:64]
0x108Ch AESD8	W	AES_DIN [63:56]
	R	AES_DOUT[63:56]
0x108Dh AESD9	W	AES_DIN [55:48]
	R	AES_DOUT[55:45]
0x108Eh AESD10	W	AES_DIN [47:40]
	R	AES_DOUT[47:40]
0x108Fh AESD11	W	AES_DIN [39:32]
	R	AES_DOUT[39:32]
0x1090h AESD12	W	AES_DIN [31:24]
	R	AES_DOUT[31:24]
0x109Ah AESD13	W	AES_DIN [23:16]
	R	AES_DOUT[23:16]
0x1092h AESD14	W	AES_DIN [15:8]
	R	AES_DOUT[15:8]
0x1093h	W	AES_DIN [7:0]

AESD15	R	AES_DOUT[7:0]							
0x1094h TXPKT0	W/R	TX_PACKET [15:8]							
0x1095h TXPKT1	W/R	TX_PACKET [7:0]							
0x1096h RXPKT0	W/R	RX_PACKET [15:8]							
0x1097h RXPKT1	W/R	RX_PACKET [7:0]							
0x1098h AESCTL0	W/R	CCM_TXEN_GO	CCM_RXDE_GO	CCM_RX_ON	AES_GO	--	--	--	CCM_TX_ON
0x1099h AESCTL1	W	TXPKT_R	RXDEC_A	CCM_RN	FBX	--	TXPKTS2	TXPKTS1	TXPKTS0
	R	--	--	CCM_OK_FLG	CCM_FAIL_FLG	--	--	--	--
0x109Ah ADCCTL	W	BUFS	CKS1	CKS0	MODE	MVS2	MVS1	MVS0	ADCE
	R	--	--	--	MODE	MVS2	MVS1	MVS0	ADCE
0x109Bh ADCAVG1	W	ADCIE	--	--	--	ADIVL	ADCYC	ENADC	DTMP
	R	MVADC11	MVADC10	MVADC9	MVADC8	ADC11	ADC10	ADC9	ADC8
0x109Ch ADCAVG2	R	MVADC7	MVADC6	MVADC5	MVADC4	MVADC3	MVADC2	MVADC1	MVADC0
0x109Dh ADCAVG3	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
0x109Eh TMRINV	W	TMR_INV[7]	TMR_INV[6]	TMR_INV[5]	TMR_INV[4]	TMR_INV[3]	TMR_INV[2]	TMR_INV[1]	TMR_INV[0]
0x109Fh TMRCTL	W	TMRON	TMRIE	TMRIF	--	TMRCKS[2]	TMRCKS[1]	TMRCKS[0]	TMR_CE
	R	--	TMRIE	TMRIF	--	--	--	--	--
0x10A0h INTIE	W	--	--	--	--	BBIE3	BBIE2	BBIE1	BBIE0
0x10A1h EXT1	W	EBOD	--	SVREF	CELA	PDNFHR	QDSFHR	PDNFLR	QDSFLR
0x10A2h EXT2	W	ENDL[2]	ENDL[1]	ENDL[0]	PDNS	ENAV	QDSA	ENDV	QDSD
0x10A3h EXT3	W	OPHC1	OPHC0	CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
0x10A4h EXT4	W	QDPA	PDNR	-	FBG4	FBG3	FBG2	FBG1	FBG0
0x10A5h EXT5	W	MXDM	MXDL	CMVS1	CMVS0	BFHC1	BFHC0	RGVP1	RGVP0
0x10A6h EXT6		-	-	STM[5:0]					
0x10A7h PA	W	PALY2[3:0]				PALY1[3:0]			

Legend: -- = unimplemented

Control Register Description

9.2.0 RSTCTL (Address: 0x1000h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSTCTL	W	RESETN	FWPRN	FRPRN	ADC12RN	FIFORN	BFCRN	--	--
	R	PWR	FECF	CRCF	CER	XER	PLLER	TRSR	TRER
Reset		0	0	0	0	0	0	0	0

RESETN: Software reset for baseband
FWPRN: Software reset for TX fifo pointer.
FRPRN: Software reset for RX fifo pointer.
FIFORN: Software reset for RX fifo.
BFCRN: Software reset for IF Filter Bank Calibration
ADC12RN: Software reset for ADC12-bits

CER: Chip Enable Status**(Read Only).**
[0]: Disable.
[1]: Enable.

XER: Crystal Status**(Read Only).**
[0]: Disable.
[1]: Enable.

PLLER: PLL Status. **(Read Only).**
[0]: Disable.
[1]: Enable.

TRSR: TRX Mode Status. **(Read Only).**
[0]: RX mode.
[1]: TX mode.

TRER: TRX Status. **(Read Only).**
[0]: Disable.
[1]: Enable.

FECF: FEC latch error flag. (FECF is read clear.)
[0]: FEC pass. **[1]:** FEC error.

CRCF: CRC latch error flag. (CRCF is read clear.)
[0]: CRC pass. **[1]:** CRC error.

PWR: Power Status (Read Only).
[0]: Power off. **[1]:** Power on.

9.2.1 MODEC1 (Address: 0x1001h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MODEC1	W	STRB7	STRB6	STRB5	STRB4	STRB3	STRB2	STRB1	STRB0
	R	ARCWTR	P_CKO	P_IRQ1O	P_IRQ2O	FPF	FSYNC	ENC_FLAG	--
Reset		0	0	0	0	0	0	0	0

Strobe Command								Description
STRB 7	STRB 6	STRB 5	STRB 4	STRB 3	STRB 2	STRB 1	STRB 0	
1	0	0	0	0	x	x	x	Sleep mode
1	0	0	1	x	x	x	x	Idle mode
1	0	1	0	x	x	x	x	Standby mode
1	0	1	1	x	x	x	x	PLL mode
1	1	0	0	x	x	x	x	RX mode
1	1	0	1	x	x	x	x	TX mode

9.2.2 MODEC2 (Address: 0x1002h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MODEC2	W	XEC	~~CCE~~	FMS	WOR_EN	FMT	--	HBS	ADCM
	R	XEC	~~CCE~~	FMS	WOR_EN	FMT	--	HBS	ADCM
Reset		0	0	0	0	0	0	0	0

XEC: **Reserved. Should set to [1]**

FMS: Direct/FIFO mode select.
[0]: Direct mode. **[1]:** FIFO mode.

WOR_EN: WOR or WOT function enable.
[0]: Disable. **[1]:** Enable.

FMT: FIFO mode test.
[0]:
[1]: Test.

HBS: Reserved for internal usage only.

ADCM: ADC measurement (Auto clear when done).
[0]: Disable. **[1]:** Enable.

9.2.3 MODEC3 (Address: 0x1003h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MODEC3	W	FIFOREV	MSCD	VBS	SWT	VCC	VBC	FBC	RSSCR
	R	FIFOREV	MSCD	VBS	SWT	VCC	VBC	FBC	RSSCR
Reset		0	0	0	0	0	0	0	0

FIFOREV: Reverse TX and RX FIFO.
[0]: Disable.
[1]: Enable.

VBS: Reserved. Should set to [0].

SWT: VCO Current and ADC clock and System clock select. Recommend SWT = [0].
[0]: Original
[1]: Update

VCC: VCO Current Calibration. (Write only, Shall be set to [1].)
[0]: Disable. **[1]:** Enable.

VBC: VCO Bank Calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

FBC: IF Filter Bank Calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

RSSCR: RSSI Calibration. (Auto clear when done)
[0]: Disable. **[1]:** Enable.

9.2.4 CAL1 (Address: 0x1004h) & CAL2 (Address: 0x1005h)

9.2.4.1 CAL1 (Address: 0x1004h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CAL1	W	MSCRC	VTL2	VTL1	VTL0	VTH2	VTH1	VTH0	MVBS
	R	FCD4	FCD3	FCD2	FCD1	FCD0	VB2	VB1	VB0
Reset		0	0	0	0	0	0	0	0

MSCRC: CRC Filtering Enable. Recommend MSCRC = [1].
[0]: Disable. **[1]:** Enable.

VTL[2:0]: VT low threshold setting for VCO calibration. Recommend VTL = [100].
[000]: VTL=0.06V. **[001]:** VTL=0.12V. **[010]:** VTL=0.18V. **[011]:** VTL=0.24V. **[100]:** VTL=0.3V. **[101]:** VTL=0.36V.
[110]: VTL=0.42V. **[111]:** VTL=0.48V.

VTH[2:0]: VT high threshold setting for VCO calibration. Recommend VTH = [111].
[000]: VTH=Vdd-0.06V. **[001]:** VTH=Vdd-0.12V. **[010]:** VTH=Vdd-0.18V. **[011]:** VTH=Vdd-0.24V. **[100]:** VTH=Vdd-0.3V.
[101]: VTH=Vdd-0.36V. **[110]:** VTH=Vdd-0.42V. **[111]:** VTH=Vdd-0.48V.

MVBS: VCO band calibration select.
[0]: Auto. **[1]:** Manual.

9.2.4.2 CAL2 (Address: 0x1005h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CAL2	W	MVB2	MVB1	MVB0	MFBS	MFB3	MFB2	MFB1	MFB0
	R	DVT1	DVT0	VBCF	FBCF	FB3	FB2	FB1	FB0
Reset		0	0	0	0	0	0	0	0

MVB[2:0]: VCO bank manual setting. VCO frequency increases when MVB decreases.
MFBS: Manual IF filter bank select. 0: Auto, 1: Manual.
[0]: Auto. **[1]:** Manual.

MFB[3:0]: Manual IF filter bank setting.

9.2.5 FIFO1 (Address: 0x1006h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO1	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
Reset		0	0	0	0	0	0	0	0

FEP[7:0]: fifo end pointer in byte for TX FIFO and RX FIFO.
FIFO Length Setting = FEP[7:0] + 1 ;
For example if FEP = 0x3F, it means FIFO length is 64 bytes.

9.2.6 FIFO2 (Address: 0x1007h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO2	W	FPM1	FPM0	TPSA5	TPSA4	TPSA3	TPSA2	TPSA1	TPSA0
Reset		0	0	0	0	0	0	0	0

FPM[1:0]: fifo pointer margin.
Used in FIFO extension mode

FPM[1:0]	Bytes in TX FIFO	Bytes in RX FIFO
00	4	60
01	8	56
10	12	52
11	16	48

TPSA[5:0]: TX payload start address in byte. Used for segment FIFO.

9.2.7 RCOSC1 (Address: 0x1008h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCOSC1	W	RCOT2	RCOT1	RCOT0	MVS1	MVS0	MCALS	MAN	ENCAL
	R	NUMLH11	NUMLH10	NUMLH9	NUMLH8	VBD	RCOC9	RCOC8	ENCAL
Reset		0	0	0	0	0	0	0	0

RCOT [2:0]: RC Oscillator current setting.

MVS[1:0]: WOR Calibration sample clock select based on CKOT.
[00]: 1/2. **[01]:** 1/4. **[10]:** 1/8. **[11]:** 1/16.

MCALS: WOR Calibration select.
[0]: Continuous mode. **[1]:** Single mode.

MAN: WOR Calibration Manual select.
[0]: Auto
[1]: Manual

ENCAL: WOR Calibration Enable. ENCAL shall be [0] when WOR calibration is finished.
[0]: Disable. **[1]:** Enable.

ENCAL: WOR Calibration Flag (read only).

NUMLH[11:0]: WOR Calibration result. (Read only.)

9.2.8 RCOSC2 (Address: 0x1009h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCOSC2	W	--	--	--	--	RTCPUN	SLPO	MRCT9	MRCT8
	R	NUMLH7	NUMLH6	NUMLH5	NUMLH4	NUMLH3	NUMLH2	NUMLH1	NUMLH0
Reset		0	0	0	0	0	0	0	0

MRCT[9:0]: Manual setting of RC Timer for WOR mode.

9.2.9 RCOSC3 (Address: 0x100Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCOSC3	W	MRCT7	MRCT6	MRCT5	MRCT4	MRCT3	MRCT2	MRCT1	MRCT0
	R	RCOC7	RCOC6	RCOC5	RCOC4	RCOC3	RCOC2	RCOC1	RCOC0
Reset		0	0	0	0	0	0	0	0

MRCT[9:0]: Manual setting of RC Timer for WOR mode.

9.2.10 RCOSC4 (Address: 0x100Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCOSC4	W	RCTS	XCC32K	XCP32K1	XCP32K0	TGNUM11	TGNUM10	TGNUM9	TGNUM8
Reset		0	0	0	0	0	0	0	0

RCTS: Internal / External 32.768k Hz oscillator selection.
[0]: Internal. [1]: External.

XCC32K: Reserved for internal usage only.
XCP32K[1:0]: Reserved for internal usage only.

TGNUM[11:0]: Target Number for RC-OSC Calibration.

9.2.11 RCOSC5 (Address: 0x100Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCOSC5	W	TGNUM7	TGNUM6	TGNUM5	TGNUM4	TGNUM3	TGNUM2	TGNUM1	TGNUM0

Reset		0	0	0	0	0	0	0	0

TGNUM[11:0]: Target Number for RC-OSC Calibration.

9.2.12 SYCK1 (Address: 0x100Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYCK1	W/R	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
Reset		0	0	0	0	0	0	0	0

GRC[4:0]: Generation Reference Clock Divider.
GRC [4:0] is the clock divider to generate a PFD clock for the internal CLK Generator.

$$f_{CGRF} = \frac{f_{xtal}}{GRC[4:0]+1}$$

CSC[2:0]: System Clock Divider setting.
CSC is the clock divider of F_{MSCK} to generate the wanted data clock and IF calibration clock where F_{MSCK} is either from Xtal itself (CGS = 0) or from the internal CLK Generator (CGS = 1).

$$f_{CSCK} = \frac{f_{MSCK}}{CSC[2:0]+1}$$

9.2.13 SYCK2 (Address: 0x100Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYCK2	W/R	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS
Reset		0	0	0	0	0	0	0	0

SDR[6:0]: Data Rate Divider.

$$Data\,rate = \frac{1}{128} \cdot \frac{f_{system}}{SDR[6:0]+1}$$ where Fsystem is system clock.

If DMOS (0Ah) = 0, $$Data\,rate = \frac{1}{128} \cdot \frac{f_{CSCK}}{SDR[6:0]+1}$$ (recommended).

If DMOS (0Ah) = 1, $$Data\,rate = \frac{1}{64} \cdot \frac{f_{CSCK}}{SDR[6:0]+1}$$

GRS: Reference Clock Selection for the internal CLK Generator.
[0]: PLL CLK Gen. = F_{CGRF} x 48, where F_{CGRF} is from below GRC divider
[1]: PLL CLK Gen. = F_{CGRF} x 32

9.2.14 PLL1 (Address: 0x100Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL1	W/R	IP8	CRCINV	CHF2I	CHI2I	CHF1	CHF0	CHI1	CHI0
Reset		0	0	0	0	0	0	0	0

CRCINV: CRC Inverted Select.
[0]: disable. **[1]:** enable

CHF2I: Fractional-N Charge Pump Current Scale.
[0]: normal fractional-N synthesizer Charge-pump current
[1]: fractional-N synthesizer charge-pump current scale(x1.5)

CHI2I: Reserved.
CHI[1:0]: Reserved. CHI shall be [00].

CHF[1:0]: charge-pump current setting for fractional-N synthesizer. Recommend CHF = [01].
[00]: 48uA
[01]: 96uA
[10]: 192uA
[11]: 384uA

CHF[1:0]	
CHF2I=0	CHF2I=1
50uA	75 uA
100uA	150 uA
200uA	300 uA
400uA	600 uA

9.2.15 PLL2 (Address: 0x1010h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL2	W/R	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
Reset		0	0	0	0	0	0	0	0

IP[8:0]: LO frequency Integer Part setting.

9.2.16 PLL3 (Address: 0x1011h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL3	W/R	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8
Reset		0	0	0	0	0	0	0	0

FP[15:0]: LO Frequency Fractional Part setting.

9.2.17 PLL4 (Address: 0x1012h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL4	W/R	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
Reset		0	0	0	0	0	0	0	0

FP[15:0]: LO Frequency Fractional Part setting.

$$f_{\mathrm{LO\_BASE}} = f_{PFD} \cdot (IP[8:0] + \frac{FP[15:0]}{2^{16}}) \quad \text{(unit: Hz)}$$

where $f_{\mathrm{LO\_BASE}}$, the base frequency of VCO

where $f_{\mathrm{PFD}} = f_{Xtal} \div (RFC[3:0]+1)$, the comparison frequency of RF_PLL.

A9129's RF frequency is implemented by an offset scheme regarding to the below formula.

The wanted RF frequency is equal to VCO frequency, $F_{RF} = F_{VCO} = F_{LO\_BASE} + F_{OFFSET}$.

where f_{OFFSET}, the offset frequency of VCO is set by FPA [15:0] (09h, page 2) $f_{\mathrm{OFFSET}} = f_{PFD} \cdot (\frac{FPA.[15:0] \cdot 2^6}{2^{16}})$

Please refer to Chapter 13 for details.

9.2.18 PLL5(Address: 0x1013h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL5	W	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8
	R	AFC	FC[14:8]						
Reset		0	0	0	0	0	0	0	0

AFC: Auto Frequency Compensation selection.
[0]: manual
[1]: auto

FC[14:0]: PLL Fractional Part Compensation value.
[Write]：Manual setting to LO fractional part compensation value when AFC = [0].
[Read]：Frequency offset value when AFC = [1].

9.2.19 PLL6(Address: 0x1014h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL6	W	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0
	R	FC[7:0]							
Reset		0	0	0	0	0	0	0	0

FC[14:0]: PLL Fractional Part Compensation value.
[Write]：Manual setting to LO fractional part compensation value when AFC = [0].
[Read]：Frequency offset value when AFC = [1].

9.2.20 PLL7 (Address: 0x1015h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL7	W	CPS	XCC	CKX2	INTLP	PDL2	PDL1	PDL0	MD0
Reset		0	0	0	0	0	0	0	0

CPS: Charge Pump tri-state setting. Recommend CPS = [1].
[0]: Tri-state.
[1]: Normal operation.

XCC: Crystal Current setting.
[0]: Low current. **[1]:** High current.

CKX2: Reserved. CKX2 shall be [0].

INTLP: Internal loop filter manual setting.

PDL[2:0]: PLL Settling Delay Time setting.

PDL [2:0]	PLL Delay Timer	Note
000	20 us	
001	40 us	
010	60 us	
011	80 us	Recommend
100	100 us	
101	120 us	
110	140 us	
111	160 us	

MD0: LO Buffer current select.
[0]: Low current
[1]: High current

9.2.21 PLL8 (Address: 0x1016h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL8	W	ADCR	VCI	TXDBG	ISDIV	SDPW1	SDPW0	NSDO	EDI
Reset		0	0	0	0	0	0	0	0

ADCR: Reserved. ADCR should be= [0].

VCI: VCO current calibration test bit. Reserved. VCI shall be [0].

TXDBG: TX Debug mode. TXDBG shall be [0].
[0]: Disable
[1]: Enable

ISDIV: Divider current test bit. Recommend ISDIV = [0].
[0]: low current.
[1]: high current.

SDPW[1:0]: Pulse Width of sigma-delta modulator. SDPW shall be [00].

NSDO: Mash sigma delta order setting. Recommend NSDO = [0].
[0]: order 2. **[1]:** order 3.

EDI: Dither Noise setting. Recommend EDI = [0].
[0]: Disable. **[1]:** Enable.

9.2.22 PLL9 (Address: 0x1017h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL9	W	VICMP	IA14	IA13	IA12	IA11	IA10	IA9	IA8
Reset		0	0	0	0	0	0	0	0

VICMP: Reserved. VICMP shall be [0].

IA[14:0]: Reserved. IA shall be [0x0000].

9.2.23 PLL10 (Address: 0x1018h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL10	W	IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0
Reset		0	0	0	0	0	0	0	0

IA[14:0]: Reserved. IA shall be [0x0000].

9.2.24 PLL11 (Address: 0x1019h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL11	W	RFC3	RFC2	RFC1	RFC0	RIC11	RIC10	RIC9	RIC8
Reset		0	0	0	0	0	0	0	0

RFC[3:0]: R-Counter for Fractional-N PLL
RFC is used to divide crystal frequency for the comparison frequency of the Franc-N PLL by
F_{PFD} = Fxtal / (RFC[3:0]+1)

RIC[11:0]: Reserved. RIC shall be [0x000]

9.2.25 PLL12 (Address: 0x101Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL12	W	RIC7	RIC6	RIC5	RIC4	RIC3	RIC2	RIC1	RIC0
Reset		0	0	0	0	0	0	0	0

RFC[3:0]: R-Counter for Fractional-N PLL
RFC is used to divide crystal frequency for the comparison frequency of the Franc-N PLL by
F_{PFD} = Fxtal / (RFC[3:0]+1)

RIC[11:0]: Reserved. RIC shall be [0x000]

9.2.26 CLOCK (Address: 0x101Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLOCK	W	HFB	EDIVS	XCP1	XCP0	INTXC	RBS	CGS	XS
	R	--	--	--	--	--	--	CGS	XS
Reset		0	0	0	0	0	0	0	0

HFB: High frequency band select. 0: Low band, 1: High band.

EDIVS: Synthesizer Selection. EDIVS shall be [0].
[0]: Fractional-N PLL
[1]: Reserved

XCP[1:0]: Crystal Regulating Couple setting. Recommend XCP =[00].

INTXC: Internal Crystal Load selection. Recommend INTXC = [1].
[0]: Use external capacitors. **[1]:** Use on-chip capacitors.

RBS: REGA bandgap setting.

CGS: Clock Generation Selection.
[0]: Disable, F_{MSCK} = Xtal freq.
[1]: Enable, F_{MSCK} = CLK Generator. Please refer to chapter 12 for details.

XS: Crystal Oscillator Selection. Recommend XS = [1].
[0]: Disable **[1]:** Enable

9.2.27 TX1 (Address: 0x101Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX1	W	TXDI	TDC1	TDC0	TME	GS	FDP2	FDP1	FDP0
Reset		0	0	0	0	0	0	0	0

TXDI: TX data inverted. Recommend TXDI = [0].
[0]: normal. **[1]:** invert

TDC[1:0]: TX Driver current setting.
Please refer to Chapter 8 and A9129 App. Note for programmable TX output power.

TME: TX Modulation Enable.
[0]: Disable.
[1]: Enable.

GS: Gaussian Filter Selection.
[0]: Disable.
[1]: Enable.

FDP[2:0]: Frequency Deviation Exponential Coefficient setting.

9.2.28 TX2 (Address: 0x101Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX2	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Reset		0	0	0	0	0	0	0	0

FD[7:0]: TX Frequency Deviation setting.

For both Gaussian filter is enabled (GS =1) or disabled（GS = 0）：

$$f_{dev} = 2 \cdot f_{PFD} \cdot FD[7:0] \cdot \frac{2^{FDP[2:0]}}{2^{19}}$$ (unit: Hz)

where $f_{\mathrm{PFD}} = f_{Xtal} \div (RFC[3:0]+1)$, is the comparison frequency of RF_PLL.

Note2: please refer to Chapter 13 for details.

9.2.29 TX3 (Address: 0x101Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX3	W	MCNTR	DPRY2	DPRY1	DPRY0	BT1	BT0	TDLY1	TDLY0
Reset		0	0	0	0	0	0	0	0

MCNTR: Divided by 2 select.

[0]: $PF8M = f_{\mathrm{MCNT}} \div 2$ where PF8M is one of baseband clock sources.

[1]: $PF8M = f_{\mathrm{MCNT}}$

where $f_{\mathrm{MCNT}} = f_{MSCK} \div (MCNT[1:0])$, located in 0x08 page 8.

Please refer to Chapter 12 for details.

DPR [2:0]: Scaling of PDL and TDL. Recommend DPR = [000].

BT [1:0]: Moving average for Gaussian filter select.
If GS = [0],
Gaussian filter is disabled, **BT = [00]:** not average. **[01]:** 2 bit average. **[10]:** 4 bit average. **[11]:** 8 bit average
That means BT is used to smooth TX data transition.
If GS = [1],
Gaussian filter is enabled, **BT = [00]:** 2.0. **[01]:** 1.0. **[10]:** 0.5. **[11]:** 0.5
That means BT is used to configure shape of Gaussian filter.

TDL[1:0]:TX Settling Delay select.

TDL [1:0]	TX Delay Timer	Note
00	20 us	Recommend
01	40 us	
10	60 us	
11	80 us	

9.2.30 TX4 (Address: 0x101Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX4	W	PAC1	PAC0	TBG5	TBG4	TBG3	TBG2	TBG1	TBG0
Reset		0	0	0	0	0	0	0	0

PAC[1:0]: PA current setting.

Please refer to Chapter 8 and A9129 App. Note for programmable TX output power.

TBG[5:0]: TX Buffer Gain setting.
Please refer to Chapter 8 and A9129 App. Note for programmable TX output power.

9.2.31 WOR1 (Address: 0x1020h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WOR1	W	WRDLY9	WRDLY8	WRDLY5	WRDLY4	WRDLY3	WRDLY2	WRDLY1	WRDLY0
Reset		0	0	0	0	0	0	0	0

WOR_AC [8:0]: 9-bits WOR Active Period.
WOR Active Period = (WOR_AC[8:0]+1) x (1/4096), (244us ~ 125ms).

WOR_SL [9:0]: 10-bits WOR Sleep Period.
WOR Sleep Period = (WOR_SL[9:0]+1) x (32/4096), (7.8ms ~ 7.99s).

9.2.32 WOR2 (Address: 0x1021h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WOR2	W	WORDLY7	WORDLY6	WORDLY5	WORDLY4	WORDLY3	WORDLY2	WORDLY1	WORDLY0
Reset		0	0	0	0	0	0	0	0

WOR_AC [5:0]: 6-bits WOR Active Period.
WOR Active Period = (WOR_AC[5:0]+1) x (1/4096), (244us ~ 15.6ms).

WOR_SL [9:0]: 10-bits WOR Sleep Period.
WOR Sleep Period = (WOR_SL[9:0]+1) x (32/4096), (7.8ms ~ 7.99s).

9.2.33 WOR3 (Address: 0x1022h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WOR3	W	**LFIFOREV**	WOR_SEL	RS_DLY2	RS_DLY1	RS_DLY0	RSSC_D1	RSSC_D0	WOR_CD
Reset		0	0	0	0	0	0	0	0

WOR_SEL: TWWS=1 setting. [0]:RX valid packet. **[1]:** Carrier detect/preamble ok/sync ok.

RS_DLY [2:0]: RSSI Measurement Delay while in RX mode. Recommend RS_DLY = [000].
[000]: 10us. **[001]:** 20us. **[010]:** 30us. **[011]:** 40us. **[100]:** 50us. **[101]:** 60us. **[110]:** 70us. **[111]:** 80us.

RSSC_D [1:0]: RSSI calibration Delay setting. Recommend RSSC_D = [00].
[00]: 10us. **[01]:** 20us. **[10]:** 30us. **[11]:** 40us.

WOR_CD: Wake up MCU select.

9.2.34 WOR4 (Address: 0x1023h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WOR4	W	WN3	WN2	WN1	WN0	WOR_S	TMRE	TSEL	TWOR
Reset		0	0	0	0	0	0	0	0

WN[3:0]: The number of RX wake up times.
Wake up times = (WN[3:0] + 1).

WOR_S: Wake up MCU select.

[WOR_CD, WOR_S]	Wake up MCU select.

[00]	By Frame Sync OK
[01]	By preamble Detect OK.
[1x]	By carrier detect OK.

TMRE: WOR timer enable bit
[0]: Disable
[1]: Enable

TSEL: TWOR Duty select.
[0]: Use WOR_AC [5:0]. (where WOR_AC is located in 08h, page 1)
[1]: Use WOR_SL [9:0]. (where WOR_SL is located in 08h, page 1)

TWOR: Wake up MCU Mode select.
[0]: By WOR mode. Wake up MCU while receiving a packet.
[1]: By TWOR mode. Wake up MCU by TWOR timer.

9.2.35 RFI1 (Address: 0x1024h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFI1	W	CDSEL1	CDSEL0	PRRC1	PRRC0	RSM1	RSM0	RMP1	RMP0
	R	RHM[7:0]							
Reset		0	0	0	0	0	0	0	0

CDSEL [1:0]: Carrier Detect select by GIO1S.
If GIO1S is set to be [0010], Carrier Detect scheme has below tree options.
[0X]: RSSI Carrier Detect.
[10]: In-band Carrier Detect.
[11]: RSSI Carrier Detect plus In-band Carrier Detect.

PRRC [1:0]: Reserved. PRRC shall be [10].

RSM [1:0]: RSSI Margin. Recommend RSM = [01].
RSM = (RTH – RTL).
[00]: 5. **[01]:** 10. **[10]:** 15. **[11]:** 20.

RMP [1:0]: PA Ramp up/down Timing Scale setting.
[00]: 1. **[01]:** 2. **[10]:** 4. **[11]:** 8.

RHM [7:0]: RSSI calibration high threshold level (Read Only).

9.2.36 RFI2 (Address: 0x1025h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFI2	W	QCLIM	TRT2	TRT1	TRT0	ASMV2	ASMV1	ASMV0	AMVS
	R	RLM[7:0]							
Reset		0	0	0	0	0	0	0	0

QCLIM: Reserved. Shall be [0].

TRT [2:0]: TX Ramp down discharge current select. Recommend TRT =[111].

ASMV [2:0]: TX Ramp up Timing Select. Recommend ASMV =[111].
[000]: 2us, **[001]:** 4us. **[010]:** 6us. **[011]:** 8us. **[100]:** 10us, **[101]:** 12us. **[110]:** 14us. **[111]:** 16us.
Actual TX ramp up time = ASMV [2:0] x RMP[1:0]

AMVS : PA Ramp Up Enable. Recommend AMVS = [1].
[0]: Disable. **[1]:** Enable.

RLM [7:0]: RSSI calibration low threshold (Read Only).

9.2.36 PM1 (Address: 0x1026h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

PM1	W	RC_DLY2	RC_DLY1	RC_DLY0	CELS	RGC1	RGC0	STS	QDS
Reset		0	0	0	0	0	0	0	0

RC_DLY[2:0]: RSSI calibration RL Delay setting. Recommend RC_DLY= [000]
[000]: 100us. [001]: 300us. [010]: 500us. [011]: 700us.
[100]: 900us. [101]: 1.1ms. [110]: 1.3ms. [111]: 1.5ms.

CELS: Reserved. Shall be [0].

RGC[1:0]: Reserved. Recommend RGC = [01].

STS: Reserved. Shall be [0].

QDS: VDD_A Quick Discharge select. Recommend QDS = [1].
[0]: Normal. **[1]:** Quick discharge.

9.2.37 PM2 (Address: 0x1027h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PM2	W	SPSS	RGV1	RGV0	BVT2	BVT1	BVT0	PRE_S	BDS
	R	--	--	--	--	--	--	**VBD**	**BODF**
Reset		0	0	0	0	0	0	0	0

SPSS: Mode Back select if WOT/WOR is enabled. Recommend SPSS = [0].
[0]: While WN≥1, the WOT/WOR operating will return to Standby mode. For example, if WN=2, the WOR operation period will be: Sleep -> RX -> Standby -> RX -> Standby -> RX -> Sleep.
[1]: While WN≥1, the WOT/WOR operating will return to PLL mode. For example, if WN=2, the WOR operation period will be: Sleep -> RX -> PLL -> RX -> PLL -> RX -> Sleep.

RGV [1:0]: Digital Regulator Voltage select. Recommend RGV = [01].
[00]: 1.9V
[01]: 1.8V
[10]: 1.7V
[11]: 1.6V

BVT [2:0]: Battery Voltage Threshold select.
[000]: 2.0V. **[001]:** 2.1V. **[010]:** 2.2V. **[011]:** 2.3V. **[100]:** 2.4V. **[101]:** 2.5V. **[110]:** 2.6V. **[111]:** 2.7V.

PRE_S: Preamble Detect Select.
[0]: Normal preamble detection operation.
[1]: PMDO=1 when preamble is matched to ID, or PMDO=0 and it will keep doing re-preamble matching scheme.
NOTE: PMDO will be hold when ID is matched no matter PRE_S=0 or 1.

BDS: Battery Detection selection.
[0]: Disable. **[1]:** Enable.

VBD: Battery Detection flag (Read Only).
[0]: Battery Low.
[1]: Battery High.

9.2.38 RTH1 (Address: 0x1028h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTH1	W	IRTH7	IRTH6	IRTH5	IRTH4	IRTH3	IRTH2	IRTH1	IRTH0
Reset		0	0	0	0	0	0	0	0

IRTH[7:0]: AGC high Threshold. Recommend IRTH = [0x03].

9.2.39 RTH2 (Address: 0x1029h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTH2	W	IRTL7	IRTL6	IRTL5	IRTL4	IRTL3	IRTL2	IRTL1	IRTL0
Reset		0	0	0	0	0	0	0	0

IRTL[7:0]: AGC low Threshold. Recommend IRTL = [0x02].

If ADC ≤ IRTL. DVT[1:0] (0Eh) = 11.
If ADC ≥ IRTH. DVT[1:0] (0Eh) = 00.
If IRTL ≤ ADC ≤ IRTH. DVT[1:0] (0Eh) = 01.

9.2.40 AGC1 (Address: 0x102Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AGC1	W	EXTL	VRSEL	MS	MSCL4	MSCL3	MSCL2	MSCL1	MSCL0
	R	--	--	LGC1	LGC0	MGC1	MGC0	IGC1	IGC0
Reset		0	0	0	0	0	0	0	0

EXTL: VCO Calibration test bit. EXTL shall be [0].

VRSEL: AGC Function select.
[0]: RSSI AGC. **[1]:** wideband AGC.

MS: AGC Manual Scale select. Recommend MS = [0].
[0]: Auto (RL−RH).
[1]: Manual by MSCL[4:0].

MSCL[4:0]: AGC Manual Scale setting.

LGC[1:0]: LNA Gain Check (Read Only).

MGC[1:0]: Mixer Gain Check (Read Only).

IGC[1:0]: BPF Gain Check. (Read only)

9.2.41 AGC2 (Address: 0x102Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AGC2	W	HDM	AGCE	ERSSM	EXRSI	LGM1	LGM0	MGM1	MGM0
Reset		0	0	0	0	0	0	0	0

HDM: AGC HOLD select.
[0]: No hold.
[1]: Hold Gain Switching when ID is sync.

AGCE: Auto Gain Control Enable.
[0]: Disable. **[1]:** Enable.

ERSSM : Ending mode for RSSI measurement. Recommend ERSSM = [0].
[0]: RSSI value frozen before leaving RX.
[1]: RSSI value frozen when valid frame sync (ID and header check ok).

EXRSI: Reserved. EXRSI shall be [0].

LGM [1:0]: LNA Gain Attenuation select. Recommend LGM = [00].
[00]: -18dB. **[01]:** -12dB. **[10]:** -6dB. **[11]:** Max.

MGM [1:0]: Mixer Gain Attenuation select. Recommend MGM = [00].
[00]: -18dB. **[01]:** -12dB. **[10]:** -6dB. **[11]:** Max.

9.2.42 AGC3 (Address: 0x102Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AGC3	W	RGVA1	RGVA0	RGVT1	RGVT0	LHM1	LHM0	MHM1	MHM0
	R	--	--	--	--	LHC1	LHC0	MHC1	MHC0
Reset		0	0	0	0	0	0	0	0

RGVA[1:0]: Analog Regulator Voltage Select. Recommend RGVA = [00].
[00]: 1.8V
[01]: 1.9V
[10]: 2.0V
[11]: 2.1V

RGVT[1:0]: PA Regulator Voltage Select. Recommend RGVT = [10].
[00]: 1.8V
[01]: 1.9V
[10]: 2.0V
[11]: 2.1V

LHM[1:0]: LNA Current Select. Recommend LHM = [10].
[00]: min.
[01]: mid.
[10]: high
[11]: max

MHM[1:0]: Mixer Current Select. Recommend MHM = [10].
[00]: min.
[01]: mid.
[10]: high
[11]: max

LHC[1:0]: LNA Current Check. (Read only)

MHC[1:0]: Mixer Current Check. (Read only)

9.2.43 AGC4 (Address: 0x102Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AGC4	W	IGM1	IGM0	CA1	CA0	RSAGC1	RSAGC0	TXIB1	TXIB0
Reset		0	0	0	0	0	0	0	0

IGM[1:0]: BPF Gain Select. Recommend IGM = [11].
[00]: -18dB. **[01]:** -12dB. **[10]:** -6dB. **[11]:** Max.

CA[1:0]: AGC peak detect test bit. CA shall be [00].

RSAGC[1:0]: Reserved. RSAGC shall be [00].

TXIB[1:0]: Reserved. TXIB shall be [00].

9.2.44 CKO1 (Address: 0x102Eh)

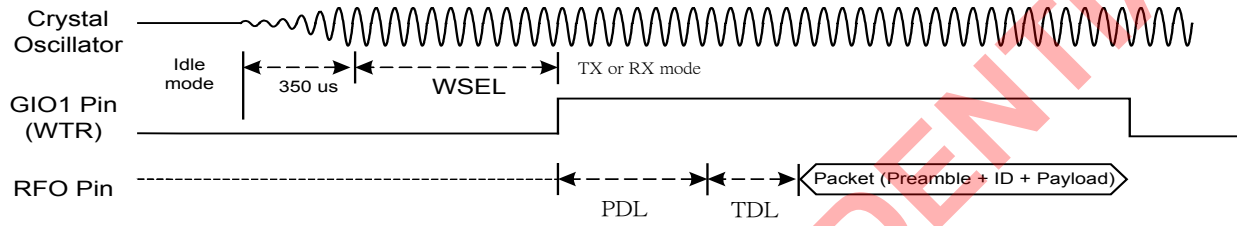
Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKO1	W	XCL4	XCL3	XCL2	XCL1	XCL0	WSEL2	WSEL1	WSEL0
Reset		0	0	0	0	0	0	0	0

XCL[4:0]: On-chip Crystal Capacitor Load setting.
Set XCL = [10000] as the first value to fine tune the carrier frequency and minimize the frequency drift if Xtal Cload = 20pF.
XCL is active when INTXC=1 and Each XCL step is typical 1.68 pF.
XCL is the on-chip capacitor for Xtal oscillator to fine tune offset frequency of the wanted RF carrier.
Please refer to chapter 11 or contact AMICCOM's FAE.

XCL[4:0]	Xtal C-load (pF)

00000	0
00001	1.68
00010	3.36
…	
11110	50.4
11111	52.08

WSEL[2:0]: Crystal Settling Delay setting (200us ~ 2.5ms). Recommend WSEL = [011].
[000]: 200us. **[001]:** 400us. **[010]:** 600us. **[011]:** 800us.
[100]: 1ms. **[101]:** 1.5ms. **[110]:** 2ms. **[111]:** 2.5ms.



9.2.45 CKO2 (Address: 0x102Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKO2	W		CKOSM3	CKOSM2	CKOSM1	CKOSM0	CKOIM	~~CKOEM~~	SCT
Reset		0	0	0	0	0	0	0	0

CKOS [3:0]: CKO pin output select.

CKOS [3:0]	state
[0000]	DCK (TX data clock)
[0001]	RCK (RX recovery clock)
[0010]	FPF (FIFO pointer flag for FIFO extension)
[0011]	Logic OR gate by EOP, EOVBC, EOFBC, EOVCC and RSSC_OK. (Internal usage only)
[0100]	BBCK
[0101]	BBCK
[0110]	BBCK
[0111]	Reserved
[1000]	WCK
[1001]	PF8M (FSYCK)
[1010]	ROSC
[1011]	EOADC
[1100]	OKADCN
[1101]	EOCAL
[1110]	VPOAK
[1111]	SYCK_o. (System clock without Crystal settling time)

CKOI: CKO pin Output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

CKOE: CKO pin Output Enable.
[0]: High Z. **[1]:** Enable.

SCT: Reserved. SCT shall be [1].

9.2.46 GPIO1 (Address: 0x1030h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GPIO1	W	WRCKS	STRR	GIO1S3	GIO1S 2	GIO1S 1	GIO1S 0	G1I	G1OE
Reset		0	0	0	0	0	0	0	0

WRCKS: WOR Reference clock select.
[0]: WOR Ref clock when PF8M is equal or close to 6.4MHz.
[1]: WOR Ref clock when PF8M is equal or close to 8MHz.

STRR: Direct mode modem data can be accessed via GPIO pin.
[0]: P_DTDM.
[1]: Direct mode TX Data (DTD = 0).

GIO1S [3:0]: GIO1 pin function select.

GIO1S [3:0]	TX state	RX state
[0000]	ARCWTR (Wait until TX or RX finished)	
[0001]	EOAC (end of access code)	FSYNC (frame sync)
[0010]	TMEO (TX modulation enable)	CD (carrier detect)
[0011]	External sync input (for direct mode), when SCT=0 Preamble Detect Output (PMDO), when SCT=1	
[0100]	TWOR	
[0101]	In phase demodulator input(DMIQ) or DVT[1](AGC)	
[0110]	SDO (4 wires SPI data out)	
[0111]	TRXD In/Out (Direct mode)	
[1000]	RXD (Direct mode)	
[1001]	TXD (Direct mode)	
[1010]	PDN_RX	
[1011]	External FSYNC input in RX direct mode *	
[1100]	VPOAK (Valid Packet or Auto ACK OK Output)	
[1101]	FPF	
[1110]	PDN_TX	
[1111]	FMTDO (FIFO mode TX Data Output testing)	

If GIO1S = [1011] and direct mode is selected, the internal frame sync function will be disabled. In such case, A9129 supports to accept an external frame sync signal from MCU to feed to GIO1 pin to determine the timing of fixing DC estimation voltage of demodulator.

G1I: GIO1 pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

G1OE: GIO1pin output enable.
[0]: High Z. **[1]:** Enable.

9.2.47 GPIO2 (Address: 0x1031h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GPIO2	W	MCNT1	MCNT0	GIO2S3	GIO2S 2	GIO2S 1	GIO2S 0	G2I	G2OE
Reset		0	0	0	0	0	0	0	0

MCNT[1:0]: Main Clock Divider.
[00]: $f_{MCNT} = f_{MSCK}$

[01]: $f_{MCNT} = f_{MSCK} / 2$

[10]: $f_{MCNT} = f_{MSCK} / 3$

[11]: $f_{MCNT} = f_{MSCK} / 4$

Please refer to Chapter 12 for details.

GIO2S [3:0]: GIO2 pin function select.

GIO2S [3:0]	TX state	RX state
[0000]	ARCWTR (Wait until TX or RX finished)	
[0001]	EOAC (end of access code)	FSYNC (frame sync)
[0010]	TMEO (TX modulation enable)	CD (carrier detect)
[0011]	External sync input (for direct mode), when SCT=0 Preamble Detect Output (PMDO), when SCT=1	
[0100]	MCU wakeup signal (TWWS) or WTR	
[0101]	Quadrature phase demodulator input (DMII).or DVT[0](AGC)	
[0110]	SDO (4 wires SPI data out)	
[0111]	TRXD In/Out (Direct mode)	
[1000]	RXD (Direct mode)	
[1001]	TXD (Direct mode)	
[1010]	PDN_TX	
[1011]	External FSYNC input in RX direct mode *	
[1100]	VPOAK (Valid Packet or Auto ACK OK Output)	
[1101]	FPF	
[1110]	Battery Detect flag. (BDF)	
[1111]	FMRDI. (FIFO mode RX input for testing) (for internal testing)	

If GIO2S = [1011] and direct mode is selected, the internal frame sync function will be disabled. In such case, A9129 supports to accept an external frame sync signal from MCU to feed to GIO2 pin to determine the timing of fixing DC estimation voltage of demodulator.

G2I: GIO2 pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

G2OE: GIO2 pin output enable.
[0]: High Z. **[1]:** Enable.

9.2.48 PIN1 (Address: 0x1032h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIN1	W	RFT2	RFT1	RFT0	PRS	SCMDS	WMODE	INFS	~~SCKI~~
Reset		0	0	0	0	0	0	0	0

RFT [2:0]: RF Analog Pin Configuration. Recommend RFT= [000].

{XADS, RFT[2:0]}	BP_BG (Pin 30)	RSSI (Pin 1)
[0000]	Band-gap voltage	RSSI voltage
[0001]	Analog temperature voltage	RSSI voltage
[0010]	Band-gap voltage	No connection
[0011]	Analog temperature voltage	No connection
[0100]	BPF positive in phase output	BPF negative in phase output
[0101]	BPF positive quadrature phase output	BPF negative quadrature phase output
[0110]	RSSI voltage	No connection
[0111]	RSSI voltage	No connection
[1000]	Band-gap voltage	External ADC input source
[1001]	Analog temperature voltage	External ADC input source
[1010]	Band-gap voltage	External ADC input source
[1011]	Analog temperature voltage	External ADC input source
[1100]	No connection	External ADC input source
[1101]	No connection	External ADC input source

[1110]	No connection	External ADC input source
[1111]	No connection	External ADC input source

PRS: Read frequency mode for AFC=1. Recommend PRS= [0].
[0]: no frequency compensation.
[1]: frequency offset in AFC mode

SCMDS: Strobe Command select. Recommend SCMDS= [1].
[0]: register control. **[1]:** strobe control.

WMODE: WOT or WOR select for WORE=1.
[1]: WOT (Wake-on-TX).
[0]: WOR (Wake-on-RX).

INFS: Infinite FIFO length select.
[0]: fixed length. **[1]:** infinite length

9.2.49 PIN2 (Address: 0x1033h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIN2	W	IRQI	IRQS1	IRQS0	IRQOE	CKOIK	CKOSK1	CKOSK0	--
Reset		0	0	0	0	0	0	0	0

IRQI: Reserved. IRQI shall be [0].

IRQS[1:0]: Reserved. Use GIO1S/ GIO2S instead. Shall be [00].

IRQOE: Reserved. Use G1OE/ G2OE instead. Shall be [0].

CKOIK: Reserved. Use 08h page 9 instead. Shall be [0].

CKOSK[1:0]: Reserved. Use 08h page 9 CKOS instead. Shall be [00].

9.2.50 VCB1 (Address: 0x1034h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCB1	W	CDTM1	CDTM0	FEP13	FEP12	FEP11	FEP10	FEP9	FEP8
	R	--	--	--	VCCF	VCB[3:0]			
Reset		0	0	0	0	0	0	0	0

CDTM[1:0]: Carrier detect number of times setting.
[00]: 16. **[01]:** 32 **[10]:** 64. **[11]:**128

FEP[13:8]: FIFO End Pointer for TX FIFO and Rx FIFO. Please see 9.2.9.13 FIFO (address:08h) Page 13.

VCCF : VCO Current Auto Calibration Flag (Read Only).
[0]: Pass. **[1]:** Fail.

VCB [3:0]: VCO Current Calibration Value (Read Only).
MVCS= 0: Auto calibration value.
MVCS= 1: Manual calibration value.

9.2.51 VCB2 (Address: 0x1035h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCB2	W	PKT1	PKT0	PKS	VCOC3	VCOC2	VCOC1	VCOC0	MVCS
Reset		0	0	0	0	0	0	0	0

PKT[1:0]: VCO Peak Detect threshold test bit. PKT shall be [00].

PKS: VCO Current Calibration Mode Select. Recommend PKS = [0].
[0]: Normal.
[1]: VCO current calibration by peak detection.

VCOC [3:0]: VCO Current Calibration result. Recommend VCOC = [0010].
If SWT = [0] @ 0Fh, then VCOC= [1000].
If SWT = [1] @ 0Fh, then VCOC[3:0] = Manual setting.

MVCS: VCO current calibration select. Recommend MVCS = [0].
[0]: Auto. **[1]:** Manual.

9.2.52 CHG1 (Address: 0x1036h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHG1	W	CBG2	CBG1	CBG0	QDTX	FPL3	FPL2	FPL1	FPL0
	R	--	--	--	--	FPL3	FPL2	FPL1	FPL0
Reset		0	0	0	0	0	0	0	0

CBG[2:0]: Reserved for internal usage.

QDTX: Reserved for internal usage only.

FPL [3:0]: VCO Calibration Fractional Part Setting for Low Boundary Channel Group.
Please refer to A9129's reference code for the wanted RF band.

9.2.53 CHG2 (Address: 0x1037h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHG2	W/R	IPL7	IPL6	IPL5	IPL4	IPL3	IPL2	IPL1	IPL0
Reset		0	0	0	0	0	0	0	0

IPL [7:0]: VCO Calibration Integer Part Setting for Low Boundary Channel Group.
Please refer to A9129's reference code for the wanted RF band.

9.2.54 CHG3 (Address: 0x1038h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHG3	W/R	CSLP1	CSLP0	MSLP	RSLP	FPH3	FPH2	FPH1	FPH0
Reset		0	0	0	0	0	0	0	0

FPH [3:0]: VCO Calibration Fractional Part Setting for High Boundary Channel Group.
Please refer to A9129's reference code for the wanted RF band.

9.2.55 CHG4 (Address: 0x1039h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHG4	W/R	IPH7	IPH6	IPH5	IPH4	IPH3	IPH2	IPH1	IPH0
Reset		0	0	0	0	0	0	0	0

IPH [7:0]: VCO Calibration Integer Part Setting for High Boundary Channel Group.
Please refer to A9129's reference code for the wanted RF band.

9.2.56 IF1 (Address: 0x103Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IF1	W/R	AIF	IFOA14	IFOA13	IFOA12	IFOA11	IFOA10	IFOA9	IFOA8
Reset		0	0	0	0	0	0	0	0

AIF: Auto IF enable.
[0]: disable. **[1]:** enable.

IFOA[14:0]: Auto IF offset frequency setting.

$$IFOA = \frac{f_{IFREF}}{f_{PFD}} * 65536$$

$$ex: IFBW = 100KHz, f_{IFREF} = 200KHz, Datarate = 100Kbps$$

$$IFOA = \frac{200K}{12.8M} * 65536 = 1024$$

9.2.57 IF2 (Address: 0x103Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IF2	W/R	IFOA7	IFOA6	IFOA5	IFOA4	IFOA3	IFOA2	IFOA1	IFOA0
Reset		0	0	0	0	0	0	0	0

IFOA[14:0]: Auto IF offset frequency setting.

9.2.58 IF3 (Address: 0x103Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IF3	W	FPA15	FPA14	FPA13	FPA12	FPA11	FPA10	FPA9	FPA8
Reset		0	0	0	0	0	0	0	0

FPA[15:0]: LO setting for frequency offset.

$$f_{\text{OFFSET}} = f_{PFD} \cdot (\frac{FPA[15:0] \cdot 2^6}{2^{16}}) \quad \text{(unit: Hz)}$$

Where F_{PFD} = Fxtal / (RFC[3:0]+1)

From PLL II (02h), $f_{\text{LO\_BASE}} = f_{PFD} \cdot (IP[8:0] + \frac{FP[15:0]}{2^{16}})$ (unit: Hz)

Therefore, VLO frequency $F_{LO} = F_{RF} = F_{LO\_BASE} + F_{OFFSET}$.

Please refer to Ch13 for details.

9.2.59 IF4 (Address: 0x103Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FI4	W	FPA7	FPA6	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0
Reset		0	0	0	0	0	0	0	0

FPA[15:0]: LO setting for frequency offset.

9.2.60 ACK1 (Address: 0x103Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACK1	W	RNUM3	RNUM2	RNUM1	RNUM0	MRCKS	CDRS1	CDRS0	SYNCS
	R	-	--	ARTEF	VPOAKF	RCR[3:0]			
Reset		0	0	0	0	0	0	0	0

MRCKS: Reserved for internal usage only. Shall be set to [0].

RNUM[3:0]:Reserved for internal usage only. Shall be set to [011]..

CDRS[1:0]: Carrier detect range select. Recommend CDRS = [01].
[00]: 8. **[01]:** 16. **[10]:** 24. **[11]:**32 .

SYNCS: RX demodulation sync word detect type select.
[0]: Sync word detect by re-preamble.

[1]: Sync word detect by using 64bytes buffer.

ARTEF: Auto-resend ending flag (read only).
[0]: Resend on going. **[1]:** Finish resending.

VPOAK: Valid Packet or ACK OK Flag (ready only).
This flag is clear by Strobe Command.
[0]: Neither valid packet nor ACK OK.
[1]: Valid packet or ACK OK.

RCR [3:0]: Auto Resend Cycle Decremented Count (read only).
Decremented of ARC[3:0] during auto-resend.

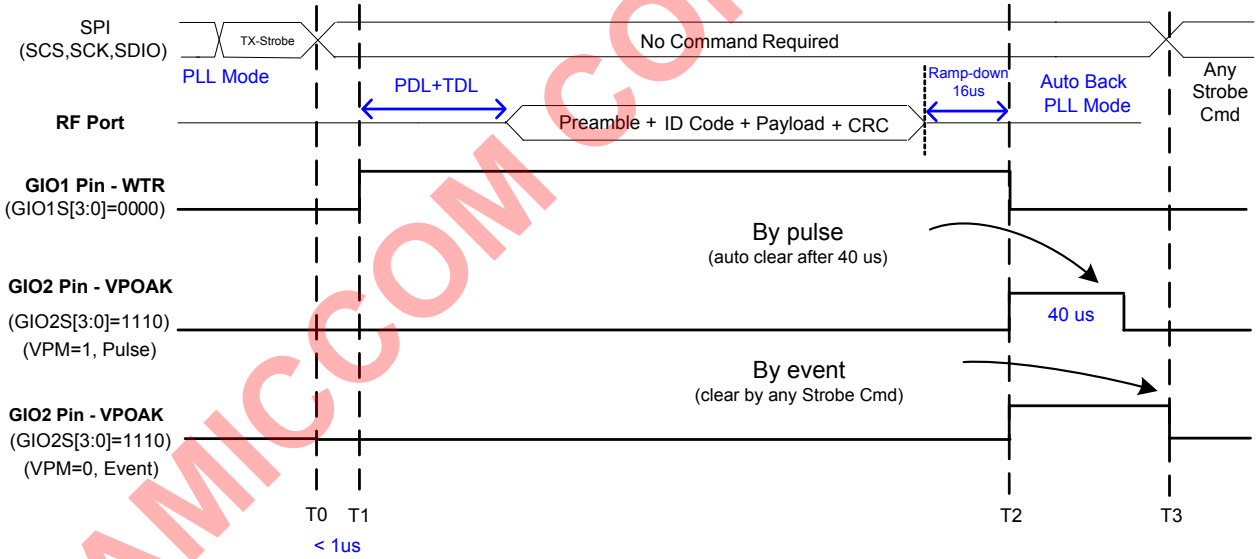
9.2.61 ACK2 (Address: 0x103Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACK2	W/R	VKM	VPM	ARTMS	ARC3	ARC2	ARC1	ARC0	EARKS
Reset		0	0	0	0	0	0	0	0

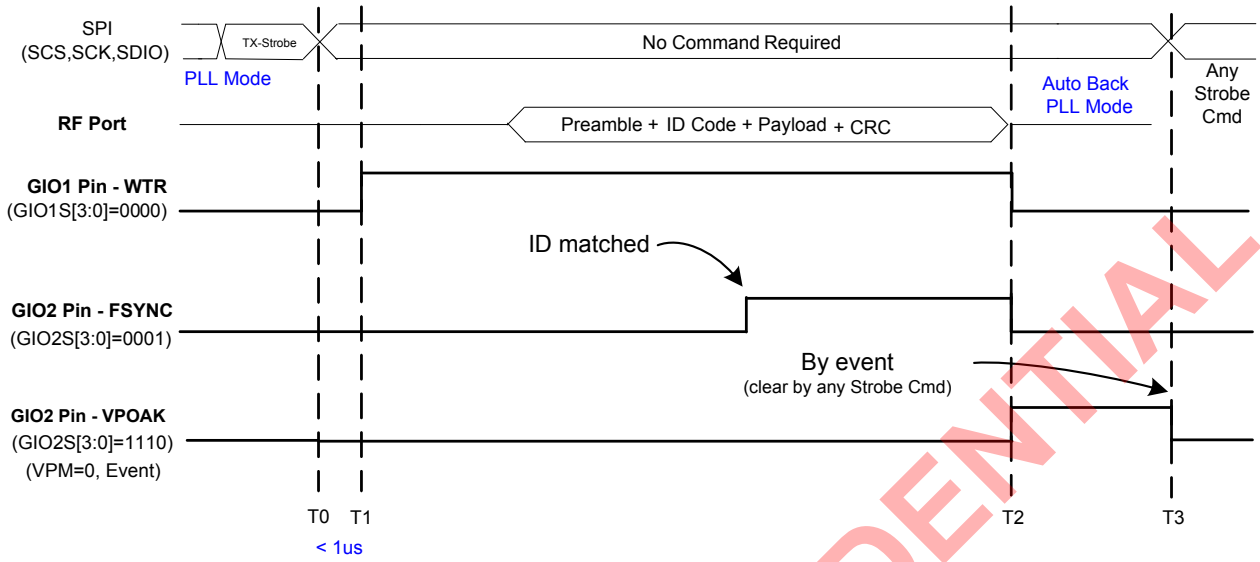
VKM: Valid Packet mode select.
[0]: by event. **[1]:** by pulse.

VPM: Valid Pulse width select.
[0]: 10u. **[1]:** 30u.

TX Mode (**disable** auto-resend, EARKS=0).



RX Mode (**disable** Auto-ack, EAKKS =0).



Note1, If auto-resend is enabled (EAR = 1), WTR behavior is different while it is output to GIO1 and GIO2.
Note2, If auto-ack is enabled (EAK = 1), WTR behavior is different while it is output to GIO1 and GIO2.
Note3, VPOAK's behavior is controlled by VPM (0Bh) and VPW (0Bh).
Refer to chapter 19 for details

ARTMS: Auto-resend Interval select.
[0]: random interval. **[1]:** fixed interval.

ARC [3:0] : Auto-resend Cycle Setting.
[0000]: resend disable.
[0001]: 1 **[0010]:** 2 **[0011]:** 3 **[0100]:** 4 **[0101]:** 5 **[0110]:** 6 **[0111]:** 7
[1000]: 8 **[1001]:** 9 **[1010]:** 10 **[1011]:** 11 **[1100]:** 12 **[1101]:** 13 **[1110]:** 14 **[1111]:** 15

EARKS: Auto-ack or auto-resend enable.
[0]: disable. **[1]:** enable auto-resend (TX) or enable auto-ack (RX)

9.2.62 ART1 (Address: 0x1040h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ART1	W/R	RND7	RND6	RND5	RND4	RND3	RND2	RND1	RND0
Reset		0	0	0	0	0	0	0	0

RND [7:0]: Random seed for auto-resend interval.

9.2.63 ART2 (Address: 0x1041h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ART2	W/R	ARD7	ARD6	ARD5	ARD4	ARD3	ARD2	ARD1	ARD0
Reset		0	0	0	0	0	0	0	0

ARD[7:0] : Auto Resend Delay
ARD Delay = 200 us * (ARD+1) → (200us ~ 51.2 ms)
Each step is 200 us.
[0000-0000]: 200 us.
[0000-0001]: 400 us.
[0000-0010]: 600 us.
…
…
[1111-1111]: 51.2 ms.

9.2.64 SYN1 (Address: 0x1042h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYN1	W	CST	WHT9	CRC16	CRC_MODE1	CRC_MODE0	-	EAF	DC_SEL
	R	FC1BTX[7:0]							
Reset		0	0	0	0	0	0	0	0

CST: DC average length selection. CST shall be [0].
[0]: DC average length unchanged. **[1]:** DC average length halves.

WHT9: Whitening with PN9 generator(X^9+X^5+1)

CRC16: CRC-16-CCITT register reset value setting when CRC_MODE=[00]. [0]: 0x1D0F. **[1]:** 0xFFFF.

CRC_MODE[1:0]: CRC Mode Select.
[00]: CRC-16-CCITT($X^{16}+X^{12}+X^5+1$).
[01]: CRC-16-DNP($X^{16}+X^{13}+X^{12}+X^{11}+X^{10}+X^8+X^6+X^5+X^2+1$).
[10]: CRC-16-IBM($X^{16}+X^{15}+X^2+1$)
[11]: CRC-8($X^8+X^7+X^3+X^{2+}1$)

EAF: Auto ack fifo selet. [1]: select.

DC_SEL:
[0]: By FSYNC (frame sync)
[1]: By DC average value, DCV[7:0]

FC1BTX[7:0]: FIFO control byte for TX transmission.(read only)

9.2.65 SYN2 (Address: 0x1043h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYN2	W	FCL	EDRL	RNUM12	RNUM11	RNUM10	RCK_sel	dbuf_sel1	dbuf_sel0
	R	FC1BRX[7:0]							
Reset		0	0	0	0	0	0	0	0

FCL: FIFO control byte enable. [1]: enable.
EDRL: Dynamic length enable. [1]: enable.
RNUM1[2:0]: Reserved for internal usage only. Shall be set to [011].
RCK_SEL: Reserved for internal usage only. Shall be set to [0].
DBUF_SEL[1:0]: Reserved for internal usage only. Shall be set to [00].

FC1BRX[7:0]: FIFO control byte received by RX.(read only)

9.2.66 AFEP1 (Address: 0x1044h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AFEP1	W	ACKFEP7	ACKFEP6	ACKFEP5	ACKFEP4	ACKFEP3	ACKFEP2	ACKFEP1	ACKFEP0
	R	--	LENFIFO[13:8]						
Reset		0	0	0	0	0	0	0	0

ACKFEP[7:0]: ACK FIFO length setting.

9.2.67 AFEP2 (Address: 0x1045h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AFEP2	W	WRDLY8	WRDLY7	WRDLY6	TX_1DLY4	TX_1DLY3	TX_1DLY2	TX_1DLY1	TX_1DLY0
	R	LENFIFO[7:0]							
Reset		0	0	0	0	0	0	0	0

TX1DLY[4:0]: TX Settling Delay scale. TX settling delay = 20us*(1+TDL[1:0]) + 1us*(1+TX1DLY)

LENFIFO [7:0]: Dynamic length received by RX.

9.2.68 DC (Address: 0x1046h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DC	-	-	-	-	-	-	-	-	-
	R	DCOUT[7:0]							
Reset		0	0	0	0	0	0	0	0

9.2.69 LPS (Address: 0x1047h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LPS	W	-	-	-	-	INTLPS	INTLP_MAN	CAL_VBS	--
Reset		0	0	0	0	0	0	0	0

INTLPS: Internal loop filter controlled by VCO band calibration. [1]: auto control. **[0]:** manual control.

INTLP_MAN: Reserved for internal usage only. Shall be set to [0].

CAL_VBS: Reserved for internal usage only. Shall be set to [0].

9.2.70 AUX (Address: 0x1048h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX	W	HBHC	-	-	-	-	-	-	-
Reset		0	0	0	0	0	0	0	0

HBHC: Reserved for internal usage only. Shall be set to [0].

9.2.71 WCK (Address: 0x1049h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WCK	W	WCKSEL1	WCKSEL0	B315	--	--	SYCKG	WOR_RST	WOR_HOLD
Reset		0	0	0	0	0	0	0	0

WCKSEL[1:0]: RC osc calibration refrence clock select. [00]: CSCK. **[01]:** CSCK/2. **[10]:** CSCK/4. **[11]:** CSCK/8

B315: Reserved for internal usage only. Shall be set to [0].

SYCKG: Crystal clock watch from CKO. [0]: disable. **[1]:** enable.

WOR_RST: TWWS width setting. [0]: pulse, reset by EOP. **[1]:** reset by strobe command.

WOR_HOLD: WOR hold RX setting when carrier detected or preamble ok. [0]: No hold. **[1]:** Hold RX.

9.2.72 CDET1 (Address: 0x104Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CDET1	W	CDTH17	CDTH16	CDTH15	CDTH14	CDTH13	CDTH12	CDTH11	CDTH10
Reset		0	0	0	0	0	0	0	0

CDTH[7:0]: In band carrier detect threshold manual setting.

9.2.73 CDET2 (Address: 0x104Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CDET2	W	RGS	ADCCS	--	EXADVR	RCHC	--	--	CD_SEL
Reset		0	0	0	0	0	0	0	0

RGS: VDD_D voltage setting in Sleep mode.
[0]:.Normal [1]: lower

ADCCS: **Reserved. Should set to [0]**

EXADVR: Reserved for internal usage only.

RCHC: Reserved for internal usage only. Shall be set to [0].

CD_SEL: In band carrier detect threshold manual setting select by using CDTH[7:0]. [1]: manual

9.2.74 NA

9.2.75 RX1 (Address: 0x104Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX1	W	MLP1	MLP0	SLF2	SLF1	SLF0	ETH2	ETH1	ETH0
	R	--	--	--	--	--	--	--	ADCO[8]
Reset		0	0	0	0	0	0	0	0

MLP[1:0]: Symbol recovery loop filter setting after ID SYNC. MLP shall be [01].

SLF [2:0]: Symbol recovery loop filter setting. SLF shall be [100].

ETH [2:0] (bit 15/8/7): ID code error bit tolerance. Recommend ETH = [001].
ETH [2:0] is located in [Bit15, Bit8, Bit7]
[000]: 0 bit. **[001]:** 1bit. **[010]:** 2 bits. **[011]:** 3 bits. **[100]:** 4 bits. **[101]:** 5 bits. **[110]:** 6 bits. **[111]:** 7 bits.

ADCO[8:0]: RSSI value if AGC =1 (Read Only).

9.2.76 RX2 (Address: 0x1050h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX2	W	DMT	DMOS	DMG1	DMG0	IFBW1	IFBW0	ULS	RXDI
	R	ADCO[7:0]]							
Reset		0	0	0	0	0	0	0	0

DMT : Demodulator test bit. DMT shall be [0].
[0]: Normal.
[1]: Test mode.

DMOS: Demodulator over-sample select. Recommend DMOS = [1].
[0]: x16.
[1]: x32.

DMG [1:0]: Demodulator Gain select. Recommend DMG = [01].
[00]: x1. **[01]:** x3. **[1x]:** x5.

IFBW [1:0]: IF Band Pass Filter select.
[00]: 50KHz. data rate ≦50Kbps. (Xtal shall be chosen ± 10 ppm stability in case of RX sensitivity degradation.)
[01]: 100KHz. 50K < data rate ≦100Kbps.

[10]: 150KHz. 100K < data rate ≦150Kbps.
[11]: 250KHz. 150K < data rate ≦250Kbps.

ULS: RX Up/Low side band select. Recommend ULS = [0].
[0]: Up side band, TX A-terminal frequency – IF = RX B-terminal frequency
[1]: Low side band, TX A-terminal frequency + IF = RX B-terminal frequency

RXDI: RX Data Invert. Recommend RXDI = [0].
[0]: normal. **[1]:** inverted.

9.2.77 RX3 (Address: 0x1051h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX3	W	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0
Reset		0	0	0	0	0	0	0	0

DCV[7:0]: Data DC average value setting. Recommend DCV = [10010].
This setting is only active when DCM (0x1052h) = [00].

9.2.78 RX4 (Address: 0x1052h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX4	W	PMD2	PMD1	PMD0	DCL2	DCL1	DCL0	DCM1	DCM0
Reset		0	0	0	0	0	0	0	0

PMD[2:0]: Preamble pattern detection. Recommend PMD = [100].
When DCM[1:0] = 01, 10, 11, chip will execute preamble length detection automatically.
[000]: 0 bit
[001]: 4 bits
[010]: 8 bits (Default value)
[011]: 16 bits
[100]: 24 bits.
[101] and [11x]: 32bits.
Remark: detection length setting should be smaller than the setting value of PML[1:0](0x1054h).

DCL[2:0]: Data Length of Peak Detect average setting. Recommend DCL = [010].
DCL[2:0] is used to let A9129 detects n times “0” or n times ”1” to result DC estimation voltage of demodulator.

DCL[2:0]	DC average	
	Before ID Sync	After ID Sync
000	4	32
001	8	32
010	16	32
011	32	32
100	4	64
101	8	64
110	16	64
111	32	64

For example,
If DCL[2:0] = 000,
Before ID sync, by peak detect method to update a new DC value for every 4 times 1” and 4 times ”0” .
After ID sync, by peak detect method, to update a new DC value for every 32 times “1” and 32 times ”0” .

DCM [1:0]: Demodulator DC estimation mode. Recommend DCM = [01].
[00]: By DC average value, DCV[7:0],(0Bh).
[01]: DC holds after preamble detected.
[10]: DC holds after ID detected.

[11]: DC value when chip receive specific data length (set by DCL[:2:0])..

9.2.79 CODE1 (Address: 0x1053h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CODE1	W	WS6	WS5	WS4	WS3	WS2	WS1	WS0	MCS
Reset		0	0	0	0	0	0	0	0

WS [6:0]: Data Whitening Seed (data encryption key, only for FIFO mode).

MCS: Manchester Code Enable. (only for FIFO mode)
[0]: Disable. **[1]:** Enable.

9.2.80 CODE2 (Address: 0x1054h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CODE2	W	WHTS	FECS	CRCS	PML2	PML1	PML0	IDL1	IDL0
Reset		0	0	0	0	0	0	0	0

WHTS: Data Whitening. (Data Encryption, only for FIFO mode)
[0]: Disable. **[1]:** Enable (The data is whitened by multiplying with PN7).

FECS: FEC Select. (only for FIFO mode)
[0]: Disable. **[1]:** Enable (The FEC is (7, 4) Hamming code).

CRCS: CRC Select. (only for FIFO mode)
[0]: Disable. **[1]:** Enable.

PML [2:0] (bit 15 / 1 / 0): Preamble Length Select. Recommend PML= [011].
[000]: 1 byte. **[001]:** 2 bytes. **[010]:** 3 bytes. **[011]:** 4 bytes.
[100]: 16 byte. **[101]:** 32 bytes. **[110]:** 48 bytes. **[111]:** 64 bytes.

IDL[1:0] (bit 14 / 2): ID code length setting. Recommend IDL=[01].
IDL [1:0] = [Bit14, Bit2].
[00]: 2 bytes. **[01]:** 4 bytes. **[10]:** 6 bytes. **[11]:** 8 bytes.

9.2.81 ADC1 (Address: 0x1055h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC1	W	ARSSI	RADC	AVS1	AVS0	MVSEL1	MVSEL0	XADSR	CDM
Reset		0	0	0	0	0	0	0	0

ARSSI: Auto RSSI measurement enable.
[0]: Disable. **[1]:** Enable.
ARSSI shall be [1] for auto RSSI measurement before MCU issues RX strobe command.

RADC: ADC Read Out Average Mode.
[0]: 1, 2, 4, 8 average mode. If RADC = 0, ADC average is set by AVSEL[1:0] (0Ch).
[1]: 8, 16, 32, 64 average mode. If RADC = 1, ADC average is set by MVSEL[1:0] (0Ch).

AVSEL [1:0]: ADC average mode. Recommend AVSEL = [10].
[00]: No average. **[01]:** 2. **[10]:** 4. **[11]:** 8.

MVSEL [1:0]: ADC average mode for VCO calibration and RSSI. Recommend MVSEL = [10].
[00]: 8. **[01]:** 16. **[10]:** 32. **[11]:** 64.

XADSR: ADC input signal source select.
[0]: Internal temperature sensor or RSSI signal.
[1]: External signal source.

CDM: Carrier Detect enable
[0]: RSSI/Temperature measurement.
[1]: Carrier detect

9.2.82 ADC2 (Address: 0x1056h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC2	W	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
	R	ADC[7:0]							
Reset		0	0	0	0	0	0	0	0

RTH[7:0]: Threshold value of Carrier Detect (Active in RX mode only).
CD (Carrier Detect) =1 when RSSI ≧ RTH.
CD (Carrier Detect) =0 when RSSI < RTL.

ADC[7:0]: RSSI value

9.2.83 ID0 (Address: 0x1057h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID0	W/R	IDR[63:56]							
Reset		0	0	0	0	0	0	0	0

IDR[63:0]: ID Data.

9.2.84 ID1 (Address: 0x1058h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID1	W/R	IDR[55:48]							
Reset		0	0	0	0	0	0	0	0

IDR[63:0]: ID Data.

9.2.85 ID2 (Address: 0x1059h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID2	W/R	IDR[47:40]							
Reset		0	0	0	0	0	0	0	0

IDR[63:0]: ID Data.

9.2.86 ID3 (Address: 0x105Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID3	W/R	IDR[39:32]							
Reset		0	0	0	0	0	0	0	0

IDR[63:0]: ID Data.

9.2.87 ID4 (Address: 0x105Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID4	W/R	IDR[31:24]							
Reset		0	0	0	0	0	0	0	0

IDR[63:0]: ID Data.

9.2.88 ID5 (Address: 0x105Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID5	W/R	IDR[23:16]							
Reset		0	0	0	0	0	0	0	0

IDR[63:0]: ID Data.

9.2.89 ID6 (Address: 0x105Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID6	W/R	IDR[15:8]							
Reset		0	0	0	0	0	0	0	0

IDR[63:0]: ID Data.

9.2.90 ID7 (Address: 0x105Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID7	W/R	IDR[7:0]							
Reset		0	0	0	0	0	0	0	0

IDR[63:0]: ID Data.

9.2.91 DID0 (Address: 0x105Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DID0	W/R	DID[31:24]							
Reset		0	0	0	0	0	0	0	0

DID[31:0]: Device ID.

9.2.92 DID1 (Address: 0x1060h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DID1	W/R	DID[23:16]							
Reset		0	0	0	0	0	0	0	0

DID[31:0]: Device ID.

9.2.93 DID2 (Address: 0x1061h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DID2	W/R	DID[15:8]							
Reset		0	0	0	0	0	0	0	0

DID[31:0]: Device ID.

9.2.94 DID3 (Address: 0x1062h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DID3	W/R	DID[7:0]							

Reset		0	0	0	0	0	0	0	0

DID[31:0]: Device ID.

9.2.95 NONCE0 (Address: 0x1063h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE0	W/R	NONCE[135:128]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.96 NONCE1 (Address: 0x1064h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE1	W/R	NONCE[127:120]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.97 NONCE2 (Address: 0x1065h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE2	W/R	NONCE[119:112]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.98 NONCE3 (Address: 0x1066h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE3	W/R	NONCE[111:104]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.99 NONCE4 (Address: 0x1067h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE4	W/R	NONCE[103:96]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.100 NONCE5 (Address: 0x1068h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE5	W/R	NONCE[95:88]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.101 NONCE6 (Address: 0x1069h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE6	W/R	NONCE[87:80]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.102 NONCE7 (Address: 0x106Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE7	W/R	NONCE[79:72]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.103 NONCE8 (Address: 0x106Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE8	W/R	NONCE[71:64]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.104 NONCE9 (Address: 0x106Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE9	W/R	NONCE[63:56]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.105 NONCE10 (Address: 0x106Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE10	W/R	NONCE[55:48]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.106 NONCE11 (Address: 0x106Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE11	W/R	NONCE[47:40]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.107 NONCE12 (Address: 0x106Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE12	W/R	NONCE[39:32]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.108 NONCE13 (Address: 0x1070h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE13	W/R	NONCE[31:24]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.109 NONCE14 (Address: 0x1071h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE14	W/R	NONCE[23:16]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.110 NONCE15 (Address: 0x1072h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE15	W/R	NONCE[15:8]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.111 NONCE16 (Address: 0x1073h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NONCE16	W/R	NONCE[7:0]							
Reset		0	0	0	0	0	0	0	0

NONCE[135:0]: CCM Nonce Setting.

9.2.112 AESK0 (Address: 0x1074h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESK0	W/R	AES_KEY[127:120]							
Reset		0	0	0	0	0	0	0	0

AES_KEY: 128 bits AES KEY for CCM operation.

9.2.113 AESK1 (Address: 0x1075h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESK1	W/R	AES_KEY [119:112]							
Reset		0	0	0	0	0	0	0	0

AES_KEY: 128 bits AES KEY for CCM operation.

9.2.114 AESK2 (Address: 0x1076h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

AESK2	W/R	AES_KEY [111:104]							
Reset		0	0	0	0	0	0	0	0

AES_KEY: 128 bits AES KEY for CCM operation.

9.2.115 AESK3 (Address: 0x1077h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESK3	W/R	AES_KEY [103:96]							
Reset		0	0	0	0	0	0	0	0

AES_KEY: 128 bits AES KEY for CCM operation.

9.2.116 AESK4 (Address: 0x1078h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESK4	W/R	AES_KEY [95:88]							
Reset		0	0	0	0	0	0	0	0

AES_KEY: 128 bits AES KEY for CCM operation.

9.2.117 AESK5 (Address: 0x1079h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESK5	W/R	AES_KEY [87:80]							
Reset		0	0	0	0	0	0	0	0

AES_KEY: 128 bits AES KEY for CCM operation.

9.2.118 AESK6 (Address: 0x107Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESK6	W/R	AES_KEY [79:72]							
Reset		0	0	0	0	0	0	0	0

AES_KEY: 128 bits AES KEY for CCM operation.

9.2.119 AESK7 (Address: 0x107Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESK7	W/R	AES_KEY [71:64]							
Reset		0	0	0	0	0	0	0	0

AES_KEY: 128 bits AES KEY for CCM operation.

9.2.120 AESK8 (Address: 0x107Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESK8	W/R	AES_KEY [63:56]							
Reset		0	0	0	0	0	0	0	0

9.2.121 AESK9 (Address: 0x107Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESK9	W/R	AES_KEY [55:48]							
Reset		0	0	0	0	0	0	0	0

AES_KEY: 128 bits AES KEY for CCM operation.

9.2.122 AESK10 (Address: 0x107Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESK10	W/R	AES_KEY [47:40]							
Reset		0	0	0	0	0	0	0	0

AES_KEY: 128 bits AES KEY for CCM operation.

9.2.123 AESK11 (Address: 0x107Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESK11	W/R	AES_KEY [39:32]							
Reset		0	0	0	0	0	0	0	0

AES_KEY: 128 bits AES KEY for CCM operation.

9.2.124 AESK12 (Address: 0x1080h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESK12	W/R	AES_KEY [31:24]							
Reset		0	0	0	0	0	0	0	0

AES_KEY: 128 bits AES KEY for CCM operation.

9.2.125 AESK13 (Address: 0x1081h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESK13	W/R	AES_KEY [23:16]							
Reset		0	0	0	0	0	0	0	0

AES_KEY: 128 bits AES KEY for CCM operation.

9.2.126 AESK14 (Address: 0x1082h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESK14	W/R	AES_KEY [15:8]							
Reset		0	0	0	0	0	0	0	0

AES_KEY: 128 bits AES KEY for CCM operation.

9.2.127 AESK15 (Address: 0x1083h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESK15	W/R	AES_KEY [7:0]							
Reset		0	0	0	0	0	0	0	0

AES_KEY: 128 bits AES KEY for CCM operation.

9.2.128 AESD0 (Address: 0x1084h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD0	W	AES_DIN [127:120]							
	R	AES_DOUT[127:120]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.129 AESD1 (Address: 0x1085h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD1	W	AES_DIN [119:112]							
	R	AES_DOUT[119:112]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.130 AESD2 (Address: 0x1086h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD2	W	AES_DIN [111:104]							
	R	AES_DOUT[111:104]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.131 AESD3 (Address: 0x1087h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD3	W	AES_DIN [103:96]							
	R	AES_DOUT[103:96]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.132 AESD4 (Address: 0x1088h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD4	W	AES_DIN [95:88]							
	R	AES_DOUT[95:88]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.133 AESD5 (Address: 0x1089h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD5	W	AES_DIN [87:80]							
	R	AES_DOUT[87:80]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.134 AESD6 (Address: 0x108Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD6	W	AES_DIN [79:72]							

	R	AES_DOUT[79:72]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.135 AESD7 (Address: 0x108Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD7	W	AES_DIN [71:64]							
	R	AES_DOUT[71:64]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.136 AESD8 (Address: 0x108Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD8	W	AES_DIN [63:56]							
	R	AES_DOUT[63:56]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.137 AESD9 (Address: 0x108Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD9	W	AES_DIN [55:48]							
	R	AES_DOUT[55:45]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.138 AESD10 (Address: 0x108Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD10	W	AES_DIN [47:40]							
	R	AES_DOUT[47:40]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.139 AESD11 (Address: 0x108Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD11	W	AES_DIN [39:32]							
	R	AES_DOUT[39:32]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.140 AESD12 (Address: 0x1090h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD12	W	AES_DIN [31:24]							
	R	AES_DOUT[31:24]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.141 AESD13 (Address: 0x1091h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD13	W	AES_DIN [23:16]							
	R	AES_DOUT[23:16]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.142 AESD14 (Address: 0x1092h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD14	W	AES_DIN [15:8]							
	R	AES_DOUT[15:8]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.143 AESD15 (Address: 0x1093h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESD15	W	AES_DIN [7:0]							
	R	AES_DOUT[7:0]							
Reset		0	0	0	0	0	0	0	0

AES_DATA: 128 bits AES Data for CCM operation.

9.2.144 TXPKT0 (Address: 0x1094h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TXPKT0	W/R	TX_PACKET [15:8]							
Reset		0	0	0	0	0	0	0	0

TX_PACKET[15:0]: Transmitted CCM-Counter for CCM-AES128 encryption.

9.2.145 TXPKT1 (Address: 0x1095h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TXPKT1	W/R	TX_PACKET [7:0]							
Reset		0	0	0	0	0	0	0	0

TX_PACKET[15:0]: Transmitted CCM-Counter for CCM-AES128 encryption.

9.2.146 RXPKT0 (Address: 0x1096h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RXPKT0	W/R	RX_PACKET [15:8]							
Reset		0	0	0	0	0	0	0	0

RX_PACKET[15:0]: Received CCM-Counter for CCM-AES128 decryption.

9.2.147 RXPKT1 (Address: 0x1097h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RXPKT1	W/R	RX_PACKET [7:0]							
Reset		0	0	0	0	0	0	0	0

RX_PACKET[15:0]: Received CCM-Counter for CCM-AES128 decryption.

9.2.148 AESCTL0 (Address: 0x1098h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESCTL0	W	CCM_TXEN_GO	CCM_RXDE_GO	CCM_RX_ON	AES_GO	--	--	--	CCM_TX_ON
Reset		0	0	0	0	0	0	0	0

CCM_TX_ON: Enable CCM Encryption / Decryption Function for Transmit..
[0]: Disable. **[1]:** Enable.

CCM_RX_ON: Enable CCM Encryption / Decryption Function for Receive..
[0]: Disable. **[1]:** Enable.

AES_GO: Enable AES Encryption.
[0]: Disable. **[1]:** Enable. (Auto clear)

CCM_TXENGO: Enable CCM Encryption for Transmit.
[0]: Disable. **[1]:** Enable. (Auto clear)

CCM_RXDEGO: Enable CCM Encryption for Receive.
[0]: Disable. **[1]:** Enable. (Auto clear)

9.2.149 AESCTL1(Address: 0x1099h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AESCTL1	W	TXPKT_R	RXDEC_A	CCM_RN	FBX	--	TXPKTS2	TXPKTS1	TXPKTS0
	R	--	--	CCM_OK_FLG	CCM_FAIL_FLG	--	--	--	--
Reset		0	0	0	0	0	0	0	0

CCM_OK: CCM Encryption / Decryption OK Flag.

CCM_FAIL: CCM Encryption / Decryption Fail Flag.

CCM_RN : CCM reset.

FBX : Reserved for internal usage only.

TXPKT_R: Randomize parameter for TX Packet Number.
[0]: Manual setting. [1]: Random number.

RXDEC_A: Auto CCM Decryption when received.
[0]: Manual. [1]: Auto.

TXPKS[2:0]: TX Packet Number select when segment CCM TX function used.

9.2.150 ADCCTL (Address: 0x109Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCCTL	W	BUFS	CKS[1]	CKS[0]	MODE	MVS[2]	MVS[1]	MVS[0]	ADCE
	R	--	--	--	MODE	MVS[2]	MVS[1]	MVS[0]	ADCE
Reset		0	0	0	0	0	0	0	0

BUFS: **input buffer select for 12 bit ADC.**
[0]: disable. **[1]:** enable.

ADCE: 12-bit ADC Enable.
[0]: Disable.
[1]: Enable. (auto clear when MODE = 0)

MVS[3:0]: ADC average mode select.
[000]: No moving average
[001]: 2 times average mode.

[010]: 4 times average mode.
[011]: 8 times average mode.
[100]: 16 times average mode.
[101]: 32 times average mode.
[110]: 64 times average mode.
[111]: 128 times average mode.

MODE: ADC mode select.
[0]: Single mode.
[1]: Continuous mode.

CKS[1:0]: ADC source clock select.
[00]: 4 MHz.
[01]: 2 MHz.
[10]: 1 MHz.
[11]: 500 KHz.

9.2.151 ADCAVG1 (Address: 0x109Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCAVG1	W	ADCIE	--	--	--	ADIVL	ADCYC	ENADC	DTMP
	R	MVADC[11]	MVADC[10]	MVADC[9]	MVADC[8]	ADC[11]	ADC[10]	ADC[9]	ADC[8]
Reset		0	0	0	0	0	0	0	0

ADCIE : 12-bits interrupt enable.
[0]: disable. **[1]:** enable.

ADIVL: Reserved. Should set to [0]
ADCYC: Reserved. Should set to [0]

ENADC: Enable ADC.

MVADC [11:0]: Moving average ADC output value

ADC [11:0]: ADC output value
MVADC[11:0]: Moving average ADC value.

9.2.152 ADCAVG2 (Address: 0x109Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCAVG2	R	MVADC[7]	MVADC[6]	MVADC[5]	MVADC[4]	MVADC[3]	MVADC[2]	MVADC[1]	MVADC[0]
Reset		0	0	0	0	0	0	0	0

MVADC[11:0]: Moving average ADC value.

9.2.153 ADCAVG3 (Address: 0x109Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCAVG3	R	ADC[7]	ADC[6]	ADC[5]	ADC[4]	ADC[3]	ADC[2]	ADC[1]	ADC[0]
Reset		0	0	0	0	0	0	0	0

ADC[11:0]: ADC value.

9.2.154 TMRINV (Address: 0x109Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRINV	W/R	TMR_INV[7:0]							
Reset		0	0	0	0	0	0	0	0

TMR_INV[7:0]: Timer interval setting.
Timer interval can be set to be:

TMRCKS[2:0] = 000: 7.808ms ~ 2s
TMRCKS[2:0] = 001: 16.616ms ~ 4s
TMRCKS[2:0] = 010: 31.232ms ~ 8s
TMRCKS[2:0] = 011: 62.464ms ~ 1.6ms
TMRCKS[2:0] = 100: 124.925ms ~ 3.18s
TMRCKS[2:0] = 101: 249.856ms ~ 6.37s
TMRCKS[2:0] = 110: 499.712ms ~ 12.74s
TMRCKS[2:0] = 111: 1s ~ 254.8s

9.2.155 TMRCTL (Address: 0x109Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRCTL	W	TMRON	TMRIE	TMRIF	--	TMRCKS[2:0]			TMRCE
Reset		0	0	0	0	0	0	0	0

TMRON: TMRCK ON.
TMRIE: Timer Interrupt Enable.
TMRIF: Timer Interrupt Flag. (Write to clear)
TMRCKS[2:0]: Select Timer Source Clock
[000]: 128Hz
[001]: 64Hz
[010]: 32Hz
[011]: 16Hz
[100]: 8Hz
[101]: 4Hz
[110]: 2Hz
[111]: 1Hz

TMRCE: Start Timer counting.
[0]: Stop.
[1]: Start.

9.2.156 INTIE (Address: 0x10A0h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	W	--	--	--	--	BBIE3	BBIE2	BBIE1	BBIE0
Reset		0	0	0	0	0	0	0	0

BBIE3: FSYNC interrupt enable.
[0]: Disable. [1]: Enable

BBIE2: FPF interrupt enable.
[0]: Disable. [1]: Enable

BBIE1: ARCWTR interrupt enable.
[0]: Disable. **[1]:** Enable

BBIE0: Wake BB interrupt enable.
[0]: Disable. [1]: Enable

9.2.157 EXT1 (Address: 0x10A1h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXT1	W	EBOD	--	SVREF	CELA	PDNFHR	QDSFHR	PDNFLR	QDSFLR
Reset		0	0	0	0	0	0	0	0

EBOD: Reserved for internal usage.

SVREF: Reserved for internal usage. Recommend SVREF = [0].

CELA: Reserved for internal usage.

PDNFHR: Flash power control for VDD_H. Recommend PDNFHR=[1].

QDSFHR: Flash power control for VDD_H. Recommend QDSFHR=[0].

PDNFLR: Flash power control for VDD_S. Recommend PDNFLR=[1].

QDSFLR: Flash power control for VDD_S. Recommend QDSFLR=[0].

9.2.158 EXT2 (Address: 0x10A2h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXT2	W	ENDL[2]	ENDL[1]	ENDL[0]	PDNS	ENAV	QDSA	ENDV	QDSD
Reset		0	0	0	0	0	0	0	0

ENDL[2:0]: Reserved for internal usage only

PDNS: Power manager to turn on REGOD Recommend PDNS = [0]

ENAV: REGOA and REGOS connection.

QDSA: quick discharge select for REGOA.

ENDV: REGOA is connected to REGOD.

QDSD: quick discharge select for REGOD.

PM mode: Low power operation select.

	MCU STOP
PM2(sleep)	ENAV=0, QDSA=1, ENDV=1, QDSD=0
PM3(deep sleep)	ENAV=0, QDSA=1, ENDV=0, QDSD=1

9.2.159 EXT3 (Address: 0x10A3h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXT3	W	OPHC1	OPHC0	CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
Reset		0	0	0	0	0	0	0	0

OPHC: Reserved for internal usage only.

CTR [5:0]: ADC voltage SPI fine trim setting.

9.2.160 EXT4 (Address: 0x10A4h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXT4	W	QDPA	PDNR	-	FBG4	FBG3	FBG2	FBG1	FBG0
Reset		0	0	0	0	0	0	0	0

QDPA: Reserved for internal usage only.

PDNR: Reserved for internal usage only.

FBG[4:0]: Bandgap voltage SPI fine trim setting.

9.2.161 EXT5 (Address: 0x10A5h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXT5	W	MXDM	MXDL	CMVS1	CMVS0	BFHC1	BFHC0	RGVP1	RGVP0
Reset		0	0	0	0	0	0	0	0

MXDM : Reserved for internal usage only.

MXDL : Reserved for internal usage only.

CMVS[1:0] : Reserved for internal usage only.

BFHC[1:0] : Reserved for internal usage only.

RGVP [1:0]: PLL Regulator Voltage select. Recommend RGVP = [00].
[00]: 1.2V
[01]: 1.3V
[10]: 1.4V
[11]: 1.5V

9.2.162 EXT6 (Address: 0x10A6h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXT6	W	-	-	STM[5:0]					
Reset		0	0	0	0	0	0	0	0

STM [5:0]: ADC voltage fine trim setting.

9.2.163 PA (Address: 0x10A7h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA	W	PALY1[3:0]				PALY2[3:0]			
Reset		0	0	0	0	0	0	0	0

PALY1[3:0]: Delay PDN_TX rising edge for PA control.

PALY2[3:0]: Delay PDN_TX falling edge for PA control.

10.SoC Architectural Overview

A9129 microcontroller is instruction set compatible with the industry standard 8051. Besides FSK/GFSK modulation RF transceiver, A9129 integrates many features, three 8/16bit counters/timers, watchdog timer, RTC, UART, SPI interface, I^2C interface, 2 channels PWM, 4 channels ADC, battery detector. The interrupt controller is extended to support 6 interrupt sources; watchdog timer, RTC, SPI, I^2C, ADC, RF and AES engine. A9129 includes TTAG (2-wire) debug circuitry that provides full time, real-time, in-circuit debugging.

10.1 Pipeline 8051 CPU

A9129 microcontroller has pipelined RSIC architecture 10 times faster compared to standard 8051 architecture. The pipeline 8051 is fully compatible with the MCS-51™ instruction set. User can use standard 8051 assemblers and compilers to develop software. The pipelined architecture 8051 has greatly increases its instruction throughput over the standard 8051 architecture. A9129 has a total of 110 instructions. The table below shows the total number of instructions that require each execution time. For more detail information of instruction, please refer Table 10.1.

Clock to Execute	1	2	3	4	5	6
Number of instructions	24	38	29	11	8	1

10.2 Memory Organization

The memory organization of A9129 is similar to the standard 8051. The memory organization is shown as figure 10.1

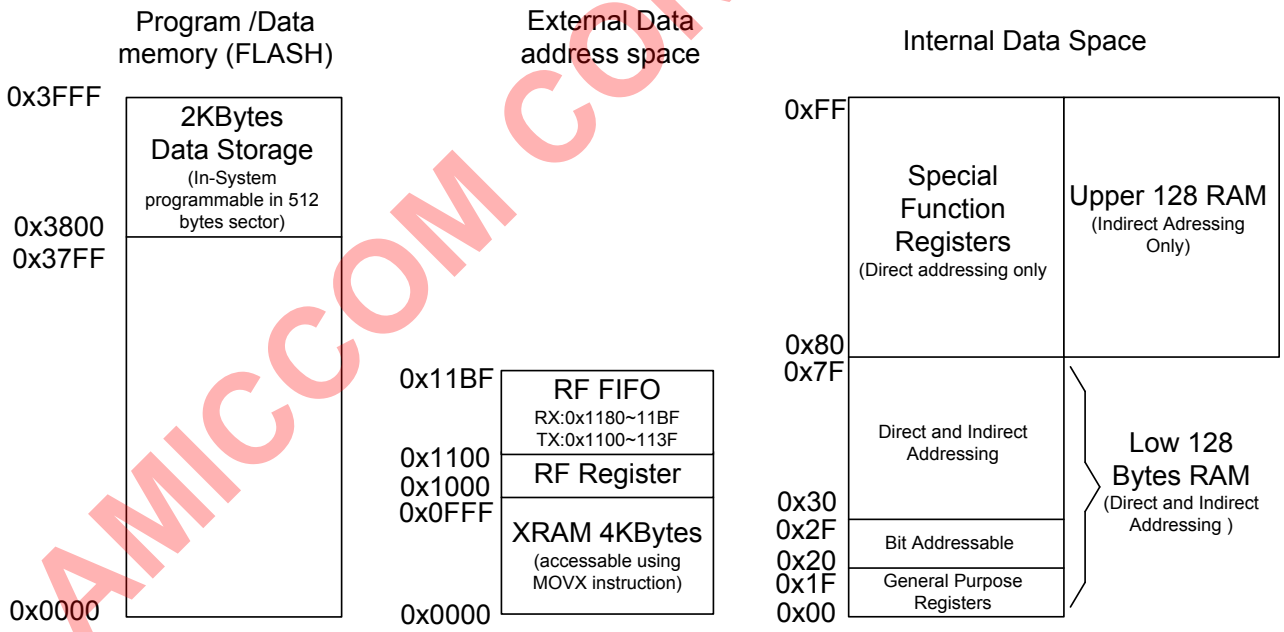


Figure 10.1 Memory Organization

10.2.1 Program memory

The standard 8051 core has 64KB program memory space. A9129 implements 16KB flash in one 16x 8Kb flash macro. The last 2KB program memory space (0x 3800 ~ 0x3FFF) supports IAP (In-Application Programming) function. The each block size in this area is 128Bytes. User has 16 blocks in 2KB program memory space to storage data. Program memory is normally assumed to be read-only. However, A9129 can write to program memory by IAP function call. Please reference application note to write program memory.

10.2.2 Data memory

The A9129 includes 256 bytes of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers and scratch pad memory. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode. The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFR) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory. Figure 10.1 illustrates the data memory organization of the A9129.

10.2.3 General Purpose Registers

The lower 32 bytes of data memory, locations 0x00 through 0x1F, may be addressed as four banks of general-purpose registers. Each bank consists of eight byte-wide registers designated R0 through R7. Only one of these banks may be enabled at a time. Two bits in the program status word, RS0 (PSW.3) and RS1 (PSW.4), select the active register bank (see description of the PSW in SFR Definition 9.4). This allows fast context switching when entering subroutines and interrupt service routines. Indirect addressing modes use registers R0 and R1 as index registers.

10.2.4 Bit Addressable Locations

In addition to direct access to data memory organized as bytes, the sixteen data memory locations at 0x20 through 0x2F are also accessible as 128 individually addressable bits. Each bit has a bit address from 0x00 to 0x7F. Bit 0 of the byte at 0x20 has bit address 0x00 while bit7 of the byte at 0x20 has bit address 0x07. Bit 7 of the byte at 0x2F has bit address 0x7F. A bit access is distinguished from a full byte access by the type of instruction used (bit source or destination operands as opposed to a byte source or destination). The MCS-51™ assembly language allows an alternate notation for bit addressing of the form XX.B where XX is the byte address and B is the bit position within the byte. For example, the instruction:
MOV C, 22.3h moves the Boolean value at 0x13 (bit 3 of the byte at location 0x22) into the Carry flag.

10.2.5 Special Function Registers

The direct-access data memory locations from 0x80 to 0xFF constitute the special function registers (SFRs). The SFRs provide control and data exchange with the CIP-51's resources and peripherals. The CIP-51 duplicates the SFRs found in a typical 8051 implementation as well as implementing additional SFRs used to configure and access the sub-systems unique to the MCU. This allows the addition of new functionality while retaining compatibility with the MCS-51™ instruction set. Table 9.2 lists the SFRs implemented in the CIP-51 System Controller.
The SFR registers are accessed anytime the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFRs with addresses ending in 0x0 or 0x8 (e.g. P0, TCON, SCON0, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided. Refer to the corresponding pages of the data sheet, as indicated in Table 9.2 for a detailed description of each register.

10.2.6 Stack

A9129 has 8-bit stack point called SP (0x81) located in the internal RAM space. It is incremented before data is stored during PUSH and CALL execution and decremented after data is popped during POP, RET and RETI execution. In the other words it always points to the last valid stack byte. The SP is accessed as any other SFRS.

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
81h SP Reset	R/W	0	0	0	0	0	1	1	1

Stack pointer register

10.2.7 Data Pointer Register

A9129 are implemented dual data pointer registers, auto increment and auto decrement to speed up data block copying. DPTR0 and DPTR1 are located at four SFR addresses. Active DPTR register is selected by SEL bit (0x86.0). If SEL = 0 the DPTR0 is selected otherwise DPTR1.

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
82h	R/W								

DPL0 Reset		0	0	0	0	0	0	0	0

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
83h DPH0 Reset	R/W	0	0	0	0	0	0	0	0

Data Pointer Register DPTR0

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
84h DPL1 Reset	R/W	0	0	0	0	0	0	0	0

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
85h DPH1 Reset	R/W	0	0	0	0	0	0	0	0

Data Pointer 1 Register DPTR1

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
86h DPS Reset	R/W	ID1 0	ID0 0	TSL 0	AU 0		- 0	- 0	SEL 0

Data Pointers Select Register

ID[1:0] - Increment/decrement function select. See table below.
TSL - Toggle select enable. When set, this bit allows the following DPTR related instruction to toggle the SEL bit following execution of the instruction:

```
MOVC A, @A+DPTR
INC DPTR
MOVX @DPTR, A
MOVX A, @DPTR
MOV DPTR, #data16
```

When TSL=0, DPTR related instructions do not affect state of SEL bit.

AU -When set to '1' performs automatic increment(0)/ decrement(1) of selected DPTR according to IDx bits, after each MOVX @DPTR, MOVC @DPTR instructions
SEL - Select active data pointer – see table below
- - Unimplemented bit. Read as 0 or 1.

ID1	ID0	SEL=1	SEL=0
0	0	INC DPTR1	INC DPTR
0	1	INC DPTR1	DEC DPTR
1	0	DEC DPTR1	INC DPTR
1	1	DEC DPTR1	DEC DPTR

Table DPTR0, DPTR1 operations

Selected data pointer register in used in the following instructions:

```
MOVX @DPTR,A
MOVX A,@DPTR
MOVC A,A+DPTR
JMP @A+DPTR
```

```
INC DPTR
MOV DPTR,#data16
```

10.2.8 RF Registers, RF FIFO

RF registers are RF radio control registers and located in 0x0800 ~ 0x08ff. Please refer the section 9.2 and the related function setting in the datasheet. A9129 has 256 Bytes FIFO located from 0x0900 to 0x09FF. There are 128 bytes FIFO from 0x0900 ~ 0x097F for data transmitting. There are 128 bytes FIFO from 0x0980 ~ 0x09FF for data receiving.

10.3 Instruction set

A9129 use a high performance, pipeline 8051 core and it is fully compatible with the standard MCS-51™ instruction set. Standard 8051 development tools can used to develop software for A9129. All A9129 instruction sets are the binary and functional equivalent of the MCS-51™. However, instruct timing is different with the standard 8051. All instruction timings are specified in the terms of clock cycles as shown in the table 10.1

Mnemonic	Description	Code	Bytes	Cycles
ACALL addr11	Absolute subroutine call	0x11-0xF1	2	4
ADD A,#data	Add immediate data to accumulator	0x24	2	2
ADD A,@Ri	Add indirect RAM to accumulator	0x26-0x27	1	2
ADD A,direct	Add direct byte to accumulator	0x25	2	2
ADD A,Rn	Add register to accumulator	0x28-0x2F	1	1
ADDC A,#data	Add immediate data to A with carry flag	0x34	2	2
ADDC A,@Ri	Add indirect RAM to A with carry flag	0x36-0x37	1	2
ADDC A,direct	Add direct byte to A with carry flag	0x35	2	2
ADDC A,Rn	Add register to accumulator with carry flag	0x38-0x3F	1	1
AJMP addr11	Absolute jump	0x01-0xE1	2	3
ANL C,/bit	AND complement of direct bit to carry	0xB0	2	2
ANL A,#data	AND immediate data to accumulator	0x54	2	2
ANL A,@Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A,direct	AND direct byte to accumulator	0x55	2	2
ANL A,Rn	AND register to accumulator	0x58-0x5F	1	1
ANL C,bit	AND direct bit to carry flag	0x82	2	2
ANL direct,#data	AND immediate data to direct byte	0x53	3	3
ANL direct,A	AND accumulator to direct byte	0x52	2	3
CJNE @Ri,#data	Compare immediate to ind. and jump if not equal	0xB6-0xB7	3	5
CJNE A,#datare	Compare immediate to A and jump if not equal	0xB4	3	4
CJNE A,directre	Compare direct byte to A and jump if not equal	0xB5	3	5
CJNE Rn,#datar	Compare immediate to reg. and jump if not equal	0xB8-0xBF	3	4
CLR A	Clear accumulator	0xE4	1	1
CLR bit	Clear direct bit	0xC2	2	3
CLR C	Clear carry flag	0xC3	1	1

CPL A	Complement accumulator	0xF4	1	1
CPL bit	Complement direct bit	0xB2	2	3
CPL C	Complement carry flag	0xB3	1	1
DA A	Decimal adjust accumulator	0xD4	1	3
DEC @Ri	Decrement indirect RAM	0x16-0x17	2	3
DEC A	Decrement accumulator	0x14	1	1
DEC direct	Decrement direct byte	0x15	1	3
DEC Rn	Decrement register	0x18-0x1F	1	2
DIV A,B	Divide A by B	0x84	1	6
DJNZ direct,rel	Decrement direct byte and jump if not zero	0xD5	3	5
DJNZ Rn,rel	Decrement register and jump if not zero	0xD8-0xDF	2	4
INC @Ri	Increment indirect RAM	0x06-0x07	1	3
INC A	Increment accumulator	0x04	1	1
INC direct	Increment directbyte	0x05	2	3
INC Rn	Increment register	0x08-0x0F	1	2
INC DPTR	Increment data pointer	0xA3	1	1
JB bit,rel	Jump if direct bit is set	0x20	3	5
JBC bit,directre	Jump if direct bit is set and clear bit	0x10	3	5
JC rel	Jump if carry flag is set	0x40	2	3
JMP@A+DPTR	Jump indirect relative to the DPTR	0x73	1	5
JNB bit,rel	Jumpifdirectbitisnotset	0x30	3	5
JNC	Jump if carry flag is not set	0x50	2	3
JNZ rel	Jump if accumulator is not zero	0x70	2	4
JZ rel	Jump if accumulator is zero	0x60	2	4
LCALL addr16	Long subroutine call	0x12	3	4
LJMP addr16	Long jump	0x02	3	4
MOV A,@Ri	Move indirect RAM to accumulator	0xE6-0xE7	1	2
MOV bit,C	Move carry flag to direct bit	0x92	2	3
MOV @Ri,#data	Move immediate data to indirect RAM	0x76-0x77	2	2
MOV @Ri,A	Move accumulator to indirect RAM	0xF6-0xF7	1	2
MOV @Ri,direct	Move direct byte to indirect RAM	0xA6-0xA7	2	3
MOV A,#data	Move immediate data to accumulator	0x74	2	2
MOV A,direct	Move direct byte to accumulator	0xE5	2	2
MOV A,Rn	Move register to accumulator	0xE8-0xEF	1	1
MOV C,bit	Move direct bit to carry flag	0xA2	2	2
MOV direct,#data	Move immediate data to direct byte	0x75	3	3
MOV direct,@Ri	Move indirect RAM to direct byte	0x86-0x87	2	3

MOV direct,A	Move accumulator to direct byte	0xF5	2	2
MOV direct,Rn	Move register to direct byte	0x88-0x8F	2	2
MOV direct1,direct2	Move direct byte to direct byte	0x85	3	3
MOV DPTR,#data16	Load 16-bit constant in to active DPTR	0x90	3	3
MOV Rn,#data	Move immediate data to register	0x78-0x7F	2	2
MOV Rn,A	Move accumulator to register	0xF8-0xFF	1	1
MOV Rn,direct	Move direct byte to register	0xA8-0xAF	2	3
MOVC A,@A+DPTR	Move code byte relative to DPTR to accumulator	0x93	1	5
MOVC A,@A+PC	Move code byte relative to PC to accumulator	0x83	1	4
MOVX @DPTR,A	Move A to external SRAM (16-bitaddress)	0xF0	1	1
MOVX @Ri,A	Move A to external RAM (8-bitaddress)	0xF2-0xF3	1	2
MOVX A,@DPTR	Move external RAM (16-bitaddress) to A	0xE0	1	2
MOVX A,@Ri	Move external RAM (8-bitaddress) to A	0xE2-0xE3	1	2
MUL A,B	Multiply A and B	0xA4	1	2
NOP	No operation	0x00	1	1
ORL direct,A	OR accumulator to direct byte	0x42	2	3
ORL A,#data	OR immediate data to accumulator	0x44	2	2
ORL A,@Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A,direct	OR direct byte to accumulator	0x45	2	2
ORL A,Rn	OR register to accumulator	0x48-0x4F	1	1
ORL C,/bit	OR complement of direct bit to carry	0xA0	2	2
ORL C,bit	OR direct bit to carry flag	0x72	2	2
ORL direct,#data	OR immediate data to direct byte	0x43	3	3
POP direct	Pop direct byte from internal ram stack	0xD0	2	2
PUSH direct	Push direct byte on to internal ram stack	0xC0	2	3
RET	Return from subroutine	0x22	1	4
RETI	Return from interrupt	0x32	1	4
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SETB C	Set carry flag	0xD3	1	1
SETB bit	Set direct bit	0xD2	2	3
SJMP rel	Short jump (relative address)	0x80	2	3
SUBB A,@Ri	Subtract indirect RAM from A with borrow	0x96-0x97	1	2
SUBB A,direct	Subtract direct byte from A with borrow	0x95	2	2
SUBB A,#data	Subtract immediate data from A with borrow	0x94	2	2

SUBB A,Rn	Subtract register from A with borrow	0x98-0x9F	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	1
XCH A,@Ri	Exchange indirect RAM with accumulator	0xC6-0xC7	1	3
XCH A,direct	Exchange direct byte with accumulator	0xC5	2	3
XCH A,Rn	Exchange register with accumulator	0xC8-0xCF	1	2
XCHD A,@Ri	Exchange low-order nibble indirect RAM with A	0xD6-0xD7	1	3
XRL direct,#data	ExclusiveOR immediate data to direct byte	0x63	3	3
XRL A,#data	ExclusiveOR immediate data to accumulator	0x64	2	2
XRL A,@Ri	ExclusiveOR indirect RAM to accumulator	0x66-0x67	1	2
XRL A,direct	ExclusiveOR direct byte to accumulator	0x65	2	2
XRL A,Rn	ExclusiveOR register to accumulator	0x68-0x6F	1	1
XRL direct,A	ExclusiveOR accumulator to direct byte	0x62	2	3

Table 10.1 Instruction set sorted by alphabet

10.4 External interrupt handler

This section describes 8051 external interrupts and their functionality. For peripheral related interrupts, please refer to an appropriate peripheral section. The external interrupts symbol is shown in figure above. And the pins functionality is described in the following table. All pins are one directional. There are no three-state output pins and internal signals.

Name	ACTIVE	TYPE	DESCRIPTION
int0(P3.2)	low/falling	Input	External interrupt 0 line
int1(P3.3)	low/falling	Input	External interrupt 1 line
int2(P0.7)	low	Input	External interrupt 2 line
RF_int	failing		
Key_int	failing		

Table 10.2 External interrupts pins description

10.4.1 FUNCTIONALITY

All 8051 IP cores have implemented two levels interrupt priority control. Each external interrupt can be in high or low level priority group by setting or clearing a bit in the IP(0xB8), EIP(0xF8), and DEVICR(0xCF) registers. External interrupt pins are activated at low level or by a falling edge. Interrupt requests are sampled each system clock at the rising edge of CLK.

Interrupt flag	Function	Active level/edge	Flag resets	Vector[1]	Natural priority
IE0	Device pin INT0	Low/falling	Hardware	0x03	1
TF0	Internal, Timer 0	-	Hardware	0x0B	2
IE1	Device pin INT1	Low/falling	Hardware	0x13	3
TF1	Internal, Timer 1	-	Hardware	0x1B	4
TI0 & RI0	Interrupt, UART0	-	Software	0x23	5
TF2	Interrupt, Timer 2	-	Software	0x2B	6
INT2F	Device pin INT2	Low	Hardware	0x3B	8
RFINT	Interrupt, RF	-	Software	0x53	11
KEYINT	Interrupt, Key	-	Software	0x5B	12
WDIF	Internal, Watchdog	-	Software	0x63	13
I2CMIF	Internal, I2C MASTER MODULE	-	Software	0x6B	14
I2CSIF SPIIF	Internal, DI2CS/ Internal, SPI	-	Software	0x73	15

Table10.3 8051 interrupts summary

1- This is a default location when IRQ_INTERVAL = 8, in other case is equal to (IRQ_INTERVAL* n) + 3, when n = (natural Priority - 1)

Each interrupt vector can be individually enabled or disabled by setting or clearing a corresponding bit in the IE(0xA8), EIE(0xE8), DEVICR(0xCF). The IE contains global interrupt system disable(0) / enable(1) bit called EA.

IE register (0xA8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A8h IE	R/W	EA	-	ET2	ES0	ET1	EX1	ET0	EX0
Reset		0	0	0	0	0	0	0	0

EA：Enable global interrupts
EX0：Enable INT0 interrupts
ET0：Enable Timer 0 interrupts
EX1：Enable INT1 interrupts
ET1：Enable Timer 1 interrupts
ES0：Enable UART0 interrupts
ET2：Enable Timer 2 interrupts

All of bits that generate interrupts can be set or cleared by software, with the same result as if they had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled by software. The exceptions of this rule are the request flags IE0 and IE1. If the external interrupts 0 or 1 are programmed to be level activated, IE0 and IE1 are controlled by the external source via pin INT0 and INT1, respectively. Thus, writing a one to these bits will not set the request flag IE0 and/or IE1. The same exception is related to INT2F, INT5F, and INT6F – external interrupts number 2, 3, 4, 5, 6.

IP register (0xB8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B8h IP	R/W	-	-	PT2	PS0	PT1	PX1	PT0	PX0
Reset		0	0	0	0	0	0	0	0

PX0：INT0 priority level control (at 1-high-level)
PT0：Timer 0 priority level control (at 1-high-level)
PX1：INT1 priority level control (at 1-high-level)
PT1：Timer 1 priority level control (at 1-high-level)
PS0：UART0 priority level control (at 1-high-level)
PT2：Timer 2 priority level control (at 1-high-level)

TCON register (0x88)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
88h TCON	R/W	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Reset		0	0	0	0	0	0	0	0

IT0：INT0 level (at 0) / edge (at 1) sensitivity
IT1：INT1 level (at 0) / edge (at 1) sensitivity
IE0：INT0 interrupt flag
Cleared by hardware when processor branches to interrupt routine
IE1：INT1 interrupt flag
Cleared by hardware when processor branches to interrupt routine
TF0：Timer 0 interrupt (overflow) flag
Cleared by hardware when processor branches to interrupt routine
TF1：Timer 1 interrupt (overflow) flag
Cleared by hardware when processor branches to interrupt routine

SCON0 register (0x98)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
98h SCON0	R/W	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Reset		0	0	0	0	0	0	0	0

RI0：UART0 receiver interrupt flag
TI0：UART0 transmitter interrupt flag

EIE register (0xE8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E8h EIE	R/W	EI2CS ESPI	EI2CM	EWDI	EKEYINT	ERFINT	EINT4	EINT3	EINT2
Reset		0	0	0	0	0	0	0	0

EINT2：Enable INT2 interrupts
EINT3：Enable INT3
EINT4：Enable INT4
ERFINT：Enable RF INT
EKEYINT：Enable KEY INT
EWDI：Enable Watchdog interrupts
EI2CM：Enable I2C MASTER MODULE interrupts
EI2CS：Enable DI2CS interrupts
ESPI：Enable SPI MODULE interrupts

EIP register (0xF8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F8h EIP	R/W	PI2CS PSPI	PI2CM	PWDI	PKEYINT	PRFINT	PINT4	PINT3	PINT2
Reset		0	0	0	0	0	0	0	0

PINT2：INT2 priority level control (at 1-high-level)
PINT3：INT3 (at 1-high-level)
PINT4：INT4 (at 1-high-level)
PRFINT：RFINT priority level control (at 1-high-level)
PKEYINT：KEYINT priority level control (at 1-high-level)
PWDI：Watchdog priority level control (at 1-high-level)
PI2CM：I2C MASTER MODULE priority level control (at 1-high-level)
PI2CS：I2C MODULE priority level control (at 1-high-level)
PSPI：SPI MODULE priority level control (at 1-high-level)

EIF register (0x91)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
91h EIF	R/W	I2CSF SPIF	I2CMF	-	INT6F	INT5F	-	-	INT2F
Reset		0	0	0	0	0	0	0	0

INT2F：INT2 interrupt flag
Should be cleared by external hardware when processor branches to interrupt routine. This bit is a copy of INT2 pin updated every CLK period. It cannot be set by software.
RFINT：RFINT interrupt flag
Must be cleared by software writing 0x08 when controlled by INT5 pin, else must be cleared by software writing 0x08 when Compare2 is enabled CCEN[5:4]=10. It cannot be set by software.
KEYINT：KEYINT interrupt flag
Must be cleared by software writing 0x10 when controlled by INT6 pin, else must be cleared by software writing 0x10 when Compare3 is enabled CCEN[7:6]=10. It cannot be set by software.
I2CMIF：I2C MASTER MODULE interrupt flag. Must be cleared by software writing 0x40. It cannot be set by software

I2CSIF：I2C MODULE interrupt flag
SPIIF：SPI MODULE interrupt flag
Software should determine the source of interrupt by checking both modules' interrupt related bits. Must be cleared by software writing 0x80. It cannot be set by software.

Note2: A peripheral related bit is available if this peripheral device is included in the system. Can be modified upon request. Please check your configuration.

SPIIF：SPI MODULE interrupt flag
Software should determine the source of interrupt by checking both modules' interrupt related bits. Must be cleared by software writing 0x80. It cannot be set by software.

Key interrupt
1. P0 / P1 ==> 1 個 wakeup bit, control 2 個 pin.
2. P3 ==> 1 個 wakeup bit, control 1 個 pin.

10.5 Reset Circuit

RSFLAG (0xBA):

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BAh RSFLAG	R	-	-	-	-	-	BODF	RESETNF	PORF
Reset		0	0	0	0	0	0	0	0

PORF (power-on reset flag)
= 1: Occurred Power-on Reset
= 0: No Power-on Reset
RESETNF (resetn flag)
= 1: Occurred ResetN reset
= 0: No ResetN resetno resetn reset
BODF (Low voltage detect) flag
= 1: Occurred Low Voltage Reset
= 0: No Low Voltage reset

The BODF bit will probably be set to 1 when the voltage of REGI pin rising time is larger than 5ms(0 to 3V).

11. I/O Ports

A9129 has 24 Digital I/O Pins. There are separated to 3 Ports (Port0, Port1 and Port3) and each of the Port pin can be defined as general-purpose I/O (GPIO) or peripheral I/O signals connected to the timers, UART, I2C and SPI functions. Thus, each pin can also be used to wake A9129 up from sleep mode. User can select each pin function by setting register. Each port has itself port register like P0 (0x80), P1 (0x90) and P3 (0xB0) that are both byte addressable and bit addressable. When reading, the logic levels of the Port's input pins are returned. Each port has three registers to setting Pull-up (PU), Output-enable (OE) and Wake-up enable (WUE). As shown the bellow block diagram, Fig. 11.1. Unused I/O pins should have a defined level and not be left floating. One way to do this is to leave the pin unconnected and configure the pin as a general-purpose I/O input with pull-up resistor.

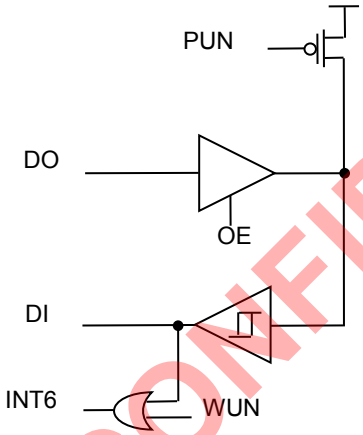


Figure11.1 Ports I/O block diagram

Table 11.1 OE and PUN setting and Output(P) and Input(DI)

OE	PUN	P	DI
0	0	1	1
0	1	HZ	INH
1	X	DO	DO

Table 11.2 WUN setting and INT6 source

WUN	INT6
0	DI
1	1

11.2 FUNCTIONALITY

It has three 8-bit full bi-directional ports, P0, P1 and P3. Each port bit can be individually accessed by bit addressable instructions.

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80h P0	R/W								
Reset		0	0	0	0	0	0	0	0

Port 0 register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
90h P1	R/W								
Reset		0	0	0	0	0	0	0	0

Port 1 register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B0h P3	R/W								
Reset		0	0	0	0	0	0	0	0

Port 3 register

Read and write accesses to the I/O port are performed via their corresponding SFRs P0(0x80), P1(0x90), and P3(0xB0). Some port-reading instructions read the data register and others read the port's pin. The "Read-Modify-Write" instructions are directed to the data registers and are shown below. All the other instructions used to read a port exclusively read the port's pin.

Instruction	Function description
ANL	Logic AND
ORL	Logic OR
XRL	Logic eXclusive OR
JBC	Jump if bit is set and clear
CPL	Complement bit
INC, DEC	Increment, decrement byte
DJNZ	Decrement and jump if not zero
MOV Px.y, C	Move carry bit to y of port x
CLR Px.y	Clear bit y of port x
SETB Px.y	Set bit y of port x

Table11.2 Read-modify-write instructions

According the Table 11.1, all Port pins can be configured as Output, Input with pull-up resistor(around 100 Kohm) or Input. Please refer the following truth table to know every function setting. When OE=1, this pin is configured as Output. Otherwise OE =0, this pin is configured as Input. User can set PU =1 or 0 depending on application. When OE =1, PU=0 is recommended for saving power. Please notice that: please set P3.2, P3.3, P3.4 and P3.5 to output high or input with pull-up in PM mode to save leakage current.

OE	PU	P	DI
1	X	DO	DO
0	1	Pull-up	P
0	0	HZ	Input

All Port pins can wake A9129 up when WUEN=1 and configured GPIO. All Port pins' WEU signals connect one AND gate to INT2. It means pin wake up function needs INT2 ISR to take care this interrupt.

WUEN	WUNDI
1	1
0	DI

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B2h P0PU	R/W								
Reset		0	0	0	0	0	0	0	0

Port 0 Pull Up Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B3h P0OE	R/W								
Reset		0	0	0	0	0	0	0	0

Port 0 Output Enable Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B4h	R/W								

P0WUE									
Reset		0	0	0	0	0	0	0	0

Port 0 Wake Up Enable Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B5h P1PU	R/W								
Reset		0	0	0	0	0	0	0	0

Port 1 Pull Up Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B6h P1OE	R/W								
Reset		0	0	0	0	0	0	0	0

Port 1 Output Enable Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B7h P1WUE	R/W								
Reset		0	0	0	0	0	0	0	0

Port 1 Wake Up Enable Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AAh P3PU	R/W								
Reset		0	0	0	0	0	0	0	0

Port 3Pull Up Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ABh P3OE	R/W								
Reset		0	0	0	0	0	0	0	0

Port 3 Output Enable Register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACh P3WUE	R/W								
Reset		0	0	0	0	0	0	0	0

Port 3 Wake Up Enable Register

IOSEL Register (0xBB)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BBh IOSEL	R/W	ADCIOS2	ADCIOS1	ADCIOS0	RTCIOS	BBIOS	-	I2CIOS	URT0IOS
Reset		0	0	0	0	0	0	0	0

URT0IOS (UART0 I/O select)
[1]: Port 3.0 and Port3.1 are selected for UART0 mode0
[0]: Port 3.0 and Port3.1 are normal I/O
I2CIOS (I2C I/O select)
[1]: The pad is selected for I2C
[0]: The pad is normal I/O
BBIOS (Base band I/O select)
[1]: Output
[0]: Input
RTCIOS (Real-time clock I/O select)

[1]: The pad is for RTC clock
[0]: The pad is normal I/O
ADCIOS[2:0] (ADC I/O select)
ADCIOS0
[1]: Enable ADC analog input
[0]: Disable ADC analog input
ADCIOS[2:1]
[00]: Select P3.2 as the ADC analog input
[01]: Select P3.3 as the ADC analog input
[10]: Select P3.4 as the ADC analog input
[11]: Select P3.5 as the ADC analog input

12. Timer 0 & 1 &2

A9129 contains three 16-bit timer/counters, Timer 0, Timer 1 and Timer 2. Timer 0 and Timer 1 in the “timer mode“, timer registers are incremented every 4/12/CLK periods depends on CKCON (0x8E) setting, when appropriate timer is enabled. In the “counter mode” the timer registers are incremented every falling transition on theirs corresponding input pins: T0 or T1. The input pins are sampled every CLK period.

The Timer 2 is one of the most powerful peripheral units of the core. It can be used for all kinds of digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc.

12.1 Timer 0 & 1 PINS DESCRIPTION

The pins functionality is described in the following table. All pins are one directional.

PIN	ACTIVE	TYPE	DESCRIPTION
T0(P3.4)	Falling	Input	Timer 0 clock line
GATE0(P3.2)	High	Input	Timer 0 clock line gate control
T1(P3.5)	Falling	Input	Tiner 1 clock line
GATE1(P3.3)	High	Input	Timer 1clock line gate control

Table12.1 Timer 0, 1 pins description

12.2 Timer 0 & 1 FUNCTIONALITY

12.2.1 OVERVIEW

Timer 0 and Timer 1 are fully compatible with the standard 8051 timers. Each timer consists of two 8-bit registers TH0 (0x8C), TL0 (0x8A), TH1 (0x8D), TL1 (0x8B). Timers 0, 1 work in the same four modes. The modes are described below.

M1	M0	Mode	Function description
0	0	0	THx operates as 8-bit timer/counter with a divide by 32 prescaler served by lower 5-bit of TLx.
0	1	1	16-bit timer/counter. THx and TLx are cascaded.
1	0	2	TLx operates as 8-bit timer/counter with 8-bit auto-reload by THx.
1	1	3	TL0 is configured as 8-bit timer/counter controlled by the standard Timer 0 bits. TH0 is an 8-bit timer controlled by the Timer 1 controls bits. Timer 1 holds its count.

Table12.2 Timer 0 and 1 modes

12.2.2 Timer 0 & 1 Registers

TMOD register (0x89)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
89h TMOD	R/W	GATE1	CT	M1	M0	GATE0	CT	M1	M0
		Timer 1 control bits				Timer 0 control bits			
Reset		0	0	0	0	0	0	0	0

GATE：Gating control
=1, Timer x enabled while GATEx pin is high and TRx control bit is set.
=0, Timer x enabled while TRx control bit is set.
CT：Counter or timer select bit
=1, Counter mode, Timer x clock from Tx pin.
=0, Timer mode, internally clocked.
M[1：0]：Mode select bits
TCON register (0x88)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
88h TCON	R/W	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Reset		0	0	0	0	0	0	0	0

TR0：Timer 0 run control bit
=1, enabled.

=0, disabled.

TR1：Timer 1 run control bit

=1, enabled.

=0, disabled.

TF0：Timer 0 interrupt (overflow) flag.

Cleared by hardware when processor branches to interrupt routine.

TF1：Timer 1 interrupt (overflow) flag.

Cleared by hardware when processor branches to interrupt routine.

CKCON register (0x8E)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8Eh CKCON	R/W	-	-	-	T1M	T0M	MD2	MD1	MD0
Reset		0	0	0	0	0	0	0	0

T0M：This bit controls the division of the system clock that drives Timer 0.

=1, Timer 0 uses a divided-by-4 of the system clock frequency.

=0, Timer 0 uses a divided-by-12 of the system clock frequency.

T1M：This bit controls the division of the system clock that drives Timer 1.

=1, Timer 1 uses a divided-by-4 of the system clock frequency.

=0, Timer 1 uses a divided-by-12 of the system clock frequency.

IE register (0xA8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A8h IE	R/W	EA	-	ET2	ES0	ET1	EX1	ET0	EX0
Reset		0	0	0	0	0	0	0	0

EA：Enable global interrupts.

ET0：Enable Timer 0 interrupts.

ET1：Enable Timer 1 interrupts.

IP register (0xB8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B8h IP	R/W	-	-	PT2	PS0	PT1	PX1	PT0	PX0
Reset		0	0	0	0	0	0	0	0

PT0：Timer 0 priority level control (at 1-high level)

PT1：Timer 1 priority level control (at 1-high level)

Timer 0, 1 related bits that generate interrupts can be set or cleared by software, with the same result as if they had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled by software.

Interrupt flag	Function	Active level/edge	Flag resets	Vector	Natural priority
TF0	Internal, Timer 0	-	Hardware	0x0B	2
TF1	Internal, Timer 1	-	Hardware	0x1B	4

Table12.3 Timer 0, 1 interrupts

12.2.3 Timer 0 – Mode 0

In this mode, the Timer 0 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s. Timer 0 interrupt flag TF0 is set. The counted input is enabled to the Timer 0 when TCON.4 = 1 and either TMOD.3 = 1 or GATE0 = 1. (Setting TMOD.3 = 1 allows the Timer 0 to be controlled by external input GATE0, to facilitate pulse width measurement). The 13-bit register consists of all 8-bit of TH0 and lower 5 bits of TL0.The upper 3 bits of TL0 are indeterminate and should be ignored.

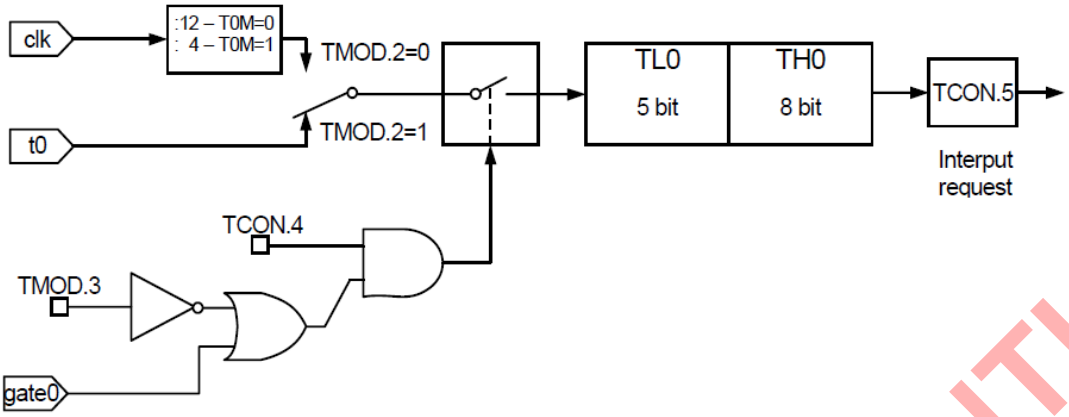


Figure12.1 Timer/Counter 0, Mode 0：13-Bit Timer/Counter

12.2.4 Timer 0 – Mode 1

Mode 1 is the same as Mode 0, except that the timer register is running with all 16 bits. Mode 1 is shown in figure below.

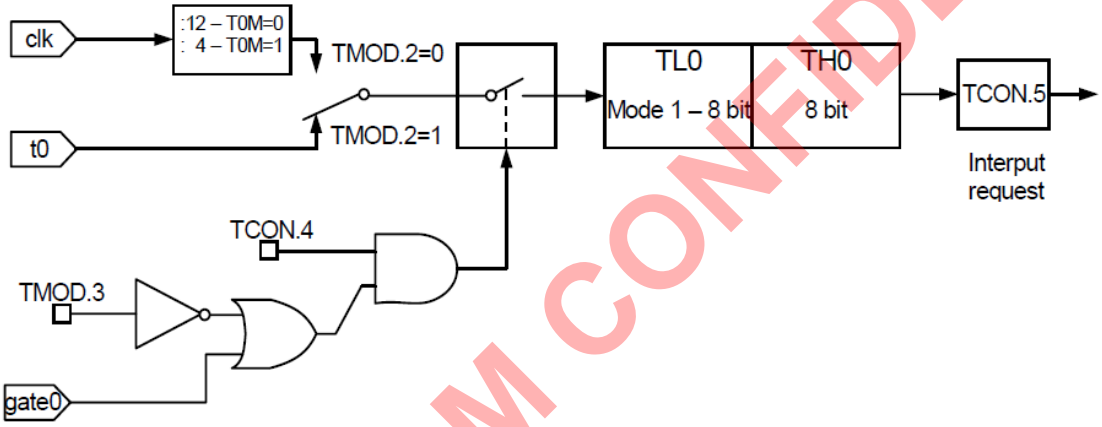


Figure12.2 Timer/Counter 0, Mode 1：16-Bit Timer/Counter

12.2.5 Timer 0 – Mode 2

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reloads, as shown in figure below. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is loaded by software. The reload leaves TH0 unchanged.

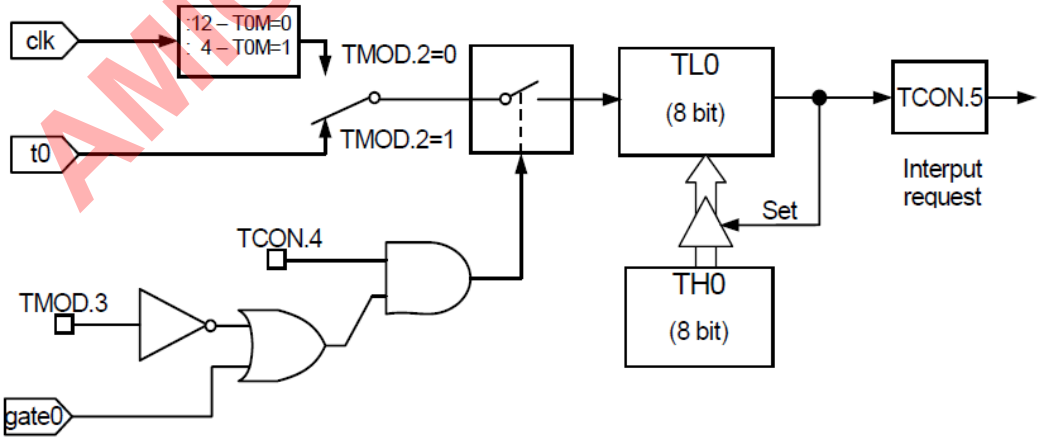


Figure12.3 Timer/Counter 0, Mode 2：8-Bit Timer/Counter with Auto-Reload

12.2.6 Timer 0 – Mode 3

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in figure below. TL0 uses the Timer 0 control bits：C/T, GATE, TR0, GATE0 and TF0. TH0 is locked into a timer function and use the TR1 and TF1 flag from Timer1 and controls Timer1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer/counter. When Timer 0 is in Mode 3, Timer 1 can be turned off by switching it into its own Mode 3, or can still be used by the serial channel as a baud rate generator, or in any application where interrupt from Timer 1 is not required.

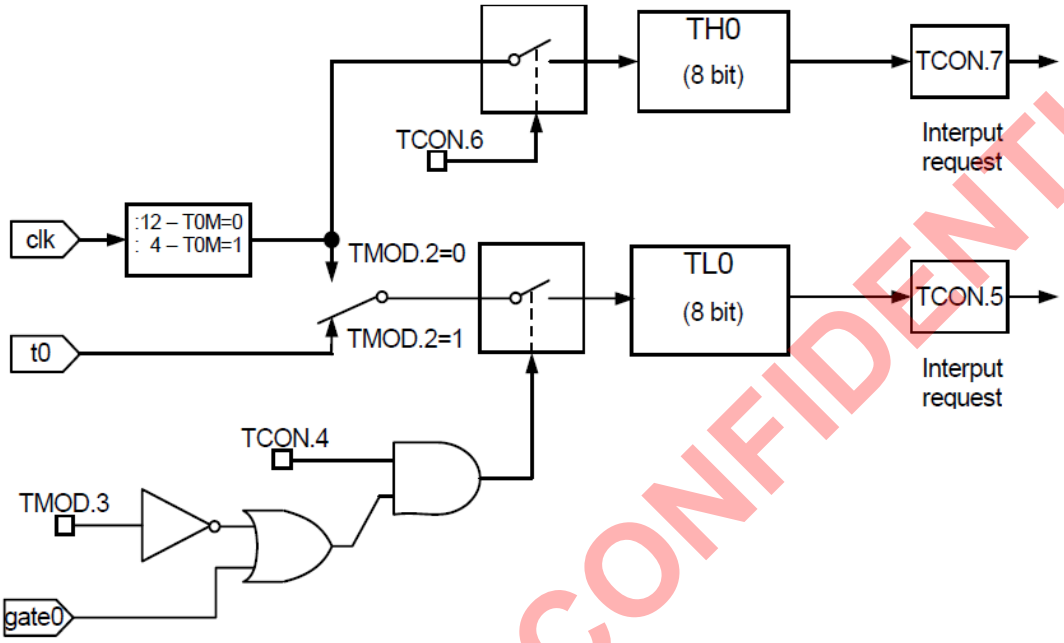


Figure12.4 Timer/Counter 0, Mode 3：Two 8-Bit Timers/Counters

12.2.7 Timer 1 – Mode 0

In this Mode, the Timer1 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, Timer1 interrupt flag TF1 is set. The counted input is enabled to the Timer1 when TCON.6 = 1 and either TMOD.6 = 0 or GATE1 = 1. (Setting TMOD.7 = 1 allows the Timer1 to be controlled by external input GATE1, to facilitate pulse width measurements). The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored.

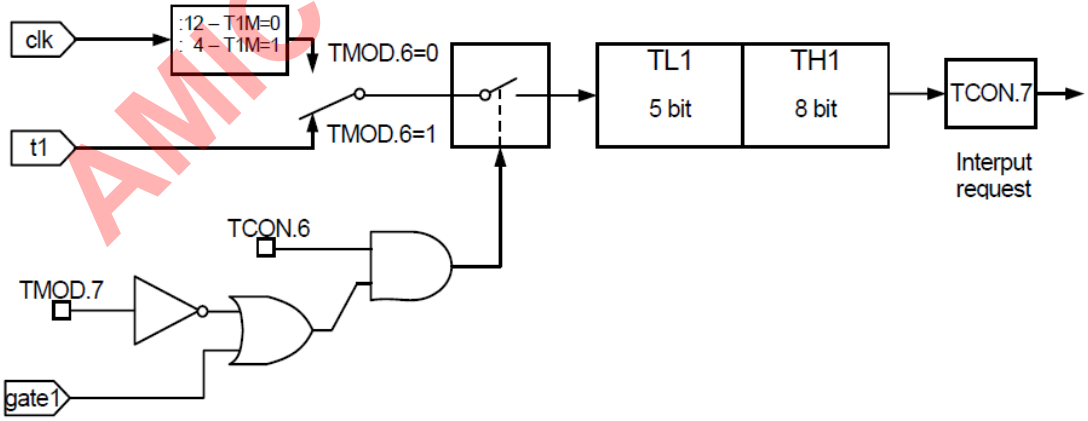


Figure12.5 Timer/Counter 1, Mode 0：13-Bit Timers/Counters

12.2.8 Timer 1 – Mode 1

Mode 1 is the same as Mode 0, except that timer register is running with all 16 bits. Mode 1 is shown in figure below.

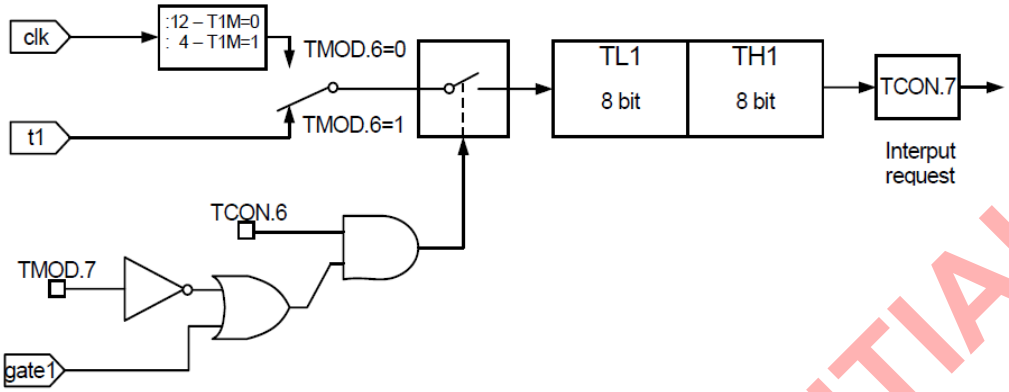


Figure12.6 Timer/Counter 1, Mode 0：16-Bit Timers/Counter

12.2.9 Timer 1 – Mode 2

Mode 2 configures the timer register as an 8-bit counter (TL1) with automatic reloads, as shown in figure below. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is loaded by software. The reload leaves TH1 unchanged.

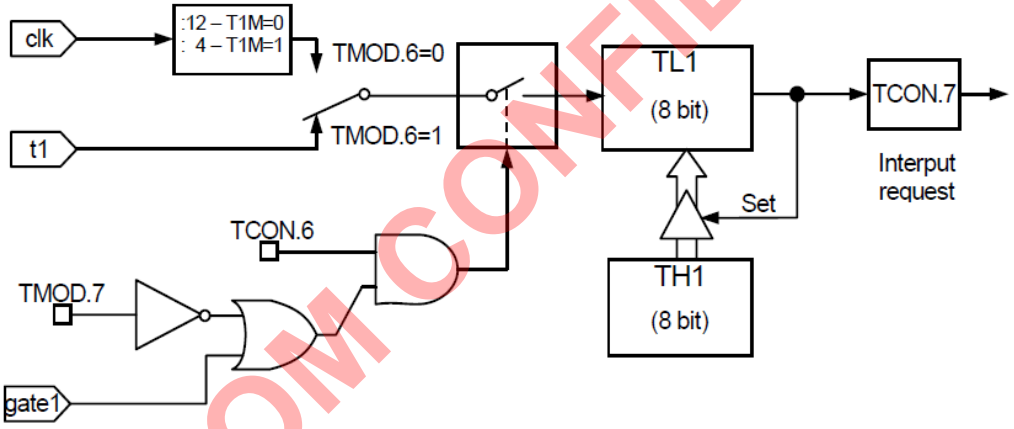


Figure12.7 Timer/Counter 1, Mode 2：8-Bit Timer/Counter with Auto-Reload

12.2.10 Timer 1 – Mode 3

Timer 1 in Mode 3 is held counting. The effect is the same as setting TR1=0.

12.3 Timer2 PINS DESCRIPTION

The Timer 2 pins functionality is described in the following table. All pins are one directional.

PIN	ACTIVE	TYPE	DESCRIPTION
t2(P1.0)	falling	INPUT	Timer 2 clock line
t2ex(P1.1)	high	INPUT	Timer 2 control

Table12.4 Compare/Capture pins description

12.4 Timer2 FUNCTIONALITY

12.4.1 OVERVIEW

Timer 2 is fully compatible with the standard 8052 Timer 2. It is up counter. Totally five SFRs control the Timer 2 operation: TH2/TL2(0xCD/0xCC) counter registers, RLDH/RLDL (0xCB/0xCA) capture registers and T2CON(0xC8) control register. Timer 2 works in the three modes selected by T2CON bits as shown in table below.

RCLK, TCLK	CPRL2	TR2	Function description
0	0	1	16-bit auto-reload mode. The Timer 2 overflow sets TF2 bit and the TH2,TL2 registers reloaded 16-bit value from RLDH, RLDL.
0	1	1	16-bit capture mode. The Timer 2 overflow sets TF2 bit. When the EXEN2 = 1, the TH2, TL2 register values are stored into RLDH, RLDL while falling edge is detected on T2EX pin.
1	X	1	Baud rate generator for the UART0 interface. It auto-reloads its counter with RLDH, RLDL values each overflows.
X	X	0	Timer 2 is off

Table12.5 Timer 2 modes

12.4.2 Timer 2 Registers

T2CON register (0xC8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C8h APOL Reset	R/W	TF2 0	EXF2 0	RCLK 0	TCLK 0	EXEN2 0	TR2 0	CT2 0	CPRL2 0

EXF2：Falling edge indicator on T2EX pin when EXEN = 1. Must be cleared by software.

RCLK：Receive clock enable

=1, UART0 receiver is clocked by Timer 2 overflow pulses

=0, UART0 receiver is clocked by Timer 2 overflow pulses

TCLK：Transmit clock enable

=1, UART0 transmitter is clocked by Timer 2 overflow pulses

=0, UART0 transmitter is clocked by Timer 2 overflow pulses

EXEN2：Enable T2EX pin functionality.

=1, Allows capture or reload as a result of T2EX pin falling edge.

=0, ignore T2EX events

TR2：Start / Stop Timer 2

=1, start

=0, stop

CT2：Timer / counter select

=1, external event counter. Clock source is T2 pin.

=0, timer 2 Internally clocked

CPRL2：Capture / Reload select

=1, T2EX pin falling edge causes capture to occur when EXEN2 = 1

=0, automatic reload occurs：on Timer 2 overflow or falling edge T2EX pin when EXEN2 = 1. When RCLK or TCLK is set this bit is ignored and automatic reload on Timer 2 overflow is forced.

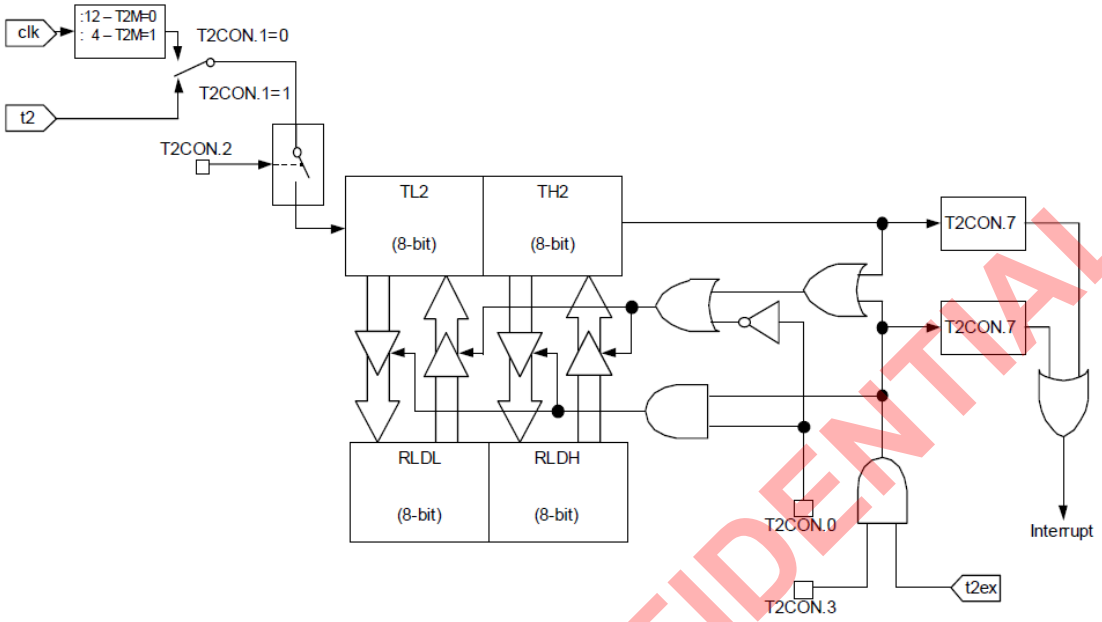


Figure12.9 Timer 2 block diagram in timer mode

CKCON register (0x8E)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8Eh CKCON	R/W	-	-	-	T1M	T0M	MD2	MD1	MD0
Reset		0	0	0	0	0	0	0	0

T2M：This bit controls the division of the system clock that drives Timer 2. This bit has no effect when the timer is in baud rate generator mode.

=1, Timer 2 uses a divide-by-4 of the system clock frequency.

=0, Timer 2 uses a divide-by-12 of the system clock frequency.

Timer 2 interrupt related bits are shown below. An interrupt can be turned on/off by IE (0xA8) register, and set into high/low priority group by IP register.

IE register (0xA8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A8h IE	R/W	EA	-	ET2	ES0	ET1	EX1	ET0	EX0
Reset		0	0	0	0	0	0	0	0

EA：Enable global interrupts.

ET2：Enable Timer 2 interrupts.

IP register (0xB8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B8h IP	R/W	-	-	PT2	PS0	PT1	PX1	PT0	PX0
Reset		0	0	0	0	0	0	0	0

PT2：Timer 2 priority level control (at 1-high level)

-：Unimplemented bit. Read as 0 or 1.

T2CON register (0xC8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C8h T2CON Reset	R/W	TF2 0	EXF2 0	RCLK 0	TCLK 0	EXEN2 0	TR2 0	CT2 0	CPRL2 0

TF2：Timer 2 interrupt (overflow) flag. Must be cleared by software.
The flag will not be set when either RCLK or TCLK is set.

All Timer 2 related bits generate interrupts can be set or cleared by software, with the same result as if they had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled by software.

Interrupt flag	Function	Active level / edge	Flag resets	Vector	Natural priority
TF2	Interrnal, Timer2	-	Software	0x2B	6

Table12.6 Timer 2 interrupt

Interrupt is also generated at falling edge of T2EX pin, while EXEN2 bit is set. This interrupt doesn't set TF2 flag, but EXF2 only and also uses 0x2B vector. Please see picture below. Timer2 internal logic configured as baud-rate generator is shwon below.

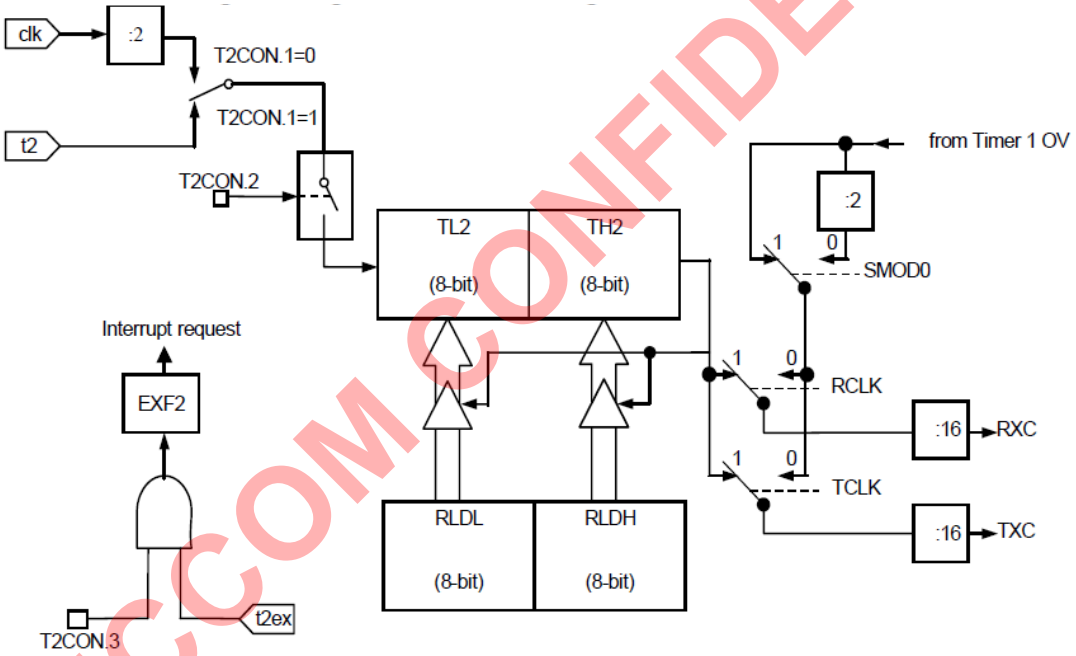


Figure12.9 Timer 2 block diagram as UART0 baud rate generator

Please note that SMOD0 bit is ignored by UART when clocked by Timer2. The RLCK/TCLK frequency is equal to：

$$xCLK = \frac{CLK}{2 \cdot (65536 - RLD)}$$

$$where\, xCLK = TCLK, RCLK$$

13. UART 0

UART0 is full duplex, meaning it can transmit and receive concurrently. It is receive double-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register, and reading SBUF0 reads a physically separate receive register. The serial port can operate in 4 modes: one synchronous and three asynchronous modes. Mode 2 and 3 has a special feature for multiprocessor communications. This feature is enabled by setting SM02 bit in SCON0 register. The master processor first sends out an address byte, which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM02 = 1, no slave will be interrupted by a data byte. An address byte will interrupt all slaves. The addressed slave will clear its SM02 bit and prepare to receive the data bytes that will be coming. The slaves that were not being addressed leave their SM02 set and ignoring the incoming data.

13.1 UART0 PINS DESCRIPTION

The UART0 pins functionality is described in the following table. All pins are one directional. There are no three-state output pins and internal signals.

PIN	ACTIVE	TYPE	DESCRIPTION
Rxd_0(P3.0)	-	Input / Output	Serial receiver I_0 / O_0
Txd_0(P3.1)	-	Output	Serial transmitter line 0

Table13.1 UART0 pins description

13.2 FUNCTIONALITY

The UART0 has the same functionality as a standard 8051 UART. The UART0 related registers are: SBUF0(0x99), SCON0(0x98), PCON(0x87), IE(0xA8) and IP(0xB8). The UART0 data buffer (SBUF0) consists of two separate registers: transmit and receive registers. A data writes into the SBUF0 sets this data in UART0 output register and starts a transmission. A data reads from SBUF0, reads data from the UART0 receive register.

SBUF0 register (0x99)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
99h SBUF0	R/W								
Reset		0	0	0	0	0	0	0	0

SB0[7:0]：UART0 buffer

SCON0 register (0x98)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
98h SCON0	R/W	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Reset		0	0	0	0	0	0	0	0

SM02：Enable a multiprocessor communication feature

SM0[1:0]：Sets baud rate

SM00	SM01	Mode	Description	Baud Rate
0	0	0	Shift register	$F_{CLK}/12$, $F_{CLK}/4$
0	1	1	8-bit UART	Variable(16bit)
1	0	2	9-bit UART	$F_{CLK}/32$ or $F_{CLK}/64$
1	1	3	9-bit UART	Variable(16bit)

Timer 2 cannot be used as baud rate generator when Compare Capture unit is present in the system. The UART0 baud rates are presented in the table below.

Mode	Baud Rate
Mode 0	FCLK/12
Mode 1, 3	Timer 1 overflow rate – $T1_{ov}$
	SMOD0 = 0 $T1_{ov}/32$
	SMOD0 = 1 $T1_{ov}/16$
	Timer 2 overflow rate – $T2_{ov}$
	SMOD0 = x $T2_{ov}/16$
Mode 2	SMOD0 = 0 $F_{CLK}/64$
	SMOD0 = 1 $F_{CLK}/32$

The SMOD0 bit is located in PCON register.

REN0：If set, enable serial reception. Cleared by software to disable reception.
TB08：The 9th transmitted data bit in Modes 2 and 3. Set or cleared by the CPU, depending on the function it performs (parity check, multiprocessor communication etc.)
RB08：In Modes 2 and 3 it is the 9th data bit received. In Mode 1, if SM02 is 0, RB08 is the stop bit. In Mode 0 this bit is not used.

PCON register (0x87)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
87h PCON	R/W	SMOD0	SMOD1	-	PWE	-	SWB	STOP	PMM
Reset		0	0	0	0	0	0	0	0

SMOD0：UART0 double baud rate bit when clocked by Timer 1 only.

- INTERRUPTS

UART0 interrupt related bits are shown below. An interrupt can be turned on / off by IE register, and set into high / low priority group by IP register.

IE register (0xA8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A8h IE	R/W	EA	-	ET2	ES0	ET1	EX1	ET0	EX0
Reset		0	0	0	0	0	0	0	0

ES0：RI0 & TI0 interrupt enable flag

IP register (0xB8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B8h IP	R/W	-	-	PT2	PS0	PT1	PX1	PT0	PX0
Reset		0	0	0	0	0	0	0	0

PS0：RI0 & TI0 interrupt priority flag

SCON0 register (0x98)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
98h SCON0	R/W	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Reset		0	0	0	0	0	0	0	0

TI0：Transmit interrupt flag, set by hardware after completion of a serial transfer.
Must be cleared by software.
RI0：Receive interrupt flag, set by hardware after completion of a serial reception.
Must be cleared by software.

All of bits that generate interrupts can be set or cleared by software, with the same result as if they had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled by software.

Interrupt flag	Function	Active level / edge	Flag resets	Vector	Natural priority
TI0 & RI0	Internal, UART0	-	Software	0x23	5

Table13.3 UART0 interrupt

13.3 OPERATING MODES

13.3.1 UART0 MODE 0, SYNCHRONOUS

Pin RXD0I serves as input and RXD0O as output. TXD0 output is a shift clock. The baud rate is fixed at 1/12 of the CLK clock frequency. Eight bits are transmitted with LSB first. Reception is initialized by setting the flags in SCON0 as follows: RI0=0 and REN0=1.

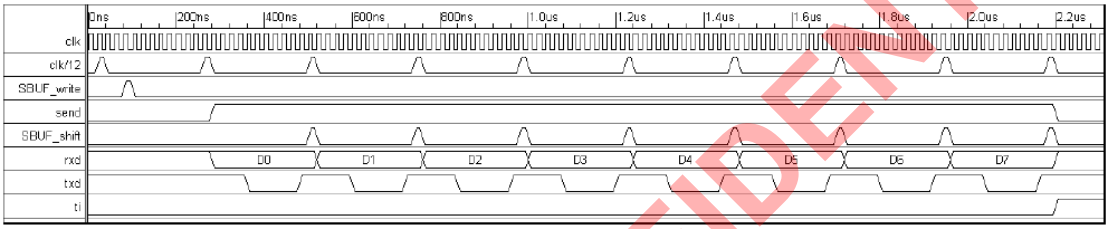


Figure13.3 UART0 transmission mode 0 timing diagram

13.3.2 UART0 MODE 1, 8-BIT UART, VARIABLE BAUD RATE, TIMER CLOCK SOURCE

Pin RXD0I serves as input, and TXD0 serves as serial output. 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading SBUF0, and stop bit sets the flag RB08 in the SFR SCON0. The baud rate is variable and depends from Timer 1 or Timer 2 mode. To enable Timer 2 clocking set the TCLK, RCLK bits located in T2CON (0xC8) register. SMOD0 bit is ignored when UART is clocked by Timer2.

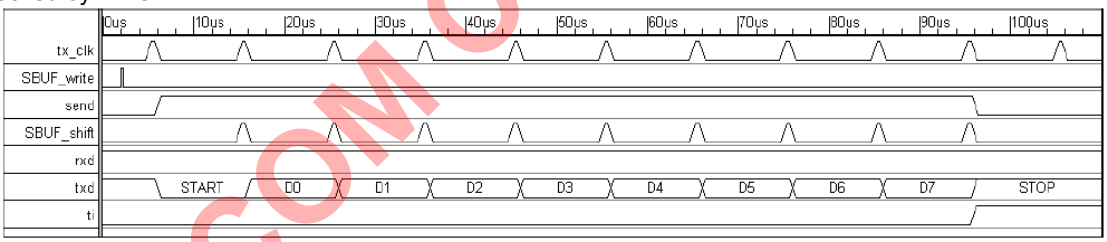


Figure13.4 UART0 transmission mode 1 timing diagram

13.3.3 UART0 MODE 2, 9-BIT UART, FIXED BAUD RATE

This mode is similar to Mode 1 with two differences. The baud rate is fixed at 1/32 or 1/64 of CLK clock frequency, and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the UART0 interface: at transmission, bit TB08 in SCON0 is output as the 9th bit, and at receive, the 9th bit affects RB08 in SCON0.

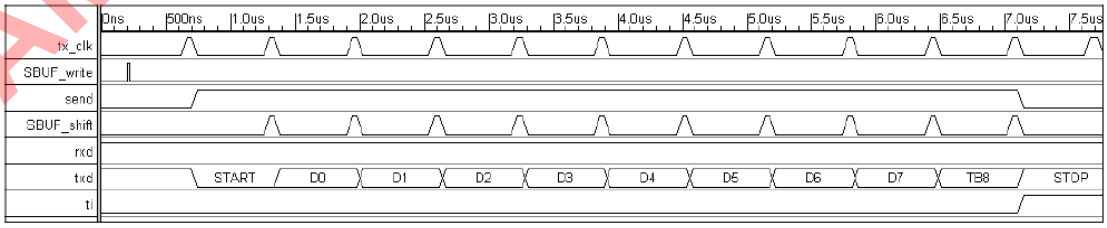


Figure13.5 UART0 transmission mode 2 timing diagram

13.3.4 UART0 MODE 3, 9-BIT UART, VARIABLE BAUD RATE, TIMER CLOCK SOURCE

The only difference between Mode 2 and Mode 3 is that the baud rate is a variable in Mode 3. When REN0=1 data receiving is enabled. The baud rate is variable and depends from Timer 1 or Timer 2 mode. To enable Timer 2 clocking set the TCLK, RCLK bits located in T2CON (0xC8) register. SMOD0 bit is ignored when UART is clocked by Timer2.

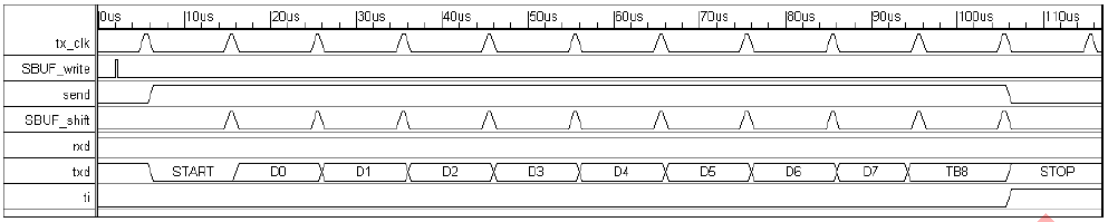


Figure13.6 UART0 transmission mode 3 timing diagram

A9129 supports different crystal frequency by programmable "Clock Register" (0Dh). Based on this, three important internal clocks F_{CGR} , F_{DR} and F_{SYCK} are generated.

(1) F_{XTAL}: Crystal frequency.
(2) F_{XREF}: Crystal Ref. Clock = F_{XTAL} * (DBL+1).
(3) F_{CGR}: Clock Generation Reference = 2MHz = F_{XREF} / (GRC+1), where F_{CGR} is used to generate 32M PLL.
(4) F_{MCLK}: Master Clock is either F_{XREF}: or 32M PLL, where F_{MCLK} is used to generate F_{SYCK}.
(5) F_{SYCK}: System Clock = 16MHz=F_{MCLK} / CSC= 32 * F_{IF}, where F_{IF} is recommended to set 500KHz.
(6) F_{DR}: Data Rate Clock = F_{IF} / (SDR+1).
(7) F_{FPD}: VCO Compared Clock = = F_{XREF} / (RRC+1).

13.4 Serial Baud rate for SBRG_EN

We support a maximum 4% inaccuracy baud rate if SBRG_EN is active. The correlative register is as below:

UART0_

SBRG0H	9EH	Serial Baud rate Generator 0, high byte
SBRG0L	9FH	Serial Baud rate Generator 0, low byte

SBRG0H: Address: 9Eh

7	6	5	4	3	2	1	0
SBRG_EN	BRG_M[10]	BRG_M[9]	BRG_M[8]	BRG_M[7]	BRG_M[6]	BRG_M[5]	BRG_M[4]

Used to configure the Baud rate of UART0 and it must be accessed together with SBRG0L.

SBRG0L: Address: 9Fh

7	6	5	4	3	2	1	0
BRG_M[3]	BRG_M[2]	BRG_M[1]	BRG_M[0]	BRG_F[3]	BRG_F[2]	BRG_F[1]	BRG_F[0]

Used to configure the Baud rate of UART0 and it must be accessed together with SBRG0H.

UART1_

SBRG1H	A6H	Serial Baud rate Generator 0, high byte
SBRG1L	A7H	Serial Baud rate Generator 0, low byte

SBRG1H: Address: A6H

7	6	5	4	3	2	1	0
SBRG_EN	BRG_M[10]	BRG_M[9]	BRG_M[8]	BRG_M[7]	BRG_M[6]	BRG_M[5]	BRG_M[4]

Used to configure the Baud rate of UART1 and it must be accessed together with SBRG1L.

SBRG1L: Address: A7H

7	6	5	4	3	2	1	0
BRG_M[3]	BRG_M[2]	BRG_M[1]	BRG_M[0]	BRG_F[3]	BRG_F[2]	BRG_F[1]	BRG_F[0]

Used to configure the Baud rate of UART1 and it must be accessed together with SBRG1H.

If SBRG_EN (SBRG0H.7) = 1

UART0 Baud rate = Fosc / (16 * (BRG_M[10:0]+1)+BRG_F[3:0])

Baud rate supporting table:

Crystal		12.8MHz		
Baud Rate	BRG_M	BRG_F	Actual	Error
600	1332	5	600	0.0%
1200	665	11	1200	0.0%
2400	332	5	2400	0.0%
4800	165	11	4799	0.0%
9600	82	5	9602	0.0%
14400	54	9	14398	0.0%
19200	40	11	19190	0.0%
38400	19	13	38438	0.1%
56000	13	5	55895	-0.2%
57600	12	14	57658	0.1%
115200	5	15	115315	0.1%
128000	5	4	128000	0.0%
230400	2	8	228571	-0.8%
256000	2	2	256000	0.0%
460800	0	12	457143	-0.8%

Crystal		16MHz		
Baud Rate	BRG_M	BRG_F	Actual	Error
600	1665	11	600	0.0%
1200	832	5	1200	0.0%
2400	415	11	2400	0.0%
4800	207	5	4800	0.0%
9600	103	3	9598	0.0%
14400	68	7	14401	0.0%
19200	51	1	19208	0.0%
38400	25	1	38369	-0.1%
56000	16	14	55944	-0.1%
57600	16	6	57554	-0.1%
115200	7	11	115108	-0.1%
128000	6	13	128000	0.0%
230400	3	5	231884	0.6%
256000	2	15	253968	-0.8%
460800	1	3	457143	-0.8%
921600	0	1	941176	2.1%

Crystal		19.2MHz		
Baud Rate	BRG_M	BRG_F	Actual	Error
600	1999	1	600	0.0%
1200	999	1	1200	0.0%
2400	499	1	2400	0.0%
4800	249	1	4800	0.0%
9600	124	1	9600	0.0%
14400	82	5	14404	0.0%
19200	61	8	19200	0.0%
38400	30	4	38400	0.0%
56000	20	7	55977	0.0%
57600	19	13	57658	0.1%
115200	9	7	114970	-0.2%
128000	8	6	128000	0.0%
230400	4	3	231325	0.4%
256000	3	11	256000	0.0%
460800	1	10	457143	-0.8%
921600	0	5	914286	-0.8%

Remark: Not setting BRG_F to 0.

14. IIC interface

A9129's I²C peripheral provides two-wire interface between the device and I²C -compatible device by the two-wire I²C serial bus. The I²C peripheral supports the following functions.

- Conforms to v2.1 of the I²C specification (published by Philips Semiconductor)
- Master transmitter / receiver
- Slave transmitter / receiver
- Flexible transmission speed modes: Standard (up to 100 Kb/s) and Fast (up to 400Kb/s)
- Multi-master systems supported
- Supports 7-bit addressing modes on the I²C bus
- Interrupt generation
- Allows operation from a wide range of input clock frequencies (build-in 8-bit timer)

PIN 23 and PIN 24 are I²C Interface in A9129. The alternate function is Port 0.5 and Port 0.6. User can set BBSEL (BBH) to set up the PIN function. Please refer the Chapter 11 for more detail information.

PIN	TYPE	DESCRIPTION
SCL(P0.5)	INPUT /OUTPUT	I²C clock input /output
SDA(P0.6)	INPUT/ OUTPUT	I²C data input /output

Table14.1 I2C interface pins description

14.1 Master mode I²C

The I²C master mode provides an interface between a microprocessor and an I²C bus. It can be programmed to operate with arbitration and clock synchronization to allow it to operate in multi-master systems. Master mode I²C supports transmission speeds up to 400Kb/s.

14.1.1 I²C REGISTERS

There are six registers used to interface to the host: the Control, Status, Slave Address, Transmitted Data, Received Data and Timer Period Register.

Register	Address
Slave address – I2CMSA	0xF4
Control – I2CMCR	0xF5
Transmitted data I2CBUF	0xF6
Timer period - I2CMTP	0xF7

Table14.2 I²C Registers for writing

Register	Address
Slave address – I2CMSA	0xF4
Status – I2CMSR	0xF5
Received data - I2CBUF	0xF6
Timer period - I2CMTP	0xF7

Table14.3 I²C Registers for reading

■ **I²C Master mode Timer Period Register**

To generate wide range of SCL frequencies the core have built-in 8-bit timer. Programming sequence must be done at least once after system reset. After reset, register have 0x01 value by default.

SCL_PERIOD = 2 x (1+TIMER_PRD) x (SCL_LP + 1) x CLK_PRD
For example： - CLK_PRD = 33,33ns (CLK_FRQ = 30MHz)； - TIMER_PRD = 3； - SCL_LP = 6；
SCL_PERIOD = 2 x (1 + 3) x (6 + 1) x 33,33ns = 3200ns = 2,666us
SCL_FREQUENCY = 1 / 2,666us = 375 KHz
SCL_PRD - SCL line period (I2C clock line)

TIMER PRD	**-Timer period register value (range 1 to 255)**
SCL_LP	**- SCL_LOW_PERIOD constant value (range 2 to 15)**
CLK_PRD	**- System clock period (1/f_{clk})**

I2CMTP (0xE7)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E7h I2CMTP	R/W	0	P.6	P.5	P.4	P.3	P.2	P.1	P.0
Reset		0	0	0	0	0	0	0	1

■ I²C CONTROL AND STATUS REGISTERS

The Control Register consists of eight bits: the RUN, START, STOP, ACK, HS, ADDR, SLRST and RSTB bit.

The RSTB bit performs reset of whole I²C controller and behaves identically as external reset provided by RST pin. Using this bit software application can reinitialize I²C mater module when some problem is encountered on I²C bus. In case when I²C Slave device blocks I²C bus, then SLRST bit should be set along with RUN bit (just after issuing the RSTB). SLRST bit causes that I²C master module generates 9 SCK clocks (no START is generated) to recover Slave device to known state and issues at the end STOP. This bit is automatically cleared by I²C MASTER MODULE, thus, it is always read as '0'. The BUSY bit should be checked to know when this transmission is ended.

The START bit will cause the generation of the START, or REPEATED START condition. The STOP bit determines if the cycle will stop at the end of the data cycle, or continue on to a burst. To generate a single send cycle, the Slave Address register is written with the desired address, the R/S bit is set to '0', and Control Register is written with HS=0, ACK=x, STOP=1, START=1, RUN=1 (binary xxx0x111 x-mean 0 or 1) to perform the operation and stop. When the operation is completed (or aborted due an error), the interrupt is generated. The data may be read from Received Data Register. When I²C MASTER MODULE core operates in Master receiver mode the ACK bit must be set normally to logic 1. This cause the I²C MASTER MODULE bus controller to send acknowledge automatically after each byte. This bit must be reset when the I²C MASTER MODULE bus controller requires no further data to be sent from slave transmitter.

The ADDR bit along with RUN bit cause the generation of the START condition and transmission of Slave Address. Next STOP can end transmission, or REPEATED START generates the START and ADDRRESS sequence once again. In both cases STOP can ends transmission. See I²C MASTER MODULE ACK Polling chapter for details.

I2CMCR (0xF5)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F5h I2CMCR	R/W	RSTB	SLRST	ADDR	HS	ACK	STOP	START	RUN
Reset		0	0	0	0	0	0	0	0

RSTB	SLRST	ADDR	HS	R/S	ACK	STOP	START	RUN	OPERATION
0	0	0	0	0	-	0	1	1	START condition followed by SEND (Master remains in Transmitter mode)
0	0	0	0	0	-	1	1	1	START condition followed by SEND and STOP condition
0	0	0	0	1	0	0	1	1	START condition followed by RECEIVE operation with **negative Acknowledge** (Master remains in Receiver mode)
0	0	0	0	1	0	1	1	1	START condition followed by RECEIVE and STOP condition
0	0	0	0	1	1	0	1	1	START condition followed by RECEIVE (Master remains in Receiver mode)
0	0	0	0	1	1	1	1	1	**forbidden sequence**
0	0	0	1	0	0	0	0	1	Master Code sending and switching to High-speed mode
1	0	0	-	-	-	-	-	-	I2CM module software reset
0	1	0	0	0	0	0	0	1	Reset slaves connected to I2C bus by generating 9 SCK clocks followed by STOP
0	0	1	0	0	0	0	0	1	START condition followed by Slave Address

Table14.4 Control bits combinations permitted in IDLE state *

RSTB	SLRST	ADDR	HS	R/S	ACK	STOP	START	RUN	OPERATION
0	0	0	0	-	-	0	0	1	SEND operation (Master remains in Transmitter mode)
0	0	0	0	-	-	1	0	0	STOP condition
0	0	0	0	-	-	1	0	1	SEND followed by STOP condition
0	0	0	0	0	-	0	1	1	Repeated START condition followed by SEND (Master remains in Transmitter mode)
0	0	0	0	0	-	1	1	1	Repeated START condition followed by SEND and STOP condition
0	0	0	0	1	0	0	1	1	Repeated START condition followed by RECEIVE operation with **negative Acknowledge** (Master remains in Receiver mode)
0	0	0	0	1	0	1	1	1	Repeated START condition followed by SEND and STOP condition
0	0	0	0	1	1	0	1	1	Repeated START condition followed by RECEIVE (Master remains in Receiver mode)
0	0	0	0	1	1	1	1	1	**forbidden sequence**
1	0	0	-	-	-	-	-	-	I2CM module software reset
0	0	1	0	0	-	0	1	1	Repeated START condition followed by Slave Address

Table14.5 Control bits combinations permitted in Master Transmitter mode

RSTB	SLRST	ADDR	HS	R/S	ACK	STOP	START	RUN	OPERATION
0	0	0	0	-	0	0	0	1	RECEIVE operation with **negative Acknowledge** (Master remains in Receiver mode)
0	0	0	0	-	-	1	0	0	STOP condition**
0	0	0	0	-	0	1	0	1	RECEIVE followed by STOP condition
0	0	0	0	-	1	0	0	1	RECEIVE operation (Master remains in Receiver mode)
0	0	0	0	-	1	1	0	1	**forbidden sequence**
0	0	0	0	1	0	0	1	1	Repeated START condition followed by RECEIVE operation with **negative Acknowledge** (Master remains in Receiver mode)
0	0	0	0	1	0	1	1	1	Repeated START condition followed by RECEIVE and STOP condition
0	0	0	0	1	1	0	1	1	Repeated START condition followed by RECEIVE (Master remains in Receiver mode)
0	0	0	0	0	-	0	1	1	Repeated START condition followed by SEND (Master remains in Transmitter mode)
0	0	0	0	0	-	1	1	1	Repeated START condition followed by SEND and STOP condition
1	0	0	-	-	-	-	-	-	I2CM module software reset

Table14.6 Control bits combinations permitted in Master Receiver mode

The status Register is consisted of six bits : the BUSY bit, the ERROR bit, the ADDR_ACK bit, the DATA_ACK bit, the ARB_LOST bit, and the IDLE bit.

I2CMSR (0xF5)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F5h I2CMSR	R/W	-	BUS_ BUSY	IDLE	ARB_ LOST	DATA_ ACK	ADDR_ ACK	ERROR	BUSY
Reset	0x20	0	0	1	0	0	0	0	0

IDLE：This bit indicates that I²C BUS controller is in the IDLE state。
BUSY：This bit indicates that I²C BUS controller receiving, or transmitting data on the bus, and other bits of Status register are no valid;
BUS_BUSY：This bit indicates that the Bus is Busy, and access is not possible. This bit is set / reset by START and STOP conditions;
ERROR：This bit indicates that due the last operation an error occurred: slave address wasn't acknowledged, transmitted data wasn't acknowledged, or I²C Bus controller lost the arbitration;
ADDR_ACK：This bit indicates that due the last operation slave address wasn't acknowledged;
ARB_LOST：This bit indicates that due the last operation I²C Bus controller lost the arbitration;

■ **SLAVE ADDRESS REGISTER**

The Slave address Register consists of eight bits：Seven address bits (A6-A0), and Receive/ not send bit R/S. The R/S bit determines if the next operation will be a Receive (high), or Send (low).

I2CMSA (0xF4)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F4h I2CMCA	R/W	A.6	A.5	A.4	A.3	A.2	A.1	A.0	R/S
Reset		0	0	0	0	0	0	0	0

■ **I²C Buffer – RECEIVER AND TRANSMITTER REGISTERS**

I²C module has two separated 1 byte buffer in receiver and transmitter and these are located in the same address (0xF6). The Transmitted Data Register consists of eight data bits which will be sent on the bus due the next Send, or Burst Send operation. The first send bit is D.7 (MSB).

I2CBUF (0xF6)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F6h I2CBUF	R/W	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.P
Reset		0	0	0	0	0	0	0	0

The Receiver Data Register consists of eight data bits which have been received on the bus due the last receive, or Burst Receive operation.
I2CBUF (0xF6)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F6h I2CBUF	R/W	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.P
Reset		0	0	0	0	0	0	0	0

14.1.2 I²C MASTER MODULE AVAILABLE SPEED MODES

Default transmission parameter/constant values are shown in sections below. SCL clock frequency can be changed by modification of timer period values as show in the table below.

■ I²C **MASTER MODULE STANDARD MODE**

Typical configuration values for Standard speed mode：

The following table gives an example parameters for standard I²C speed mode.

System clock	TIMER_PERIOD	Transmission speed
4 MHz	1 (01h)	100kb/s
6 MHz	2 (02h)	100kb/s
10 MHz	4 (04h)	100kb/s
16 MHz	7 (07h)	100kb/s
20 MHz	9 (09h)	100kb/s

Table14.7 I2C MASTER MODULE Timer period values for standard speed mode

■ I²C **MASTER MODULE FAST MODE**

Typical configuration values for Fast speed mode：

The following table gives example parameters for Fast I²C speed mode.

System clock	TIMER_PERIOD	Transmission speed
10 MHz	1 (01h)	250 Kb/s
16 MHz	1 (01h)	400 Kb/s
20 MHz	2 (02h)	333 Kb/s

Table14.8 I²C MASTER MODULE Timer period values for Fast speed mode

14.1.3 I²C MASTER MODULE AVAILABLE COMMAND SEQUENCES

■ I²C **MASTER MODULE SINGLE SEND**

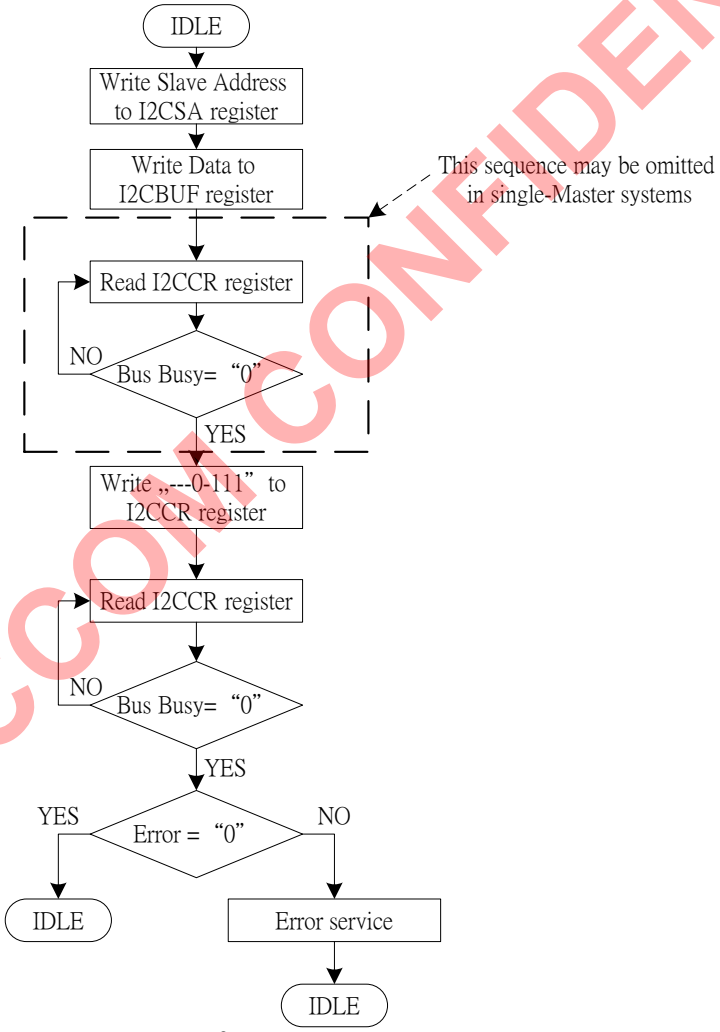


Figure14.1 I²C MASTER MODULE Single SEND flowchart

■ I²C MASTER MODULE SINGLE RECEIVE

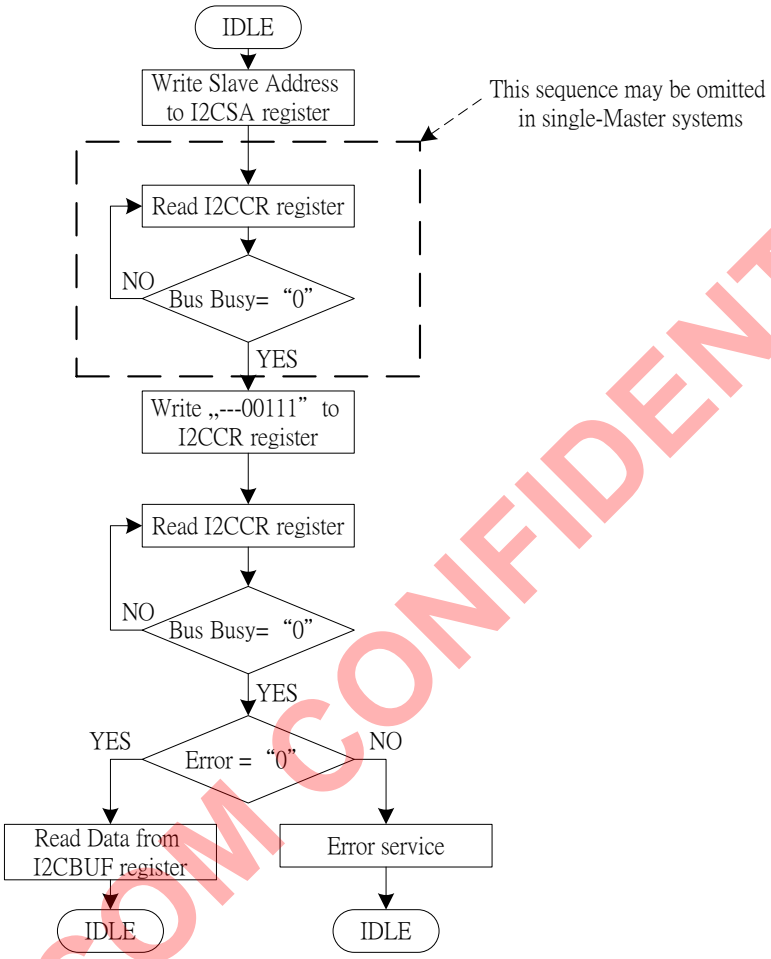


Figure14.2 Single RECEIVE flowchart

■ I²C MASTER MODULE BURST SEND

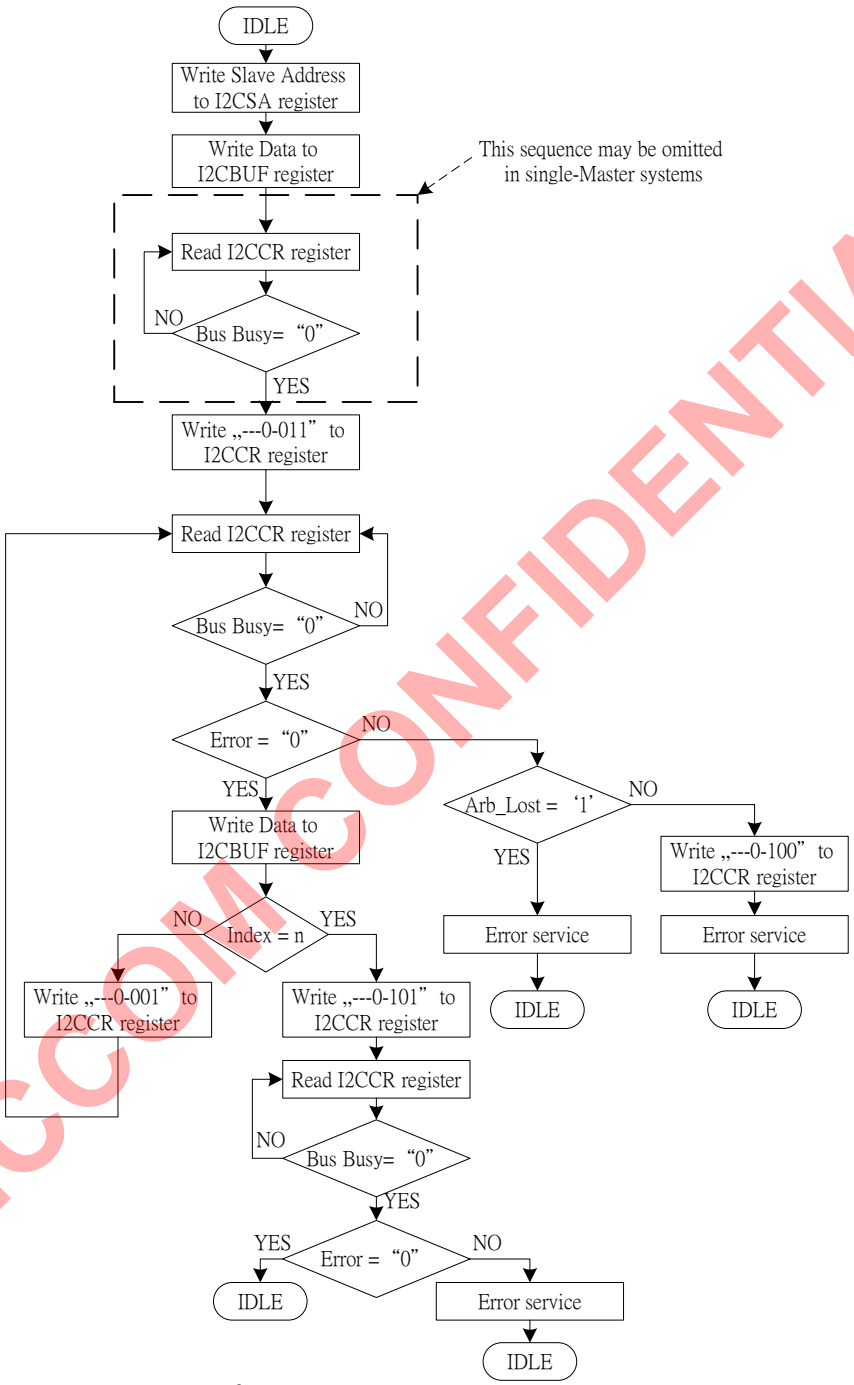


Figure14.3 I²C MASTER MODULE Sending n bytes flowchart

■ I²C **MASTER MODULE BURST RECEIVE**

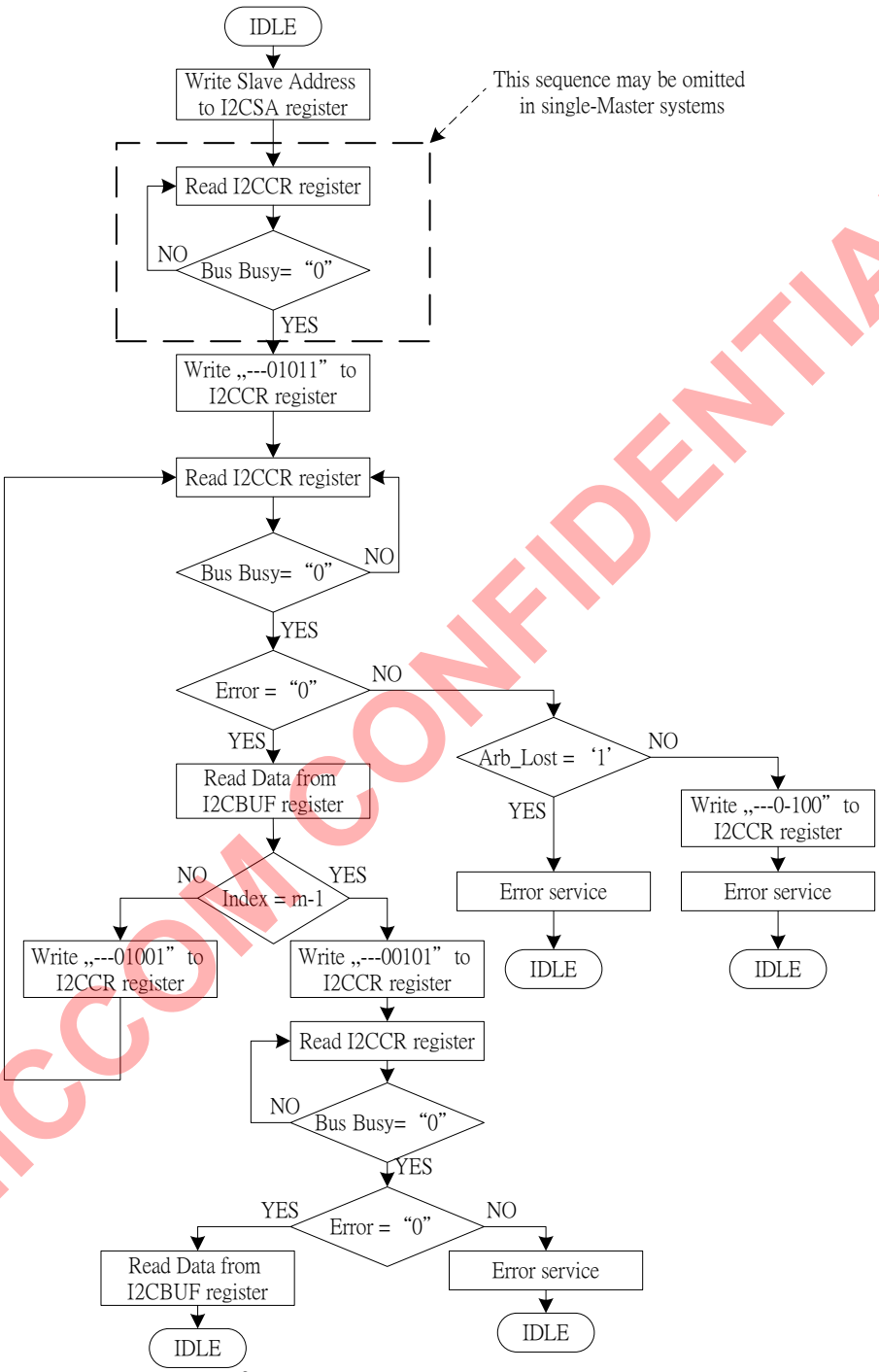


Figure14.4 I²C MASTER MODULE Receiving m bytes flowchart

■ I²C **MASTER MODULE BURST RECEIVE AFTER BURST SEND**

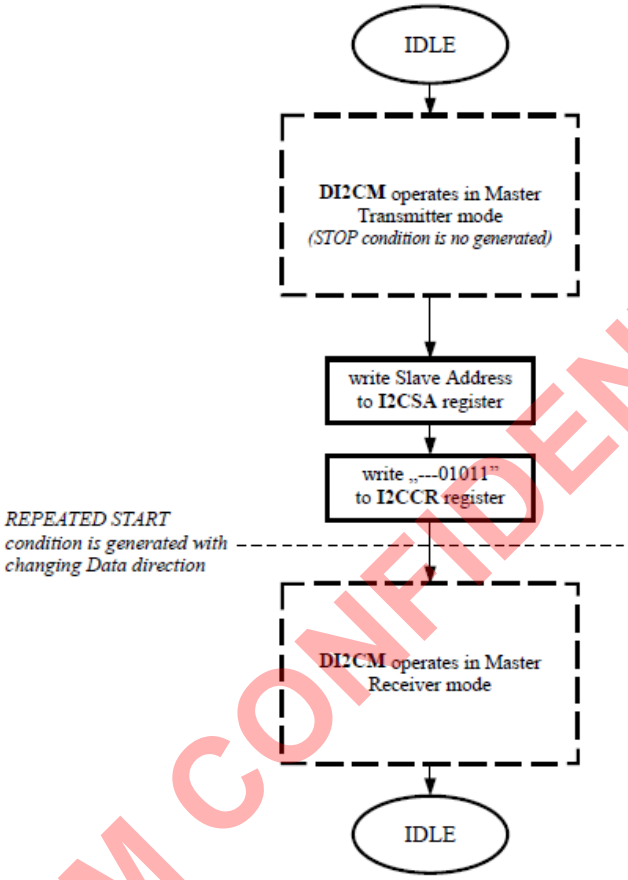


Figure14.5 I²C MASTER MODULE Sending n bytes then Repeated Start and Receiving m bytes flowchart

■ I²C **MASTER MODULE BURST SEND AFTER BURST RECEIVE**

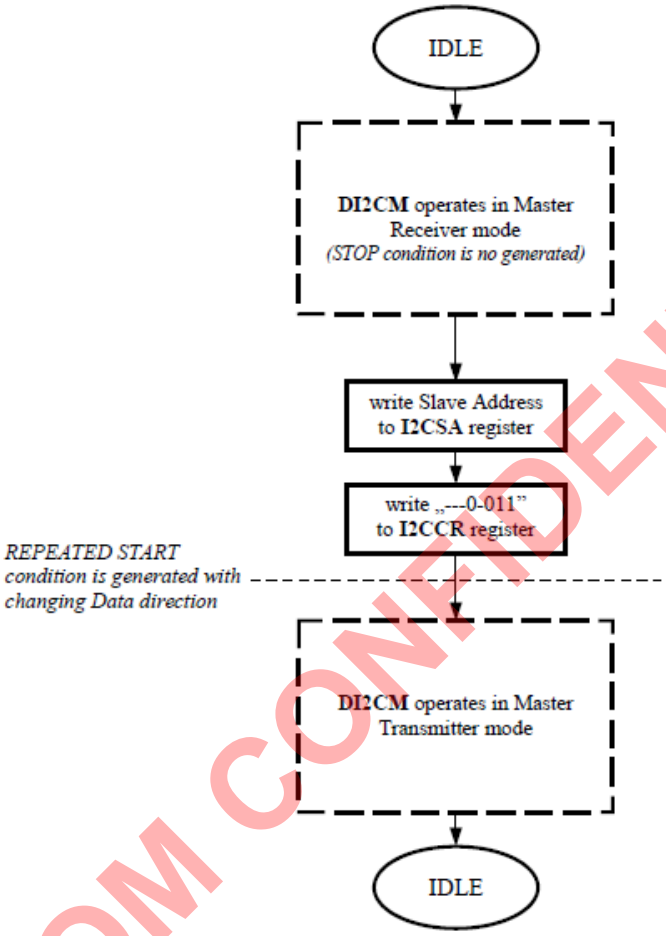


Figure14.6 I²C MASTER MODULE Receiving m bytes then Repeated Start and Sending n bytes flowchart

■ I²C **MASTER MODULE ACK POLLING**

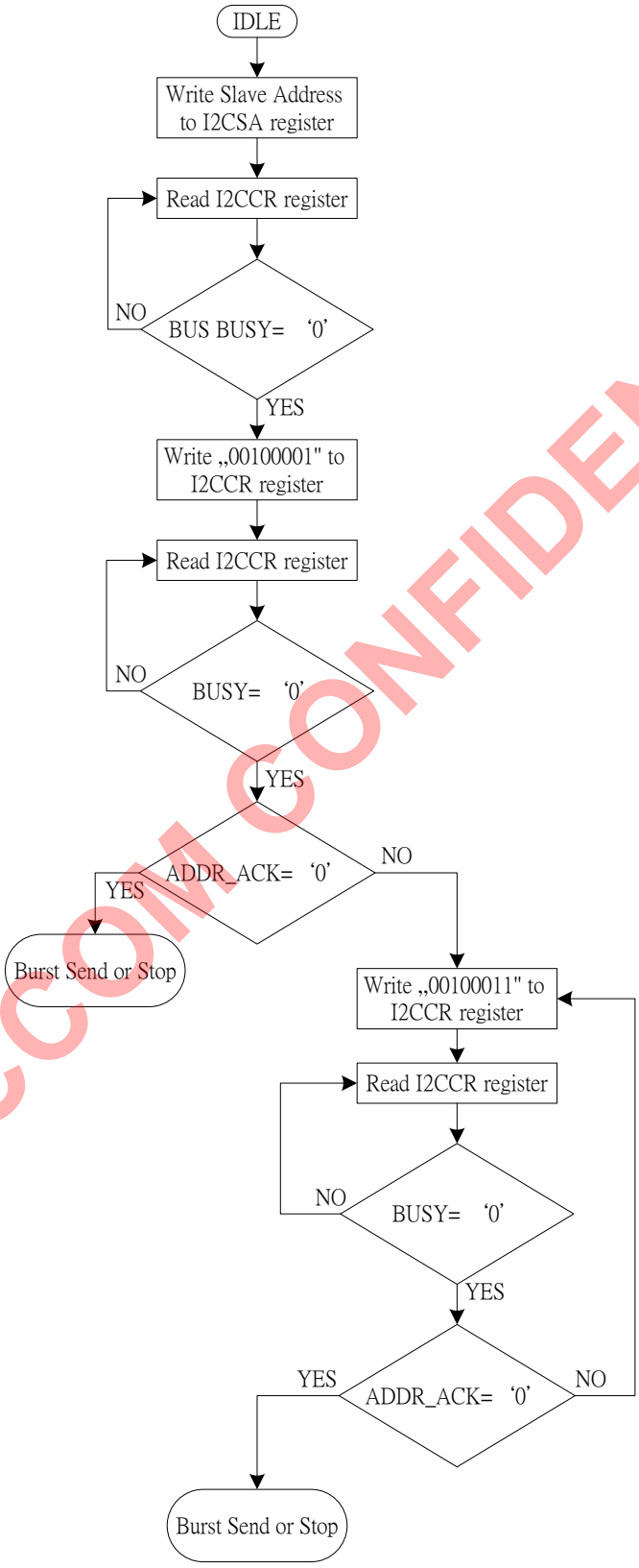


Figure14.7 I2C MASTER MODULE ACK Polling flowchart

14.3 I²C MASTER MODULE INTERRUPT GENERATION

I²C MASTER MODULE interrupt flag is automatically asserted when I²C transfer (send or receive a byte) is completed or transfer error has occurred. I2CMIF flag has to be cleared by software.

Interrupt flag	Function	Active level/edge	Flag resets	Vector	Natural priority
I2CMIF	Internal, I2C MASTER MODULE	-	Software	0x6B	14

Table14.9 I2C MASTER MODULE interrupt summary

I²C MASTER MODULE related interrupt bits have been summarized below. The IE (0xA8) contains global interrupt system disable (0) / enable (1) bit called EA.

EIE (0xE8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E8h EIE Reset	R/W	EI2CS ESPI 0	EI2CM 0	EWDI 0	EINT6 0	EINT5 0	EINT4 0	EINT3 0	EINT2 0

EI2CM：Enable I²C MASTER MODULE interrupts

EIP (0xF8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F8h EIP Reset	R/W	PI2CS PSPI 0	PI2CM 0	PWDI 0	PINT6 0	PINT5 0	PINT4 0	PINT3 0	PINT2 0

PI2CM：I²C MASTER MODULE priority level control (at 1-high-level)

EIF (0x91)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
91h EIF Reset	R/W	I2CSF SPIF 0	I2CMF 0	- 0	INT6F 0	INT5F 0	- 0	- 0	INT2F 0

I2CMIF：I²C MASTER MODULE interrupt flag

Must be cleared by software writing logic '1'. Writing '0' does not change its content.

14.4 Slave mode I²C

The I²C module provides an interface between a microprocessor and I²C bus. It can works as a slave receiver or transmitter depending on working mode determined by microprocessor/microcontroller. The core incorporates all features required by I²C specification. The I²C module supports all the transmission modes: Standard and Fast.

14.4.1 I2C MODULE INTERNAL REGISTERS

There are five registers used to interface to the target device：The Own Address, Control, Status, Transmitted Data and Received Data registers.

Register	Address
Own address – I2CSOA	0xF1
Control – I2CSCR	0xF2
Transmitted data – I2CSBUF	0xF3

Table14.10 I2C MODULE Registers for writing

Register	Address
Own address – I2CSOA	0xF1
Control – I2CSSR	0xF2
Received data – I2CSBUF	0xF3

Table14.11 I2C MODULE Registers for reading

■ **I2CSOA – OWN ADDRESS REGISTER**

The Own Address Register consists of seven address bits which identify I²C module core on I²C Bus. This register can be read and written at the address 0xF1.

I2CSOA (0xF1)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F1h I2CSOA	R/W	-	A.6	A.5	A.4	A.3	A.2	A.1	A0
Reset		0	0	0	0	0	0	0	0

■ **I2CSCR – CONTROL AND STATUS REGISTERS**

The Control Register consists of the bits：The RSTB and DA bit. The RSTB bit performs reset of whole I²C controller and behaves identically as external reset provided by RST pin. Using this bit software application can reinitialize I²C module when some problem is encountered on I²C bus. The DA bit enables (‘1’) and disable (‘0’) the I²C module device operation. DA is set immediately to ‘1’ when CPU write DA=1. This register can be only written at address 0xF2. Reading this address puts status register on data bus – see below.

I2CSCR (0xF2)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F2h I2CSCR	R/W	RSTB	DA	-	-	RECFINCLR	SENDFINCLR	-	-
Reset		0	0	0	0	0	0	0	0

DA：Device Active – enable or disable the I²C module device operation;
RSTB：Reset of whole I²C controller by writing ‘1’ to this bit. It behaves identically as RST pin
RECFINCLR：Writing ‘1’ to this bit clears RECFIN bit from the I²C MODULE status register.
SENDFINCLR：Writing ‘1’ to this bit clears SENDFIN bit from the I2C MODULE status register.

The Status Register consists of five bits: the DA, BUSACTIVE, RECFIN, SENDFIN bit, RREQ bit, TREQ bit. The receive finished RECFIN bit indicates that Master I²C controller has finished transmitting of data during single or burst receive operations. It also causes generation of interrupt on IRQ pin. The send finished SENDFIN bit indicates that Master I²C controller has finished receiving of data during single or burst send operations. It also causes generation of interrupt on IRQ pin. The Receive Request RREQ bit indicates that I²C module device has received data byte from I²C master. I²C module host device (usually CPU) should read one data byte from the Received Data register I2CSBUF. The Transmit Request TREQ bit indicates that I²C MODULE device is addressed as Slave Transmitter and I²C module host device (usually CPU) should write one data byte into the Transmitted Data register I2CSBUF. The BUSACTIVE ‘1’ signalizes that any transmission (send, receive or own address detection) is in progress. BUSACTIVE is cleared (‘0’) automatically by I²C module in case when there is no any transmission. This is read only bit.

The DA bit should be polled (read) when CPU wrote DA=0. The DA bit is not immediately cleared when any I²C transmission (send, receive or own address detection) is in progress. When current transmission has completed then this bit is cleared to ‘0’ and I²C module become inactive.

I2CSSR (0xF2)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F2h I2CSSR	R/W		DA	-	BUSACTIVE	RECFIN	SENDFIN	TREQ	RREQ
Reset		0	0	0	0	0	0	0	0

DA：Device Active – enable (‘1’) or disable (‘0’) the I²C MODULE device operation;
BUSACTIVE：Bus ACTIVE – ‘1’ signalizes that any transmission: send, receive or own address detection is in progress;

RREQ：Indicates that I²C module device has received data byte from I²C master;
It is automatically cleared by read of I2CSBUF.
TREQ：Indicates that I²C module device is addressed as transmitter and requires data byte from host device;
It is automatically cleared by write data I2CSBUF.
RECFIN：Indicates that Master I²C controller has ended transmit operation. It means that no more RREQ will be set during this single or burst I²C module receive operation. It is cleared by writing '1' to the RECFINCLR bit in the I²C module control register.
SENDFIN：Indicates that Master I²C controller has ended receive operation. It means that no more TREQ will be set during this single or burst I²C module send operation. It is cleared by writing '1' to the SENDFINCLR bit in the I²C control register.
NOTE：All bits are active at HIGH level ('1').

■ **I2CSBUF – RECEIVER AND TRANSMITTER REGISTERS**

The Transmitter Data Register consists of eight Data bits which will be sent on the bus due the next Send operation. The first send bit is the D.7(MSB).
I2CSBUF (0xF3)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F3h I2CSBUF	R/W	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.0
Reset		0	0	0	0	0	0	0	0

The Receiver Data Register consists of eight data bits which have been received on the bus due the last Receive operation.
I2CSBUF (0xF3)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F3h I2CSBUF	R/W	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.0
Reset		0	0	0	0	0	0	0	0

14.5 AVAILABLE I²C MODULE TRANSMISSION MODES

This chapter describes all available transmission modes of the I²C module core. Default I²C own address for all presented waveforms is 0x39 ("0111001").

14.5.1 I²C module SINGLE RECEIVE

The figure below shows a set of sequences during Single data Receive by I²C MODULE. Single receive sequences：

- ✧ Start condition
- ✧ I²C module is addressed by I²C Master as receiver
- ✧ Address is acknowledged by I²C module
- ✧ Data is received by I²C module
- ✧ Data is acknowledged by I²C module
- ✧ Stop condition

14.5.2 I²C module SINGLE SEND

The figure below shows a set of sequences during Single data Send by I²C MODULE. Single send sequences：

- ✧ Start condition
- ✧ I²C module is addressed by I²C Master as transmitter
- ✧ Address is acknowledged by I²C module
- ✧ Data is transmitted by I²C module
- ✧ Data is not acknowledged by I²C Master
- ✧ Stop condition

14.5.3 I²C module BURST RECEIVE

The figure below shows a set of sequences during Burst data Receive by I²C module. Burst receive sequences：

- ✧ Start condition
- ✧ I²C module is addressed by I²C Master as receiver
- ✧ Address is acknowledged by I²C module
- ✧ (1)Data is received by I²C module

- ✧ (2)Data is acknowledged by I²C module
- ✧ STOP condition

Sequences (1) and (2) are repeated until Stop condition occurs.

14.5.4 I²C module BURST SEND

The figure below shows a set of sequences during Burst Data Send by I²C module. Burst send sequences：

- ✧ Start condition
- ✧ I²C module is addressed by I²C Master as transmitter
- ✧ Address is acknowledged by I²C module
- ✧ (1)Data is transmitted by I²C module
- ✧ (2)Data is acknowledged by I²C Master
- ✧ (3)Last data is not acknowledged by I²C Master
- ✧ Stop condition

Sequences (1) and (2) are repeated until last transmitted data is not acknowledged (3) by I²C Master.

14.5.5 AVAILABLE I²C module COMMAND SEQUENCES FLOWCHART

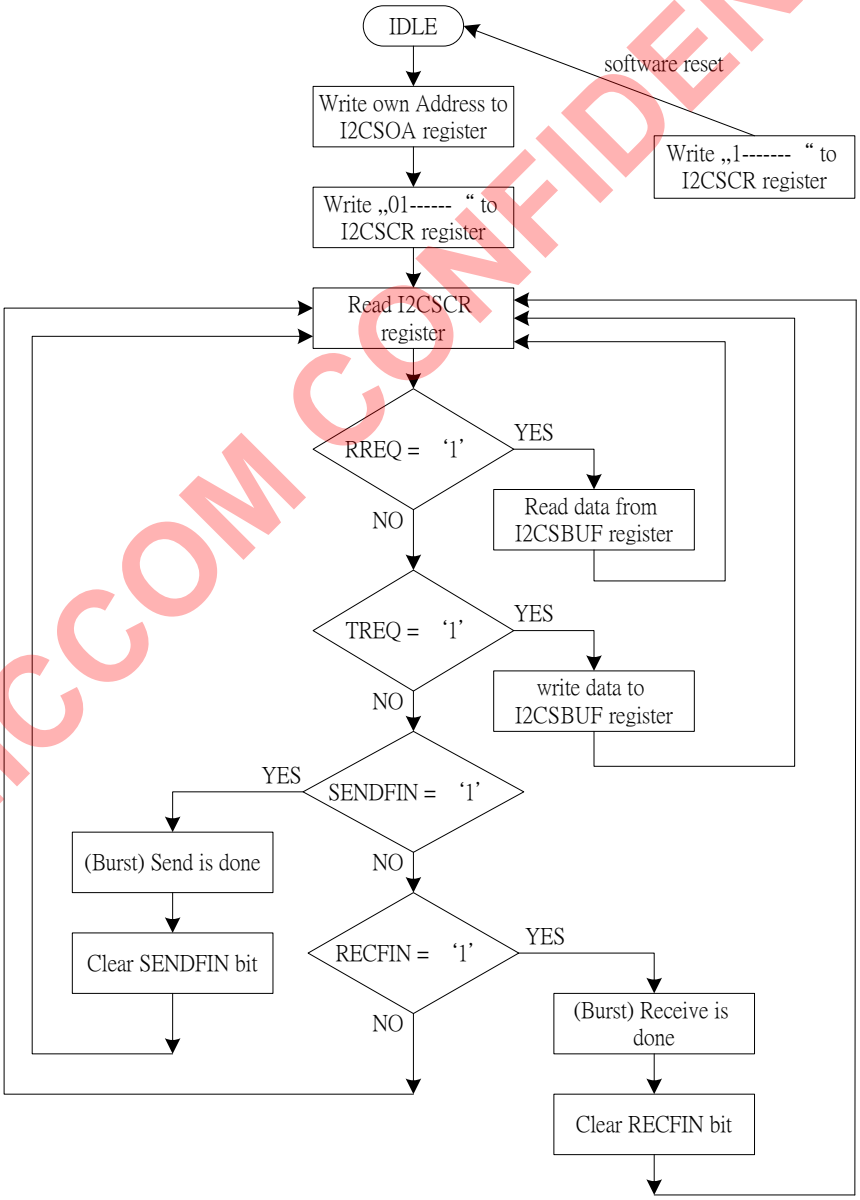


Figure14.8 Available I2C MODULE command sequences flowchart

14.6 I²C MODULE INTERRUPT GENERATION

I²C MODULE interrupt flag is automatically asserted when I²C transfer (send or receive a byte) is completed or transfer error has occurred. I2CSIF flag has to be cleared by software.

Interrupt flag	Function	Active level/edge	Flag resets	Vector	Natural priority
I2CSIF	Internal, DI2CS	-	Software	0x73	15

Table14.12 I2C MODULE interrupt summary

I²C MODULE related interrupt bits have been summarized below. The IE (0xA8) contains global interrupt system disable (0) / enable (1) bit called EA.

EIE (0xE8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E8h EIE	R/W	EI2CS ESPI	EI2CM	EWDI	EINT6	EINT5	EINT4	EINT3	EINT2
Reset		0	0	0	0	0	0	0	0

EI2CS：Enable I²C MODULE interrupts

EIP (0xF8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F8h EIP	R/W	PI2CS PSPI	PI2CM	PWDI	PINT6	PINT5	PINT4	PINT3	PINT2
Reset		0	0	0	0	0	0	0	0

PI2CS：I²C MODULE priority level control (at 1-high-level)

EIF (0x91)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
91h EIF	R/W	I2CSF SPIF	I2CMF	-	INT6F	INT5F	-	-	INT2F
Reset		0	0	0	0	0	0	0	0

I2CSIF：I²C MODULE interrupt flag

Software should determine the source of interrupt by check both modules' interrupt related bits. Must be cleared by software writing 0x80. It cannot be set by software.

-：Unimplemented bit. Read as 0 or 1.

15. SPI interface

The SPI is a fully configurable SPI master/slave device, which allows user to configure polarity and phase of serial clock signal SCK.

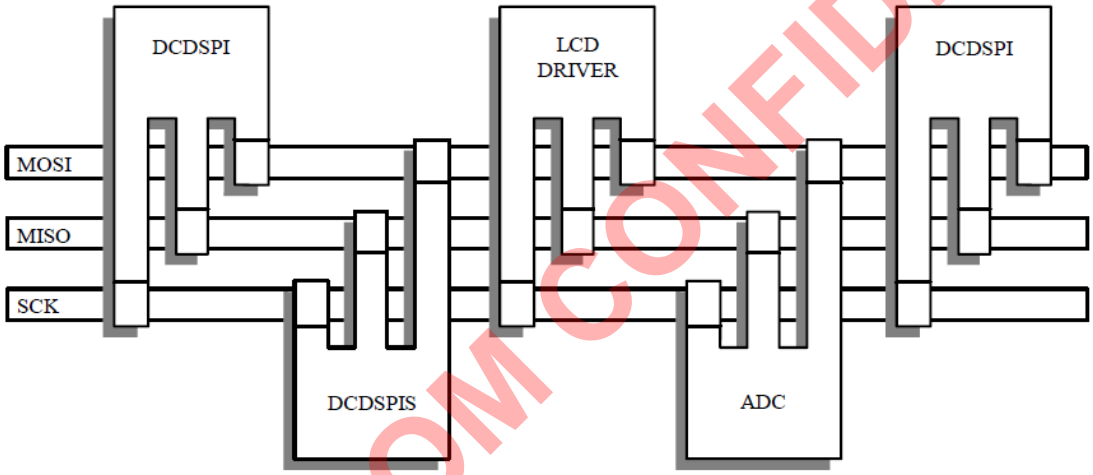
The SPI allows the microcontroller to communicate with serial peripheral devices. It is also capable of inter-processor communications in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information on the two independent serial data lines. SPI data are simultaneously transmitted and received.

The SPI is a technology independent design that can be implemented in a variety of process technologies.

The SPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. The system can be configured as a master or a slave device. Data rates as high as System clock divided by four (CLK/4). Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, software selects one of four different bit rates for the serial clock.

The SPI automatically drive selected by SSCR (Slave Select Control Register) slave select outputs (SS7O – SS0O), and address SPI slave device to exchange serially shifted data.

Error-detection logic is included to support inter-processor communications. A write-collision detector indicates when an attempt is made to write data to the serial shift register while a transfer is in progress. A multiple-master mode-fault detector automatically disables SPI output drivers if more than one SPI devices simultaneously attempts to be become bus master.



15.1 KEY FEATURES

All features listed below are included in the current version of SPI core.

- SPI Master
  - Full duplex synchronous serial data transfer
  - Master operation
  - Multi-master system supported
  - Up to 8 SPI slaves can be addressed
  - System error detection
  - Interrupt generation
  - Supports speeds up to 1/4 up to system clock
  - Bit rates generated 1/4, 1/8, 1/32, 1/64, 1/128, 1/512 of system clock
  - Four transfer formats supported
  - Simple interface allows easy connection to microcontrollers
- SPI Slave
  - Full duplex synchronous serial data transfer
  - Slave operation
  - System error detection
  - Interrupt generation
  - Supports speeds up to 1/4 of system clock

- Simple interface allows easy connection to microcontrollers
- Four transfer formats supported

- Fully synthesizable, static synchronous design with no internal tri-states

15.2 SPI PINS DESCRIPTION

PIN	TYPE	ACTIVE	DESCRIPTION
Scki_Scko(P0.0)	INPUT / OUTPUT	-	SPI clock input / output
MOSI(P0.1)	INPUT / OUTPUT	-	Master serial data output / Slave serial data input
MISO(P0.2)	INPUT / OUTPUT	-	Master serial data input / Slave serial data output
SSO(P0.3)	OUTPUT	low	Slave select output

Table15.1 SPI pins description

15.3 SPI HARDWARE DESCRIPTION

15.3.1 BLOCK DIAGRAM

When an SPI transfer occurs, an 8-bit character is shifted out on data pin while a different 8-bit character is simultaneously shifted in a second data pin. Another way to view this transfer is that an 8-bit shift register in the master and another 8-bit shift register in the slave are connected as a circular 16-bit shift register. When a transfer occurs, this distributed shift register is shifted eight bit positions; thus, the characters in the master and slave are effectively exchanged.

The central element in the SPI system is the block containing the shift register and the read data buffer. The system is single buffered in the transmit direction and double buffered in the receive direction. This fact means new data for transmission cannot be written to the shifter until the previous transaction is complete; however, received data is transferred into a parallel read data buffer so the shifter is free to accept a second serial character. As long as the first character is read out of the read data buffer before the next serial character is ready to be transferred, no overrun condition will occur.

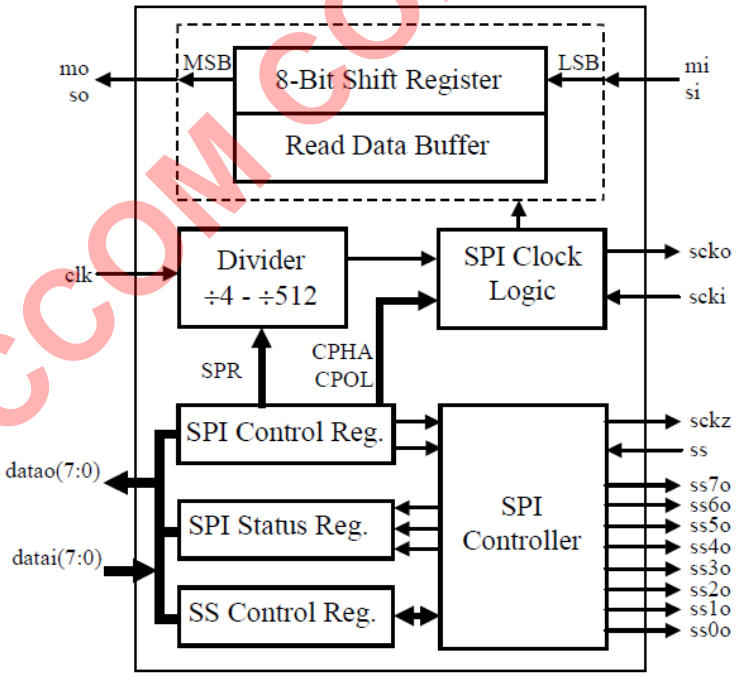


Figure 15.2 SPI Block Diagram

The eight pins are associated with the SPI: the SS, clock pins SCKI, SCKO and SCKEN, master pins MI and MO and slave pins SOEN, SI and SO.

The SS input pin in a master mode is used to detect mode-fault errors. A low on this pin indicates that some other device in a multi-master system has become a master and trying to select the SPI MODULE as a slave. The SS input pin in a slave mode is used to enable transfer.

The SCKI pin is used when the SPI is configured as a slave. The input clock from a master synchronizes data transfer between a master and the slave devices. The slave device ignore the SCKI signal unless the SS (slave select) pin is active low.

The SCKO and SCKEN pins are used as the SPI clock signal reference in a master mode. When the master initiates a transfer eight clock cycles is automatically generated on the SCKO pin.

When the SPI is configured as a slave the SI pin is the slave input data line, and the SO is the slave output data line.

When the SPI is configured as a master, the MI pin is the master input data line, and the MO is the master output data line.

15.3.2 INTERNAL REGISTERS

- **SPI Control Register**

The control register may be read or written at any time, is used to configure the SPI System.

SPCR (0xEC)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ECh EIE	R/W	SPIE	SPE	SPR2	MSTR	CPOL	CPHA	SPR1	SPR0
Reset		0	0	0	0	0	1	0	0

SPIE：SPI interrupt enable
= 0, interrupts are disabled, polling mode is used
= 1, interrupts are enabled

SPE：SPI system enable
= 0, system is off
= 1, system is on

MSTR：Master/Slave mode select
= 0, slave
= 1, master

CPOL：Clock polarity select
= 0, high level; SCK idle low
= 1, low level; SCK idle high

CPHA：Clock phase.. Select one of two different transfer formats

SPR[2:0]：SPI clock rate select bits. See the table below

SPR2	SPR1	SPR0	System clock divided by
0	0	0	4
0	0	1	8
0	1	0	16
0	1	1	32
1	0	0	64
1	0	1	128
1	1	0	256
1	1	1	512

- **Slave Select Control Register**

The control register may be read or written at any time. It is used to configure which slave select output should be driven while SPI master transfer. Contents of SSCR register is automatically assigned on SS7O-SS0O pins when SPI master transmission starts.

SSCR (0xEF)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EFh SSCR	R/W	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0
Reset		1	1	1	1	1	1	1	1

SS7 – SS0
= 0, Pin SSxO assigned while Master Transfer
= 1, Pin SSxO is forced to logic 1

- **SPI Status Register**

SPSR (0xED)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

EDh EIE	R/W	SPIF	WCOL	-	MODF	-	-	-	SSCEN
Reset		0	0	0	0	0	1	0	0

SPIF：SPI interrupt request. The flag is automatically set to one at the end of an SPI transfer.
WCOL：Write collision error status flag. The flag is automatically set if the SPDR is written while a transfer is in process.
MODF：SPI mode-fault error status flag
This flag is set if SS pin goes to active low while the SPI is configured as a master (MSTR = 1)
SSCEN：
= 1, auto SS assertions enabled
= 0, auto SS assertions disabled – SSO always shows contents of SSCR

SPI status register (SPSR) contains flags indicating the completion of transfer or occurrence of system errors. All flags are set automatically when the corresponding event occur and cleared by software sequence. SPIF and WCOL are automatically cleared by reading SPSR followed by an access of the SPDR. MODF flag is cleared by reading SPSR with MODF set followed by a write to SPCR.

The SSCSEN bit is a enable bit of automatic Slave Select Outputs assertion. When SSCEN is set (‘1’) then during master transmission the SSXO lines are automatically loaded with contents of SSCR register before each byte transfer, and deasserted when byte is transferred. When SSCEN bit is cleared the SSXO lines always shows contents of the SSCR register, regardless of the transmission is in progress or SPI MODULE is in IDLE state.

- Receiver and Transmitter Registers

The Transmitted Data Register consists of eight data bits, which will be sending on the bus due the next Send operation. The first send bit is the D.7 (MSB).

SPDR (0xEE)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEh SPDR	R/W	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.0
Reset		0	0	0	0	0	1	0	0

The Received Data Register consists of eight data bits, which were received on the bus due the last Receive operation.

SPDR (0xEE)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEh SPDR	R/W	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.0
Reset		0	0	0	0	0	1	0	0

15.4 MASTER OPERATIONS

When the SPI MODULE core is configured as a SPI master, the transfer is initiated by write to the SPDR register. When the new byte is written to the SPDR register, SPI MODULE begins transfer on the nearest BAUD timer overflow. The serial clock SCK is generated by the SPI MODULE. In master mode the SPI MODULE activates the SCKEN to enable the SCK output driver.

The SPI MODULE in master mode can select one of the eight SPI slave devices, through the SSxO lines. The SSxO lines – Slave Select output lines are loaded with contents of the SSCR register (0x03). The SSCEN bit from the SPSR register select between automatic SSxO lines control and software control. When set the automatic Slave Select outputs assertion is enabled. With SSCEN bit set in master mode the SSXO lines are automatically loaded with contents of SSCR register before each byte transfer, and de-asserted when byte is transferred. When SSCEN bit is cleared the SSXO lines are controlled by the software, and always shows contents of the SSCR register, regardless of the transmission is in progress or the SPI MODULE is in IDLE state.

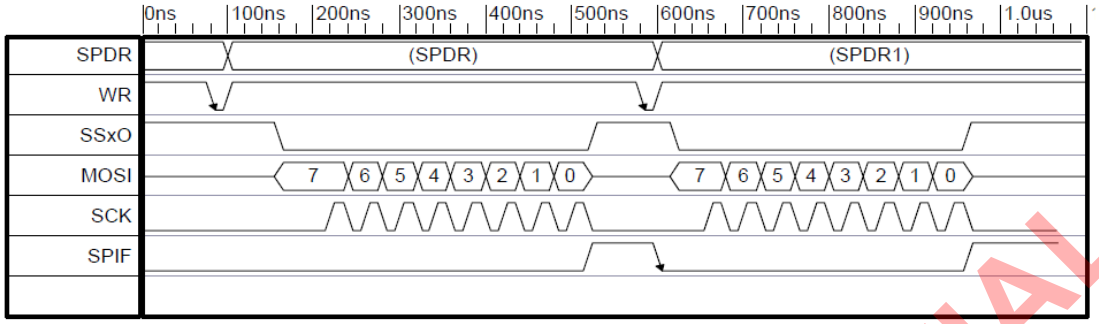


Figure15.3 Automatic slave select lines assertion

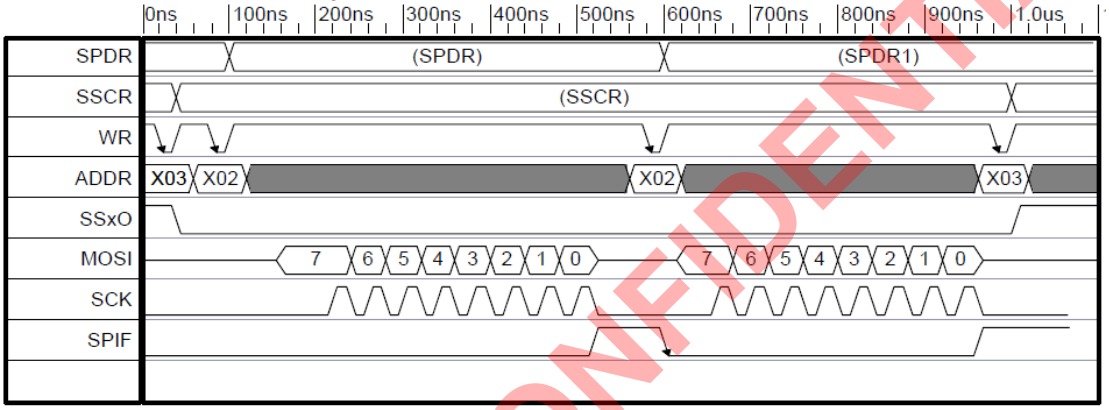


Figure15.4 Software controlled SSxO lines

15.4.1 MASTER MODE ERRORS

In master mode two system errors can be detected by the SPI MODULE. The first type of error arises in multiple-master system when more than one SPI device simultaneously tries to be a master. This error is called a Mode Fault. The second error type, a Write Collision, indicates that CPU tried to write the SPDR register while transfer was in progress.

◆ **MODE FAULT ERROR**

Mode fault error occur when the SPI MODULE is configured as a master and some other SPI master device will select this device as if it were a slave. If a Mode Fault Error occur：

- ✧ The MSTR bit is forced to zero to reconfigure the SPI MODULE as a slave.
- ✧ The SPE bit is forced to zero to disable the SPI MODULE system
- ✧ The MODF status flag is set and an interrupt request is generated

The MODF flag is cleared by reading SPSR with MODF set followed by a write to SPCR

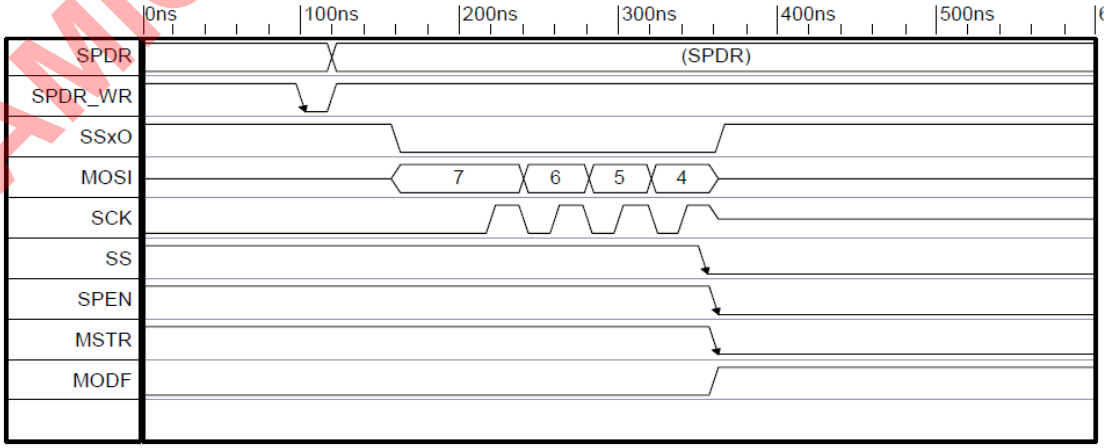


Figure15.5 Mode Fault Error generation

◆ **WRITE-COLLISION ERROR**

A write collision occurs if the SPI MODULE data register is written while a transfer is in progress. The transfer continues undisturbed, and the write data that caused the error is not written to the shifter. The Write Collision is indicated by the WCOL flag in SPSR (3) register.

The WCOL flag is set automatically by hardware, when the WCOL error condition occurs. To clear the WCOL bit, user should execute the following sequence:

- ✧ Read contents of the SPSR register
- ✧ Perform access to the SPDR register (read or write)

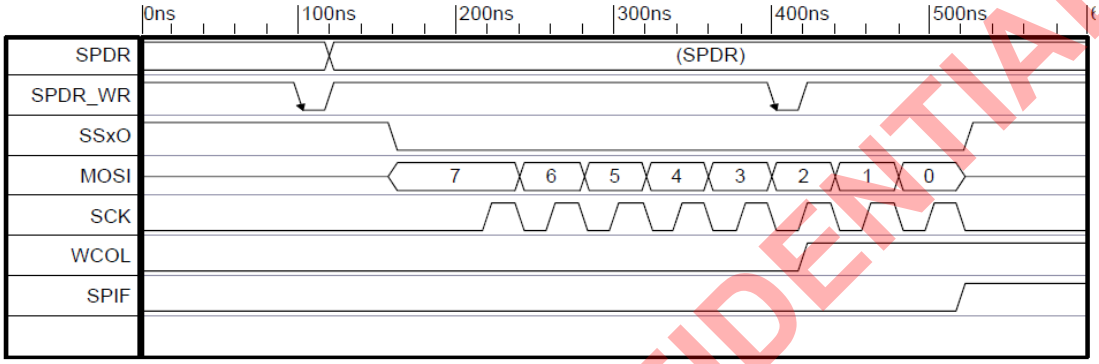


Figure15.6 Write Collision Error in SPI Master mode

15.5 SLAVE OPERATIONS

When configured as SPI Slave the SPI MODULE transfer is initiated by external SPI master module by assertion of the SPI MODULE Slave Select input, and generation of the SCK serial clock.

Before transfer starts, the SPI master has to assert the Slave Select line to determine which SPI slave will be used to exchange data. The SS is asserted (cleared = 0), the clock signal connected to the SXCK line will cause the SPI MODULE slave to shift into receiver shift register contents of the MOSI line, and drives the MISO line with contents of the Transmitter Shift register. When all eight bits are shifted in/out the SPI MODULE generates the Interrupt request by setting the IRQ output.

In SPI MODULE slave mode only one transfer error is possible – Write Collision Error.

15.5.1 SLAVE MODE ERRORS

In slave mode, only the Write Collision Error can be detected by the SPI MODULE.

The Write Collision Error occurs when the SPDR register write is performed while the SPI MODULE transfer is in progress.

In SLAVE mode when the CPHA is cleared, the write collision error may occur as long as the SS Slave Select line is driven low, even if all bits are already transferred. This is because there is not clearly specified the transfer beginning, and SS driven low after full byte transfer may indicate beginning of the next byte transfer.

◆ **WRITE-COLLISION ERROR**

A write collision occurs if the SPI MODULE data register is written while a transfer is in progress. The transfer continues undisturbed, and the write data that caused the error is not written to the shifter. The Write Collision is indicated by the WCOL flag in SPSR (3) register.

The WCOL flag is set automatically by hardware, when the WCOL error condition occurs. To clear the WCLO bit, user should execute the following sequence:

- ✧ Read contents of the SPSR register
- ✧ Perform access to the SPDR register (read or write)

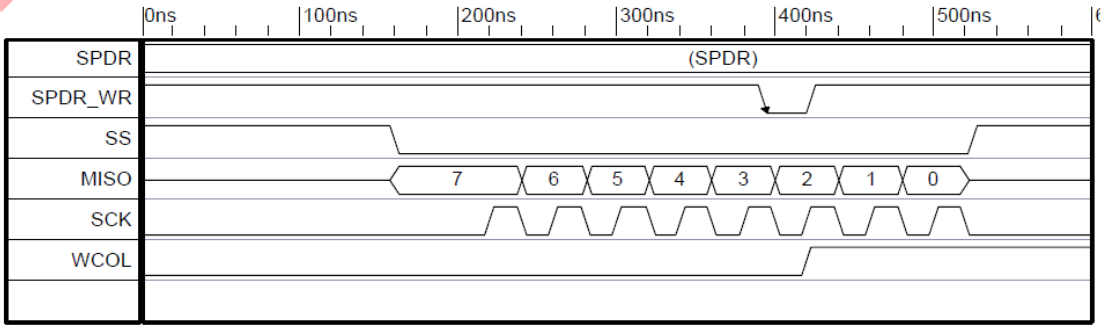


Figure15.7 Write Collision Error – SPI Slave mode – SPDR write during transfer

Figure below shows the WCOL generation, in case that the CPHA is cleared. As it is shown the WCOL generation is cause by any S{DR register write with SS line cleared. It is done even if the SPI master didn't generate the serial clock SCK. This is because there is not clearly specified the transfer beginning, and SS driven low after full byte transfer may indicate beginning of the next byte transfer.

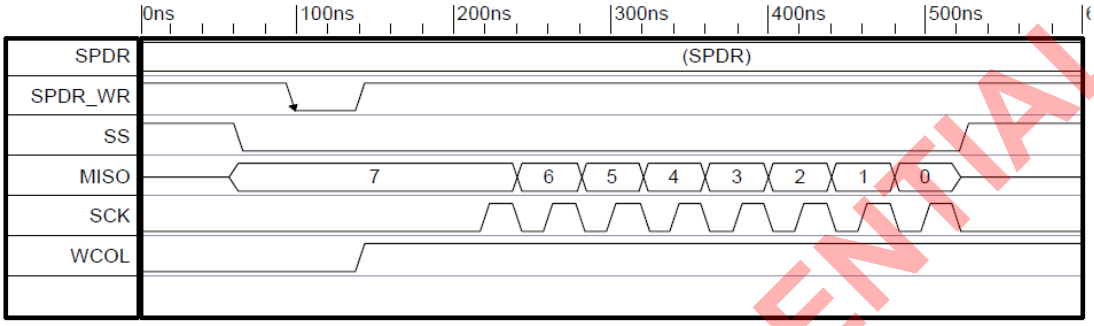


Figure15.8 WCOL Error-SPI Slave mode-SPDR write when CPHA = 0 and SS = 0

15.6 CLOCK CONTROL LOGIC

15.6.1 SPI CLOCK PHASE AND POLARITY CONTROLS

Software can select any of four combinations of serial clock (SCK) phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the SPI MODULE allows direct interface to almost any existing synchronous serial peripheral.

15.6.2 SPI MODULE TRANSFER FORMATS

During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows individual selection of a slave SPI device; slave devices that are not selected do not interfere with SPI bus activities. On a master SPI device, the slave select line can optionally be used to indicate a multiple-master bus contention.

15.6.3 CPHA EQUALS ZERO TRANSFER FORMAT

Figure below shows a timing diagram of an SPI transfer where CPHA is 0. Two waveforms are shown for SCK: one for CPOL equals 0 and another for CPOL equals 1. The diagram may be interpreted as a master or slave timing diagram since the SCK, master in/slave out (MISO), and master out/slave in (MOSI) pins are directly connected between the master and the slave. The MISO signal is the output from the slave, and the MOSI signal is the output from the master. The SS line is the slave select input to the slave; the SS pin of the master is not shown but is assumed to be inactive. The SS pin of the master must be high. This timing diagram functionally depicts how a transfer takes place; it should not be used as a replacement for data-sheet parametric information.

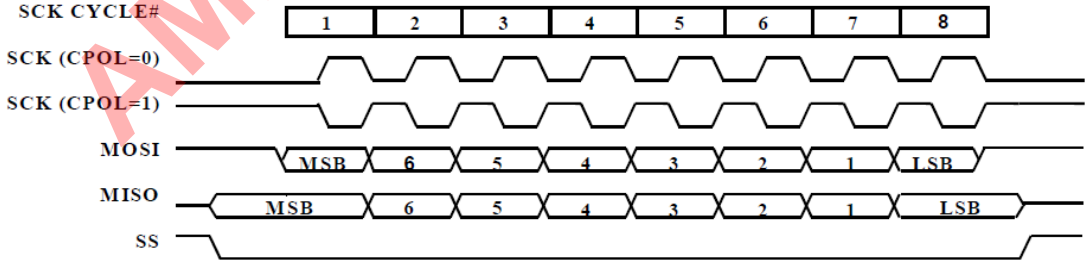


Figure15.9 CPHA Equals Zero SPI Transfer Format

When CPHA = 0, the SS line must be de-asserted and reasserted between each successive serial byte. Also, if the slave writes data to the SPI data register (SPDR) while SS is active low, a write-collision error results. When CPHA = 1, the SS line may remain active low between successive transfers (can be tied low at all times). This format is sometimes preferred in systems having a single fixed master and a single slave driving the MISO data line.

15.6.4 CPHA EQUALS ONE TRANSFER FORMAT

Figure below is a timing diagram of an SPI transfer where CPHA = 1. Two waveforms are shown for SCK: one for CPOL = 0 and another for CPOL = 1. The diagram may be interpreted as a master or slave timing diagram since the SCK, MISO, and MOSI pins are directly connected between the master and the slave. The MISO signal is the output from the slave, and the MOSI signal is the output from the master. The SS line is the slave select input to the slave; the SS pin of the master is not shown but is assumed to be inactive. The SS pin of the master must be high or must be reconfigured as a general-purpose output not affecting the SPI.

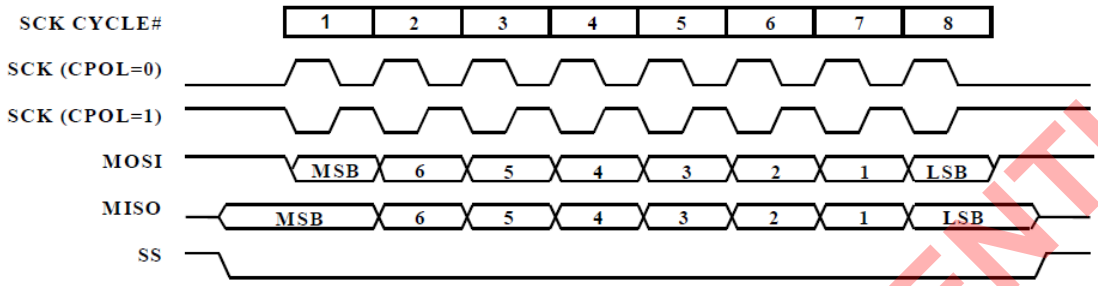


Figure15.10 CPHA Equals One SPI Transfer Format

15.7 SPI DATA TRANSFER

15.7.1 TRANSFER BEGINNING PERIOD (INITIATION DELAY)

All SPI transfers are started and controlled by a master SPI device. As a slave, the SPI MODULE considers a transfer to begin with the first SCK edge or the falling edge of SS, depending on the CPHA format selected. When CPHA = 0, the falling edge of SS indicates the beginning of a transfer. When CPHA = 1, the first edge on the SCK indicates the start of the transfer. In either CPHA format, a transfer can be aborted by taking the SS line high, which causes the SPI slave logic and bit counters to be reset. The SCK rate selected has no effect on slave operations since the clock from the master is controlling transfers.

When the SPI is configured as a master, transfers are started by a software write to the SPDR.

15.7.2 TRANSFER ENDING PERIOD

An SPI transfer is technically complete when the SPIF flag is set, but, depending on the configuration of the SPI system, there may be additional tasks. Because the SPI bit rate does not affect timing of the ending period, only the fastest rate is considered in discussions of the ending period. When the SPI is configured as a master, SPIF is set at the end of the eighth SCK cycle. When CPHA equals 1, SCK is inactive for the last half of the eighth SCK cycle.

When the SPI is operating as a slave, the ending period is different because the SCK line can be asynchronous to the MCU clocks of the slave and because the slave does not have access to as much information about SCK cycles as the master. For example, when CPHA = 1, where the last SCK edge occurs in the middle of the eighth SCK cycle, the slave has no way of knowing when the end of the last SCK cycle is. For these reasons, the slave considers the transfer complete after the last bit of serial data has been sampled, which corresponds to the middle of the eighth SCK cycle.

The SPIF flag is set at the end of a transfer, but the slave is not permitted to write new data to the SPDR while the SS line is still low.

15.8 TIMING DIAGRAMS

15.8.1 MASTER TRANSMISSION

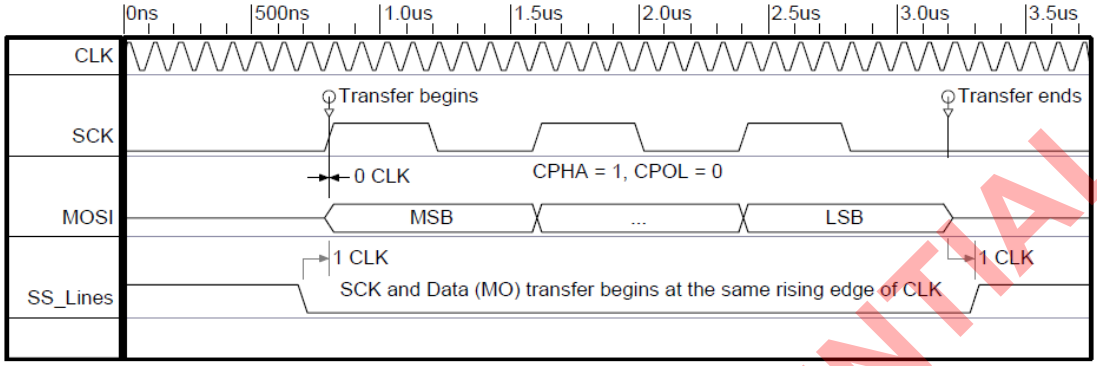


Figure15.11 Master mode timing diagram

15.8.2 SLAVE TRANSMISSION

At a beginning of transfer in Slave mode, the data on serial output (MISO) appears on first rising edge after falling edge on Slave Select (SS) line. Next bits of serial data are driving into MISO line on first rising edge of CLK after SKC active edge (in this case rising edge of SCK).

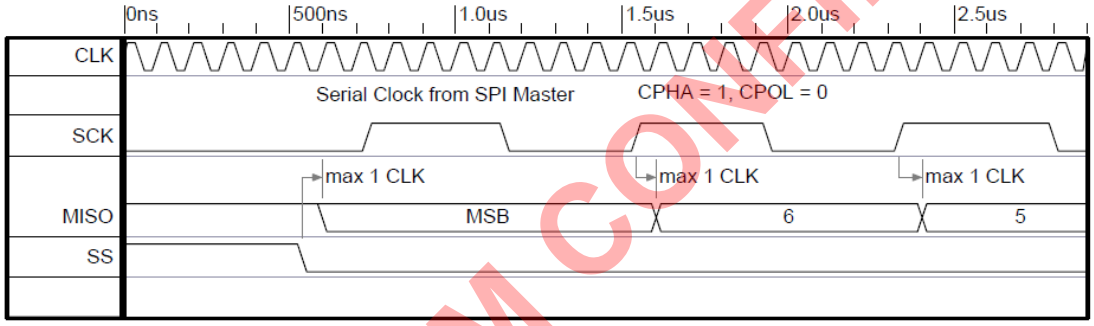


Figure15.12 Slave mode timing diagram

15.9 SPI MODULE INTERRUPT GENERATION

When interrupt is enabled (SPIE bit in SPCR=1), SPI interrupt flag is automatically asserted when SPI transfer is completed or transfer error has occurred. SPIIF flag has to be cleared by software.

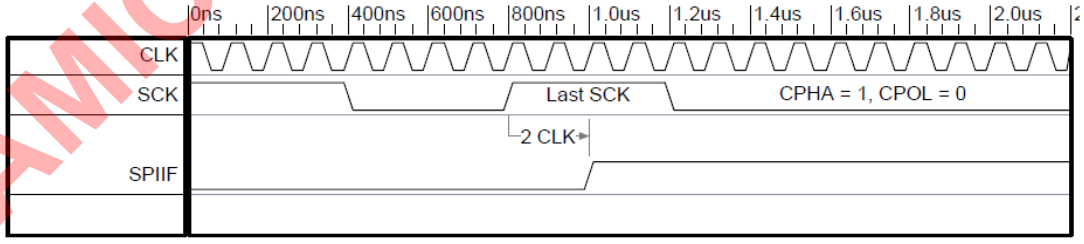


Figure15.13 Interrupt generation

Table15.2 SPI interrupt summary

Interrupt flag	Function	Active level/edge	Flag resets	Vector	Natural priority
SPIIF	Internal, SPI	-	Software	0x73	15

SPI related interrupt bits have been summarized below. The IE (0xA8) contains global interrupt system disable (0) / enable (1) bit called EA.

EIE (0xE8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E8h EIE	R/W	EI2CS ESPI	EI2CM	EWDI	EINT6	EINT5	EINT4	EINT3	EINT2
Reset		0	0	0	0	0	0	0	0

ESPI：Enable SPI Interrupts

EIP (0xF8)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F8h EIP	R/W	PI2CS PSPI	PI2CM	PWDI	PINT6	PINT5	PINT4	PINT3	PINT2
Reset		0	0	0	0	0	0	0	0

PSPI：SPI priority level control (at 1-high-level)

EIF (0x91)

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
91h EIF	R/W	I2CSF SPIF	I2CMF	-	INT6F	INT5F	-	-	INT2F
Reset		0	0	0	0	0	0	0	0

SPIIF：SPI interrupt flag
Must be cleared by software

16. PWM

A9129 has two channels Pulse width modulator (PWM) output. Every channel PWM has an 8-bit counter with comparator, a control register (PWMxCON) and two setting registers (PWMxH and PWMxL). User can select clock source by setting PWMxCON. Enable PWM output and function by setting PWMxEN = 1; otherwise disable PWM output and function by setting PWMxEN =0. When user set PWMxEN=0, it output LOW single and reload the PWMxL to itself. When the counter is enabled and matches the content of PWMxH, its output is asserted HIGH; when the counter is overflow, its output is asserted LOW and reload PWMxL to itself. The pulse frequency and the duty cycle for 8-bit PWM is given by the below equation

$$\text{Pulse frequency} = \text{System clock} / 2^{\text{pwxclk}+1} / (256-\text{PWMxL})$$
$$\text{Duty cycle} = (256-\text{PWMxH}) / (256-\text{PWMxL})$$

Noted: PWMxH must be larger than PWMxL. Otherwise, PWM output always is LOW.

16.1 PWM FUNCTIONALITY

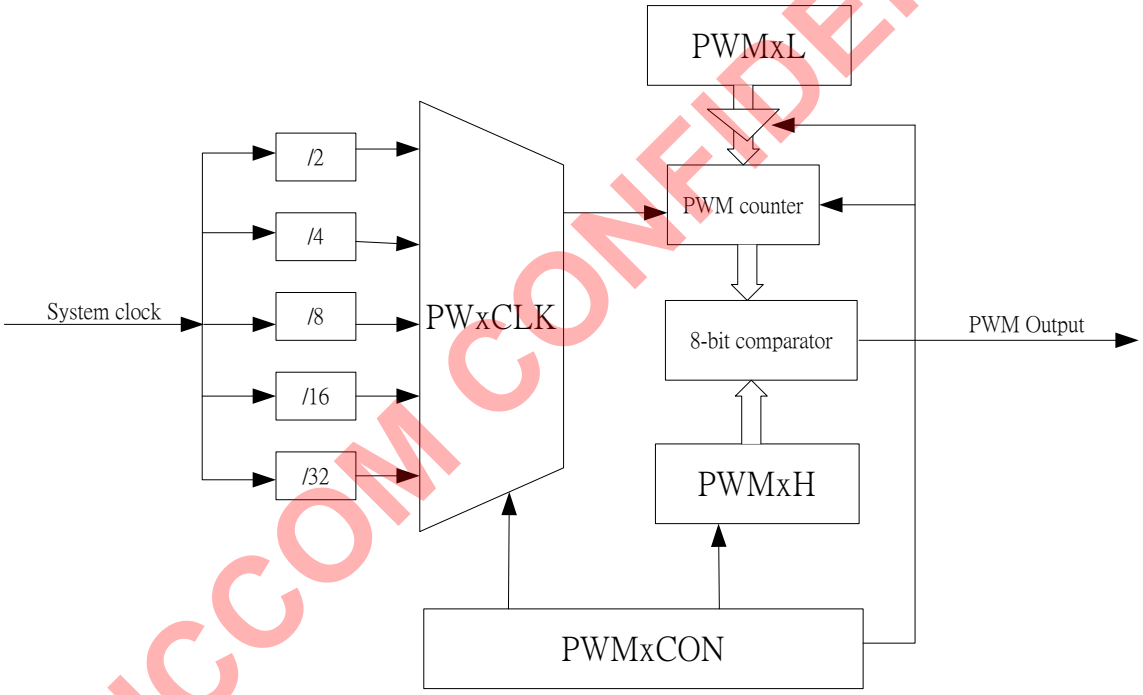


Figure16.1 PWM Block Diagram

The PWM pins functionality is described in the following table. All pins are one directional.

PIN	ACTIVE	TYPE	DESCRIPTION
PWM0(P3.6)		OUTPUT	PWM 0 output
PWM1(P3.7)		OUTPUT	PWM 1 output

Table16.1 PWM PIN define

16.1.1 PWM Registers

PWM0/1 is new design from AMICCOM. They can output pulse width modulation. User adjusts to duty cycle by setting PWMxH. PWM counter is up counter. PWM counter is not access directly by MCU. User can set or reset PWM counter by setting PWMxCON. When PWMxEN =1, PWM counter start to count. When PWMxEN=0, PWM counter stop counting and reload PWMxL to itself. PWxCLK is clock divider. It divide system clock to 2,4,8,16 and 32 by setting PWxCLK.

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A9h	R/W	PWM0EN	-	-	-	-	PW0CLK2	PW0CLK1	PW0CLK0

PWM0CON									
Reset		0	0	0	0	0	0	0	0

PWM0CON: PWM channel 0 control register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AAh PWM0H	R/W								
Reset		0	0	0	0	0	0	0	0

PWM0H: PWM channel 0 output HIGH register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ABh PWM0L	R/W								
Reset		0	0	0	0	0	0	0	0

PWM0L: PWM channel 0 frequency setting register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B0h PWM1CON	R/W	PWM1EN	-	-	-	-	PW1CLK2	PW1CLK1	PW1CLK0
Reset		0	0	0	0	0	0	0	0

PWM1CON: PWM channel 1 control register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B1h PWM1H	R/W								
Reset		0	0	0	0	0	0	0	0

PWM1H: PWM channel 1 output HIGH register

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B2h PWM1L	R/W								
Reset		0	0	0	0	0	0	0	0

PWM1L: PWM channel 1 frequency setting register

17. ADC (Analog to Digital Converter)

A9129 has three built-in ADC. One is 8-bits ADC that do RSSI measurement as well as carrier detection function. The ADC clock (F_{ADC}) is 4MHz. The ADC converting time is 20 x ADC clock periods. Another is 4 channel 12bit SAR ADC for general purpose use to measure the external analog signal. The other is 24bit ADC for measure thermal resister.

Bit		Mode	
XADS	RSS	Standby	RX
0	1	None	RSSI / Carrier detect

Table 17.1 Setting of ADC function

Relative Control Register

MODEC2 (Address: 0x802h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MODEC2	W/R	STRR	ARSSI	FIFOREV	MSCD	WOR_EN	FMT	FMS	ADCM
Reset		0	0	0	0	0	0	0	0

RX (Address: 0x820h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX	W	--	AGCE	BW1	BW0	RXDI	DMG1	DMG0	ULS
	R	ADCO8	--	--	--	--	--	--	--
Reset		0	0	0	0	0	0	0	0

ADCC (Address: 0x821h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCC	W	MXD	RADC	AVS1	AVS0	MVS1	MVS0	XADSR	CDM
	R	ADCO7	ADCO6	ADCO5	ADCO4	ADCO3	ADCO2	ADCO1	ADCO0
Reset		0	0	0	0	0	0	0	0

RSSI (Address: 0x824h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSSI	W	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Reset		0	0	0	0	0	0	0	0

17.1 RSSI Measurement

A9129 contains a built-in 8-bit ADC for internal temperature measurement, RSSI measurement.

XADS	CDM	None Rx state	RX state
0	0	Temperature measurement	RSSI measurement
0	1	N/A	Carrier detector

The conversion time of 8-bit ADC is depends on the clock input to ADC. It takes 20 cycles to complete the conversion. The clock source of ADC comes from Crystal oscillator, and according to the setting of bit GRC[4:0] in system clock register, user can select the ADC clock source to be 800KHz or 1.2MHz.

17.2 Temperature Measurement

A9129 has a simple on-chip temperature sensor. Set bit =0 in ADC register first, then enable bit ADCM=1 in the mode control

register to start the measurement of temperature. When the measurement is completed, the bit ADCM will be cleared to 0. User can then read the ADC[7:0] values from the ADC register.

17.3 RSSI Measurement

A9129 has a built-in RSSI (received signal strength indicator) read from ADC to measure the received RF signal strength. When the measurement procedure is completed, the RSSI value can be read form ADC register, the range of RSSI is 0~511. Larger signal strength is corresponding to smaller RSSI value, and vice versa. In RX state, set bit CDM=0 in ADC register, and then set bit ADCM=1 in mode control register to start the RSSI measurement. Once the measurement is completed, the bit ADCM will be cleared to 0. User can read the RSSI value from ADCO[8:0] (0x09).

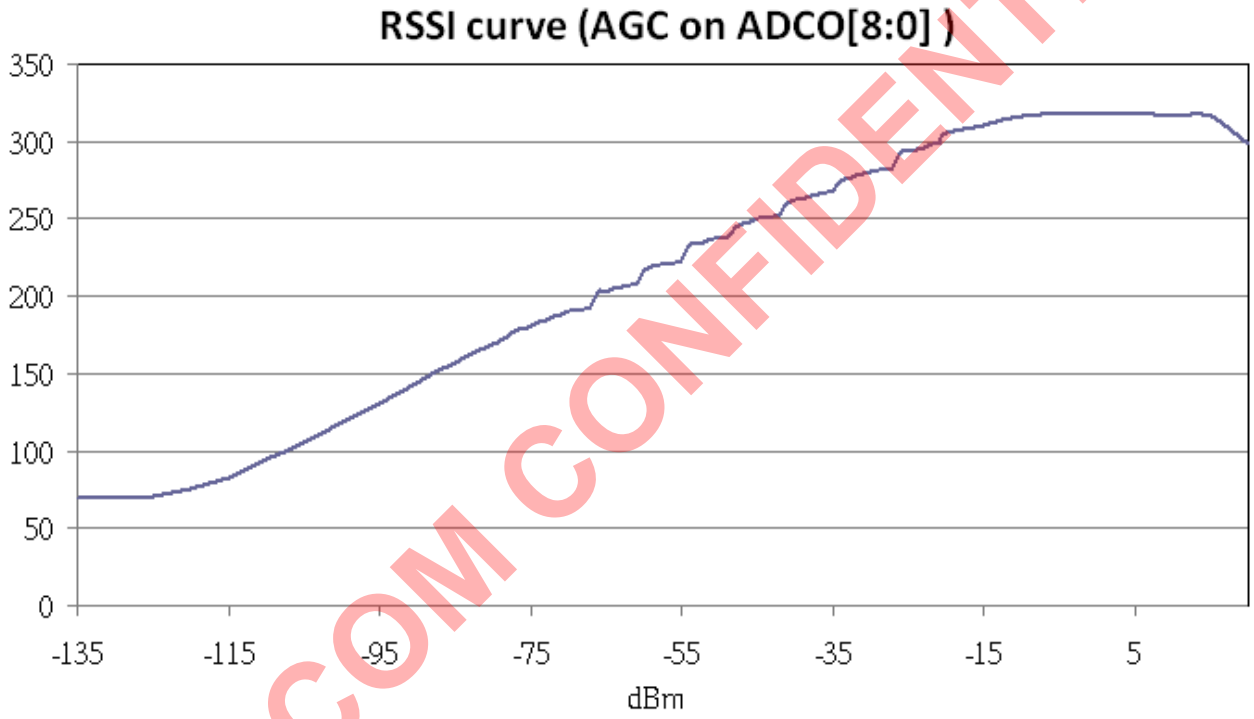


Figure 17.1 Typical RSSI characteristic.

17.4 Carrier Detect

A9129 provides an CD signal (output from GIO1 or GIO2) to monitor that there is a carrier or not. If the carrier signal strength is greater than the value set by bit RTH[7:0] in ADC register, CD will go high, or it will stay low. In RX state, set ADC register bit CDM=1, set mode control register bit ADCM=1 to start the carrier signal measurement. The value is stored in bit ADC[7:0] and it will be updated in each measurement period till the end of detection action.

17.5 Battery Detect

A9129 has a built-in battery detector to check supply voltage (REGI pin). The detecting range is 2.0V ~ 2.7V in 8 levels.

Relative Control Register
BD (Address: 0x832h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BD	W	CA1	CA0	RGV1	RGV0	BVT2	BVT1	BVT0	**BDS**

	R	--	--	--	VBD	--	--	--	BODF
Reset		0	0	0	0	0	0	0	0

BVT[1:0]: Battery detection threshold.
[00]: 2.0V. [01]: 2.2V. [10]: 2.4V. [11]: 2.6V.
When REGI < Threshold, BDF= low.
When REGI > Threshold, BDF= high.

Below is the procedure to detect low voltage input (ex. below 2.1V):

1. Set A9129 in standby or PLL mode.
2. Set BVT[2:0] (0830h) = [001] and enable BDS (0830h) = 1.
3. After 100 us, BDS is auto clear.
4. MCU reads BDF (0830h).
   If REGI pin > 2.1V,
   BDF = 1 (battery high). Else, BDF = 0 (battery low).

18. Power Management

The power consumption of A9129 comes from two parts. One is RF part and the other is digital part (includes MCU core and peripherals). In the RF part, the idle mode use the minimum power and the TX or RX mode use the maximum power consumptions. Use changes RF status by setting the strobe control, register(0800h). For more detail information, please refer chapter 20.1. In this chapter only introduces digital parts. Low power operation is enabled through different power modes setting. A9129 has various operating mode are referred as normal mode, PM2, and PM3 (power manager mode 3). Table 19.1 shows the impact of different power modes on systems operation. There are two registers to setting power manager. One is power control register (PCON, 0x87h) and the other is power control extend register (PCONE, 0xB9h).

In PMM mode, user selects different clock be MCU core clock.in CLKSEL[2:0] (PCONE, 089h) then enable PMM (PCON, 087h). User adjusts MCU clocks depends on the required power consumption. CLKSEL[2:0] = 001 ~ 110b, the MCU core clock is the clock sources divide 2 ~ 64. **BEWARE, please choice CLKSEL firstly then enable PMM to avoid glitch. Please refer the reference code or contact AMICCOM's FAE.**

User can enable STOP to freeze MCU core clock and all digital peripherals also stop. MCU can be waked up by hardware reset, KEY wake up, KEYINT or sleep timer (WOR /TWOR). User set sleep timer, WOR or TWOR before enter STOP mode.

Note: Please return normal mode firstly and then switch PMM to STOP or STOP to PMM.

PCON (087h) Power control

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
87h PCON	R/W	SMOD	-	-	PWE	-	SWB	STOP	PMM
Reset		0	0	0	0	0	0	0	0

SWB (Switchback enable)
[1]: Enable
[0]: Disable
STOP (Stop mode)
[1]: Enable
[0]: Disable
PMM (Power manager mode)
[1]: Enable power manager mode
[0]: Disable power manager mode

PCONE(089h) Power control extend

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B9h PCONE	R/W	-	-	QD	REGAE	PM3F	CLKSEL2	CLKSEL1	CLKSEL0
Reset		0	0	0	0	0	0	0	0

QD (Quick discharge)
[1]: Quick discharge enable
[0]: Quick discharge disable
REGAE(RegA Enable)
[1]: Enable
[0]: Disable
PM3F (Power Mode 3 flag)
[1]: EnablePM3. MCU enter PM3 after STOP mode
[0]: Disable PM3
CLKSEL[2:0] (Clock Select), Select PMM (Power manager mode) clock source
[000]: Clock source div 64 as MCU clock
[001]: Clock source div 2 as MCU clock
[010]: Clock source div 4 as MCU clock
[011]: Clock source div 8 as MCU clock
[100]: Clock source div 16 as MCU clock
[101]: Clock source div 32 as MCU clock
[110]: Clock source div 64 as MCU clock
[111]: Select RTC as CPU clock when PMM=0; RTC div 2 as CPU clock when PMM=1

	MCU speed	16MHz	Internal RC	RTC	RAM	Back to Normal	LVR	RF
Normal	16MHz	ON	V	V	ON	--	V	V
PMM (Low speed)	8/4/2/1 MHz IRC/RTC	ON	V	V	ON	Interrupt / mode switch	V	V
PM2	OFF	OFF	V	V	ON	H/W reset / wakeup key / KEYINT	V	WOR/TWOR
PM3	OFF	OFF	V	V	ON (4K SRAM)	Reset Key Reset	V	WOR/TWOR

Table 18.1 Power manager

V: available, it can turn on or off by user setting
Note: P3.2, P3.3, P3.4 and P3.5, please set to output high or input with pull-up in PM mode to save leakage current.

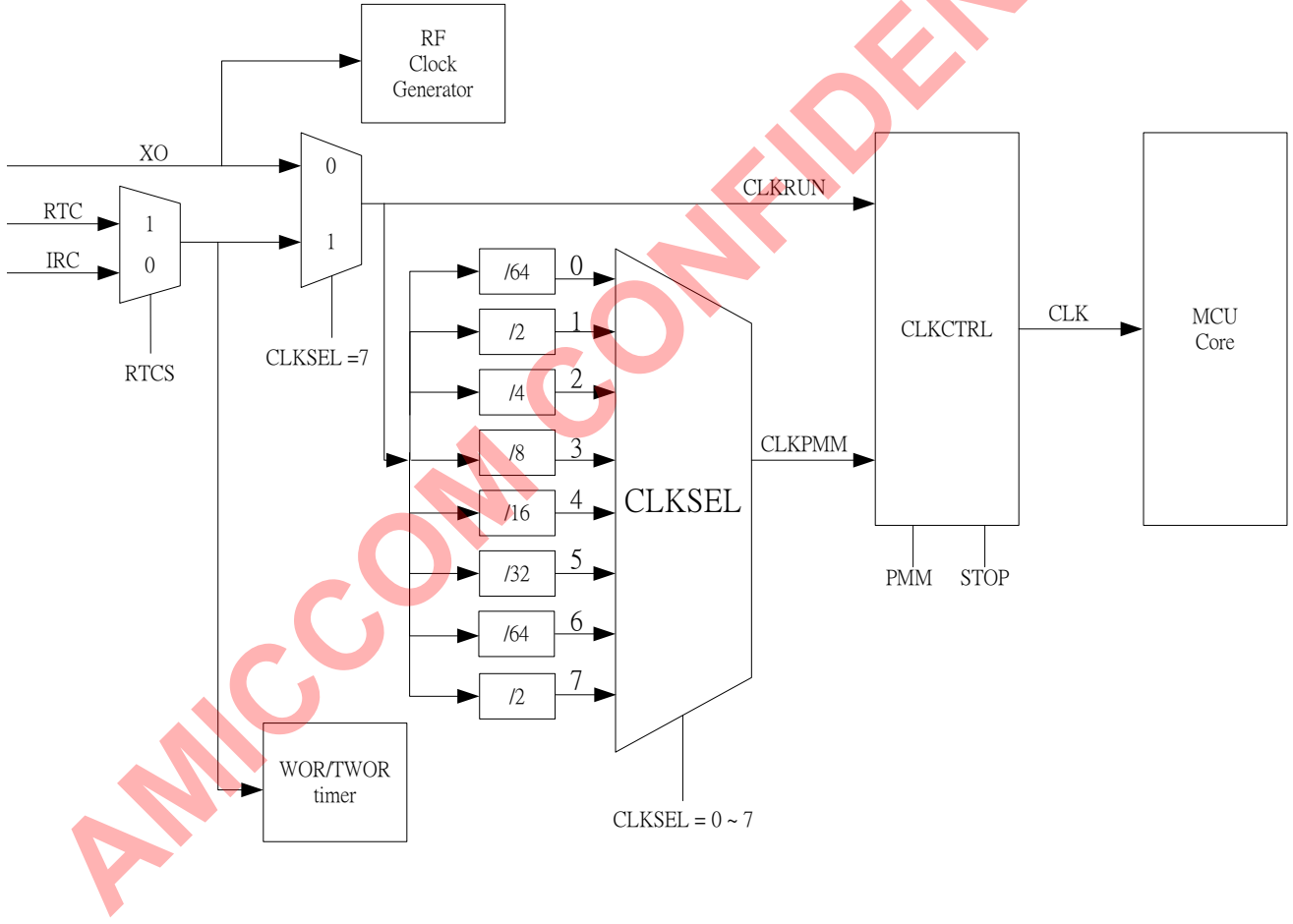


Figure 18.1 Whole chip clock sources

19. A9129 RF

A9129 integrate Sub1GHz FSK/GFSK Sigma-delta modulation transceiver and use Strobe control register (0800h) to control RF state. There are 6 Strobe commands to control internal state machine for RF operations. These modes include Sleep mode, Idle mode, Standby mode, PLL mode, RX mode and TX mode. There are two 64Bytes FIFO for data transmitting and receiving. Sleep timer is used for WOR (Wake On Rx) and time-slotted mode operation.

19.1 Strobe Command

Strobe Control Register (Address: 0800h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R					FPEN	RFSTATE2	RFSTATE1	RFSTATE0
	W	Strobe3	Strobe2	Strobe1	Strobe0			--	--
Write Reset Value		0	0	0	0	0	0	0	0

Use strobe command control RF state.
Strobe[3:0] is strobe command register.
Strobe[3:0] = 4'b1000: Sleep mode.
Strobe[3:0] = 4'b1001: Idle mode.
Strobe[3:0] = 4'b1010: Standby .
Strobe[3:0] = 4'b1011: PLL mode.
Strobe[3:0] = 4'b1100: RX mode
Strobe[3:0] = 4'b1101: TX mode

RFSTATE[2:0] is RF state flag.
RFSTATE[2:0] = 3'b000: Sleep mode.
RFSTATE[2:0] = 3'b001: Idle mode.
RFSTATE[2:0] = 3'b010: standby mode.
RFSTATE[2:0] = 3'b011: PLL mode.
RFSTATE[2:0] = 3'b100: RX mode
RFSTATE[2:0] = 3'b101: TX mode

19.1.1 Strobe Command - Sleep Mode

Refer to Strobe Control Register, user can write 0x80 to Strobe Control Register directly to set RF into Sleep mode.

19.1.2 Strobe Command - Idle Mode

Refer to Strobe Control Register, user can write 0x90 to Strobe Control Register directly to set RF into Idle mode.

19.1.3 Strobe Command - Standby Mode

Refer to Strobe Control Register, user can write 0xA0 to Strobe Control Register directly to set RF into Standby mode.

19.1.4 Strobe Command - PLL Mode

Refer to Strobe Control Register, user can write 0xB0 to Strobe Control Register directly to set RF into PLL mode.

19.1.5 Strobe Command - RX Mode

Refer to Strobe Control Register, user can write 0xC0 to Strobe Control Register directly to set RF into RX mode.

19.1.6 Strobe Command - TX Mode

Refer to Strobe Control Register, user can write 0xD0 to Strobe Control Register directly to set RF into TX mode.

19.2 RF Reset Command

In addition to power on reset (POR), A9129 could issue software reset (80h)to RF by setting Mode Register (0801h). A9129 generates an internal signal "RESETN" to initial RF circuit. After reset command, RF state is in standby mode and re-calibration is necessary.

19.3 FIFO Accessing Command

Before TX delivery, user only needs to write wanted data into TX FIFO in advance. Similarly, user can read RX FIFO once payload data is received. It is easy to delivery data to air. Below is the procedure of writing TX FIFO.

Step1: Send (n+1) bytes TX data in sequence by Data Byte 0, 1, 2 to n.
Step2: Send TX Strobe command for transmitting.

There are similar steps to read RX FIFO.

Step1: Send RX Strobe command for receiving data.
Step2: Read RX data from RX FIFO in sequence by Data Byte 0, 1, 2 to n.

20. Flash memory controller

SFR RELATED REGISTERS
FLASH memory is controlled using PCON(0x87)'s PWE bit, FLSHCTRL(0x9A) and FLSHTMR (0x9B), FLSHTPG(0x9C) and FLSHTER(0x9D). An SFR register named FLASHCTRL (0x9A) is used to control communication between CPU and flash. FLSHCTRL(0x9A) is consisted of 6bits used to control all FLASH related operations. Lower five bits of FLSHTMR (0x9B) named FREQ[4:0] determine real CLK frequency with 1MHz step resolution. FREQ[4:0] after reset is set to 20MHz by default, provides optimal timing for flash macro.

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
9Ah FLSHCTRL	R/W	CTRL.7	CTRL.6	CTRL.5	CTRL.4	CTRL.3	CTRL.2	CTRL.1	CTRL.0
Reset		0	0	0	0	0	0	0	0

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
9Bh FLSHTMR	R/W				Fewq.4	Fewq.3	Fewq.2	Fewq.1	Fewq.0
Reset		0	0	0	0	0	0	0	0

FREQ[4:0]	Frequency MHz
0x00	-
0x01	1
0x02	2
...	...
0x14	20

Table 3. FREQ intervals

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
9Ch FLSHTPG	R/W								
Reset		0	0	0	0	0	0	0	0

Address/Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
9Dh FLSHTER	R/W								

Reset		0	0	0	0	0	0	0	0

Setting higher clock frequency is not supported since given flash has limited its clock frequency up to 20 MHz by Tkp read cycle time. FLASHCTRL register is write protected by TA enable procedure listed below:

```
  CLR  EA ;disable interrupt system
MOV TA, #0xAA
MOV TA, #0x55
MOV FLASHCTRL,#<value> ; Any direct addressing instruction writing FLASHCTRL register.
  SETB  EA  ;Enable interrupt system
```

The Program Write Enable (PWE) bit, located in PCON register, is used to enable/disable PRGROMWR and PRGRRAMWR pin activity during MOVX instructions.

PCON (0x87)

7	6	5	4	3	2	1	0	Reset
SMOD0	SMOD1	-	PWE	-	SWB	STOP	PMM	0x00

Figure 4. PCON register – PWE bit

When PWE bit is set to logic 1, the MOVX @DPTR,A instruction writes data located in accumulator register in to Program Memory addressed by DPTR register (active :DPH:DPL). The MOVX @Rx,A instruction writes data located in accumulator register into program memory addressed by P2 register (bits 15:8) and Rx register (bits 7:0). Program Memory can be read by MOVC only regardless of PWE bit.

CHIP ERASE OPERATION

Chip erase operation is enabled by setting CTRL[5:0]=0x04 of FLSHCTRL register according to CPU TA enable procedure. PCON.PWE bit must be set too, then first MOVX instruction writing to program memory space at address belong to certain FLASH macro begins sector erase operation. During erase operation CPU is halted by asserting FLASHBUSY pin. When FALSH macro has been erased. FLASHBUSY pin id deactivated and FNOP is automatically written. CPU executes next instruction. CMT FLASH macro is blank and ready for new programming. To erase another FLASH macro the whole procedure needs to be repeated with changed MOVX address pointing to certain FLASH macro. Preprograming of whole FLASH macro is executed automatically without any interaction with user, before real chip erase. It extends lifecycle of CMT FLASH macro.

SECTOR ERASE OPERATION

The 16kB CMT FLASH macro has 128 sectors (128B each) which can be erased separately. Sector erase operation is enabled by setting CTRL[5:0]=0x02 of FLSHCTRL register according to CPU TA enable procedure . PCON.PWE bit must be set too, then first MOVX instruction writing to program memory space at selected sector address begins sector erase operation. During sector erase operation CPU is halted by asserting FLASHBUSY pin. When sector has been erased FLASHBUSY pin is deactivated and FNOP is automatically written. CPU executes next instruction. Selected CMT FLASH macro sector(s) is blank and ready for new programming. To erase another sectors whole procedure needs to be repeated. Preprograming of whole sector is executed automatically without any interaction with user, before real sector erase. It extend lifecycle of CMT FLASH macro.

PROGRAM OPERATION

Word program operation is enabled by setting CTRL[5:0]=0x01 of FLSHCTRL register according to CPU TA enable procedure. PCON.PWE bit must be set too, then each write to program memory space by MOVX instruction addressing odd byte begins word program operation. During program operation CPU is halted by asserting FLASHBUSY pin. When word has been programmed FLASHBUSY pin is deactivated. CPU executes next instruction which can be (i) programming of next memory word (ii) CTRL[5:0] = 0x00 according to CPU TA enable procedure. Number of programmed by bytes must be always even number(2,4,6…) . For example to program byte at address 0x003, first must be written byte at address 0x002 then second MOVX instruction write at address 0x003 begins physical write to CMT FLASH macro. When number of programmed bytes is not even then it must be filled with extra neutral byte - for FLASH macro it is 0x00. The neutral byte doesn't program any bit in a FLASH macro.

21. In Circuit Emulator (ICE)

A9129 support In Circuit Emulator on chip. It is a real-time hardware debugger as a non-intrusive system. It doesn't need to occupy any hardware resource such as the UART and Timer. User develops firmware complete producing code without any modification using ICE. It helps user to track down hidden bugs within the application running with microcontroller. The ICE with Hardware USB dongle provides a powerful SoC development tool with silicon using 2-wire protocol. The ICE fully supports Keil uVision2/3/4 interface to hardware debuggers. It allows Keil software user to work with uvision2/3/4. For more detail information, please reference Application note.

21.1 PIN define

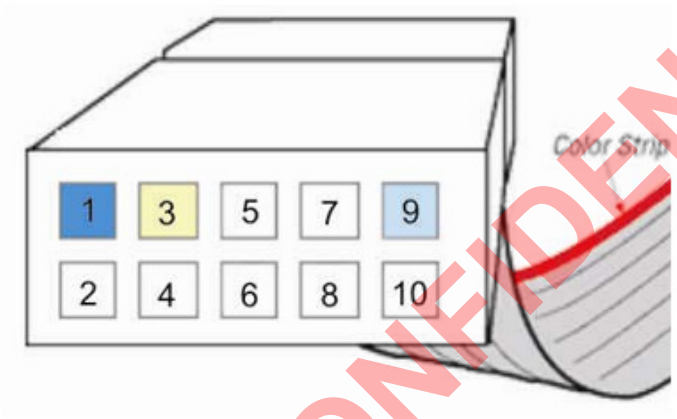


Figure 21.1 The USB connectors

Pin	Signal name	Description	Pin	Signal name	Description
1	ttck	Clock signal (in)	2	GND	Signal Ground
3	ttdio	Data (io)	4	VCCIO	Used to VCCIO detection
5	NU	Do not use	6	NU	Do not use or connect
7	NU	Do not use	8	NU	Do not use or connect
9	rsto	Reset output (od)	10	GND	Signal Ground

Figure 21.2 The Pin define within USB connector

Note: RSTO pin forces logic zero to issue reset. When RSTO is inactive its output is floating, and should be connected to global system reset with pull-up resistor. This pin can be left unconnected.

There are 10 pin in the ICE connectors. 2-wire ICE only use 2 pins (PIN1 and PIN3). The PIN9 is optional and it can connect reset signal. PIN2 and PIN10 are GND pin. PIN4 is VCCIO pin. The recommended circuit shows as the below figure. (Figure 21.3). There is a resister (100 ohm) between A8510 and pin connected the connector.

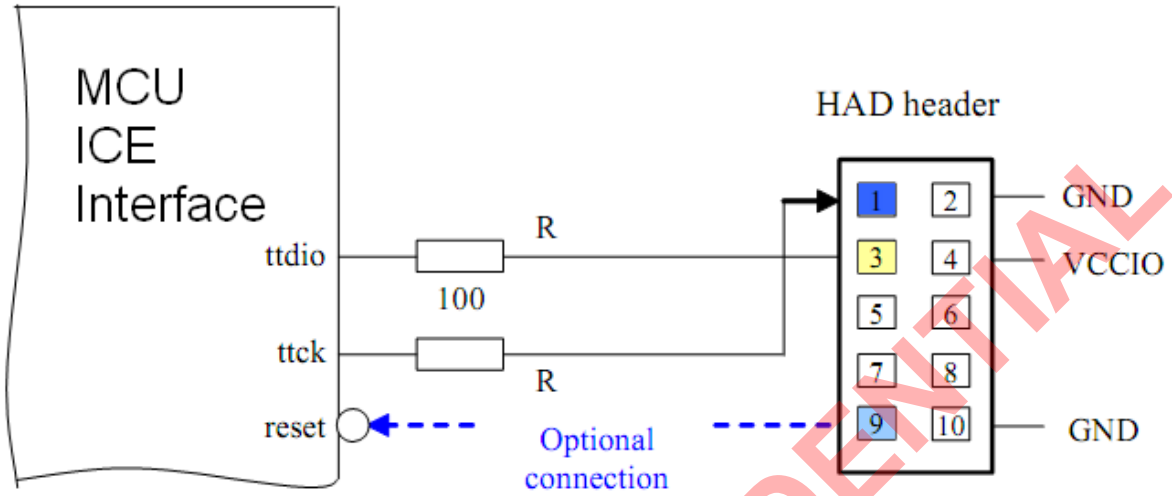


Figure 21.3 The connections between A9129 and USB connectors

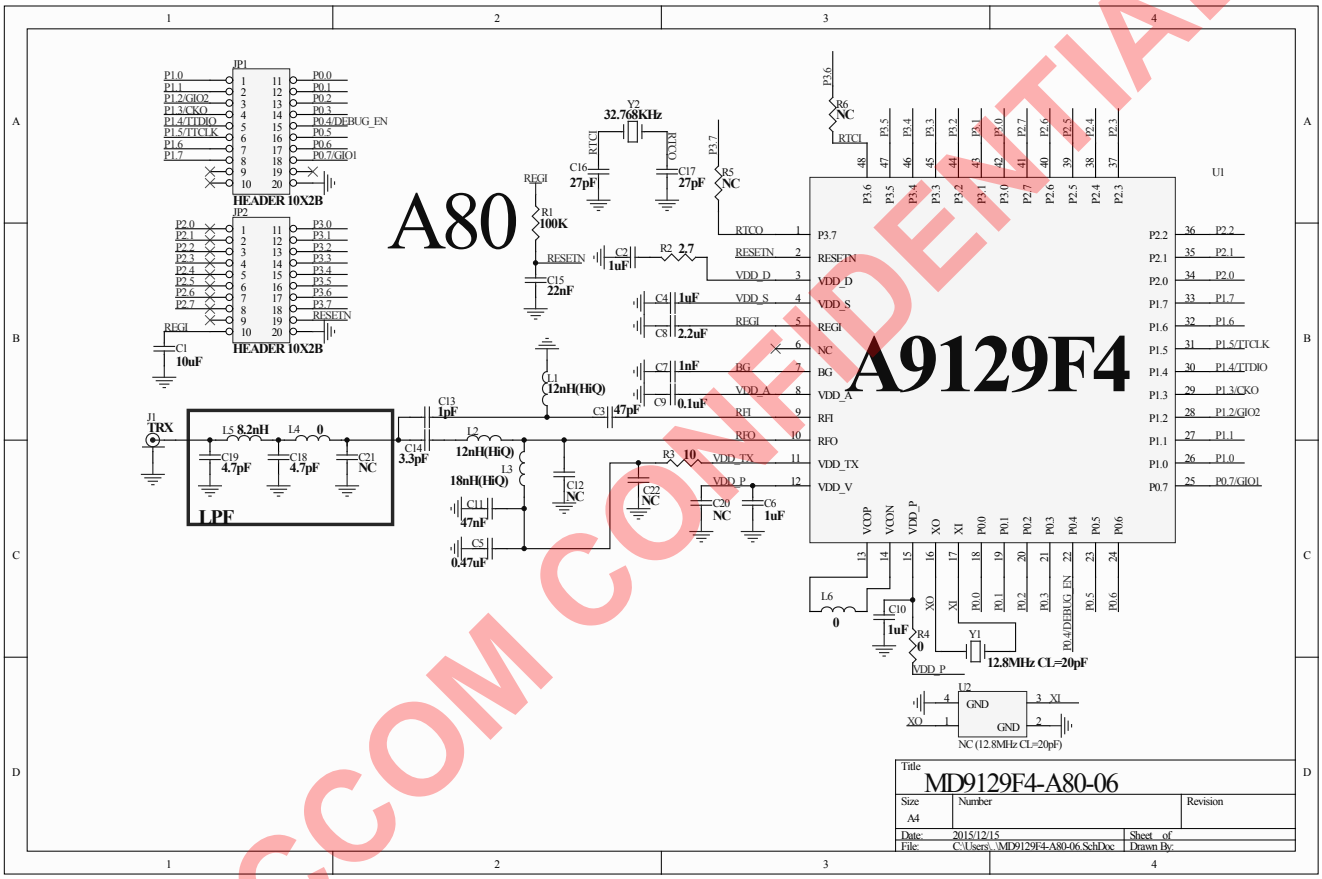
21.2 ICE Key feature

The ICE supports source level debugging, 2 hardware breakpoint, auto refresh of all register and In system programming (ISP). User can use ICE to download firmware by Keil software or AMICCOM tool.

22. Application circuit

The all modules are reference circuit and all circuit may be updated without any notice. Please contact AMICCOM FAE for the last version module spec. and circuit design.

22.1 MD9129F4-A80 (868MHz band)



23. Abbreviations

ADC	Analog to Digital Converter
AIF	Auto IF
FC	Frequency Compensation
AGC	Automatic Gain Control
BER	Bit Error Rate
BW	Bandwidth
CD	Carrier Detect
CHSP	Channel Step
CRC	Cyclic Redundancy Check
DC	Direct Current
FEC	Forward Error Correction
FIFO	First in First out
FSK	Frequency Shift Keying
ID	Identifier
ICE	In Circuit Emulator
IF	Intermediate Frequency
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
MCU	Micro Controller Unit
PFD	Phase Frequency Detector for PLL
PLL	Phase Lock Loop
POR	Power on Reset
PWM	Pulse width modulation
RX	Receiver
RXLO	Receiver Local Oscillator
RSSI	Received Signal Strength Indicator
SPI	Serial to Parallel Interface
SYCK	System Clock for digital circuit
TX	Transmitter
TXRF	Transmitter Radio Frequency
VCO	Voltage Controlled Oscillator
XOSC	Crystal Oscillator
XREF	Crystal Reference frequency
XTAL	Crystal

24. Ordering Information

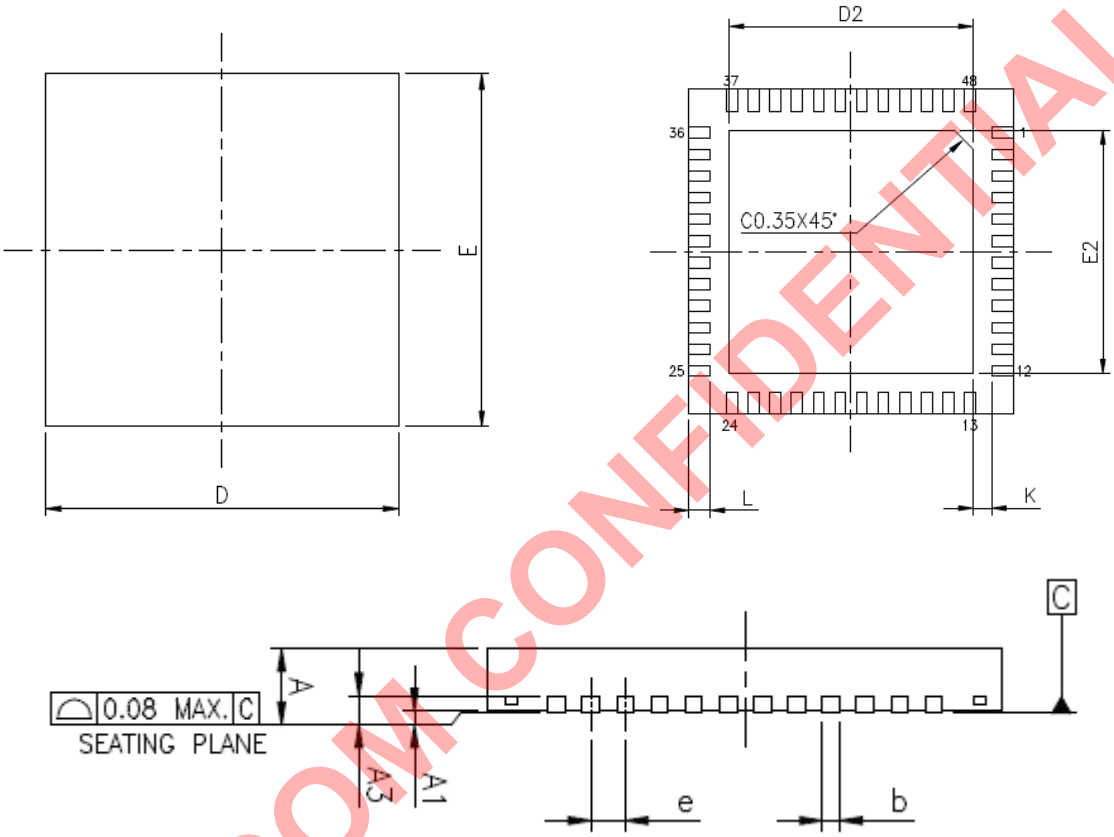
Part No.	Package	Units Per Reel / Tray
A91X29F4001AQ6C/Q	QFN48L, Pb Free, Tape & Reel, -40℃～85℃	3K
A91X29F4001AQ6C	QFN48L, Pb Free, Tray, -40℃～85℃	490EA
A91X29F4001AH	Die form, -40℃～85℃	100EA

25. Package Information

QFN6*6 48L Outline Dimensions

Top View

Bottom View

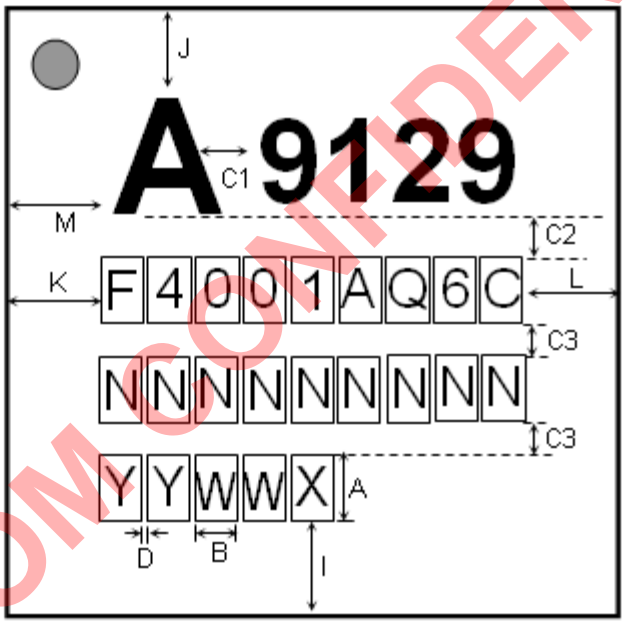


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.031	0.7	0.75	0.8
A_1	0	0.001	0.002	0.00	0.02	0.05
A_3		0.009 REF.			0.23REF.	
b	0.006	0.008	0.010	0.15	0.2	0.25
D		0.240			6.1 BSC	
D_2	0.146	0.177	0.179	3.70	4.50	4.55
E		0.240			6.1BSC	
E_2	0.146	0.177	0.179	3.70	4.50	4.55
e		0.016BSC			0.4BSC	
L	0.013	0.016	0.020	0.32	0.4	0.48
k		0.008			0.2	

26. Top Marking Information

- Part No. : **A91X29F4001AQ6C**
- Pin Count : **48**
- Package Type : **QFN**
- Dimension : **6*6 mm**
- Mark Method : **Laser Mark**
- Character Type : **Arial**

❖TOP MARKING LAYOUT:



❖ CHARACTER SIZE : (Unit in mm)

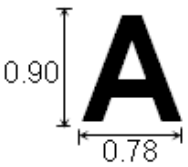
A : 0.65
B : 0.45
C1 : 0.3 **C2 : 0.4** **C3 : 0.3**
D : 0.03
M : 1.5

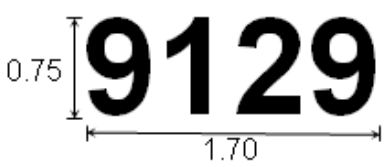
YYWW : DATECODE

X : PKG HOUSE ID

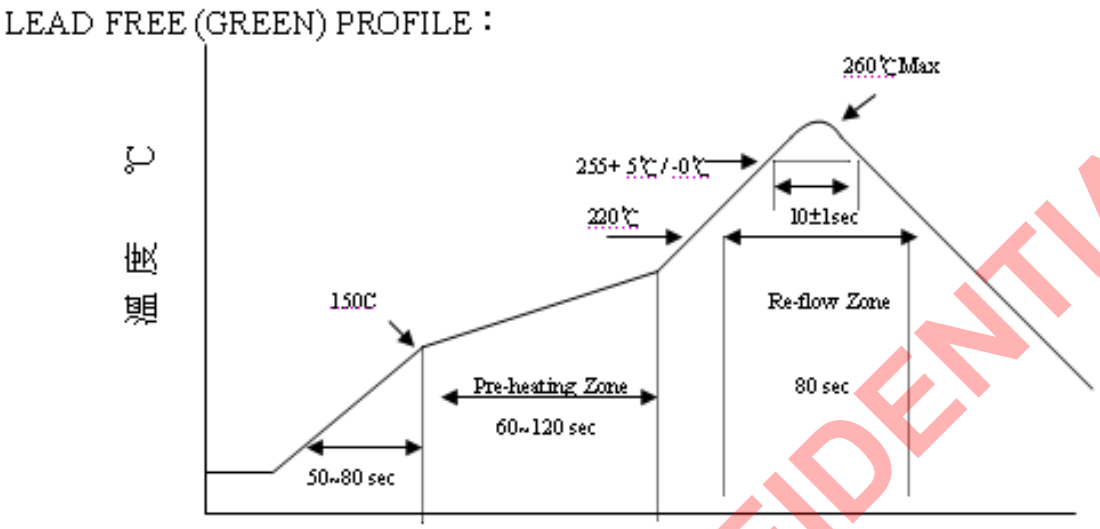
NNNNNNNNN : LOT NO.
(max. 9 characters)

I=J
K=L





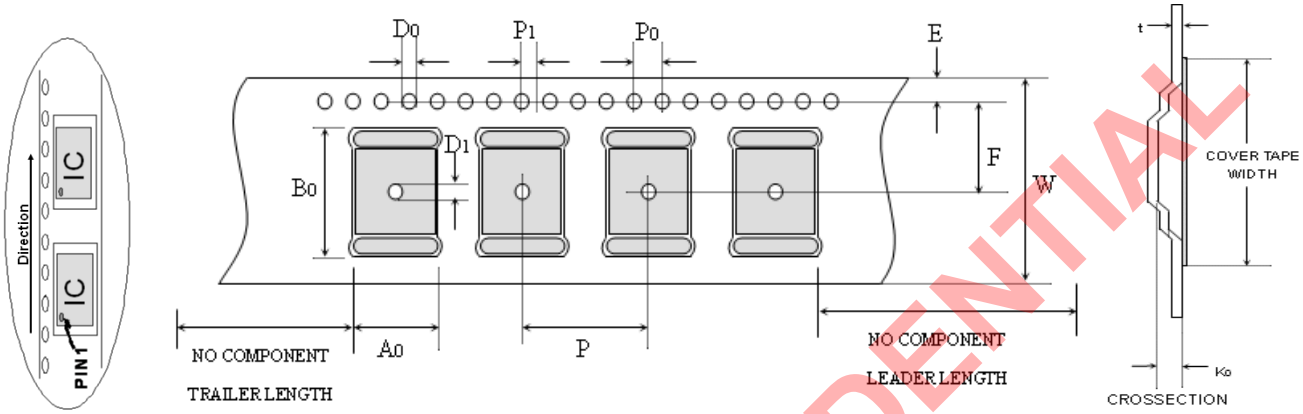
27. Reflow Profile



Actual Measurement Graph

28. Tape Reel Information

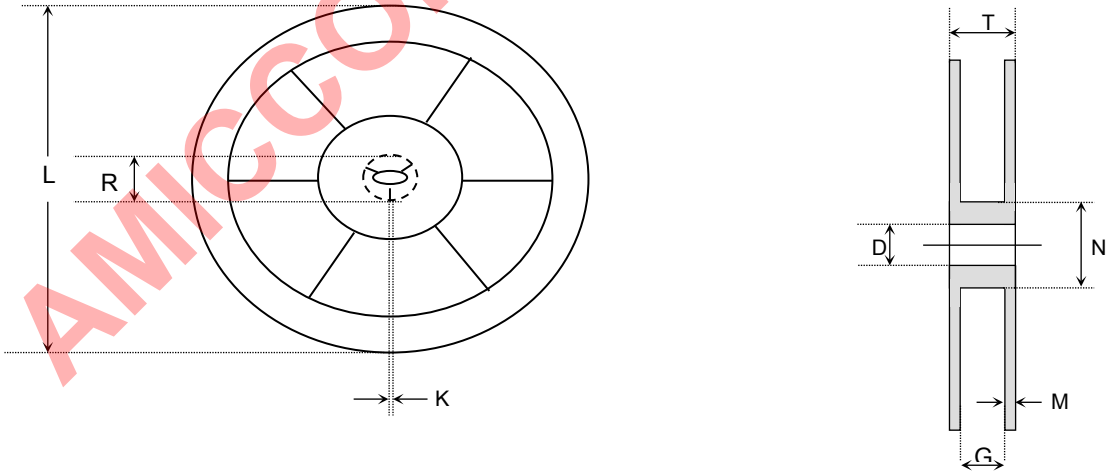
Cover / Carrier Tape Dimension



Unit: mm

TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W	K0	t	Cover tape width
QFN3*3	8±0.1	3.2 5±0.1	3.25 ±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75 ±0.1	5.5 ±0.05	12±0.3	1.25 ±0.1	0.3 ±0.05	9.3±0.1
QFN 4*4	8±0.1	4.35 ±0.1	4.35 ±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75 ±0.1	5.5 ±0.05	12±0.3	1.2 5±0.1	0.3 ±0.05	9.3±0.1
QFN 5*5	8±0.1	5.25 ±0.1	5.25 ±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75 ±0.1	5.5 ±0.05	12±0.3	1.25 ±0.1	0.3 ±0.05	9.3±0.1
QFN 6*6	12±0.1	6.3±0.1	6.3±0.1	4±0.2	2±0.1	1.5±0.1	1.5±0.5	1.75 ±0.1	7.5 ±0.1	16±0.3	1.15 ±0.2	0.3 ±0.05	13.3±0.1

REEL DIMENSIONS



Unit: mm

TYPE	G	N	M	D	K	L	R
QFN3*3/4*4/5*5	12.9±0.5	102 REF±2.0	2.3±0.2	13.15±0.35	2.0±0.5	330±3.0	19.6±2.9
QFN6*6	17±0.5	102 REF±2.0	2.3±0.2	13.15±0.35	2.0±0.5	330±3.0	19.6±2.9

29. Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only.

RF ICs AMICCOM

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