AiT Semiconductor Inc.

DESCRIPTION

The A7463 series is a monolithic control circuit containing the primary functions required for DC-DC converters.

These devices of consist internal an temperature-compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in step-down and step-up and voltage-inverting applications with minimum а number of external components.

The A7463 is available in SOP8 and DIP8 packages.

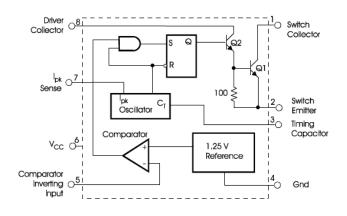
ORDERING INFORMATION

Package Type	Part Number		
SOP8	M8	A7463M8R	
		A7463M8VR	
DIP8	P8	A7463P8U	
		A7463P8VU	
	V: Halogen free Package R: Tape & Reel		
Note			
	U: Tube		
AiT provides all RoHS products			
Suffix " V " means Halogen free Package			

FEATURES

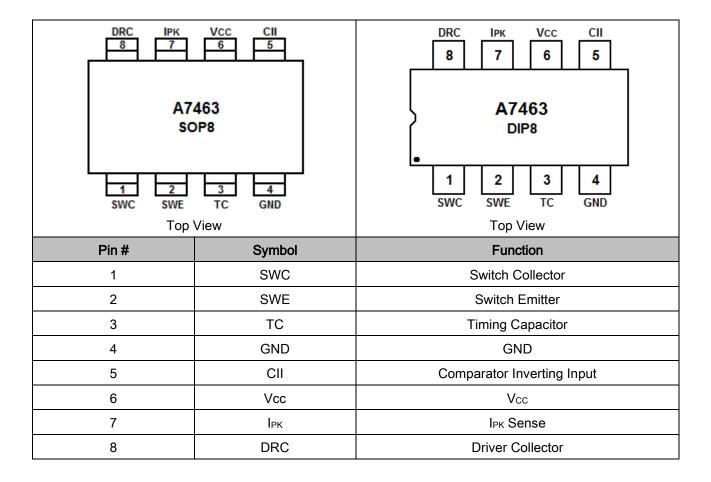
- Operation from 3.0V to 40V input
- Low standby current
- Current limiting
- Output switch current up to 1.5 A
- Adjustable output voltage
- Operation at frequencies up to 100kHz
- Precision Reference (2%)
- Available in SOP8 and DIP8 Packages

TYPICAL APPLICATION





PIN DESCRIPTION





ABSOLUTE MAXIMUM RATINGS

Vcc, Power Supply Voltage	40V _{DC}
V _{IR} , Comparator Input Voltage Range	-0.3 to +40V _{DC}
V _{C(Switch)} , Switch Collector Voltage	40V _{DC}
V _{E(Switch)} , Switch Emitter Voltage (V _{Pin1} =40V)	40V _{DC}
V _{CE(Switch)} , Switch Collector-to-Emitter Voltage	40V _{DC}
V _{C(Driver)} , Driver Collector Voltage	40V _{DC}
I _{C(Driver)} , Driver Collector Current ^{NOTE1}	100mA
I _{Sw} , Switch Current	1.5A
T _J , Operating Junction Temperature	+150°C
T _A , Operating Ambient Temperature Range	-40°C ~ +85°C
T _{STG} , Storage Temperature Range	-65°C ~ + 150°C
ESD	2500V

Stress beyond above listed "Absolute Maximum Ratings" may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. NOTE1: Maximum package power dissipation limits must be observed.



ELECTRICAL CHARACTERISTICS

 $V_{\text{CC}}\text{=}5.0V,\,T_{\text{A}}\text{=}T_{\text{Low}}$ to T_{High} unless otherwise specified

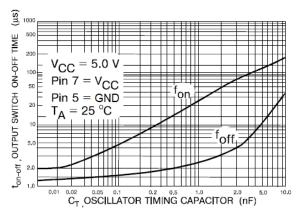
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
OSCILLATOR						
Frequency	f _{osc}	V _{Pin5} =0V, C _T =1.0nF, T _A =25°C	24	33	42	KHz
Charge current	Ichg	V _{CC} =5.0V to 40V, T _A =25°C	24	35	42	μA
Discharge current	I _{dischg}	V _{CC} =5.0V to 40V, T _A =25°C	140	220	260	μA
Discharge-to-charge current ratio	Idischg/Ichg	Pin7 to V _{CC} , T _A =25°C	5.2	6.5	7.5	
Current limit sense voltage	Vlpk(sense)	I _{chg} =I _{dischg} , T _A =25°C	250	300	350	mV
OUTPUT SWITCH NOTE 2				•		
Saturation voltage, Darlington connection	V _{CE(sat)}	I _{Sw} =1.0A, Pins1, 8 connected		1.0	1.3	V
Saturation voltage, Darlington connection	V _{CE(sat)}	I _{Sw} =1.0A, R _{Pin8} =82Ω to V _{CC} , Forced β =20		0.45	0.7	V
DC current gain	h _{FE}	I _{Sw} =1.0A, V _{CE} =5.0, T _A =25°C	50	75		
Collector off-state current	I _{C(off)}	V _{CE} =40V		40	100	μA
COMPARATOR	·					
Threshold voltage	Vth		1.225 1.21	1.25 -	1.275 1.29	V
Threshold voltage line regulation	Regline			1.4	5.0	mV
Input bias current	Іів			-20	-400	nA
TOTAL DEVICE						
Supply current	Icc	V_{CC} =5.0V to 40V, CT=1.0nF, Pin7=V _{CC} , V_{Pin5} >V _{th} , Pin2 =GND, remaining pins - open			4.0	mA

NOTE2: Low duty cycle pulse techniques are used during the test to maintain junction temperature as close to ambient temperature as possible.

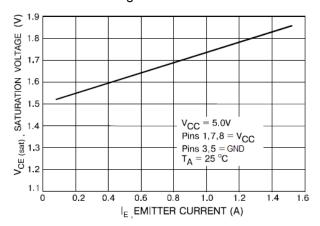


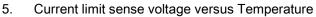
TYPICAL PERFORMANCE CHARACTERISTICS

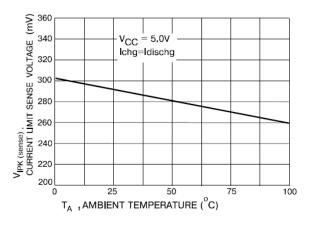
 Output Switch on-off time versus Oscillator timing capacitor



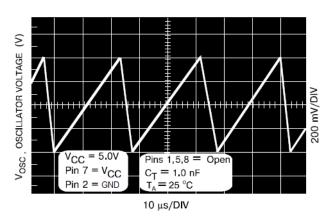
3. Emitter follower configuration output saturation voltage versus Emitter current



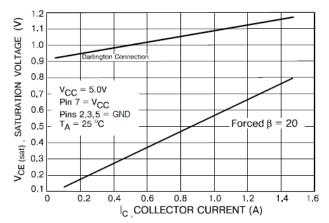




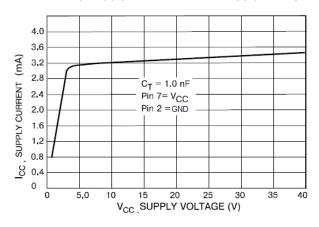
2. Timing capacitor waveform



4. Common emitter configuration output saturation voltage versus Collector current



6. Standby supply current versus Supply voltage

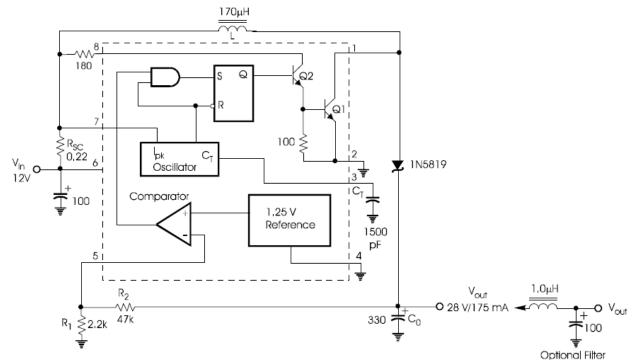




DETAILED INFORMATION

Application Information

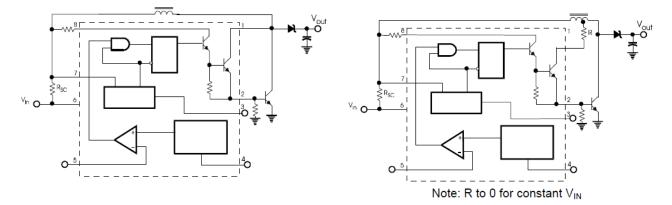
1. Step-up converter



2. External current boost connections for I_{C Peak} greater than 1.5A

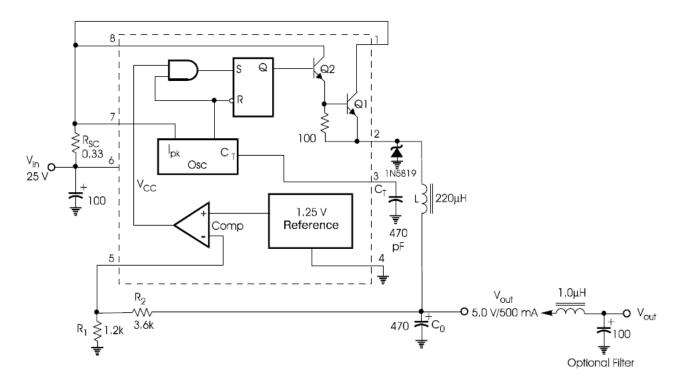
External NPN switch

External NPN saturated switch





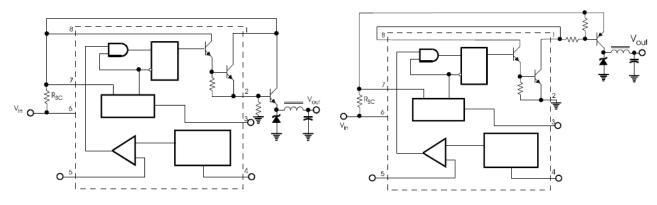
3. Step-down Converter



4. External current boost connections for I_{C Peak} greater than 1.5A

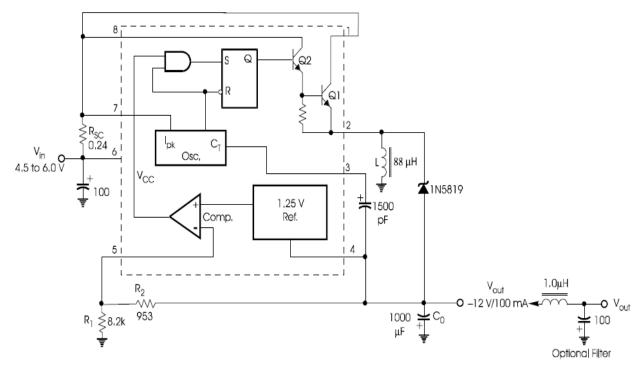
External NPN switch

External PNP saturated switch





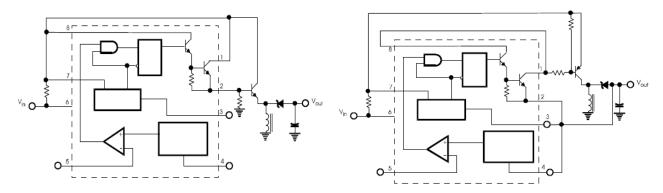
5. Voltage inverting converter



6. External current boost connections for I_{C Peak} greater than 1.5A

External NPN switch

External PNP saturated switch





Design Formula

Calculation	Step-up	Step-down	Voltage-inverting
t _{on}	$\frac{V_{out} + V_F - V_{in(\min)}}{V_{in(\min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(\min)} - V_{sat} - V_{out}}$	$\frac{\left V_{out}\right + V_{F}}{V_{in} + V_{sat}}$
(t _{on} + t _{off}) max	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
Ст	4.0 x 10 ⁻⁵ t _{on}	4.0 x 10 ⁻⁵ t _{on}	4.0 x 10 ⁻⁵ t _{on}
Ipk(switch)	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$	2I _{out(max)}	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
R _{sc}	0.3/I _{pk(Switch)}	0.3/I _{pk(Switch)}	0.3/I _{pk(Switch)}
L(min)	$\left(rac{V_{in(\min)} - V_{sat}}{I_{pk(switch)}} ight) imes t_{on(\max)}$	$\left(\frac{V_{in(\min)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) \times t_{on(\max)}$	$\left(\frac{V_{in(\min)} - V_{sat}}{I_{pk(switch)}}\right) \times t_{on(\max)}$
Co	$9 rac{I_{out}t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9 rac{I_{out}t_{on}}{V_{ripple(pp)}}$

Terms and Definitions

V_{sat} – Saturation voltage of the output switch.

 $V_{f}-$ Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{IN} – Nominal input voltage.

Vout - Desired output voltage,

$$\left|V_{out}\right| = 1.25 \left(1 + \frac{R_2}{R_1}\right)$$

 f_{min} – Minimum desired output switching frequency at the selected values of V_{IN} and $I_{\text{OUT}}.$

 $V_{ripple(p-p)}$ – Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

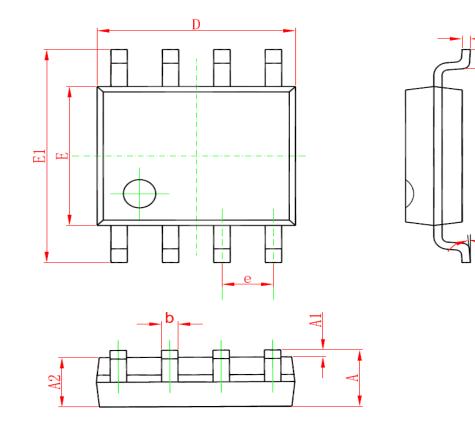


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PACKAGE INFORMATION

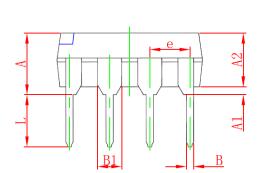
Dimension in SOP8 (Unit: mm)

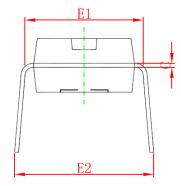


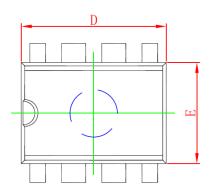
Symbol	Min	Max	
А	1.350	1.750	
A1	0.100	0.250	
A2	1.350	1.550	
b	0.330	0.510	
С	0.170	0.250	
D	4.700	5.100	
Е	3.800	4.000	
E1	5.800	6.200	
е	1.270(BSC)		
L	0.400	1.270	
θ	0°	8°	



Dimension in DIP8 (Unit: mm)







Symbol	Min	Max	
A	3.710	4.310	
A1	0.510		
A2	3.200	3.600	
В	0.380	0.570	
B1	1.524(BSC)		
С	0.204	0.360	
D	9.000	9.400	
E	6.200	6.600	
E1	7.320	7.920	
е	2.540(BSC)		
L	3.000	3.600	
E2	8.400	9.000	



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