Document Title

A7107 Data Sheet, 2.4GHz BLE Tranceiver with DC-DC Converter

Revision History

Rev. No.	History	Issue Date	Remark
0.1	Initial issue.	Aug. , 2011	Preliminary
0.2	Update Ch3, Ch8 and Ch9.	June, 2012	Preliminary
0.3	Update specification	July, 2013	Preliminary

Table of Contents

1. Typical Application

- Wireless keyboard and mice
- Remote Controller
- Sport and Fitness sensors
- BLE watches
- Heath care sensors
- Wireless toys and game controllers

2. General Description

A7107 is a single mode *Bluetooth* low energy (BLE) RF transceiver. With on chip fractional-N synthesizer *and Bluetooth* low energy compliant radio (PHY), A7107can offers an easy and robust way to support *Bluetooth* low energy connectivity of the end applications.

A7107 supports the BLE on-air data rate at 1Mbps with GFSK modulation (optional setting to 2Mbps)for frequency hopping spread sptcturm system (FHSS). A7107 operates in the BLE spectrum range (2402-2480 MHz) for 40 channels with 2MHz channel spacing, instead of classic Bluetooth technology's 79 channels (The BLE protocol is not backward compatible with classic Bluetooth protocol). User can not only use A7107 as a low power radio transport, but also implement the design of the protocol to allow low duty cycles operation. Since the BLE protocol is optimised for small bursts and very low duty cycles (of the order of 0.25%), the overall system average current is therefore in the microamp (μA) range to support battery-powered operations for years.

A7107 is a high performance and low cost 2.4GHz BLE transceiver. This device integrates both high sensitivity receiver (-90dBm @1Mbps/GFSK) and programmable power amplifier (-50 ~ 8dBm). User can configure on-air data rates to either 1Mbps or 2Mbps.

For packet handling, A7107 supports BLE's packet format including a short preamble (8-bits, self-generated), Sync word (32-bits, user definition), PDU header (8bits), PDU Length (8-bits), PDU payload (max. 296-bits) and a CRC (24-bits) adapted in the end of a packet.

For low current consumption, A7107 is integrated with both LDO and DC-DC (buck and boost converter) so that this device can be operated with a wide VDD input range from 0.9V to 3.6V. User can configure one of them (LDO or DC-DC) as a powered source for device operations.

A7107's **control registers** are accessed via 3-wire or 4-wire SPI interface including a BLE packet, RSSI value, frequency hopping to chip calibration procedures. Another one, via SPI as well, is the unique **Strobe command**, A7107 can be controlled from power saving mode (deep sleep, sleep, idle, standby) to PLL mode, TX mode and RX mode. The other connections between A7107 and MCU are GIO1 and GIO2 (multi-function GPIO) to output A7107's status so that MCU could use either polling or interrupt scheme for radio control. Overall, this device is very easy-to-use for developing a wireless application with a MCU. Those functions are very easy to use while developing a wireless system. All features are integrated in a small QFN 5X5 32 pins package.

3. Feature

- Frequency band: 2400 – 2483MHz.
- FSK and GFSK modulation.
- BLE compliant PHY radio unit.
- HW AES128 to support CCM* security.
- VDD input options (0.9V ~ 3.6V)
  - On chip DC-DC boost converter.
  - On chip DC-DC buck converter.
  - On chip LDO regulator.
- High sensitivity: -90dBm at 1Mbps data rate.
- Programmable data rate 1M / 2Mbps.
- Fast settling time synthesizer for frequency hopping system.
- Built-in thermal sensor for monitoring relative temperature.
- Built-in 1 channel 8-bits ADC for external analog voltage (0V ~ 1.2 V).
- 9-bits Digital RSSI for clear channel indication.
- Built-in Low Battery Detector.
- Support low cost crystal (16MHz).
- Support crystal sharing (1 / 2 / 4 / 8MHz) to MCU.
- Easy to use.
  - Support 3-wire or 4-wire SPI.
  - Unique Strobe command via SPI.

- Change frequency channel by ONE register setting.
- Auto RSSI measurement.
- Auto WOR (wake up when receive RX packet).
- Auto Calibrations.
- Auto IF function.
- Auto Frequency Compensation.
- Auto CRC Filtering.
- Support direct mode with recovery clock output to MCU.
- Support FIFO mode with frame sync signal to MCU.

4. PIN Configuration (QFN 5x5 32L)

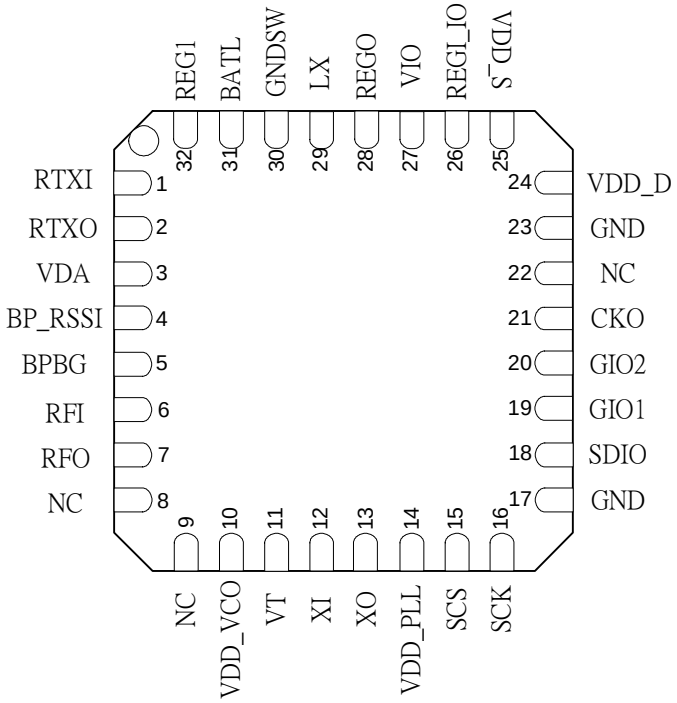


Figure 4.1 A7107 QFN Package Top View

5. PIN Description (I: Input, O: Output, I/O: Input or Output, G: Ground)

Pin No.	Symbol	I/O	Function Description
1	RTXI	I/O	Connection to 32.768Khz RTC Crystal
2	RTXO	O	Connection to 32.768Khz RTC Crystal.
3	VDA	I/O	Regulator output and voltage supply of RF part
4	BP_RSSI	O	External pin connected to bypass capacitor for RSSI reading or input pin for ADC.
5	BPBG	O	Regulator bias point
6	RFI	I	Low noise amplifier input.
7	RFO	O	Power amplifier output.
8	NC	I	No connection
9	NC	I	No connection
10	VDD_VCO	I	Voltage supply for VCO analog part
11	VT	I	VCO frequency control input, internal connected to PLL charge pump.
12	XI	I	Crystal oscillator input node
13	XO	O	Crystal oscillator output node
14	VDD_PLL	I	Voltage supply for PLL part
15	SCS	I	3 wire SPI chip select.
16	SCK	I	3 wire SPI clock input pin.
17	GND	I	Ground
18	SDIO	I/O	3 wire SPI read/write data pin.
19	GIO1	I/O	General purpose I/O pin
20	GIO2	I/O	General purpose I/O pin
21	CKO	O	Clock output pin
22	NC	I	No connection
23	GND	I	Ground
24	VDD_D	I	Supply voltage for digital part.
25	VDD_S	I	Supply voltage for low leage current digital part
26	REGI_IO	I	Supply voltage for I/O interface (ex. SCS, SCK, SDIO, GIO1, GIO2, CKO)
27	VIO	I/O	DC-DC converter voltage input for step up(buck) and output pin for step down (booster)
28	REGO	O	DC-DC regulator output for both step up and step down
29	LX	O	Inductor connection pin
30	GNDSW	I	Ground for dc-dc converter
31	BATL	I	Low battery input for step up dc-dc converter.
32	REGI	I	Linear regulator input.
	Back side plate	G	Ground. Back side plate shall be well-solder to ground to keep good RF performance

6. Block Diagram

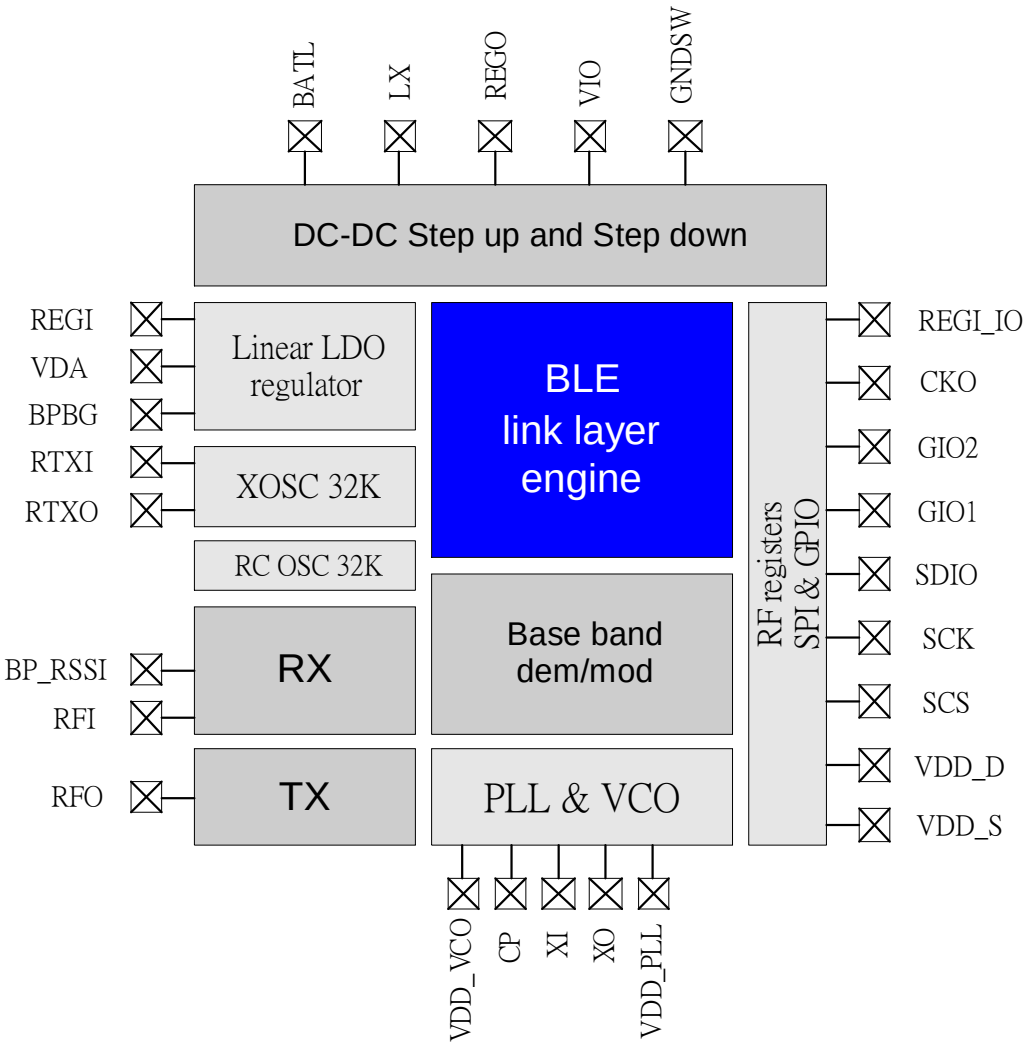


Figure 6.1 Chip Block Diagram

7. Absolution Maximum Rating

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD)	GND	-0.3 ~ 5.0	V
Other I/O pins range	GND	-0.3 ~ VDD+0.3	V
Storage Temperature range		-65 ~ 150	°C
ESD Rating	HBM *	± 2K	V
	MM *	± 100	V

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.

*Device is Moisture Sensitivity Level III (MSL 3).

8. Electrical Specifications

(Ta=25℃, REGI = 3.3V, internal regulator voltage = 1.8V, IF Filter BW = 1.2MHz, unless otherwise noted)

Parameter	Description	Min.	Type	Max.	Unit
General					
Operating Temperature		-40		85	°C
Supply Voltage range	Enable DC-DC boost	0.9		1.5	V
	Enable DC-DC buck	2.7		3.6	V
	Disable DC-DC and Enable LDO	2.0		3.6	V
Current Consumption (LDO mode)	Deep Sleep mode (no data retention)		0.1		µA
	Sleep mode(VDD_D off)		0.9		µA
	Sleep mode(VDD_D off)		2.5		µA
	Standby mode (Xtal OSC. on)		2.4		mA
	PLL mode		8		mA
	RX Mode		15		mA
	TX mode (output power -6dBm)		TBD		mA
	TX mode (output power 2dBm)		16		mA
	TX mode (output power 8dBm)		24		mA
Current Consumption (DC-DC buck) VIO=3.3V	Deep Sleep mode (no data retention)		0.1		µA
	Sleep mode		2.5		µA
	Standby mode (Xtal OSC. on)		1.2		mA
	PLL mode		6		mA
	RX Mode		12		mA
	TX mode (output power -6dBm)		TBD		mA
	TX mode (output power 2dBm)		12.5		mA
	TX mode (output power 8dBm)		TBD		mA
Synthesizer block (includes crystal oscillator, PLL and VCO.)					
Crystal start up time			0.4		ms
Crystal frequency			**16**		MHz
Crystal ESR				100	ohm
VCO Operation Frequency		2400		2483.5	MHz
PLL phase noise (LDO)	Offset 100k Offset 500K Offset 1M Offset 5M		80 100 108 110		dBc/Hz
PLL phase noise (DC-DC buck)	Offset 100k Offset 500K Offset 1M Offset 5M		75 100 105 110		dBc/Hz
PLL settling time			60		µS
TX					
Output power range		-50	0	8	dBm
Out Band Spurious Emission [1]	30MHz~1GHz			-36	dBm
	1GHz~12.75GHz			-30	dBm
	1.8GHz~ 1.9GHz			-47	dBm
	5.15GHz~ 5.3GHz			-47	dBm
Frequency deviation	1Mbps		250K		Hz
	2Mbps		500K		Hz
Data rate			1M	2M	bps
TX settling time			90		µS
RX					

Receiver sensitivity @ BER = 0.1% (LDO)	Data rate 1Mbps (F_{IF} = 1MHz)		-90		dBm
	Data rate 2Mbps (F_{IF} = 2MHz)		-88		dBm
Receiver sensitivity @ BER = 0.1% (DC-DC buck)	Data rate 1Mbps (F_{IF} = 1MHz)		-90		dBm
	Data rate 2Mbps (F_{IF} = 2MHz)		-88		dBm
IF filter bandwidth	Data rate 1Mbps (F_{IF} = 1MHz)		1.2M		Hz
	Data rate 2Mbps (F_{IF} = 2MHz)		2.4M		Hz
IF center frequency	Data rate 1Mbps		1M		Hz
	Data rate 2Mbps		2M		Hz
Interference	Co-Channel (C/I_0)		10		dBc
	1st Adjacent Channel (C/I_1)		3		dBc
	2nd Adjacent Channel (C/I_2)		-30		dBc
	3rd Adjacent Channel (C/I_3)		-31		dBc
	Image (C/I_{IM})		-16		dBc
Maximum Operating Input Power	@RF input (BER=0.1%)			0	dBm
Spurious Emission	30MHz~1GHz			-57	dBm
	1GHz~12.75GHz			-47	
RSSI Range	@RF input	-105		-50	dBm
RX ready time	Standby to RX		110		μS
LDO Regulator					
Regulator settling time	Pin 5 connected to 330pF. (Sleep to idle).		0.5		ms
Band-gap reference voltage			1.22		V
Regulator output voltage		1.79	1.8	2.3	V
DC-DC Boost conveter					
Input voltage range		0.8		1.5	V
Start up voltage		0.9			V
Output voltage		2.0	2.2	2.4	V
Efficiency@batl=1.2V	@ load current = 20mA		86		%
Maximum load current@BATL=1.2V				50	mA
DC-DC Buck conveter					
Input voltage range		2.7		3.6	V
Output voltage		2.0	2.2	2.4	V
Efficiency (with 150ohm load @ 3.0V input.)	Standby mode		91		%
	PWM mode		90		%
Efficiency (with 150ohm load @ 3.6V input.)	Standby mode		89		%
	PWM mode		88		%
Maximum load current				100	mA
Digital IO DC characteristics					
High Level Input Voltage (V_{IH})		0.8*VDD		VDD	V
Low Level Input Voltage (V_{IL})		0		0.2*VDD	V
High Level Output Voltage (V_{OH})	@I_{OH}= -0.5mA	VDD-0.4		VDD	V
Low Level Output Voltage (V_{OL})	@I_{OL}= 0.5mA	0		0.4	V

Note 1: With external RF filter that provides minimum 17dB of attenuation in the band: 30MHz ~ 2GHz and 3GHz ~12.75GHz.

9. Control Register

Address / Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h Mode	W	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN
	R	TX_NEW_DATA	RX_NEW_DATA	CRCF	CER	XER	PLLER	TRSR	TRER
01h Mode control	W	DDPC	ARSSI	AIF	DFCD	WORE	FMT	FMS	ADCM
	R	DDPC	ARSSI	AIF	CD	WORE	FMT	FMS	ADCM
02h Calc	R/W		BLE_PAGE11	BLE_PAGE0	RSSC	VDC	VCC	VBC	FBC
RF Page(BLE_PAGE=0)									
03h FIFO I	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
04h FIFO II	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
05h FIFO Data	R/W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
06h ID Data	R/W	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
07h RC OSC I	W	WOR_SL7	WOR_SL6	WOR_SL5	WOR_SL4	WOR_SL3	WOR_SL2	WOR_SL1	WOR_SL0
	R	RCOC7	RCOC6	RCOC5	RCOC4	RCOC3	RCOC2	RCOC1	RCOC0
08h RC OSC II	W	WOR_SL9	WOR_SL8	WOR_AC5	WOR_AC4	WOR_AC3	WOR_AC2	WOR_AC1	WOR_AC0
	R	NUMLH11	NUMLH10	NUMLH9	NUMLH8	--	RCOC9	RCOC8	ENCAL
09h RC OSC III	W	BBCKS1	BBCKS0	MAN	MCALS	ENCAL	RCOSC_E	TSEL	TWOR_E
	R	NUMLH7	NUMLH6	NUMLH5	NUMLH4	NUMLH3	NUMLH2	NUMLH1	NUMLH0
0Ah CKO Pin	W	ECKOE	CKOS3	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCKI
0Bh GPIO1 Pin I	W	-	-	GIO1S3	GIO1S2	GIO1S1	GIO1S0	GIO1I	GIO1OE
0Ch GPIO2 Pin II	W	-	-	GIO2S3	GIO2S2	GIO2S1	GIO2S0	GIO2I	GIO2OE
0Dh Clock	R/W	GRC3	GRC2	GRC1	GRC0	-	CSC0	CGS	XS
0Eh Data rate	R/W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
0Fh PLL I	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
10h PLL II	R/W	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IP8
11h PLL III	R/W	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
12h PLL IV	W	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8
	R	-	AC14	AC13	AC12	AC11	AC10	AC9	AC8
13h PLL V	W	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
14h TX I	W	GDR	TMDE	TXDI	TME	FS	FDP2	FDP1	FDP0
15h TX II	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
16h Delay I	W	DPR2	DPR1	DPR0	TDL1	TDL0	PDL2	PDL1	PDL0
17h Delay II	W	WSEL2	WSEL1	WSEL0	RSSC_D1	RSSC_D0	RS_DLY2	RS_DLY1	RS_DLY0
18h RX	W	MSCRC	RXSM1	RXSM0	AFC	RXDI	DMG	BWS	ULS
19h RX Gain I	W	AGCE	MIC	IGC1	IGC0	MGC1	MGC0	LGC1	LGC0
	R	-	MICR	IGCR1	IGCR0	MGCR1	MGCR0	LGCR1	LGCR0
1Ah RX Gain II	W	PKIS1	PKIS0	PKT1	PKT0	DCH1	DCH0	RSAGC1	RSAGC0
	R	-	-	-	-	-	-	VTB1	VTB0
1Bh RX Gain III	W	IFPK	VRSEL	MS	MSCL4	MSCL3	MSCL2	MSCL1	MSCL0
	R	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0

1Ch RX Gain IV	W	MXD	HPLS	IWC	MHC1	MHC0	LHC1	LHC0	IFAS
	R	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
1Dh RSSI Threshold	W	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
1Eh ADC	W	RSM1	RSM0	ERSS	FSARS	-	XADS	RSS	CDM
	R	-	-	-	-	-	BOD	BODF	ADC8
1Fh Code I	W	XDS	MCS	WHTS	CRCSW	CRCS	IDL	PML1	PML0
20h Code II	W	ETH2	DCL2	DCL1	DCL0	ETH1	ETH0	PMD1	PMD0
21h Code III	W	PML2	WS6	WS5	WS4	WS3	WS2	WS1	WS0
22h IF Calibration I	W	-	IFBC1	LIMC1	MFBS	MFB3	MFB2	MFB1	MFB0
	R	-	-	-	FBCF	FB3	FB2	FB1	FB0
23h IF Calibration II	R	-	-	-	FCD4	FCD3	FCD2	FCD1	FCD0
	W	PWORS	TRT2	TRT1	TRT0	-	ASMV2	ASMV1	ASMV0
24h VCO current Calibration	W	VCSW	PKS	VCCS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
	R	-	-	-	FVCC	VCB3	VCB2	VCB1	VCB0
25h VCO band Calibration I	W	DCD1	DCD0	DAGS	-	MVBS	MVB2	MVB1	MVB0
	R	-	-	-	-	VBCF	VB2	VB1	VB0
26h VCO band Calibration II	W	DAMV1	DAMV0	VTH2	VTH1	VTH0	VTL2	VTL1	VTL0
27h Battery detect	W	RGS	RGV1	RGV0	PACTL	BVT2	BVT1	BVT0	BDS
	R	RGS	RGV1	RGV0	BDF	BVT2	BVT1	BVT0	BDS
28h TX test	W	RMP1	RMP0	TXCS	PAC1	PAC0	TBG2	TBG1	TBG0
29h Rx DEM test I	W	DMT	DCM1	DCM0	MLP1	MLP0	SLF2	SLF1	SLF0
2Ah Rx DEM test II	W	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0
2Bh Charge Pump Current I	W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
2Ch Crystal test	W	PRS	QDS	QCLIM	DBD	XCC1	XCC0	XCP1	XCP0
2Dh PLL test	W	MDEN	PMPE	PRIC1	PRIC0	PRRC1	PRRC0	SDPW	NSDO
2Eh VCO test I	W	DEVGD2	DEVGD1	DEVGD0	TLB	TLB	RLB	RLB	VCBS
2Fh VCO test II	W	CHD3	CHD2	CHD1	CHD0	RFT3	RFT2	RFT1	RFT0
30h IFAT	W	BLE_ON	BLCKS	MSBS	--	--	HDR_ON	IFBC0	LIMC0
31h RF test I Page0	W	LBG	RGC1	RGC0	SDMS	OLM	CPCS	CPH	CPS
31h RF test II Page1	W	FGC1	FGC0	CRS2	CRS1	CRS0	SRS2	SRS1	SRS0
	R	FGC1	FGC0	CRS2	CRS1	CRS0	SRS2	SRS1	SRS0
31h RF test III Page2	W		STMP	STM5	STM4	STM3	STM2	STM1	STM0
	R	-	-	STMR5	STMR4	STMR3	STMR2	STMR1	STMR0
31h RF test IV Page3	W	CGC	DVI1	DVI0	FBG4	FBG3	FBG2	FBG1	FBG0
	R	-	-	-	FBGR4	FBGR3	FBGR2	FBGR1	FBGR0
31h RF test V Page4	W	FPS1	FPS0	CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
	R	-	-	CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
31h RF test VI	W	FPS2	MGS	MGV1	MGV0	IWA	DSA	DSB	HBW

Page5	R	-	-	VGCR1	VGCR0	IWA	DSA	DSB	HBW
31h RF test VII Page6	W	VTRB3	VTRB2	VTRB1	VTRB0	VMRB3	VMRB2	VMRB1	VMRB0
32h VCO band Calibration III	W	MDAG7	MDAG6	MDAG5	MDAG4	MDAG3	MDAG2	MDAG1	MDAG0
	R	ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
33h VCO deviation Calibration I	W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
	R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
34h VCO deviation Calibration I|	W	MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
	R	ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
35h VCO deviation Calibration I||	W/R	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
36h ADC Control	W	AVSEL1	AVSEL0	MVSEL1	MVSEL0	RADC	PAGS2	PAGS1	PAGS0
37h WOR CalibrationI Page0	W	MVS1	MVS0	--	--	--	--	--	--
37h WOR CalibrationII Page1	W	-	VMSLOPE	WCKSEL1	WCKSEL0	--	--	--	--
37h WORCalibrationIII Page2	W	TGNUM7	TGNUM6	TGNUM5	TGNUM4	TGNUM3	TGNUM2	TGNUM1	TGNUM0
37h WORCalibrationI V Page3	W					TGNUM11	TGNUM10	TGNUM9	TGNUM8
38h WOT	W	RCTS	RCOT2	SPSS		RXDCS	WAKES	RCOT1	RCOT0
39h Channel Group I	R/W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
3Ah Channel Group II	R/W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
3Bh Charge Pump Current II	W	CPTX3	CPTX2	CPTX1	CPTX0	CPRX3	CPRX2	CPRX1	CPRX0
3Ch VCO modulation Delay	W	DC_SEL	INTPRC	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
3Dh INTC	W	VRPL1	VRPL0	VCOSC5	VCOSC4	VCOSC3	VCOSC2	VCOSC1	VCOSC0
3Eh	W	MS7	MS7	MS7	MS7	MS7	MS7	MS7	MS7
3Fh	W	MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
	R	ICD7	ICD6	ICD5	ICD4	ICD3	ICD2	ICD1	ICD0
BLE_Page1(BLE_PAGE=1) (section 9.3)									
03h PWR	W	ENAV	QDSA	ENDV	QDSD	CELS	SVREF	CELA	PDNS
	R								DTSF
04h MRT1	W	MRCT7	MRCT6	MRCT5	MRCT4	MRCT3	MRCT2	MRCT1	MRCT0
05h MRT2	W	EBOD		REFS	CBG2	CBG1	CBG0	MRCT9	MRCT8
06h ADV_A	W/R	SLAVE_ADDRESS (6 BYTE)							
07h INI_A	W/R	MASTER_ADDRESS (6 BYTE)							
08h ADV	W	TX_TXADD	TX_RXADD	ADV_LEN5	ADV_LEN4	ADV_LEN3	ADV_LEN2	ADV_LEN1	ADV_LEN0

09h ADV2	W			ADV_CH_INTERVAL5	ADV_CH_INTERVAL4	ADV_CH_INTERVAL3	ADV_CH_INTERVAL2	ADV_CH_INTERVAL1	ADV_CH_INTERVAL0
0Ah PDU	W					TX_PDU3	TX_PDU2	TX_PDU1	TX_PDU0
0Bh ADV_TIMER	W	ADV_TIMEOUT_INTERVAL ,ADV_EVENT_INTERVAL, (4 BYTE)							
0Ch ADV_DATA	W	ADV_DATA (0~31 BYTE)							
0Dh SCAN_LEN	W			SCAN_LEN5	SCAN_LEN4	SCAN_LEN3	SCAN_LEN2	SCAN_LEN1	SCAN_LEN0
0Eh SCAN_DATA	W	SCAN_DATA (0~31 BYTE)							
	R	RX_ADV_HEADER(2BYTE)							
0Fh ADV_REPORT0	R	RX_INI_ADDRESS (6 BYTE)							
11h ADV_REPORT1	R	LL_DATA (22 BYTE)							
12h BLE_HW_SET	W	BLE_PD	MD0_TRX	off_sel	SSCA4	SSCA3	SSCA2	SSCA1	SSCA0
13h BLE_CS_SEL	W	-	PREDN2	PREDN1	PREDN0	PREUP2	PREUP1	PREUP0	-
14h BLE_SYN_SEL	W	MRCKS	RNUM1[2 : 0]			RNUM0[2: 0]			SYNCS
15h TX POR	W	adv_ch_sel[1:0]	MPDT[5:0]						
16h TX DLY	W				TX_5DLY4	TX_5DLY3	TX_5DLY2	TX_5DLY1	TX_5DLY0
17h CRC_INI	W	BLE TEST INITIAL CRC VALUE (3 BYTE)							
18h Header	W	TX_HEADER(2BYTE)							
	R	RX_LL_HEADER (2BYTE)							
19h OPCODE	W	LL_TERMIN	LL_BUSY_M	NE_SN_S	NAK_S	SNES	NESN	SN	
	R						NESN	SN	
1Ah EADL	W					RCHC	ENDL[2:0]		
1Bh DC	W	DC_SHIFT[7]	DC_SHIFT[6:0]						
	R	DC value [7:0]							
1Ch BUFUP	W	LATCH BUFFER							
1Dh PDN	W	POWER DOWN INT							
1Eh BLE_CMD	W/R	CON_DIS_S	SLAVE LATENCY ON HW_CLR	WHITE LIST1	WHITE LIST0	ADV_GO HW_CLR,	ADV_DIS HW_CLR	CON_DIS	
1Fh BLE_STATUS	W	MASK_INT 3BYTE							
	R	BLE_STATUS7	BLE_STATUS6	BLE_STATUS5	BLE_STATUS4	BLE_STATUS3	BLE_STATUS2	BLE_STATUS1	BLE_STATUS0
20h TX_FIF0_LEN	W	TX_LLID1	TXLLID0	TX_MD	TXLEN4	TXLEN3	TXLEN2	TXLEN1	TXLEN0
21h RX_FIF0_LEN	R	RX_LLID1	RXLLID0	RX_MD	RXLEN4	RXLEN3	RXLEN2	RXLEN1	RXLEN0
22h TRX_FIFO	W/R	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
23h BLE_GIO	W	PUB1	PUB0	SLPO_CKO	SLPO_GIO2	SLPO_GIO1	BLE_CKOE	BLE_GIO2E	BLE_GIO1E
24h Master ENC Parameter	R	MRAND,MEDIV,SKDM,IVM (22 BYTE)							
25h Slave ENC Parametre	W/R	SKDS,IVS (12 BYTE)							

26h Long_term_key	W	LONG_TERM_KEY (16 BYTE)							
2Ch LTE	W	CLR_TX FIFO	MS_SEL	-	-	LTK_AT			LE_AES HW_CLR
2Dh AES_KEY	W/R	AES_KEY (16 BYTE)							
2Eh AES_DATA_IN	W/R	AES_DATA_IN (16 BYTE)							
2Fh AES_OUT	R	AES_DATA_OUT (16 BYTE)							
31h MAP CMD	W	MAN_TX CCM_ON	MAN_RXCC M_ON	MAN_CC M_TXEN_ GO	MAN_CC M_RXDE _GO		MAN_CCM	MAPUP_ RN	CONUP_ RN
	R					CCM_OK	CCM_FAIL	MAPUPOK	CONUPOK
32h PT	W	MAPUP _Sel	adv_fix_on	CON_PU_T[5:0]					
	R	TX_BUF _FULL	INST_CNT_ MEET						
33h TX_PKT	W	TX_PACKET Number for CCM (4 bytes)							
34h RX_PKT	W	RX_PACKET Number for CCM (4 bytes)							
35h CON_INTERVAL	W	CON_IVL (2 BYTE), WIN_SIZE (1BYTE), WIN_OFF(2BYTES)							
36h MAP_UP_SEL	W	HOP(5BITS), LL_USED_CHANNEL(6BITS), CHM(40 BITS), 7BYTE							
37h CONMAP_MAN	W			Timeout _sel	HOP_ MAN	MAP_ UP_MAN	MAP_MAN	CON_MAN	BLE_UP_ MAN
38h CON EVENT	R	CONNECT_EVENT_COUNT (2BYTE)							
39h ADV MAP	W						ADV_MAP2	ADV_MAP 1	ADV_MAP 0
3Ah RXIVM_M Address 5	W	RX_IVM_M[31:0]							
3Bh PWR2	W	CKO_BLES[1:0]		WATCH_SW[1:0]		MD[1:0]		STA	PWUS
3C PN8	W	RND[7:0]							
BLE_Page2(BLE_PAGE=2) (section 9.3)									
35h FILTER ADDRESS0	W/R	ADD _TYP E	WHITE LIST0 (6BYTE)						
36h FILTER ADDRESS1	W/R	ADD _TYP E	WHITE LIST1 (6BYTE)						
37h FILTER ADDRESS2	W/R	ADD _TYP E	WHITE LIST2 (6BYTE)						
38h FILTER ADDRESS3	W/R	ADD _TYP E	WHITE LIST3 (6BYTE)						
39h FILTER ADDRESS4	W/R	ADD _TYP E	WHITE LIST4 (6BYTE)						

Legend: - = unimplemented

[3Eh],[3Fh]: write reserved for analog

[02h]:0xE0: to close REGOD

9.2 Control register description for Normal Page(BLE_PAGE=0)

9.2.1 Mode Register (Address: 00h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode	R	TX_NEW_DATA	RX_NEW_DATA	CRCF	CER	XER	PLLER	TRSR	TRER
	W	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN
Reset		--	--	--	--	--	--	--	--

RESETN: Write to this register by 0x00 to issue reset command, then it is auto clear

CRCF: CRC flag.
[0]: CRC pass. **[1]:** CRC error.

CER: RF chip enable status.
[0]: RF chip is disabled. **[1]:** RF chip is enabled.

XER: Internal crystal oscillator enabled status.
[0]: Crystal oscillator is disabled. **[1]:** Crystal oscillator is enabled.

PLLE: PLL enabled status.
[0]: PLL is disabled. **[1]:** PLL is enabled.

TRER: TRX state enabled status.
[0]: TRX is disabled. **[1]:** TRX is enabled.

TRSR: TRX Status Register.
[0]: RX state. **[1]:** TX state.
Serviceable if TRER=1 (TRX is enable).
TX_NEW_DATA:
BLE function: **[1]:** the NESN bit differs from transmitSN bit, mean that the last sent Data Chaneel PDU has been ack.
[0]: the NESN bit is the same as transmitSN bit, mean that the last sent Data Chaneel PDU has not been ack and shll be resent.
RX_NEW_DATA:
BLE function: **[1]:** the SN bit is the same as a next-ExpectedSN bit, mean that this is a new data.
[0]: the SN bit differs from next-ExpectedSN bit, mean that this is a resent Data Channel PDU.

9.2.2 Mode Control Register (Address: 01h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode Control I	R	DDPC	ARSSI	AIF	DFCD	WORE	FMT	FMS	ADCM
	W	DDPC	ARSSI	AIF	CD	WORE	FMT	FMS	ADCM
Reset		0	0	0	0	0	0	0	0

DDPC (Direct mode data pin control): Direct mode modem data can be accessed via SDIO pin when this register is enabled.
[0]: Disable. **[1]:** Enable.

ARSSI: Auto RSSI measurement while entering RX mode.
[0]: Disable. **[1]:** Enable.

AIF (Auto IF Offset): RF LO frequency will auto offset one IF frequency while entering RX mode.
[0]: Disable. **[1]:** Enable.

CD / DFCD:
DFCD (Data Filter by CD): The received package will be filtered out if Carrier Detector signal is inactive.
[0]: Disable. **[1]:** Enable.

CD: Carrier detector signal (read only).
[0]: Input power below threshold. **[1]:** Input power above threshold.

WORE: WOR (Wake On RX) Function Enable.
[0]: Disable. **[1]:** Enable.

FMT: Reserved for internal usage only. Shall be set to [0].

FMS: Direct/FIFO mode select.
[0]: Direct mode. **[1]:** FIFO mode.

ADCM: ADC measurement enable (Auto clear when done).
[0]: Disable measurement or measurement finished. **[1]:** Enable measurement.
.

9.2.3 Calibration Control Register (Address: 02h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode Control II	R/W		RESETN BLE_PAGE 1	RESETN BLE_PAGE 0	RSSC	VDC	VCC	VBC	FBC
Reset		0	0	0	0	0	0	0	0

RSSC: RSSI calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

VDC: VCO Deviation calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

VCC: VCO Current calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

VBC: VCO Bank calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

FBC: IF Filter Bank calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

BLE_PAGE[1:0]: Page select for Normal funcrtion or BLE function.
[0]: Normal. **others]**: BLE function

(NOTE): Reset BLE by writing to 0x00 when BLE_PAGE[1:0] = 3.

9.2.4 FIFO Register I (Address: 03h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO I	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
Reset		0	0	1	1	1	1	1	1

FEP [7:0]: FIFO End Pointer for TX FIFO and Rx FIFO.

9.2.5 FIFO Register II (Address: 04h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO II	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
Reset		0	1	0	0	0	0	0	0

FPM [1:0]: FIFO Pointer Margin

PSA [5:0]: Used for Segment FIFO.

9.2.6 FIFO DATA Register (Address: 05h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO DATA	R/W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
Reset		0	0	0	0	0	0	0	0

FIFO [7:0]: TX FIFO / RX FIFO
TX FIFO and RX FIFO share the same address (05h).
TX FIFO and RX FIFO are separated physical 64 Bytes.

9.2.7 ID DATA Register (Address: 06h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID DATA	R/W	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Reset		0	0	0	0	0	0	0	0

ID [7:0]: ID data.
When this address is accessed, ID Data is input or output sequential (ID Byte 0,1, 2 and 3) corresponding to Write or Read.

Refer to section 10.6 for details.

9.2.8 RC OSC Register I (Address: 07h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RC OSC I	R	RCOC7	RCOC6	RCOC5	RCOC4	RCOC3	RCOC2	RCOC1	RCOC0
	W	WOR_SL7	WOR_SL6	WOR_SL5	WOR_SL4	WOR_SL3	WOR_SL2	WOR_SL1	WOR_SL0
Reset		0	0	0	0	0	0	0	0

RCOC [7:0]: Reserved for internal usage (read only).

9.2.9 RC OSC Register II (Address: 08h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RC OSC II	W	WOR_SL9	WOR_SL8	WOR_AC5	WOR_AC4	WOR_AC3	WOR_AC2	WOR_AC1	WOR_AC0
	R	NUMLH11	NUMLH10	NUMLH9	NUMLH8		RCOC9	RCOC8	ENCAL
Reset		0	0	0	0	0	0	0	0

WOR_AC [5:0]: 6-bits WOR Active Timer for WOR and TWOR Function

WOR_SL [9:0]: 10-bits WOR Sleep Timer for WOR and TWOR Function.
WOR_SL [9:0] are located at address (07h) and (08h),

Active period = (WOR_AC+1) x (1/4092).
Sleep period = (WOR_SL+1) x (1/32) x (1/4092).

9.2.10 RC OSC Register III (Address: 09h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RC OSC III	W	BBCKS1	BBCKS0	MAN	MCALS	ENCAL	RCOSC_E	TSEL	TWOR_E
	R	NUMLH7	NUMLH6	NUMLH5	NUMLH4	NUMLH3	NUMLH2	NUMLH1	NUMLH0
Reset		0	0	0	0	0	1	0	1

BBCKS [1:0]: Clock select for internal digital block
[00]: F_{SYCK} / 8. **[01]:** F_{SYCK} / 16. **[10]:** F_{SYCK} / 32. **[11]:** F_{SYCK} / 64.
F_{SYCK} is A7107's System clock, 32 times IF center frequency.

MAN: WOR calibration manual setting select.
[0]: . **[1]:** Manual.

MCALS: WOR ENCAL reset setting.
[0]: reset when WOR CAL is ok. **[1]:** reset by SPI.

ENCAL: WOR calibration enable.
[0]: Disable. **[1]:** Enable.

RCOSC_E: Ring oscillator enalbe for WOR and TWOR function.
[0]: Disable. **[1]:** Enable.

TSEL: Timer Duty select for TWOR function.
[0]: Use WOR_AC. **[1]:** Use WOR_SL.

TWORE: Enable TWOR function.
[0]: WOR mode. **[1]:** TWOR mode.

NUMLH[11:0]: Ring Oscillator calibration value (read only).
NUMLH[11:0] are located at address (08h) and (09h),

9.2.11 CKO Pin Control Register (Address: 0Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKO Pin Control	W	ECKOE	CKOS3	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCKI
Reset		1	0	1	1	1	0	1	0

ECKOE: External Clock Output Enable for CKO pin.
[0]: Disable. **[1]:** Enable.

CKOS [3:0]: CKO pin output select.

[0000]: DCK (TX data clock).
[0001]: RCK (RX recovery clock).
[0010]: FPF (FIFO pointer flag).
[0011]: EOP, EOVBC, EOFBC, EOADC, EOVCC, OKADC, RSSC_OK (Internal usage only).
[0100]: External clock output= F_{SYCK}.
[0101]: External clock output / 2= F_{SYCK} / 2.
[0110]: External clock output / 4= F_{SYCK} / 4.
[0111]: External clock output / 8= F_{SYCK} / 8.
[1000]: WCK.(4Khz)
[1001]: PF8M(8MHz)
[1010]: TMRCK(32Khz)
[1011]: SYCK(8Khz)
[1100]: EOCAL(End of RC calibration)
[1101]: BLE clock
[1110]: 32Khz/625us/10ms clock. (selected by BLE Page 3Bh CKO_BLES[1:0])
[1111]: SPI 4-wire

CKOI: CKO pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

CKOE: CKO pin Output Enable.
[0]: High Z. **[1]:** Enable.

SCKI: SPI clock input invert.
[0]: Non-inverted input. **[1]:** Inverted input.

9.2.12 GIO1 Pin Control Register I (Address: 0Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GIO1 Pin Control I	W	--	--	GIO1S3	GIO1S2	GIO1S1	GIO1S0	GIO1I	GIO1OE
Reset		--	--	0	0	0	0	0	1

GIO1S [3:0]: GIO1 pin function select.

GIO1S [3:0]	TX state	RX state
[0000]	WTR (Wait until TX or RX finished)	
[0001]	EOAC (end of access code)	FSYNC (frame sync)
[0010]	TMEOorTMDEO (TX modulation enable)	CD (carrier detect)
[0011]	Preamble Detect Output (PMDO)	
[0100]	MCU wakeup signal (TWOR)	
[0101]	In phase demodulator input (DMII)	
[0110]	SDO (4 wires SPI data out)	
[0111]	TRXD In/Out (Direct mode)	
[1000]	RXD (Direct mode)	
[1001]	TXD (Direct mode)	
[1010]	In phase demodulator external input (EXDI0)	
[1011]	External FSYNC input in RX direct mode	
[1100]	INC	
[1101]	PDN_RX	
[1110]	MCU_INT (read BLE_Page 1Fh for BLE status)	
[1111]	SWNL/DSTL/IPNL/BOD (selected by BLE Page 3Bh WATCH_SW[1:0])	

GIO1I: GIO1 pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

GIO1OE: GIO1pin output enable.
[0]: High Z. **[1]:** Enable.

9.2.13 GIO2 Pin Control Register II (Address: 0Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GIO2 Pin Control II	W	--	--	GIO2S3	GIO2S2	GIO2S1	GIO2S0	GIO2I	GIO2OE
Reset		--	--	0	1	0	0	0	1

GIO2S [3:0]: GIO2 pin function select.

GIO2S	TX state	RX state
[0000]	WTR (Wait until TX or RX finished)	
[0001]	EOAC (end of access code)	FSYNC (frame sync)
[0010]	TMEO or TMDEO (TX modulation enable)	CD (carrier detect)
[0011]	Preamble Detect Output (PMDO)	
[0100]	MCU wakeup signal (TWOR)	
[0101]	Quadrature phase demodulator input (DMIQ)	
[0110]	SDO (4 wires SPI data out)	
[0111]	TRXD In/Out (Direct mode)	
[1000]	RXD (Direct mode)	
[1001]	TXD (Direct mode)	
[1010]	Quadrature phase demodulator external input (EXDI1)	
[1011]	External FSYNC input in RX direct mode	
[1100]	DEC	
[1101]	PDN_TX	
[1110]	MCU_INT (read BLE_Page 1Fh for BLE status)	
[1111]	SWNL/DSTL/IPNL/BOD, for internal testing (selected by BLE Page 3Bh WATCH_SW[1:0])	

GIO2I: GIO2 pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

GIO2OE: GIO2 pin Output Enable.
[0]: High Z. **[1]:** Enable.

9.2.14 Clock Register (Address: 0Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Clock	R/W	GRC3	GRC2	GRC1	GRC0	-	CSC	CGS	XS
Reset		1	1	1	1	-	1	0	1

GRC [3:0]: Clock generation reference counter. Recommend GRC = [0111] for 16MHz Xtal.
GRC [3:0] is used as a clock divider to result a 2MHz clock for the internal CLK Generator when CGS = 1.
F_{XTAL} x (DBL+1) / (GRC+1) = 2MHz.

CSC: system clock FSYCK divider select.
[00]: F_{CSCK} / 1. **[01]:** F_{CSCK} / 2.

CGS: Clock Generator enable.
[0]: Disable. **[1]:** Enable.

XS: Crystal oscillator select.
[0]: Use external clock. **[1]:** Use external crystal.

9.2.15 Data Rate Register (Address: 0Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data Rate	R/W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
Reset		0	0	0	0	0	0	0	0

SDR [7:0]: Data rate division selection.
Data rate = **F_{SYCK}** / (32*(SDR [7:0]+1)). Refer to chapter 13 for details.

9.2.16 PLL Register I (Address: 0Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL I	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
Reset		0	0	0	0	0	0	0	0

CHN [7:0]: LO channel number select.
Refer to chapter 12 for details.

9.2.17 PLL Register II (Address: 10h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

PLL II	R	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IP8
	W	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	BIP8
Reset		1	0	0	1	1	1	1	0

DBL: Crystal frequency doublers selection.
[0]: Disable. $F_{XREF} = F_{XTAL}$.
[1]: Enable. $F_{XREF} = 2 * F_{XTAL}$.
Please refer to A7107 reference code for details.

RRC [1:0]: RF PLL R counter setting. Recommend RRC = [00].
The PLL comparison frequency, $F_{PFD} = F_{CRYSTAL} *(DBL+1) / (RRC+1)$.

CHR [3:0]: PLL channel step setting.
Please refer to chapter 12 and A7107 reference code for details.

9.2.18 PLL Register III (Address: 11h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL III	R	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
	W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
Reset		0	1	0	0	1	0	1	1

BIP [8:0]: LO base frequency integer part setting.
BIP [8:0] are located at address (10h) and (11h),
Please refer to chapter 14 and A7107 reference code for details.

IP [8:0]: LO frequency integer part value (read only).
IP [8:0] are located at address (10h) and (11h),
Refer to chapter 12 for details.

9.2.19 PLL Register IV (Address: 12h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL IV	R	SYNC/FP15	AC14/FP14	AC13/FP13	AC12/P12	AC11/ FP11	AC10/FP10	AC9/FP9	AC8/FP8
	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
Reset		0	0	0	0	0	0	0	0

9.2.20 PLL Register V (Address: 13h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL V	R	AC7/FP7	AC6/FP6	AC5/FP5	AC4/FP4	AC3/FP3	AC2/FP2	AC1/FP1	AC0/FP0
	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
Reset		0	0	0	0	0	0	1	1

BFP [15:0]: LO base frequency fractional part setting.
BFP [15:0] are located at address (12h) and (13h).
Please refer to chapter 12 and A7107 reference code for details.
SYNC: sync word ok.

AC [14:0]: Auto Frequency compensation value if AFC =1.

AFC (18h)	PLL V (read only)	Note
AFC = 1	AC [14:0]	LO Freq. compensation value
AFC = 0	BFP [15:0]	LO frequency fractional part value

9.2.21 TX Register I (Address: 14h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX I	W	GDR	TMDE	TXDI	TME	FS	FDP2	FDP1	FDP0
Reset		0	1	0	1	0	1	1	0

GDR: Gaussian Filter Over Sampling Rate Select.
[0]: BT= 1 **[1]:** BT= 0.5

TMDE: TX Modulation Enable for VCO Modulation.
[0]: disable. **[1]:** enable.

TXDI: TX data invert. Recommend TXDI = [0].
[0]: Non-invert. **[1]:** Invert.

TME: TX modulation enable.
[0]: Disable. **[1]:** Enable.

FS: Filter select.
The Gaussian filter shape is change from (BT = 0.5) to (BT=1).
[0]: disable. **[1]:** enable.

FDP [2:0]: Frequency deviation power setting.
Please refer to chapter 12 and A7107 reference code for details.

9.2.22 TX Register II (Address: 15h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX II	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Reset		0	0	1	0	1	1	1	1

FD [7:0]: Frequency deviation setting.
$F_{DEV} = (F_{PFD} / 2^{16}) \times FD[7:0] \times 2^{(FDP-1)}$.
Where $F_{PFD} = F_{XTAL} * (DBL+1) / (RRC [1:0]+1)$, PLL comparison frequency.

For crystal freuqnecy= 16Mhz, the data rate 1Mbps deviation setting see blow

Data Rate	FDP[2:0]	FD[7:0]	Fdev
1Mbps	6	64	250 Khz

9.2.23 Delay Register I (Address: 16h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Delay	W	DPR2	DPR1	DPR0	TDL1	TDL0	PDL2	PDL1	PDL0
Reset		0	0	0	1	0	0	1	0

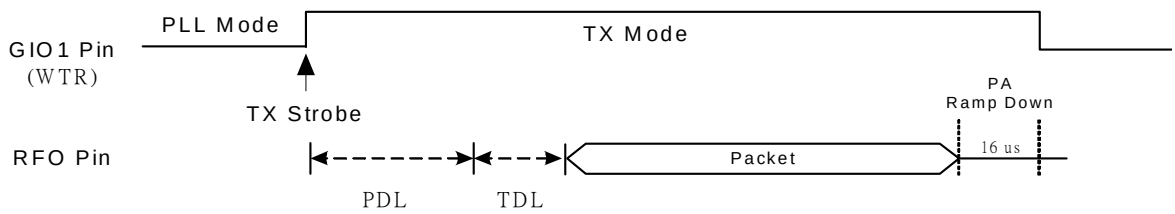
DPR [2:0]: Delay scale. Recommend DPR = [000].

TDL [1:0]: Delay for TX settling from WPLL to TX.
TDL Delay= 20 * (TDL [1:0]+1)*(DPR [2:0]+1) us.

DPR [2:0]	TDL [1:0]	WPLL to TX	Note
000	00	20 us	
000	01	40 us	
000	10	60 us	
000	11	80 us	

PDL [2:0]: Delay for TX settling from PLL to WPLL.
PDL Delay= {20 * (PDL [2:0]+1)*(DPR [2:0]+1)} us.

DPR [2:0]	PDL [2:0]	PLL to WPLL (LO freq changed)	Note
000	000	20 us	
000	001	40 us	
000	010	60 us	
000	011	80 us	
000	100	100 us	



9.2.24 Delay Register II (Address: 17h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Delay	W	WSEL2	WSEL1	WSEL0	RSSC_D1	RSSC_D0	RS_DLY2	RS_DLY1	RS_DLY0
Reset		0	1	0	0	0	0	0	1

WSEL [2:0]: XTAL settling delay setting (200us ~ 2.5ms). Recommend WSEL = [010].
[000]: 200us. **[001]:** 400us. **[010]:** 600us. **[011]:** 800us.
[100]: 1ms. **[101]:** 1.5ms. **[110]:** 2ms. **[111]:** 2.5ms.

RSSC_D [1:0]: RSSI calibration switching time (10us ~ 40us). Recommend RSSC_D = [00].
[00]: 10us. **[01]:** 20us. **[10]:** 30us. **[11]:** 40us.

RS_DLY [2:0]: RSSI measurement delay (10us ~ 80us). Recommend RS_DLY = [001].
[000]: 10us. **[001]:** 20us. **[010]:** 30us. **[011]:** 40us.
[100]: 50us. **[101]:** 60us. **[110]:** 70us. **[111]:** 80us.

9.2.25 RX Register (Address: 18h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX	W	MSCRC	RXSM1	RXSM0	AFC	RXDI	DMG	BWS	ULS
Reset		0	1	0	0	0	0	1	0

MSCRC: Mask CRC (CRC Data Filtering Enable).
[0]: Disable. **[1]:** Enable.

RXSM[1:0]: recommend set = [01] for GFSK demodulation.

AFC: Auto Frequency compensation function.
[0]: Manual setting compensated value. **[1]:** Auto compensation.

RXDI: RX data output invert. Recommend RXDI = [0].
[0]: Non-inverted output. **[1]:** Inverted output.

DMG: Reserved for internal usage only. Shall be set to [0].

BWS: IF center frequency select, Recommand BWS=0 for 1Mhz data rate.

[0]: 1Mhz.

[1]: 2Mhz.

ULS: RX Up/Low side band select. Recommend ULS = [0].
[0]: Up side band, **[1]:** Low side band.
Refer to section 12.2 for details.

9.2.26 RX Gain Register I (Address: 19h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX Gain I	W	AGCE	MIC	IGC1	IGC0	MGC1	MGC0	LGC1	LGC0
	R	-	MICR	IGCR1	IGCR0	MGCR1	MGCR0	LGCR1	LGCR0
Reset		0	1	1	1	1	1	1	1

AGCE: Auto Front end Gain Control Select.
[0]: Disable. **[1]:** Enable.

MIC: Mixer buffer gain setting.
[0]: 0dB. **[1]:** 6dB.

IGC [1:0]: IFA gain Select.
[00]: 18dB. **[01]:** 6dB. **[10]:** 12dB. **[11]:** 18dB.

MGC [1:0]: Mixer Gain select.
[00]: 0dB. **[01]:** 6dB. **[10]:** 12dB. **[11]:** 18dB.

LGC [1:0]: LNA Gain select.
[00]: 6dB. **[01]:** 12dB. **[10]:** 18dB. **[11]:** 24dB.

9.2.27 RX Gain Register II (Address: 1Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

RX Gain II	W	PKIS1	PKIS0	PKT1	PKT0	DCH1	DCH0	RSAGC1	RSAGC0
		-	-	-	-	-	-	VTB1	VTB0
Reset		0	0	0	1	0	0	0	0

PKIS[1:0]: AGC Peak Detect Current Select. Recommend PKIS = [20].

PKT[1:0]: VCO Peak Detect Current Select. Recommend PKT = [00].

DCH1: AGC Hold setting.
[0]: set by DCH0. **[1]:** no hold.

DCH0: AGC Hold setting.
[0]: Hold by preamble detects. **[1]:** hold by SYNC Word detects.

RSAGC [1:0]: AGC clock select.
[00]: IF / 8. **[01]:** IF / 4. **[10]:** IF / 2. **[11]:** IF.

VTB[1:0]: AGC Peak Detect voltage (read only).

9.2.28 RX Gain Register III (Address: 1Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX Gain III	W	IFPK	VRSEL	MS	MSCL4	MSCL3	MSCL2	MSCL1	MSCL0
	R	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0
Reset		0	0	0	0	0	0	0	0

IFPK: AGC Amplifier Current Select. Recommend IFPK = [0].

VRSEL: AGC Function select.
[0]: by RSSI AGC. **[1]:** by normal AGC.

MS: AGC Manual scale select.
[0]: by RSSI AGC. **[1]:** by normal AGC.

MS: AGC Manual scale select. Recommend MS = [0].
[0]: By RSSI (RH−RL). **[1]:** By MSCL[4:0].

MSCL[4:0]: AGC Manual Scale setting.

RH [7:0]: RSSI Calibration High Threshold (ready only).

9.2.29 RX Gain Register IV (Address: 1Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX Gain III	W	MXD	HPLS	IWC	MHC1	MHC0	LHC1	LHC0	IFAS
	R	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
Reset		0	0	0	0	1	1	1	0

MXD: Reserved for internal usage only. Shall be set to [0].

HPLS: High Power LNA Gain Select. Recommend HPLS = [0].
[0]: LGC is set to 6dB when in TX Mode. **[1]:** LGC is set to LGM[1:0].

IWC: Reserved for internal usage only. Shall be set to [0].

MHC[1:0]: mixer current select. Shall be set to [10].

LHC[1:0]: LNA current select. Shall be set to [10].

IFAS: Reserved for internal usage only. Recommand IFAS=1.

RL [7:0]: RSSI Calibration Low Threshold (ready only).

9.2.30 RSSI Threshold Register (Address: 1Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSSI Threshold	W	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Reset		1	0	0	1	0	0	0	1

RTH [7:0]: Carrier detect threshold.
Refer to reference code for details.

ADC [8:0]: ADC output value of temperature, RSSI or external voltage measurement (read only).
ADC [8:0] are located at address (1Dh) and (1Eh).
ADC input voltage= 1.2 * ADC [8:0] / 512 V.
Refer to reference code for details.

9.2.31 ADC Control Register (Address: 1Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC Control	W	RSM1	RSM0	ERSS	FSARS	-	XADS	RSS	CDM
	R	-	-	-	-	-	-	-	ADC8
Reset		0	1	0	1	-	0	1	1

RSM [1:0]: RSSI margin = RTH – RTL. Recommend RSM = [11].
[00]: 5. **[01]:** 10. **[10]:** 15. **[11]:** 20.
Refer to reference code for details.
ERSS: end enable for RSSI measurement
[0]: RSSI measurement continues until leave off RX mode.
[1]: RSSI measurement will end when carrier detected and ID code word received.

FSARS: ADC clock select. Recommend FSARS = [0].
[0]: 2MHz. **[1]:** 4MHz.

XADS: ADC input signal select.
[0]: Convert internal temperature or RSS signal. **[1]:** Convert external voltage,

RSS: Temperature/RSSI measurement select.
[0]: Temperature measurement. **[1]:** RSSI or carrier-detect measurement.

CDM: RSSI measurement mode.
[0]: Single mode. **[1]:** Continuous mode.

9.2.32 Code Register I (Address: 1Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Code I	W	XDS	MCS	WHTS	CRCSW	CRCS	IDL	PML1	PML0
Reset		0	0	0	0	0	1	1	1

XDS: VCO Modulation Data Sampling Clock selection.
[0]: 8x oversampling clk. **[1]:** XCPCK clk.

MCS: Manchester Enable.
[0]: Disable. **[1]:** Enable.

WHTS: Data whitening (Data Encryption) select.
[0]: Disable. **[1]:** Enable.

CRCSW: CRC select (BLE_ON=0).
[0]: Select CRC-16, CCITT. **[1]:** Select CRC-24 (BLE).

CRCS: CRC select.
[0]: Disable. **[1]:** Enable.

IDL: ID code length select.
[0]: 2 bytes. **[1]:** 4 bytes.

PML [2:0]: Preamble length select.
PML [2:0] are located at address (1Fh) and (21h).
[000]: 1 byte. **[001]:** 2 bytes. **[010]:** 3 bytes. **[011]:** 4 bytes. **[100]:** 5byts. **[101]**: 6bytes. **[110]:** 7bytes. **[111]:** 8bytes
Refer to reference code for details.

9.2.33 Code Register II (Address: 20h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Code II	W	ETH2	DCL2	DCL1	DCL0	ETH1	ETH0	PMD1	PMD0
Reset		0	1	1	1	0	1	1	1

DCL2: DC Estimation Average Length After Sync word Detected.
[0]: 128 bits. **[1]:** 256 bits.

DCL1: DC Estimation Average and hold mode.
[0]: 32 bits average. **[1]:** 64 bits average.

DCL0: Preamble detect delay since preamble is detected.
[0]: 4 bits for DCL1=0, 8 bits for DCL1=1.
[1]: 8 bits for DCL1=0, 16 bits for DCL1=1.

ETH [2:0]: Sync word error tolerance.
[000]: 0 bit, **[001]:** 1 bit. **[010]:** 2 bit. **[011]:** 3 bit. **[100]:** 4 bit, **[101]:** 5 bit. **[110]:** 6 bit. **[111]:** 7 bit.

PMD [1:0]: Preamble pattern detection length.
[00]: 0bit. **[01]:** 4bits. **[10]:** 8bits. **[11]:** 16bits.

Refer to chapter 16 for details.

9.2.34 Code Register III (Address: 21h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Code III	W	PML2	WS6	WS5	WS4	WS3	WS2	WS1	WS0
Reset		0	0	1	0	1	0	1	0

PML2: Preamble length select. (Refer to 1Fh).

WS [6:0]: Data Whitening seed setting (data encryption key).
The data is whitened by multiplying with PN7.
Please refer to chapter 16 for details.

9.2.35 IF Calibration Register I (Address: 22h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IF Calibration I	R	-	-	-	FBCF	FB3	FB2	FB1	FB0
	W	-	IFBC1	LIMC1	MFBS	MFB3	MFB2	MFB1	MFB0
Reset		0	0	0	0	0	1	1	0

IFBC1: IF BPF current Select. Recommend IFBC1 = [0].

LIMC1: IF limiter current select. Recommand LIMC1 = [0].

MFBS: IF filter calibration value select. Recommend MFBS = [0].
[0]: Auto calibration value. **[1]:** Manual calibration value.

MFB [3:0]: IF filter manual calibration value.

FBCF: IF filter auto calibration flag (read only).
[0]: Pass. **[1]:** Fail.

FB [3:0]: IF filter calibration value (read only).
MFBS= 0: Auto calibration value (AFB),
MFBS= 1: Manual calibration value (MFB).

9.2.36 IF Calibration Register II (Address: 23h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IF Calibration II	R	--	--	--	FCD4	FCD3	FCD2	FCD1	FCD0
	W	PWORS	TRT2	TRT1	TRT0	ASMV2	ASMV1	ASMV0	AMVS
Reset		--	--	--	--	0	0	1	1

PWORS: TX high power setting.
[0]: Disable. **[1]:** Enable.

TRT [2:0]: TX Ramp down discharge current select.

AMSV [2:0]: TX Ramp up/Ramp down Timing Select.
[000]: 4us, **[001]:** 8us. **[010]:** 12us. **[011]:** 16us. **[100]:** 20us, **[101]:** 24us. **[110]:** 28us. **[111]:** 32us.

AMVS: TX Ramp Up Enable.
[0]: Disable. **[1]:** Enable.

FCD [4:0]: IF filter calibration deviation from goal (read only).

9.2.37 VCO current Calibration Register (Address: 24h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO current Calibration	R				FVCC	VCB3	VCB2	VCB1	VCB0
	W	VCSW	PKS	VCCS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
Reset		0	0	0	0	1	0	0	0

VCSW: REGI voltage detect enable.
[0]: Disable. **[1]:** Enable.

PKS: VCO Current Calibration Mode Select. Recommend PKS = [0].

VCCS: Reserved for internal usage only. Shall be set [0].

MVCS: VCO current calibration value select. Recommend MVCS = [0].
[0]: Auto calibration value. **[1]:** Manual calibration value.

VCOC [3:0]: VCO current manual calibration value.

FVCC: VCO current auto calibration flag (read only).
[0]: Pass. **[1]:** Fail.

VCB [3:0]: VCO current calibration value (read only).
MVCS= 0: Auto calibration value (VCB).
MVCS= 1: Manual calibration value (VCOC).

9.2.38 VCO Single band Calibration Register I (Address: 25h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO Single band Calibration I	R	-	-	-	-	VBCF	VB2	VB1	VB0
	W	DCD1	DCD0	DAGS	-	MVBS	MVB2	MVB1	MVB0
Reset		1	1	0	-	0	1	0	0

DCD [1:0]: VCO Deviation Calibration Delay. Recommend DCD = [01].
Delay time = PDL (Delay Register I, 17h) × (DDC[1:0] + 1).

DAGS: DAG Calibration Value Select. Recommend DAGS = [0].
[0]: Auto calibration value. **[1]:** Manual calibration value.

MVBS: VCO bank calibration value select. Recommend MVBS = [0].
[0]: Auto calibration value. **[1]:** Manual calibration value.

MVB [2:0]: VCO band manual calibration value.

VBCF: VCO band auto calibration flag (read only).
[0]: Pass. **[1]:** Fail.

VB [2:0]: VCO bank calibration value (read only).
MVBS= 0: Auto calibration value (AVB).
MVBS= 1: Manual calibration value (MVB).

9.2.39 VCO Single band Calibration Register II (Address: 26h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO Single band Calibration II	W	DAMV1	DAMV0	VTH2	VTH1	VTH0	VTL2	VTL1	VTL0
Reset		1	0	1	1	1	0	1	1

DAMV [1:0]: Demodulator D/A Voltage Range Select. Recommend DAMV = [10].
[00]: 1/32*1.2. **[01]:** 1/16*1.2. **[10]:** 1/8*1.2. **[11]:** 1/4*1.2.

VTH [2:0]: IF AGCpeak detect upper threshold level setting. Recommand VTH=[100]
[000]: 182mV. **[001]:** 218mV. **[010]:** 254mV. **[011]:** 290mV
[100]: 326mV **[101]:** 362mV. **[110]: 398mV**. **[111]:** 434mV
Where VDD_A is on chip analog regulator output voltage

VTL [2:0]: IF AGC lower threshold level setting. Recommand VTL = [01].
[000]: 56mV. **[001]:** 74mV. **[010]:** 92mV. **[011]:** 110mV.

[100]: 128mV. **[101]:** 146mV. **[110]:** 164mV. **[111]:** 182mV

9.2.40 Battery detect Register (Address: 27h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Battery detect	R	RGS	RGV1	RGV0	BDF	BVT2	BVT1	BVT0	BDS
	W	RGS	RGV1	RGV0	PACTL	BVT2	BVT1	BVT0	BD_E
Reset		0	0	0	0	0	1	1	0

RGS: Reserved for internal usage only. Shall be set to [0]

RGV [1:0]: VDD_D and VDD_A voltage setting in non-Sleep mode. Recommend RGV = [01].
[00]: 1.9V. **[01]: 1.8**V. **[10]:** 1.7V. **[11]:** 1.6V.

PACTL: Reserved for internal usage only. Shall be set to [0].

BVT [2:0]: Battery voltage detect threshold.
For REGI voltage and Buck mode battery detect,BATS(reg0x24, b[7])=0 or BATL(pin31)=0
[000]: 1.8V. **[001]: 1.9**V. **[010]:** 2.0V. **[011]:** 2.1V.
[100]: 2.2V. **[101]:** 2.3V. **[110]:** 2.4V. **[111]:** 2.5V.
For booster mode batter detect (BATS=1 and BATL is high)
[000]: 0.75V. **[001]: 0.8**V. **[010]: 0.85**V. **[011]:** 0.9V.
[100]: 0.95V. **[101]:** 1.0V. **[110]:** 1.05V. **[111]:** 1.1V.

BD_E: Battery detect enable.
[0]: Disable. **[1]:** Enable. It will be clear after battery detection done.

BDF: Battery detection flag (read only).
[0]: Battery voltage < BVT [2:0]. **[1]:** Battery voltage ≧ BVT [2:0].

9.2.41 TX test Register (Address: 28h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX test	W	RMP1	RMP0	TXCS	PAC1	PAC0	TBG2	TBG1	TBG0
Reset		0	0	0	1	0	1	1	1

RMP [1:0]: PA ramp up timing scale. Recommend RMP = [00].

TXCS: TX Current Setting. Recommend TXCS = [1].
[0]: lowest current. **[1]:** highest current.

PAC [1:0]: PA Current Setting.

TBG [2:0]: TX Buffer Setting.

Refer to A7107 App. Note for more settings.

9.2.42 Rx DEM test Register I (Address: 29h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rx DEM test I	W	DMT	DCM1	DCM0	MLP1	MLP0	SLF2	SLF1	SLF0
Reset		0	1	1	0	0	1	0	0

DMT: Reserved for internal usage only. Shall be set to [0].

DCM [1:0]: Demodulator DC estimation mode.
[00]: Fix mode (For testing only). DC level is set by DCV [7:0].
[01]: Preamble hold mode. DC level is preamble average value.
[10]: Average and hold mode. DC level is the average value hold about 8 bit data rate later after preamble is detected.
[11]: Payload average mode (For internal usage). DC level is payload data average.

MLP [1:0]: Reserved for internal usage only. Shall be set to [11].

SLF [2:0]: Reserved for internal usage only. Shall be set to [111].

9.2.43 Rx DEM test Register II (Address: 2Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Rx DEM test II	W	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0
Reset		1	0	0	0	0	0	0	0

DCV [7:0]: Demodulator fix mode DC value. Recommend DCV = [0x80].

9.2.44 Charge Pump Current Register (Address: 2Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Charge Pump Current	W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
Reset		1	1	1	1	1	1	1	1

CPM [3:0]: Charge Pump Current Setting for VM loop.
Charge pump current = (CPM + 1) / 16 mA.

CPT [3:0]: Charge Pump Current Setting for VT loop.
Charge pump current = (CPT + 1) / 16 mA.

9.2.45 Crystal test Register (Address: 2Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Crystal test	W	PRS	QDS	QLIM	DBD	XCC1	XCC0	XCP1	XCP0
Reset		0	0	0	0	0	1	0	1

PRS: Limiter amplifier discharge manual select. Recommend PRS =[0].

QDS: Reserved for internal usage only. Shall be set to [0]

QLIM: quick charge select for IF limiter amp.
[0]: Disable. **[1]:** Enable (QLIM fall down delay 10us).

DBD: Reserved for internal usage only. Shall be set to [0].

XCC[1:0]: Crystal current setting. Shall be set to [01].

XCP [1:0]: Crystal regualting couple setting. Shall be set to [01].

9.2.46 PLL test Register (Address: 2Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL test	W	MDEN	PMPE	PRIC1	PRIC0	PRRC1	PRRC0	SDPW	NSDO
Reset		0	1	1	0	1	0	0	0

MDEN : Use for Manual VCO Calibration. Shall be set to [0].

PMPE: Reserved for internal usage only. Shall be set to [1].

PRIC [1:0]: Reserved for internal usage only. Shall be set to [01].

PRRC [1:0]: Reserved for internal usage only. Shall be set to [00].

SDPW: Reserved for internal usage only. Shall be set to [0].

NSDO: Reserved for internal usage only. Shall be set to [1].

9.2.47 VCO test Register I (Address: 2Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO test I	W	DEVGD2	DEVGD1	DEVGD0	TLB1	TLB0	RLB1	RLB0	VCBS
Reset		0	0	0	1	1	0	1	0

DEVGD [2:0]: Sigma Delta Modulator Data Delay Setting. Recommend DEVGD = [000].

TLB [1:0]: Reserved for internal usage only. Shall be set to [11].

RLB [1:0]: Reserved for internal usage only. Shall be set to [00].

VCBS: Reserved for internal usage only. Shall be set to [0].

9.2.48 VCO test Register II (Address: 2Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO test II	W	CHD3	CHD2	CHD1	CHD0	RFT3	RFT2	RFT1	RFT0
Reset		0	1	0	1	0	0	0	0

CHD [3:0]: Channel Frequency Offset for Deviation Calibration.
Offset channel number = +/- (CHD + 1).

RFT [3:0]: RF analog pin configuration for testing. Recommend RFT= [0000].

9.2.49 IFAT Register (Address: 30h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO test II	W	BLE_ON	BLCKS	MSBS			HDR_ON	IFBC0	LIMC0
Reset		1	0	0	0	0	0	1	1

BLE_ON: BLE function enable.
[0]: Disable. **[1]:** Enable.

BLCKS: BLE clock select.
[0]: Ring OSc. clock. **[1]:** CLK Generator divided.

IFBC0: IF BPF current Select. Reserved for internal usage. IFBC0 = [TBD].

LIMC0: IF limiter current select. Reserved for internal usage. LIMC0 = [TBD].

HDR_ON: Normal mode header enable. [1]: enable. **[0]:** disable.

9.2.50 RFT Test Register I(Address: 31h) Page0(36h, PAGS[2:0]=0)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFT1	W		RGC1	RGC0	SDMS	OLM	CPCS	CPH	CPS
Reset			0	1	1	0	1	1	1

RGC [1:0]: Low power band-gap current select. Recommend RGC = [01]

SMDS: Reserved for internal usage only. Shall be set to [1].

OLM : Open Loop Modulation Enable. Shall be set to [0].
[0]: Disable. **[1]:** Enable.

CPCS : Charge Pump Current Select. Shall be set to [0].
[0]: Use CPM for TX, CPT for RX.
[1]: Use CPTX for TX, CPRX for RX.

CPH: Charge Pump High Current. Shall be set to [0].
[0]: Normal. **[1]:** High.

CPS: PLL charge pump enable. Recommend CPS = [1].
[0]: Enable. **[1]:** Disable.

9.2.51 RFT Test Register II(Address: 31h) Page1(36h, PAGS[2:0]=1)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFT2	W	FGC1	FGC0	CRS2	CRS1	CRS0	SRS2	SRS1	SRS0
	R	FGC1	FGC0	CRS2	CRS1	CRS0	SRS2	SRS1	SRS0
Reset		1	1	1	0	0	1	0	0

FGC[1:0]: BPF fine gain control. Reserved for internal usage.

CRS [2:0]: RSSI voltage offset fine trim setting. Reserved for internal usage.

SRS [2:0]: RSSI voltage curve slope fine time setting. Reserved for internal usage.

9.2.52 RFT Test Register III(Address: 31h) Page2(36h, PAGS[2:0]=2)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFT3	W	STS	STMP	STM5	STM4	STM3	STM2	STM1	STM0
	R			STMR5	STMR4	STMR3	STMR2	STMR1	STMR0

Reset		0	0	1	0	0	0	0	0

STS: Reserved for internal usage only. Shall be set to [0].

STMP: Temp voltage ADC reading select.
[0]: 1 scale / degree C. **[1]:** 2 scale/degree C.

STM [5:0]: ADC voltage fine trim setting. Reserved for internal usage.

9.2.53 RFT Test Register IV(Address: 31h) Page3(36h, PAGS[2:0]=3)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFT4	W	CGC	DVI1	DVI0	FBG4	FBG3	FBG2	FBG1	FBG0
	R				FBGR4	FBGR3	FBGR2	FBGR1	FBGR0
Reset		0	0	0	1	0	0	0	0

CGC : Clock Gen. Current select. Reserved for internal usage.

DVI[1:0] : Reserved for internal usage.

FBG [4:0]: Bandgap voltage SPI fine trim setting. Reserved for internal usage.

9.2.54 RFT Test Register V(Address: 31h) Page4(36h, PAGS[2:0]=4)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFT5	W	FPS1	FPS0	CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
	R			CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
Reset		0	0	1	0	0	0	0	0

FPS[2:0]: Gaussian filter BT fine setting.
FPS[2:0] are located at address (31h, page4 and page5).
If GDR=0 (14h),

FPS[2:0]	7	6	5	4	3	2	1	0
BT	1.4	1.3	1.2	1.1	0.75	0.7	0.65	0.6

If GDR=1 (14h).

FPS[2:0]	7	6	5	4	3	2	1	0
BT	0.7	0.65	0.6	0.55	X	X	X	X

CTR [5:0]: ADC voltage SPI fine trim setting. Reserved for internal usage.

9.2.50 RFT Test Register VI(Address: 31h) Page5(36h, PAGS[2:0]=5)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFT6	W	FPS2	MGS	MGV1	MGV0	IWA	DSA	DSB	HBW
	R			VGCR1	VGCR0	IWA	DSA	DSB	HBW
Reset		0	0	0	0	0	0	0	0

FPS2: Gaussian filter BT fine setting. Refer to 31h, page 4.

MGS: IGC Manual setting select.
[0]: Auto. **[1]:** Manual.

MGV[1:0]: IGC Manual setting.

IWA: RXFE new IFAMP path gain

DSA: IFAMP Path select
[0]: ACC in original IFAMP path. **[1]:** ACC in new IFAMP path.

DSB: PDT Path select
[0]: PDT from ACC output. **[1]:** PDT from IFF output.

HBW: IF bandwidth setting.
BWS (18h) and HBW (31h, page 5) are used to select IFBW.

BWS (18h, bit)	HBW (31h, page 5)	IF(MHz)	IFBW

1	1	2000	1200
1	0	2000	2400
0	1	1000	1200
0	0	1000	1200

VGCR[1:0]:PKDET preamp gain (read only).
[00]: 0dB **[01]:** 6dB **[10]:** 12dB **[11]:** 18dB

9.2.50 RFT Test Register VII(Address: 31h) Page6(36h, PAGS[2:0]=6)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFT6	W	VTRB3	VTRB2	VTRB1	VTRB0	VMRB3	VMRB2	VMRB1	VMRB0
Reset		0	0	0	0	0	0	0	0

VTRB[3:0]: VT filter of Resiter tuning. (Each step is 1K ohm.)
[0000]: 0Ω. **[0001]:**1KΩ **[0010]:**2KΩ … **[1111]:**15KΩ

VMRB[3:0]: VM filter of Resiter tuning. (Each step is 1K ohm.)
[0000]: 0Ω. **[0001]:**1KΩ **[0010]:**2KΩ … **[1111]:**15KΩ

9.2.51 VCO Single band Calibration Register I (Address: 32h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO Single band Calibration III	R	ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
	W	DAGM7	DAGM6	DAGM5	DAGM4	DAGM3	DAGM2	DAGM1	DAGM0
Reset		1	0	0	0	0	0	0	0

DAGM [7:0]: DAG Manual Setting Value. Recommend DAGM = [0x80].

ADAG [7:0]: Auto DAG Calibration Value (read only).

9.2.52 VCO deviation Calibration Register I(Address: 33h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO Deviation I	W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
	R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
Reset		0	1	1	1	0	0	0	0

DEVS [3:0]: Deviation Output Scaling. Recommend DEVS = [0011].

DAMR_M: DAMR Manual Enable. Recommend DAMR_M = [0].
[0]: Disable. **[1]:** Enable.

VMTE_M: VMT Manual Enable. Recommend VMTE_M = [0].
[0]: Disable. **[1]:** Enable.

VMS_M: VM Manual Enable. Recommend VMS_M = [0].
[0]: Disable. **[1]:** Enable.

MSEL: VMS, VMTE and DAMR control select. Recommend MSEL = [0].
[0]: Auto control. **[1]:** Manual control.

DEVA [7:0]: Deviation Output Value (read only).
MVDS (34h)= 0: Auto calibration value ((DEVC / 8) × (DEVS + 1)),
MVDS (34h)= 1: Manual calibration value (DEVM [6:0]).

9.2.53 VCO deviation Calibration Register II(Address: 34h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO Deviation II	R	DEVC7	DEVC6	DEVC5	DEVC4	DEVC3	DEVC2	DEVC1	DEVC0
	W	MVDS	DEVM6	DEVM5	DEVM4	DEVM3	DEVM2	DEVM1	DEVM0
Reset		0	0	1	0	1	0	0	0

MVDS: VCO Deviation Calibration Select. Recommend MVDS = [0].
[0]: Auto calibration value. **[1]:** Manual calibration value.

DEVM [6:0]: VCO Deviation Manual Calibration Value.

DEVC [7:0]: VCO Deviation Auto Calibration Value (read only).

9.2.54 VCO deviation Calibration Register III(Address: 35h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO Deviation III	W/R	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
Reset		1	0	0	0	0	0	0	0

VMG [7:0]: VM Center Value for Deviation Calibration. Recommend VMG [7:0] = [0x80].

9.2.55 ADC Control Register II(Address: 36h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCII	W	AVSEL1	AVSEL0	MVSEL1	MVSEL0	RADC	PAGS2	PAGS1	PAGS0
Reset		1	0	1	0	0	0	0	0

AVSEL [1:0]: ADC average times (for Carrier / temeperature sensor / external ADC). Recommend AVSEL = [11].
[00]: No average. **[01]:** Average 2 times. **[10]:** Average 4 times. **[11]:** Average 8 times.

MVSEL [1:0]: ADC average times (for VCO calibration and RSSI). Recommend MVSEL = [11].
[00]: Average 8 times. **[01]:** Average 16 times. **[10]:** Average 32 times. **[11]:** Average 64 times.

RADC: ADC Read Out Average Mode. Recommend RADC = [0].
[0]: by AVSEL.
[1]: by MVSEL.

PAGS[2:0]: Page select for [31h] and [37h]register mapping.

9.2.56 WOR Register I (Address: 37h) Page0(0X36h, PAGS[2:0]=0)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WOR	W	MVS1	MVS0						
Reset		1	1						

MVS[1:0]: WOR calibration moving average setting.
[00]: Average 2 times. **[01]:** Average 4 times. **[10]:** Average 8 times. **[11]:** Average 16 times.

9.2.56 WOR Register II (Address: 37h) Page1(0X36h, PAGS[2:0]=1)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WOR	W		VMSLOPE	WCKSEL1	WCKSEL0				
Reset			0	0	0				

VMSLOPE: Reserved for internal usage.shall set to [0]

WCKSEL[1:0]: Ring Osc. calibration clock select.
[00]: CSCK. **[01]:** CSCK/2 **[10]:** CSCK/4. **[11]:** CSCK/16.

9.2.56 WOR Register III (Address: 37h) Page2(0X36h, PAGS[2:0]=2)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WOR	W	TGNUM7	TGNUM6	TGNUM5	TGNUM4	TGNUM3	TGNUM2	TGNUM1	TGNUM0
Reset		0	0	0	0	0	0	0	0

TGNUM[11:0]: Ring Osc. calibration target number setting.
TGNUM[11:0] are located at address (37h, WOR Register IV) and (37h, WOR Register III).

9.2.56 WOR Register IV (Address: 37h) Page3 (0X36h, PAGS[2:0]=3)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WOR	W					TGNUM11	TGNUM10	TGNUM9	TGNUM8
Reset						0	0	0	0

TGNUM[11:8]: Ring Osc. calibration target number setting (refer to 37h, WOR Register III).

9.2.57 WOT Register (Address: 38h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WOT	W	RCTS	RCOT2	SPSS		RXDCS	WAKES	RCOT1	RCOT0
Reset		0	0	0		0	0	0	1

RCTS: 32Khz source select.
[0]: internal RC oscilator **[1]:** internal 32K crystal oscillator.

RCOT[2:0]: Ring Osc. current select for RC oscillator calibration.
(Bit 6, Bit 1, Bit 0)
[00]: 240nA **[01]:** 280nA **[10]:** 320nA **[11]:** 360nA

SPSS: Mode back select in WOT mode.
[0]: Standby mode. **[1]:**PLL mode.

WAKES: BLE auto power up/down mode select.
[1]: Enable **[0]:**Disable

RXDCS: RX dc average clock setting. Recommend RXDCS=[0]

9.2.58 Channel Group Register I (Address: 39h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHGL	R/W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
Reset		0	0	1	0	1	0	0	0

CHGL [7:0]: PLL channel group low boundary setting for auto-calibration. Recommed CHGL[7:0] = 0x3C.
Refer to A7107 reference code for details.

9.2.59 Channel Group Register II (Address: 3Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHGH	R/W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
Reset		0	1	0	1	0	0	0	0

CHGH [7:0]: PLL channel group high boundary setting for auto-calibration. Recommed CHGH[7:0] = 0x78.
Refer to A7107 reference code for details.
PLL calibration frequency is divided into 3 groups by CHGL and CHGH:

	Channel
Group1	0 ~ CHGL-1
Group2	CHGL ~ CHGH-1
Group3	CHGH ~ 255

Note: Each group needs its own VCO current, bank and deviation calibration. Use the same calibration value for the frequency in the same group.

9.2.60 Charge Pump Current Register II (Address: 3Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPC II	W	CPTX3	CPTX2	CPTX1	CPTX0	CPRX3	CPRX2	CPRX1	CPRX0
Reset		0	0	1	0	0	0	1	0

CPTX [3:0]: Charge Pump Current Setting for TX mode. Recommend CPTX = [0010].
Charge pump current = (CPTX + 1) / 16 mA.

CPRX [3:0]: Charge Pump Current Setting for RX mode. Recommend CPRX = [0010].
Charge pump current = (CPRX + 1) / 16 mA.

9.2.61 VCO Modulation Delay Register (Address: 3Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO Delay	W	DC_SEL	INTPRC	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
Reset		0	0	1	0	1	0	0	0

INTPRC: Internal PLL loop filter resistor and capacitor select.
[0]: disable. **[1]:** enable

DEVFD [2:0]: VCO Modulation Data Delay by 8x over-sampling Clock. Recommend DEVFD = [010].

DEVD [2:0]: VCO Modulation Data Delay by XCPCK Clock. Recommend DEVD = [000].
DC_SEL: Initial DC value select when sync word ok.[0]: DC set by last pattern DC
[1]: DC set by Normal DC value settting by address 0x2A.

9.2.62 Internal Capacitance Register (Address: 3Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTC	W	VRPL1	VRPL0	VCOSC5	VCOSC4	VCOSC3	VCOSC2	VCOSC1	VCOSC0
Reset		0	0	0	0	0	0	0	0

VRPL [1:0]: internal PLL loop filter resistor value select.
[00]: 500 ohm. **[01]:** 666 ohm. **[10]:** 1 K ohm. **[11]:** 2K ohm.

VCOSC [5:0]: select of internal Crystal oscillator capacitor value for both pin "XI" ands "XO".
The capacitor value is about (VCOSC[5]*14.4+ VCOSC [4:0]*0.9) pF

9.2.63 Analog Test Register I (Address: 3Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Analog Test I	W	PDNX	PDNA	PDNS	PWMS	PDNDTL	DVT	STA	PDSY
Reset		-	-	-	-	-	-	-	-

PDNX: enable DC-DC swithing circuit

[1]: enable. **[0]:** disable. When using bypass mode in Buck. REGIO connected with BATH (pin 27,VIO).

PDNA: DC-DC internal analog circuit control.

[1]: enable. **[0]:** disable.

PDNS: DC-DC clock source control.
[1]: enable**, [0]:**disable.

PWMS]: PWM mode select. In buck mode, it can be set to 0 for standby mode.
[1]: enable,PWM mode, **[0]:**disable, standby mode.

PDNDTL: boost mode select.

[1]: booster. **[0]:** buck mode.

PDNDTL: boost mode select.

[1]: booster. **[0]:** buck mode.

DVT: disable synchronous switching in sleep mode.

[1]: disable**. [0]:** enable.

STA: enable to keep pin LX from ringing.

[1]: enable**. [0]:** disable.

PDSY: DC-DC reference voltage select.

[1]: internal reference voltage**. [0]:** low power bandgap reference voltage.

9.2.64 Analog Test Register II (Address: 3Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Analog Test II	W	CT	PU		PDNS_HV	RGE1	RGE0	MFC1	MFC0

	R	ICD7	ICD6	ICD5	ICD4	ICD3	ICD2	ICD1	ICD0
Reset									

CT: Internal low current regulator.enable

[1]: enable.

[0]: disable. IC enter to deep sleep mode, all of internal regulator turn off.

PDNS_HV: digital regulator enable when VDD_D is off. After VDD_D is turn off, PDNS_HV should set to 0.

[1]: enable.

[0]: disable.

RGE[1:0]: DC-DC output voltage select, Recommand set to [01].
[00]:2.1V**, [01]:**2.2V**, [10]:**2.3V**, [11]:**2.4V

MFC[1:0]: DC-DC clock frequency select, Recommand set to [00].

ICD [7:0]: Reserved for internal usage (read only). Total 4 bytes.

9.3 Control Register for BLE(BLE_PAGE=1)

The below Control registers are active when BLE Page [1:0] (02h) = [01]

9.3.1 PWR Register (Address: 03h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWR	W	ENAV	QDSA	ENDV	QDSD	CELS	SVREF	CELA	PDNS
	R								DTSF
Reset		0	1	1	0	0	0	0	1

ENAV: VDA connection with VDD_S. Recommand set to 1.
[1]: connected, **[0]:** disconnected.

QDSA: VDA quick charge, QDSA priority is higher than ENAV, When QDSA=1 and strobe command set to sleep mode, VDA turn off and disconnected to VDD_S.
[1]: enable, **[0]:**disable
[

ENDV: **VDD_D connection with VDD_S. Recommand set to 1.**
[1]: connected, **[0]:** disconnected.

QDSD: **VDD_D quick charge, QDSD priority is higher than ENDV, When QDSD=1 and strobe command set to sleep mode, VDD_D turn off and disconnected to VDD_S.**
[1]: enable, **[0]:**disable

CELS: Reserved for internal usage. Recommend CELS = [0].
SVREF: Reserved for internal usage. Recommend set = [0].

CELA: Reserved for internal usage. Recommend set = [0]
PDNS: Power manager to turn on VDD_D Recommend PDNS = [0] after IC start up.
DTSF: Reserved for internal usage.

9.3.2 MRT1 Register (Address: 04h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MRT1	W	MRCT7	MRCT6	MRCT5	MRCT4	MRCT3	MRCT2	MRCT1	MRCT0
Reset		0	0	0	0	0	0	0	0

MRCT[9:0]: WOR calibration manual setting if MAN (09h) =1.
MRCT[9:0] are located at address (04h, MRT Register I) and (05h, MRT Register II).

9.3.3 MRT2 Register (Address: 05h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MRT2	W	EBOD		REFS	CBG2	CBG1	CBG0	MRCT9	MRCT8

Reset		1	0	0		0	1	0	0

EBOD: Low voltage reset enable.
[1]: enable, **[0]:**disable

REFS: Reserved for internal usage. Recommand REFS=1
CBG[2:0]: Reserved for internal usage. Recommand set to [11]

9.3.4 BLE SALVE ADDRESS Register (Address:06h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADV_A	R	SAdd7	SAdd6	SAdd5	SAdd4	SAdd3	SAdd2	SAdd1	SAdd0
	W	SAdd7	SAdd6	SAdd5	SAdd4	SAdd3	SAdd2	SAdd1	SAdd0
Reset		--	--	--	--	--	--	--	--

Total : 6 BYTE.

SAdd[7:0]: BLE Slave address.

9.3.5 BLE MASTER ADDRESS Register (Address: 07h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INI_A	R	MAdd7	MAdd6	MAdd5	MAdd4	MAdd3	MAdd2	MAdd1	MAdd0
	W	MAdd7	MAdd6	MAdd5	MAdd4	MAdd3	MAdd2	MAdd1	MAdd0
Reset		--	--	--	--	--	--	--	--

Total : 6 BYTE.

MAdd[7:0]: BLE Mater address.

9.3.6 BLE ADV SET0 Register (Address: 08h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADV	W	TX_TXADD	TX_RX_ADD	ADVLEN5	ADVLEN4	ADVLEN3	ADVLEN2	ADVLEN1	ADVLEN0
Reset		--	--	--	--	--	--	--	--

Total : 1 BYTE.

TX TXADD : SLAVE ADDRESS Mode.
[0]: public address. **[1]:** random address.

TX_RXADD : MASTER ADDRESS Mode.
[0]: public address. **[1]:** random address.

ADVLEN [5:0] : Length of ADV DATA.

9.3.7 BLE ADV SET1 Register (Address: 09h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADV2	W	--	--	ADV_CH_INTERVAL5	ADV_CH_INTERVAL4	ADV_CH_INTERVAL3	ADV_CH_INTERVAL2	ADV_CH_INTERVAL1	ADV_CH_INTERVAL0
Reset			--	--	--	--	--	--	--

ADV_CH_IVL[5:0] : Advertising Channel interval set in periods of (0.625/4)msec.

9.3.8 BLE ADV SET2 Register (Address: 0Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDU	W					ADV_PDU3	ADV_PDU2	ADV_PDU1	ADV_PDU0
Reset		--	--	--	--	--	--	--	--

Total : 1 BYTE.

ADV_PDU_TYPE : Advertising PDU Type.
[0000]: ADV_IND. **[0001]:** ADV_DIRECT_IND. **[0010]:**ADV_NONCONN_IND. **[0110]:** ADV_SCAN_IND

9.3.9 BLE ADV SET3 Register (Address: 0Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADV_TIMER	W	ADV_SET 7	ADV_SET 6	ADV_SET 5	ADV_SET 4	ADV_SET 3	ADV_SET 2	ADV_SET 1	ADV_SET 0
Reset		--	--	--	--	--	--	--	--

Total : 4 BYTE.

ADV_SET[31:16] : ADV_TIMEOUT_INTERVAL
Periods of 1 sec.

ADV_SET[15:0] : ADV_EVENT_INTERVAL :
Periods of 625 msec.

9.3.10 BLE ADV DATA Register (Address: 0Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADV_DATA	W	ADV_ DATA 7	ADV_ DATA 6	ADV_ DATA 5	ADV_ DATA 4	ADV_ DATA 3	ADV_ DATA 2	ADV_ DATA 1	ADV_ DATA T0
Reset		--	--	--	--	--	--	--	--

Total 0~31 BYTE.

ADV_DATA : Advertising Data.

9.3.11 BLE SCAN LEN Register (Address: 0Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCAN_LEN	W			SCAN_LE N5	SCAN_LE N4	SCAN_LE N3	SCAN_LE N2	ADVLEN1	SCAN_LE N0
Reset		--	--	--	--	--	--	--	--

Total 1 BYTE.

SCANLEN[5:0] : Length of Scan Data.

9.3.12 BLE SCAN DATA Register (Address: 0Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCAN_DATA	W	SCAN _ DATA 7	SCAN _ DATA 6	SCAN _ DATA 5	SCAN _ DATA 4	SCAN _ DATA 3	SCAN _ DATA 2	SCAN _ DATA 1	SCAN _ DATA T0
	R	RX_ADV_HEADER(2BYTE)							
Reset		--	--	--	--	--	--	--	--

Total 0~31 BYTE.

SCAN_DATA : SCAN Data.
RX_ADV_HEADER(2BYTE): RX header in ADV mode

9.3.12 BLE ADV_REPORT0 Register (Address: 0Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADV_REPORT0	R	RX_INI_ADDRESS							
Reset		--	--	--	--	--	--	--	--

Total 6 BYTE.

ADV_REPORT : MASTER DEVICE ADDRESS.

9.3.13 BLE ADV_REPORT1 Register (Address: 11h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADV_REPORT1	R	LL_DATA (22 BYTE)							
Reset		--	--	--	--	--	--	--	--

Total : 6 BYTE.

LL_DATA(22 BYTE): LL control data in connect state.

CON_EVENT (2 BYTE): CONNECT EVENT INTERVAL. LL_DATA[95:80]
Period Of 1.25ms

LANTENCY (2 BYTE): CONNECT LANTENCY. LL_DATA[111:96]

CON_TIMEOUT (2 BYTE): CONNECT TIMEOUT. LL_DATA[127:112]
Period Of 10ms

9.3.14 BLE HW_SET Register (Address: 12h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BLE HW_SET	W	BLE_PD	MD0_TRX	off_sel	SSCA4	SSCA3	SSCA2	SSCA1	SSCA0
Reset		0	0	0	0	0	0	1	0

Total : 1 BYTE.

BLE_PD: Power down enable.
[0]: disable. **[1]:** enable
MD0_TRX: Reserved for BLE internal setting. Recommend MD0_TRX=[0]

Off_sel: BLE connection RX timing setting. Recommend off_sel=[0]

SSCA [2:0] : Connection window timing offset setting.
Timing shift = 0.625ms * SSCA

9.3.15 BLE CS_SEL Register (Address: 13h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BLE_CS_SEL	W		PREDN2	PREDN1	PREDN0	PREUP2	PREUP1	PREUP0	-
Reset		--	1	0	0	0	1	0	-

Total : 1 BYTE.

PREDN[2:0]: Preamble detect low threshold setting.

PREUP[2:0]: Preamble detect high threshold setting.

9.3.16 BLE SYN_SEL Register (Address: 14h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BLE_SYN_SEL	W	MRCKS	RNUM1_2	RNUM1_1	RNUM1_0	RNUM0_2	RNUM0_1	RNUM0_0	SYNCS
Reset		0	0	0	0	1	0	0	0

Total : 1 BYTE.

MRCKS: Clock Recovery timing setting.Recommand MRCKS=[0]
[0]: reset by sync word ok. [1]: reset by preamble ok..

RNUM1[2:0]: SYNC word clock recovery manual setting.

RNUM0[2:0]: SYNC word clock recovery manual setting.

SYNCS: SYNC word detect select. [1]: sync word. [0]: preamble
[0]: by sync word. **[1]:** by preamble.

9.3.17 TX ramp Register (Address: 15h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX ramp	W	ADV_CH_SEL1	ADV_CH_SEL0	MPDT5	MPDT4	MPDT3	MPDT2	MPDT1	MPDT0
Reset		0	0	1	0	0	0	0	0

Total : 1 BYTE.

MPDT[5:0]: TX ramp up/down scale setting.

ADV_CH_SEL[1:0]: Advertising fix channel setting. [00]: 37. [01]: 38. [1X]: 39. (32h ADV_FIX_ON=1)

9.3.18 TX DLY Register (Address: 16h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX DLY	W				TX_5DLY4	TX_5DLY3	TX_5DLY2	TX_5DLY1	TX_5DLY0
Reset					0	0	0	0	0

Total : 1 BYTE.

TX_5DLY[4:0]: Delay for BLE TX settling.
TX settling = 1* (TX_5DLY [4:0]+1) us.

9.3.19 CRC_INI Register (Address: 17h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRC_INI	W	BLE INITIAL CRC VALUE 3byte							
Reset									

Total : 3 BYTE.

BLE_CRC_INI: CRC-24 initial value setting.

9.3.20 Header Register (Address:18h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Header	W	TX_HEADER 2byte							
Reset	R	RX_LL_HEADER 2byte							

TX_HEADER: TX Header manual setting
RX_HEADER: RX LL control header.

9.3.21 Header Register (Address: 19h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Header	W	LL_TERMIN	LL_BUSY_M	NE_SN_S	NAK_S	SNES	NESN	SN	
	R						NESN	SN	
Reset		0	0	0	0	0	0	0	

LL_TERMIN: LL_TERMIN_IND, Connection T_Terminate Timer Timeout. (connSupervisionTimeout *10ms)

LL_BUSY_M: **LL Control Procedure Response Timeout Timer.**(40sec)

NE_SN_S: **NESN/SN rule select. [1]:** standard rule. **[0]**: NESN/SN=00/11 only . **Recommand NE_SN_S=[1].**

NAK_S: Manual setting for TX transmit old data. **Recommand NAK_S=[0]**

SENS: NESN/SN manual setting select.[1]: using NESN,SN manual setting

NESN: Next Expected Sequencr Number.

SN: Transmit Sequence Number.

9.3.22 EADL Register (Address: 1Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EADL	W					RCHC	ENDL2	ENDL1	ENDL0
Reset		0	0	0	0	0	0	0	0

ENDL[2:0]: ENTI Delayed setting. Reserved for internal usage.
RCHC: Reserved for internal usage.

9.3.23 DC Register (Address: 1Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DC	W	DC_SHIFT[7:0]							

	R	DC_Value							
Reset		1	0	0	0	0	1	0	0

DC_SHIFT: DC average by ID initial dc value shift setting. (NOTE): DC_SHIFT[7] is signed bit.

DC_Value: DC value read

9.3.24 BUF Register (Address: 1Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1Ch BUFUP	W	LATCH BUFFER							

LATCH BUFFER COMMAND: Manula update data to fifo buffer, then TX will transmit old data if resend is needed .Write addr 1Ch

9.3.25 PDN Register (Address: 1Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1Dh PDN	W	POWER DOWN INT							

POWER DOWN INT: Turn off power on interrupt command. Write addr 1Dh

9.3.26 BLE COMMAND Register (Address: 1Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BLE_CMD	W	**CON_DIS_S**	SLAVE LATENCY ON HW_CLR	WHITE LIST1	WHITE LIST0	ADV_GO HW_CLR,	ADV_DIS HW_CLR	CON_DIS	
Reset		0	0	0	0	0	0	0	--

Total : 1 BYTE.

LATENCY ON : LATENCY FUNCTION Enalbe (Hardware Clear).
[0]: disable. **[1]:** enable

FILTER_ON[1:0] : Address Filtering Enable.
[00]: PASS ALL ADDRESS in ADV STATE.
[01]: ONLY PASS ADDRESS IN WHITE LIST.
[10]: SCAN only pass in White List Address , Connect all pass.
[11]: Connect only pass in White List Address , Scan all pass.

ADV_GO : Advertising procedure enable (Hardware Clear).
[0]: disable. **[1]:** enable

ADV_DIS : Advertising procedure disable (Hardware Clear).
[0]: disable. **[1]:** enable

CON_DIS : Terminate procedure enable (Hardware Clear).
[0]: disable. **[1]:** enable

CON_DIS_S : Terminate procedure enable by slave(Hardware Clear).
[0]: disable. **[1]:** enable

9.3.27 BLE STATUS Register (Address: 1Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BLE_STATUS	R	STATUS7	STATUS6	STATUS5	STATUS4	STATUS3	STATUS2	STATUS1	STATUS0
	W	MCU_INT 3BYTE							
Reset		--	--	--	--	--	--	--	--

Total : 1 BYTE.

MCU_INT: BLE interrupt mask setting. Reserved for internal usage. Shall be set to [0x000000].

STATUS [7:0] : Check BLE Status if BLE interrupt occurs (read only).
[0x01]: ADV TIMEOUT.
[0x02]: CONNECT SUCEED.
[0x03]: CHANNEL MAP SUCCED
[0x04]: ADV POWER DOWN
[0x05]: SYNC LOSS(LOSS LINK)
[0x06]: CONNECT POWER UP
[0x07]: EMPTY PACKET TRX .
[0x08]: CONNECT RESEND / CRC ERROR
[0x09]: CONNECT / CHANNEL MAP UPDATE FAIL
[0x0A]: RX DATA RDY
[0x0B]: TX TRANSMIT OK
[0x0C]: CONNECT FAIL(time out)
[0x0D]: LL CONTROL TIMEOUT
[0x0E]: LATENCY OK.
[0x0F]: AES COMMAND OK
[0x10]: CCM OK.
[0x11]: TERMINATE.
[0x12]: START MD BIT
[0x13]: MD BIT END.
[0x14]: CONNECT UPDATE SUCCED
[0x15]: CONNECT FAIL (initial loss link 6 times).
[0x16]: RX NOT NEW DATA

9.3.28 BLE Connect TX Register (Address: 20h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX_FIFO_LEN	W	TXLLID1	TXLLID0	TXMD	TXLEN4	TXLEN3	TXLEN2	TXLEN1	TXLEN0
Reset		0	0	0	0	0	0	0	0

Total : 1 BYTE.

TXLLID[1:0] :
[00]: Reserved.
[01]: LL_DATA_PDU.
[10]: LL_DATA_PDU.
[11]: LL_CONTROL_PDU.

TXMD : TX Data Transfer.
[0]: continus data transfer in one connect interval.
[1]: one data transaction in one connect interval.

TXLEN[4:0]: TX Length select.

9.3.29 BLE Connect RX Register (Address: 21h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_FIFO_LEN	R	RXLLID1	RXLLID0	RXMD	RXLEN4	RXLEN3	RXLEN2	RXLEN1	RXLEN0
Reset		--	--	--	--	--	--	--	--

Total : 1 BYTE.

RXLLID[1:0] :
[00]: Reserved.
[01]: LL_DATA_PDU.
[10]: LL_DATA_PDU.
[11]: LL_CONTROL_PDU.

RXMD : RX Data Transfer.
[0]: continus data transfer in one connect interval.
[1]: one data transaction in one connect interval.

RXLEN[4:0]: RX Length select.

9.3.30 BLE Connect FIFO Register (Address: 22h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

TRX FIFO	R	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
	W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
Reset		--	--	--	--	--	--	--	--

9.3.31 BLE GPIO Register (Address: 23h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BLE_GIO	W	PUB1	PUB0	SLPO_CKO	SLPO_GIO 2	SLPO_GIO 1	BLE_CKOE	BLE_GIO2 E	BLE_GIO1 E
Reset		0	0	0	0	0	1	1	1

PUB[1:0]: Reserved for internal usage

SLPO_CKO: Always on domain CKO pin Output Enable. [1]: Using BLE_CKOE=1: Enable

SLPO_GIO1: Always on domain GPIO1 pin Output Enable. [1]: Using BLE_GIO1E=1: Enable.

SLPO_GIO2: Always on domain GPIO2 pin Output Enable. [1]: Using BLE_GIO2E=1: Enable.

9.3.32 BLE RX_CCM_PARAMETER Register (Address: 24h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master ENC Paramete	R	CCM_P7	CCM_P6	CCM_P5	CCM_P4	CCM_P3	CCM_P2	CCM_P1	CCM_P0
Reset		--	--	--	--	--	--	--	--

Total : 22 BYTE.

RX_CCM_PARAMETER3 (8byte) : RAND

RX_CCM_PARAMETER2 (2byte) : EDIV

RX_CCM_PARAMETER1 (8byte) : SKDM

RX_CCM_PARAMETER0 (4byte) : IVM

9.3.33 BLE TX_CCM_PARAMETER Register (Address: 25h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave ENC Paramete	W/R	CCM_P7	CCM_P6	CCM_P5	CCM_P4	CCM_P3	CCM_P2	CCM_P1	CCM_P0
Reset		--	--	--	--	--	--	--	--

Total : 12 BYTE.

RX_CCM_PARAMETER1 (8byte) : SKDS

RX_CCM_PARAMETER0 (4byte) : IVS

9.3.34 BLE LTK Register (Address: 26h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Long_term_key	W	LTK7	LTK 6	LTK 5	LTK 4	LTK 3	LTK 2	LTK 1	LTK 0
Reset		--	--	--	--	--	--	--	--

Total : 12 BYTE.

LTK: BLE CCM_Long Term Key.

9.3.35 BLE SECURITY Register0 (Address: 2Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LTE	R/W	CLR_TX FIFO	MS_SEL	-	-	LTK_AT			LE_AES HW_CLR
Reset		0	0	--	--	0	--	--	0

Total : 1 BYTE.

AES_GO : DO AES FUNCTION

CLR_TXFIFO:BLE CCM clear TX FIFO data.

MS_SEL: BLE CCM Master/Slave select. [0]: Slave. **[1]:** Master.

LTK_AT: BLE CCM nonce setting select. [0]: manual. **[1]:** Auto.

9.3.36 BLE SECURITY Register1 (Address: 2Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AES_KEY	R/W	AES KEY INPUT							
Reset		--	--	--	--	--	--	--	--

Total : 16 BYTE.

AES_KEY_INPUT : 128 bits AES KEY for CCM* operation.

9.3.37 BLE SECURITY Register2 (Address: 2Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AES_DATA_IN	R/W	AES DATA INPUT							
Reset		--	--	--	--	--	--	--	--

Total : 16 BYTE.

AES_DATA_INPUT : 128 bits AES DATA Input for CCM*operation.

(NOTE): Read AES auto generated KEYData by setting 2Ch LTK_AT=1

9.3.38 BLE SECURITY Register1 (Address: 2Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AES_DATA_OUT	R/W	AES DATA OUTPUT							
Reset		--	--	--	--	--	--	--	--

Total : 16 BYTE.

AES_DATA_OUTPUT : 128 bits AES DATA Output for CCM* operation.

9.3.39 MAP CMD Register (Address: 31h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MAP CMD	W	MAN_TXCCM_ON	MAN_RXCCM_ON	MAN_CCM_TXEN_GO	MAN_CCM_RXDE_GO		MAN_CCM	MAPUP_RN	CONUP_RN
	R					CCM_OK	CCM_FAIL	MAPUPOK	CONUPOK
Reset		0	0	0	0	--	0	0	0

Total : 1 BYTE.

MAPUP_RN : BLE Map reset enable.
[0]: disable. **[1]:** enable.

CONUP_RN : BLE Connection reset enable.
[0]: disable. **[1]:** enable
MAN_CCM: BLE Manual CCM Enable. [1]: Enable. **[0]:** Disable.

MAN_TXCCM_ON: BLE Manaul TX CCM Enable. [1]: Enable. **[0]:** Disable.

MAN_RXCCM_ON: BLE Manaul RX CCM Enable. [1]: Enable. **[0]:** Disable.

MAN_CCM_TXEN_GO: BLE Manual TX Encrypt. [1]: Start. **[0]:** Off.

MAN_CCM_RXDE_GO: BLE Manual RX Decrypt. [1]: Start. **[0]:** Off.

CCM_OK: CCM succed.

CCM_FAIL: CCM fail.

MAPUPOK: Channel map succed.

CONUPOK: Connection update succed.

9.3.40 PT Register (Address: 32h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PT	W	MAPUP_Sel	adv_fix_on	CON_PU_T[5:0]					
	R	TX_BUF_FULL	INST_CNT_MEET						
Reset				0					

Total : 1 BYTE.

CON_PU_T[2:0]: tune power up start time in connection phase for power saving mode
MAPUP_SEL: Channel map instant setting. Shall be set to [0]

ADV_FIX_ON: Advertising fix channel enable.
[0]: disable. **[1]:** enable
TX_BUF_FULL: Indicate TX FIFO is empty or not. [1]: Not Empty. **[0]:** Empty.
INST_CNT_MEET: Indicate if the instant of Channel mapping/Connection update is valid [1]: Valid. **[0]:** Invalid

9.3.41 TX PKT Register (Address: 33h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX PKT	W	TX_PACKET Number for CCM (4 bytes)							
Reset		0							

TX_PKT: BLE CCM TX Packet number. Shall be added by one while TX CCM OK

9.3.42 PKT Register (Address: 34h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX PKT	W	RX_PACKET Number for CCM (4 bytes)							
Reset		0							

RX_PKT: BLE CCM RX Packet number. Shall be added by one while RX CCM OK

9.3.43 CON_INTERVAL Register (Address: 35h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CON_INTERVAL	W	CON_IVL (2 BYTE), WIN_SIZE (1BYTE), WIN_OFF(2BYTES)							
Reset		0							

Manul setting connection parameter when 0x37 CON_MAN=1.

CON_IVL: Connection interval manual setting.

WIN_SIZE: Connection RX window size manual setting.

WIN_OFF: Connection window offset manual setting.

9.3.44 MAP UP Register (Address: 36h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MAP_UP_SEL	W	HOP(5BITS), LL_USED_CHANNEL(6BITS), CHM(40 BITS), 7BYTE							
	R	HOP(5BITS), LL_USED_CHANNEL(6BITS), CHM(40 BITS), 7BYTE							
Reset		0							

Manul setting channel parameter when 0x37 MAP_MAN=1.

LL_USED_CHANNEL: LL Channel used number manual setting.
CHM: LL used channel table manual setting.
HOP: LL Channel hopping manual setting when 0x37 HOP_MAN=1.

9.3.45 CONMAP MAN Register (Address: 37h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

CONMAP_MAN	W			Timeout_sel	HOP_MAN	MAP_UP_MAN	MAP_MAN	CON_MAN	BLE_UP_MAN
Reset		--	--	--	--	--	--	--	--

Timeout_sel: BLE timeout interrupt (ADV/CON) interval select. [0]:10ms. **[1]:** 0.625ms.

HOP_MAN: LL Channel hopping manual setting select. [1]: Manual. **[0]:** Auto

MAP_MAN: LL used channel/channel used number manual setting select. [1]: Manual. **[0]:** Auto

CON_MAN:LL Connection update parameter manaul setting select. [1]: Manual. **[0]:** Auto

BLE_UP_MAN: Manual Connection update/Channel map select. [1]: Manual update. **[0]:** Auto update

MAP_UP_MAN: Manual Channel map enable. [1]: Enable. (BLE_UP_MAN=1)

9.3.46 CON EVENT Register (Address: 38h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CON EVENT	R	CONNECT_EVENT_COUNT (2BYTE)							
Reset		--							

CONNECT_EVENT_COUNT: BLE Connection event count.

9.3.47 ADV MAP Register (Address: 39h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADV MAP	W						ADV_MAP2	ADV_MAP1	ADV_MAP0
Reset							1	1	1

ADV_MAP[2:0]: ADV used channel select.
ADV_MAP[0]=1: use BLE channel 37
ADV_MAP[1]=1: use BLE channel 38.
ADV_MAP[2]=1: use BLE channel 39.

9.3.48 RXIVM_M Register (Address: 3Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RXIVM_M	W	RX_IVM_M[31:0]							
Reset		0							

Total: 4 BYTE
RX_IVM_M: BLE CCM NONCE Manual setting when 2Ch LTK_AT=0.

9.3.49 PWR2 Register (Address: 3Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3Bh PWR2	W	CKO_BLES[1:0]		WATCH_SW[1:0]		MD[1:0]		STA	PWUS
Reset		0		0		0		0	1

CKO_BLES[1:0]: CKO Pin output select when BLE_PAGE0 0Ah CKOS[3:0]=[1110] or BLE_PAGE1 23h SLPO_cko=1.
[00]:32KHz. **[01]:**0.625ms. **[1x]:** 10ms
WATCH_SW[1:0]: GPIO Pin output select for internal usage when BLE_PAGE0 0Bh GIO1S[3:0], 0Ch GIO2S[3:0] = [1111]. [00]: SWNL **[01]:**DSTL **[10]:**IPNL.**[11]:**BOD.

MD[0]: PWM bias current setting. Recommand set to [0].
MD[1]: Reserved for internal usage
STA: Reserved for internal usage
PWUS:. Power control for REGOD setting. Shall be set to PWUS=[1]

9.3.50 PN8 Register (Address: 3Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PN8	W	RND[7:0]							
Reset		8							

RND[7:0]: Peusdo random code initial value for ADV interval setting.

9.4 Control Register for BLE(BLE_PAGE=2)

The below Control registers are active when BLE Page [1:0] (02h) = [10]

9.4.1 BLE WHITE0 Register (Address: 35h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FILTER ADDRESS0	R	White7	White6	White5	White4	White3	White2	White1	White0
	W	White7	White6	White5	White4	White3	White2	White1	White0
Reset		--	--	--	--	--	--	--	--

Total : 6 BYTE Address + 1BIT Adress Type

WHITE0 : Filter device address.

ADDRESS_TYPE0: Advertiser address type. [0]: Public **.[1]:**Random.

9.4.2 BLE WHITE1 Register (Address: 36h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FILTER ADDRESS1	R	White7	White6	White5	White4	White3	White2	White1	White0
	W	White7	White6	White5	White4	White3	White2	White1	White0
Reset		--	--	--	--	--	--	--	--

Total : 6 BYTE Address + 1BIT Adress Type

WHITE1 : Filter device address.

ADDRESS_TYPE1: Advertiser address type. [0]: Public **.[1]:**Random.

9.4.3 BLE WHITE2 Register (Address: 37h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FILTER ADDRESS2	R	White7	White6	White5	White4	White3	White2	White1	White0
	W	White7	White6	White5	White4	White3	White2	White1	White0
Reset		--	--	--	--	--	--	--	--

Total : 6 BYTE Address + 1BIT Adress Type

WHITE2 : Filter device address.

ADDRESS_TYPE2: Advertiser address type. [0]: Public **.[1]:**Random.

9.4.4 BLE WHITE3 Register (Address: 38h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FILTER ADDRESS3	R	White7	White6	White5	White4	White3	White2	White1	White0
	W	White7	White6	White5	White4	White3	White2	White1	White0
Reset		--	--	--	--	--	--	--	--

Total : 6 BYTE Address + 1BIT Adress Type

WHITE3 : Filter device address.

ADDRESS_TYPE3: Advertiser address type. [0]: Public **.[1]:**Random.

9.4.5 BLE WHITE4 Register (Address: 39h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FILTER ADDRESS4	R	White7	White6	White5	White4	White3	White2	White1	White0
	W	White7	White6	White5	White4	White3	White2	White1	White0
Reset		--	--	--	--	--	--	--	--

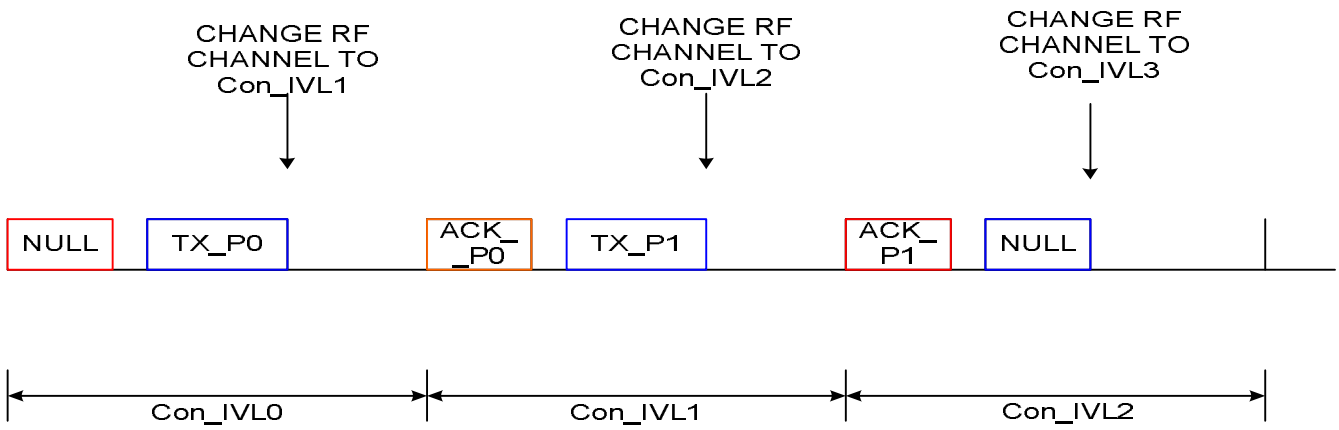
Total : 6 BYTE Address + 1BIT Adress Type

WHITE4 : Filter device address.

ADDRESS_TYPE4: Advertiser address type. [0]:Public .[1]:Random.

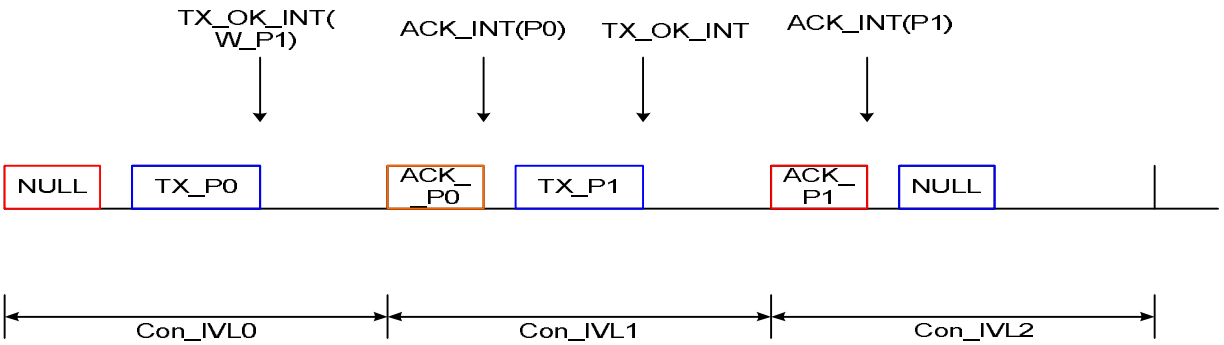
9.5 BLE RF Control Timing

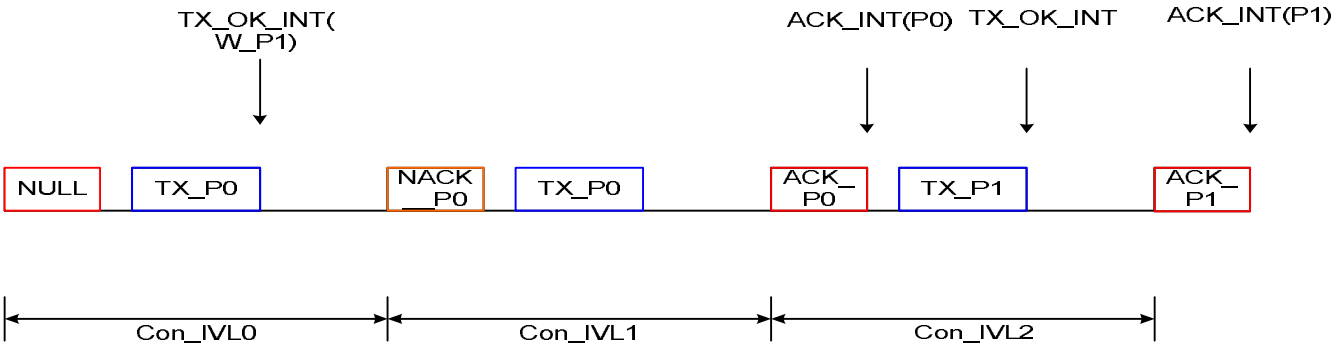
9.5.1 TX and RX Control By Link Layer



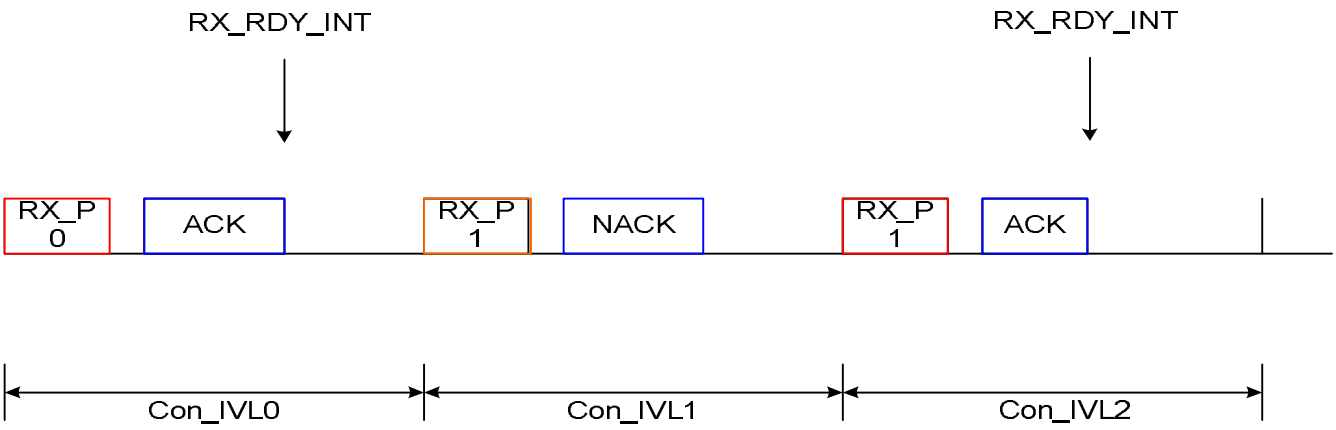
9.5.2 BLE TRX Timing Diagram

TX mode:





RX Mode :



10. SPI

A7107 only supports one SPI interface with maximum data rate up to 15Mbps. MCU should assert SCS pin low (SPI chip select) to active accessing of A7107. Via SPI interface, user can access **control registers** and issue **Strobe command**. Figure 10.1 gives an overview of SPI access manners.

3-wire SPI (SCS, SCK and SDIO) or 4-wire SPI (SCS, SCK, SDIO and GIO1/GIO2) configuration is provided. For 3-wire SPI, SDIO pin is configured as bi-direction to be data input and output. For 4-wire SPI, SDIO pin is data input and GIO1 (or GIO2) pin is data output. In such case, GIO1S (0bh) or GIO2S (0ch) should be set to [0110].

For SPI write operation, SDIO pin is latched into A7107 at the rising edge of SCK. For SPI read operation, if input address is latched by A7107, data output is aligned at falling edge of SCK. Therefore, MCU can latch data output at the rising edge of SCK.

To control A7107's internal state machine, it is very easy to send Strobe command via SPI interface. The Strobe command is a unique command set with total 8 commands. See section 10.3, 10.4 and 10.5 for details.

	SPI chip select	Data In	Data Out
3-Wire SPI	SCS pin = 0	SDIO pin	SDIO pin
4-Wire SPI	SCS pin = 0	SDIO pin	GIO1 (GIO1S=0110) / GIO2 (GIO2S=0110)

Figure 10.1 SPI Access Manners

10.1 SPI Format

The first bit (A7) is critical to indicate A7107 the following instruction is "Strobe command" or "control register". See Table 10.1 for SPI format. Based on Table 10.1, To access control registers, just set A7=0, then A6 bit is used to indicate read (A6=1) or write operation (A6=0). See Figure 10.2 (3-wire SPI) and Figure 10.3 (4-wire SPI) for details.

Address Byte (8 bits)								Data Byte (8 bits)							
CMD	R/W	Address						Data							
A7	A6	A5	A4	A3	A2	A1	A0	7	6	5	4	3	2	1	0

Table 10.1 SPI Format

Address byte:

Bit 7: Command bit

[0]: Control registers.
[1]: Strobe command.

Bit 6: R/W bit

[0]: Write data to control register.
[1]: Read data from control register.

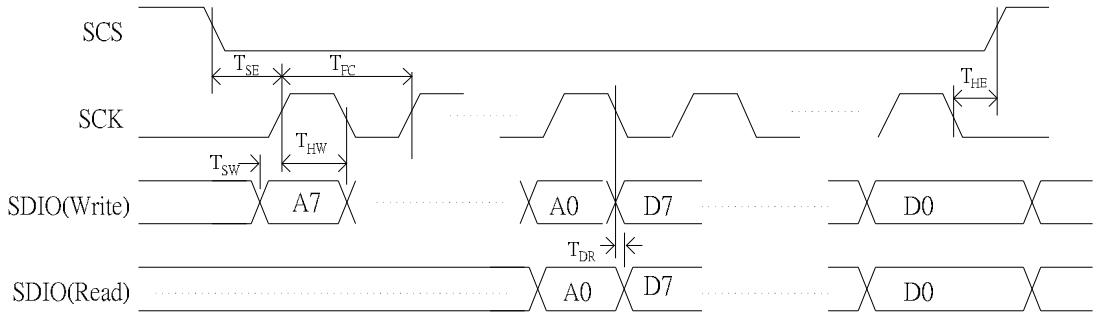
Bit [5:0]: Address of control register

Data Byte:

Bit [7:0]: SPI input or output data, see Figure 10.2 and Figure 10.3 for details.

10.2 SPI Timing Characteristic

No matter 3-wire or 4-wire SPI interface is configured, the maximum SPI data rate is 10 Mbps. To active SPI interface, SCS pin must be set to low. For correct data latching, user has to take care hold time and setup time between SCK and SDIO. See Table 10.2 for SPI timing characteristic.



Parameter	Description	Min.	Max.	Unit
F_C	FIFO clock frequency.		10	MHz
T_{SE}	Enable setup time.	50		ns
T_{HE}	Enable hold time.	50		ns
T_{SW}	TX Data setup time.	50		ns
T_{HW}	TX Data hold time.	50		ns
T_{DR}	RX Data delay time.	0	50	ns

Table 10.2 SPI Timing Characteristic

10.3 SPI Timing Chart

In this section, 3-wire and 4-wire SPI interface read / write timing are described.

10.3.1 Timing Chart of 3-wire SPI

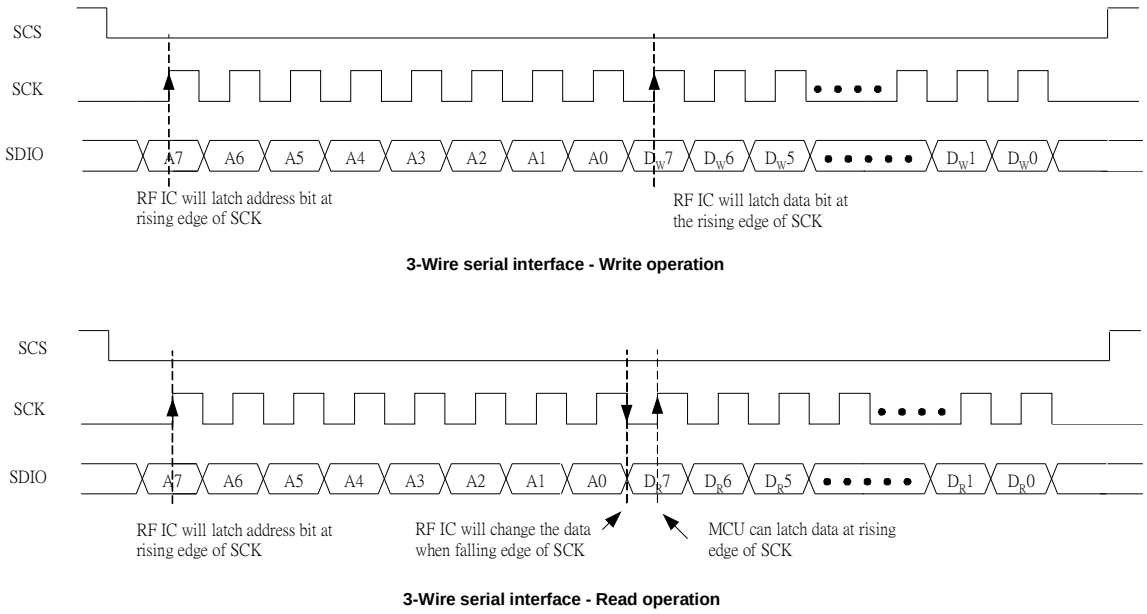


Figure 10.2 Read/Write Timing Chart of 3-Wire SPI

10.3.2 Timing Chart of 4-wire SPI

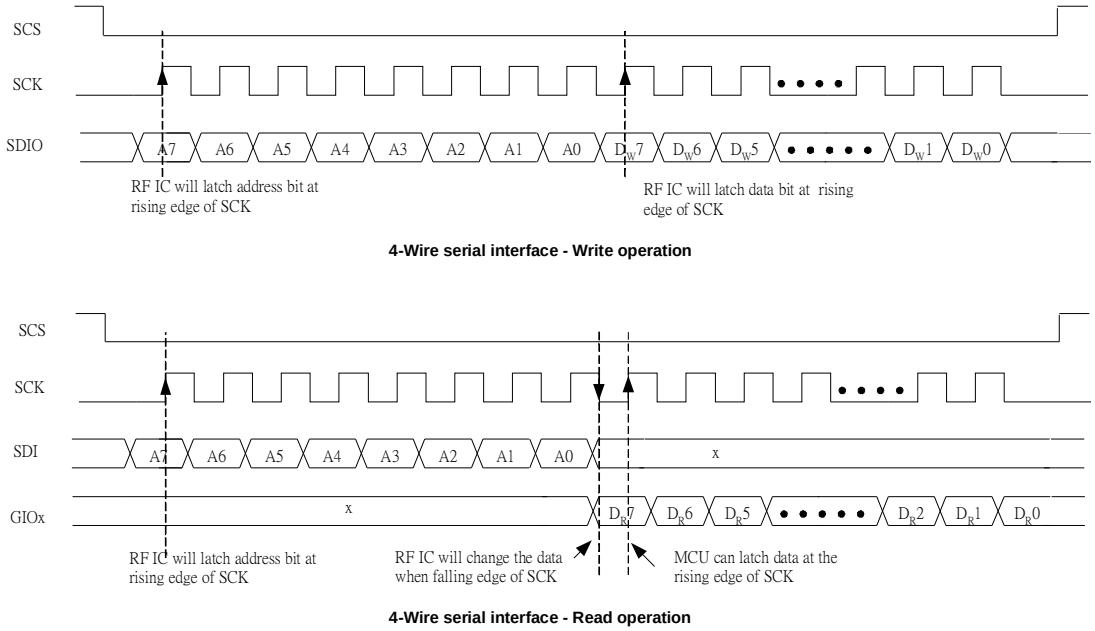


Figure 10.3 Read/Write Timing Chart of 4-Wire SPI

10.4 Strobe Commands

A7107 supports 8 Strobe commands to control internal state machine for chip's operations. Table 10.3 is the summary of Strobe commands.

Be notice, Strobe command could be defined by 4-bits (A7~A4) or 8-bits (A7~A0). If 8-bits Strobe command is selected, A3 ~ A0 are don't care conditions. In such case, SCS pin can be remaining low for asserting next commands.

Strobe Command when AFIDS =0 (3Eh) and MIDS =0 (3Eh)

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	1	0	0	0	Deep Sleep mode (I/Os are in tri-state)
1	0	0	0	1	0	1	1	Deep Sleep mode (I/Os are pulled high)
1	0	0	0	x	x	x	x	Sleep mode
1	0	0	1	x	x	x	x	Idle mode
1	0	1	0	x	x	x	x	Standby mode
1	0	1	1	x	x	x	x	PLL mode
1	1	0	0	x	x	x	x	RX mode
1	1	0	1	x	x	x	x	TX mode
1	1	1	0	x	x	x	x	FIFO write pointer reset
1	1	1	1	x	x	x	x	FIFO read pointer reset

Remark: x means " don't care"

Table 10.3 Strobe Commands by SPI interface

10.4.1 Strobe Command - Sleep Mode

Refer to Table 10.3 user can issue 4 bits (1000) Strobe command directly to set A7107 into Sleep mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	x	X	x	x	Sleep mode

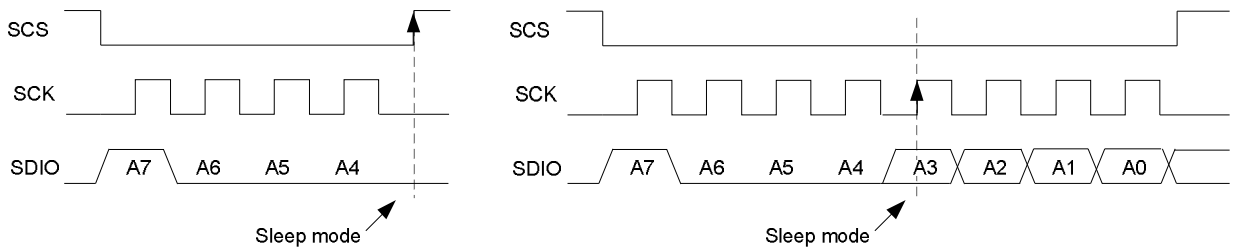


Figure 10.4 Sleep mode Command Timing Chart

10.4.2 Strobe Command - Idle Mode

Refer to Table 10.3, user can issue 4 bits (1001) Strobe command directly to set A7107 into Idle mode. Below is the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	1	x	X	x	x	Idle mode

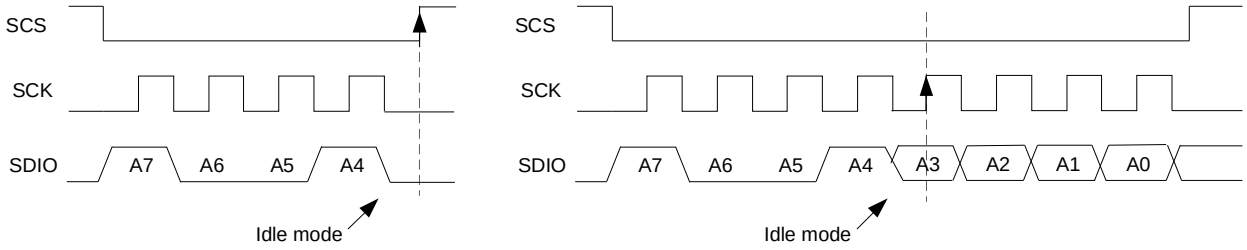


Figure 10.5 Idle mode Command Timing Chart

10.4.3 Strobe Command - Standby Mode

Refer to Table 10.3, user can issue 4 bits (1010) Strobe command directly to set A7107 into Standby mode. Below is the Strobe command table and timing chart.

Strobe Command

Strobe Command								**Description**
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	0	x	X	x	x	Standby mode

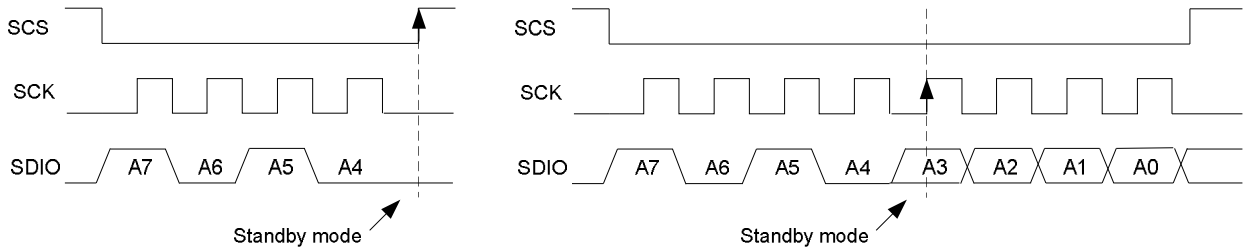


Figure 10.6 Standby mode Command Timing Chart

10.4.4 Strobe Command - PLL Mode

Refer to Table 10.3, user can issue 4 bits (1011) Strobe command directly to set A7107 into PLL mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								**Description**
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	1	x	X	x	x	PLL mode

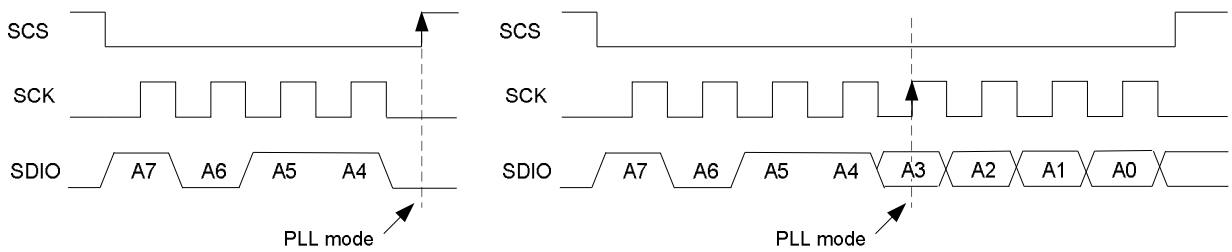


Figure 10.7 PLL mode Command Timing Chart

10.4.5 Strobe Command - RX Mode

Refer to Table 10.3, user can issue 4 bits (1100) Strobe command directly to set A7107 into RX mode. Below are the

Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	0	x	X	x	x	RX mode

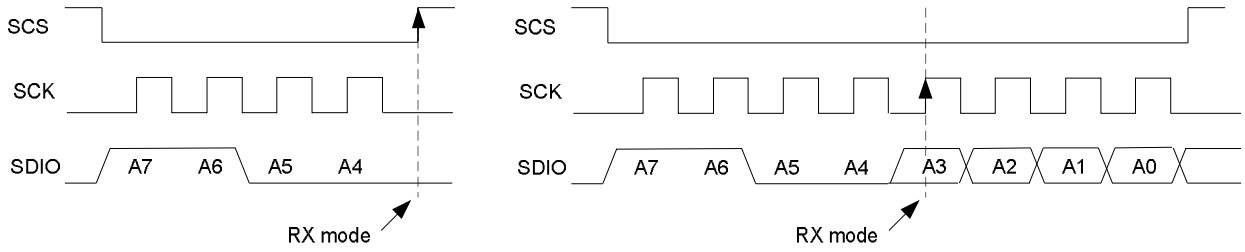


Figure 10.8 RX mode Command Timing Chart

10.4.6 Strobe Command - TX Mode

Refer to Table 10.3, user can issue 4 bits (1101) Strobe command directly to set A7107 into TX mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	1	x	x	x	x	TX mode

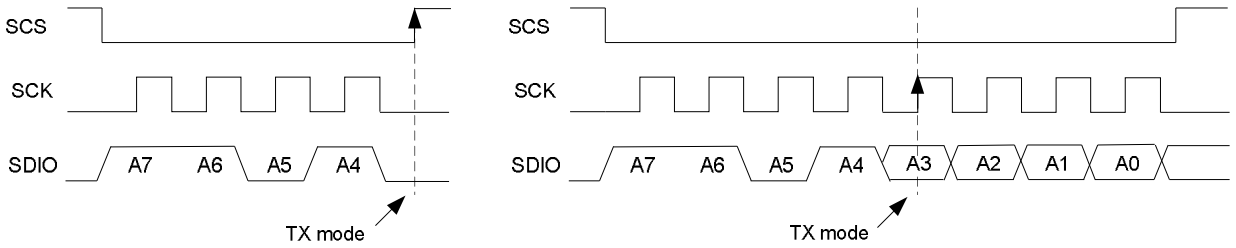


Figure 10.9 TX mode Command Timing Chart

10.4.7 Strobe Command – FIFO Write Pointer Reset

Refer to Table 10.3, user can issue 4 bits (1110) Strobe command directly to reset A7107 FIFO write pointer. Below is the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	0	x	x	x	x	FIFO write pointer reset

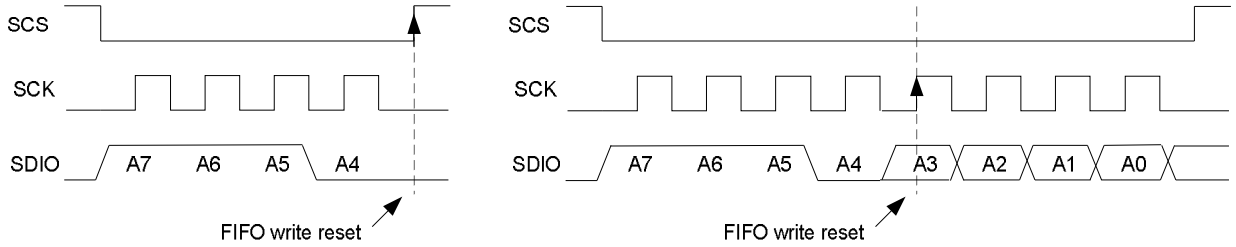


Figure 10.10 FIFO write pointer reset Command Timing Chart

10.4.8 Strobe Command – FIFO Read Pointer Reset

Refer to Table 10.3, user can issue 4 bits (1111) Strobe command directly to reset A7107 FIFO read pointer. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								**Description**
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	1	x	x	x	x	FIFO read pointer reset

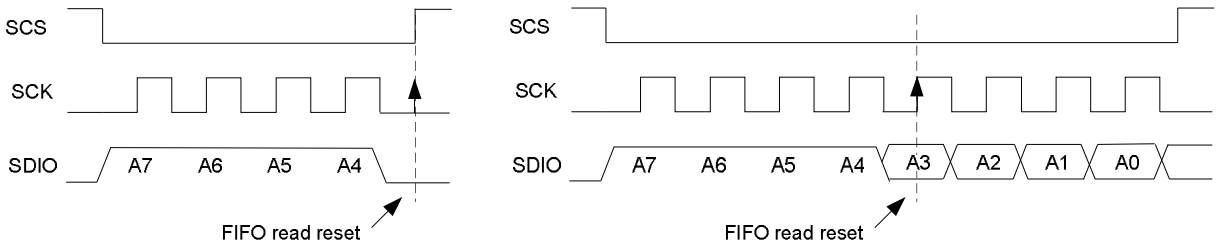


Figure 10.11 FIFO read pointer reset Command Timing Chart

10.4.9 Strobe Command – Deep Sleep Mode

Refer to Table 10.3, user can issue (8 bits) deep sleep Strobe command directly to switch off power supply to A7107.In this mode, A7107 is staying minimum current consumption. All registers are no data retention and re-calibration flow is necessary. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								**Description**
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	1	0	0	0	Tri-state of GIO1 / GIO2 (no register retention)
1	0	0	0	1	0	1	1	Internal Pull-High of GIO1 / GIO2 (no register retention)

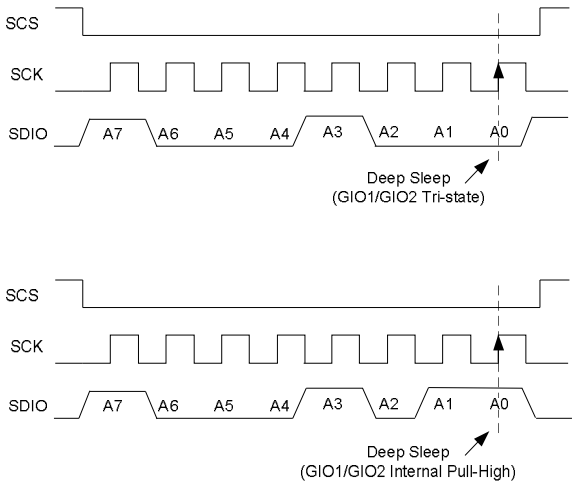


Figure 10.12 Deep Sleep Mode Timing Chart

10.5 Reset Command

In addition to power on reset (POR), MCU could issue software reset to A7107 by setting Mode Register (00h) through SPI interface as shown below. As long as 8-bits address (A7~A0) are delivered zero and data (D7~D0) are delivered zero, A7107 is informed to generate internal signal “RESETN” to initial itself. After reset command, A7107 is in standby mode and calibration procedure shall be issued again.

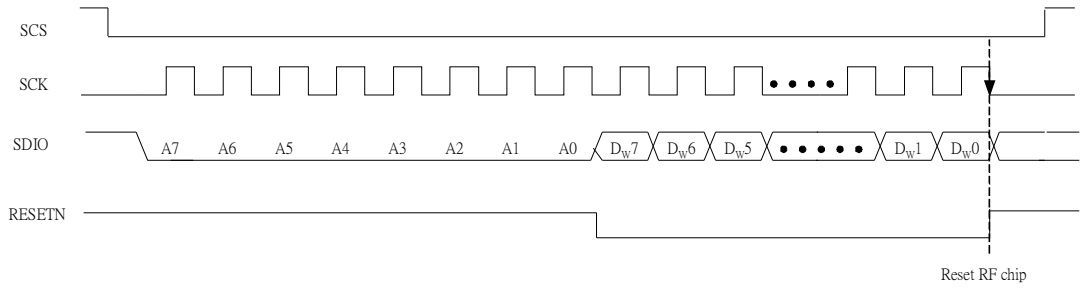


Figure 10.14 Reset Command Timing Chart

10.6 ID Accessing Command

A7107 has built-in 32-bits ID Registers for customized identification code. It is accessed via SPI interface. ID length is recommended to be 32 bits by setting IDL (1Fh). Therefore, user can toggle SCS pin to high to terminate ID accessing command when ID data is output completely.

Figure 10.13 and 10.14 are timing charts of 32-bits ID accessing via 3-wire SPI.

10.6.1 ID Write Command

User can refer to Figure 10.2 for SPI write timing chart in details. Below is the procedure of ID write command.

Step1: Deliver A7~A0 = 00000110 (A6=0 for write, A5~A0 = 000110 for ID addr, 06h).
Step2: By SDIO pin, deliver 32-bits ID into A7107 in sequence by Data Byte 0 **(recommend 5xh or Axh)**, 1, 2 and 3.
Step3: Toggle SCS pin to high when step2 is completed.

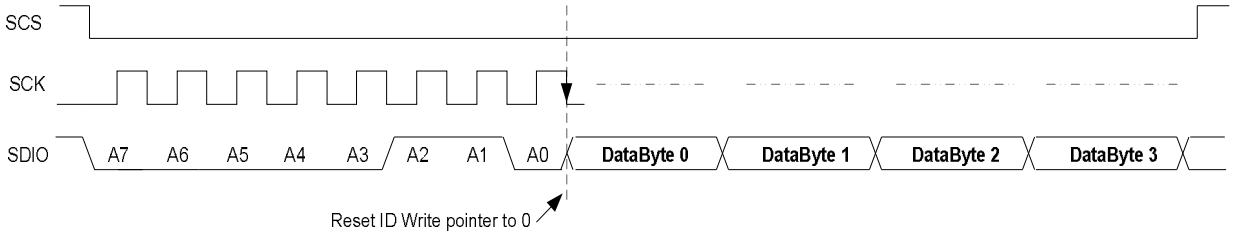


Figure 10.15 ID Write Command Timing Chart

10.6.2 ID Read Command

User can refer to Figure 10.2 for SPI read timing chart in details. Below is the procedure of ID read command.

Step1: Deliver A7~A0 = 01000110 (A6=1 for read, A5~A0 = 000110 for ID addr, 06h).
Step2: SDIO pin outputs 32-bits ID in sequence by Data Byte 0, 1, 2 and 3.
Step3: Toggle SCS pin to high when step2 is completed.

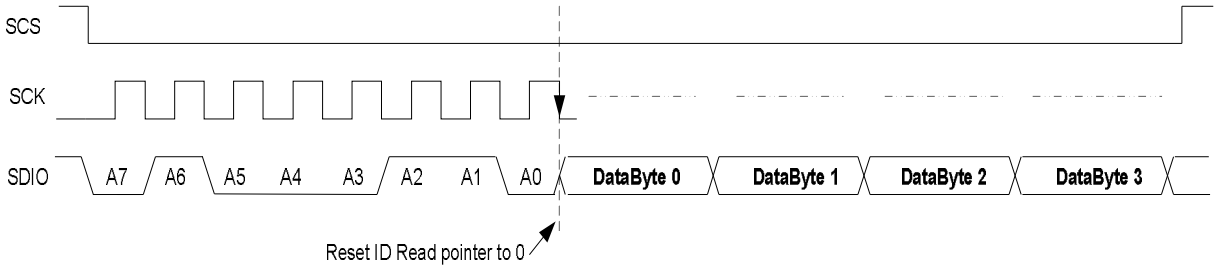


Figure 10.16 ID Read Command Timing Chart

10.7 FIFO Accessing Command

To use A7107's FIFO mode, enable FMS (01h) =1 via SPI interface. Before TX delivery, just write wanted data into TX FIFO (05h) then issue TX Strobe command. Similarly, user can read RX FIFO (05h) once payload data is received.

MCU can use polling or interrupt scheme to do FIFO accessing. FIFO status can output to GIO1 (or GIO2) pin by setting GIO1S (0Bh) or GIO2S (0Ch).

Figure 10.15 and 10.16 are timing charts of FIFO accessing via 3-wire SPI.

10.7.1 TX FIFO Write Command

User can refer to Figure 10.2 for SPI write timing chart in details. Below is the procedure of TX FIFO write command.

Step1: Deliver A7~A0 = 00000101 (A6=0 for write control register and issue FIFO A [5:0] = 05h).
Step2: By SDIO pin, deliver (n+1) bytes TX data into TX FIFO in sequence by Data Byte 0, 1, 2 to n.
Step3: Toggle SCS pin to high when step2 is completed.
Step4: Send Strobe command of TX mode (Figure 10.9) to do TX delivery.

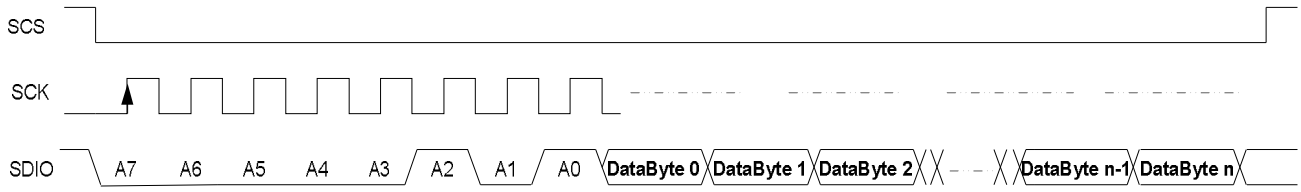


Figure 10.17 TX FIFO Write Command Timing Chart

10.7.2 Rx FIFO Read Command

User can refer to Figure 10.2 for SPI read timing chart in details. Below is the procedure of RX FIFO read command.

Step1: Deliver A7~A0 = 01000101 (A6=1 for read control register and issue FIFO at address 05h).
Step2: SDIO pin outputs RX data from RX FIFO in sequence by Data Byte 0, 1, 2 to n.
Step3: Toggle SCS pin to high when RX FIFO is read completely.

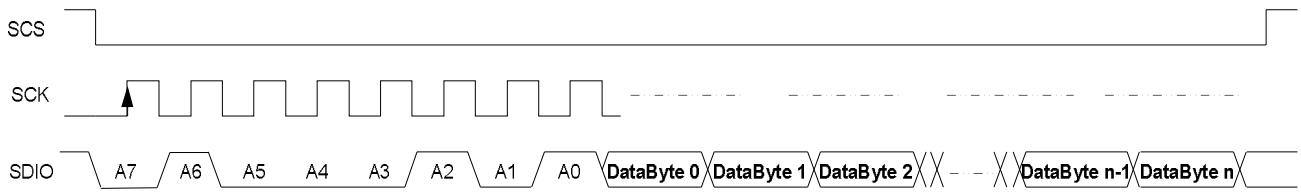


Figure 10.18 RX FIFO Read Command Timing Chart

11. State machine

From accessing data point of view, if FMS=1, FIFO mode is enabled, otherwise, A7107 is in direct mode.

	SPI chip select	SPI Clock	SPI Data In	SPI Data Out	FMS register
3-Wire SPI	SCS	SCK	SDIO	SDIO	FIFO (FMS=1) Direct (FMS=0)
4-Wire SPI	SCS	SCK	SDIO	GIO1 or GIO2	FIFO (FMS=1) Direct (FMS=0)

From current consumption point of view, A7107 has below 8 operation modes.

(1) Deep Sleep mode
(2) Sleep mode
(3) Idle mode
(4) Standby mode
(5) PLL mode
(6) TX mode
(7) RX mode
(8) Star-networking mode

11.1 Key states

After power on reset or software reset or deep sleep mode, user has to do calibration process because all control registers are in initial values. The calibration process of A7107 is very easy, user only needs to issue Strobe commands and enable calibration registers. And then, the calibrations are automatically completed by A7107's internal state machine. Table 11.1 shows a summary of key circuitry among those strobe commands.

Strobe Command when AFIDS =0 (3Eh) and MIDS =0 (3Eh)

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	1	0	0	0	Deep Sleep mode (I/Os are in tri-state)
1	0	0	0	1	0	1	1	Deep Sleep mode (I/Os are pulled high)
1	0	0	0	x	x	x	x	Sleep mode
1	0	0	1	x	x	x	x	Idle mode
1	0	1	0	x	x	x	x	Standby mode
1	0	1	1	x	x	x	x	PLL mode
1	1	0	0	x	x	x	x	RX mode
1	1	0	1	x	x	x	x	TX mode
1	1	1	0	x	x	x	x	FIFO write pointer reset
1	1	1	1	x	x	x	x	FIFO read pointer reset

Mode	Register retention	Regulator	Xtal Osc.	VCO	PLL	RX	TX	Strobe Command
Deep Sleep (Tri-state)	No	OFF	OFF	OFF	OFF	OFF	OFF	(1000-1000)b
Deep Sleep (pull-high)	No	OFF	OFF	OFF	OFF	OFF	OFF	(1000-1011)b
Sleep	Yes	ON	OFF	OFF	OFF	OFF	OFF	(1000-xxxx)b
Idle	Yes	ON	OFF	OFF	OFF	OFF	OFF	(1001-xxxx)b
Standby	Yes	ON	ON	OFF	OFF	OFF	OFF	(1010-xxxx)b
PLL	Yes	ON	ON	ON	ON	OFF	OFF	(1011-xxxx)b
TX	Yes	ON	ON	ON	ON	OFF	ON	(1101-xxxx)b
RX	Yes	ON	ON	ON	ON	ON	OFF	(1100-xxxx)b

Remark: x means "don't care"

Table 11.1. Operation mode and strobe command

12. Transceiver LO Frequency

A7107 is a half-duplex transceiver with embedded PA and LNA. For TX or RX frequency setting, user just needs to set up LO (Local Oscillator) frequency for two ways radio transmission.

To target full range of 2.4GHz ISM band (2400 MHz to 2483.5 MHz), A7107 applies offset concept by LO frequency $F_{LO} = F_{LO\_BASE} + F_{OFFSET}$. Therefore, for different applications, A7107 is easy to implement frequency hopping and multi-channels by **ONE** register setting, **PLL Register I (CHN [7:0], 0Fh).**

Below is the LO frequency block diagram.

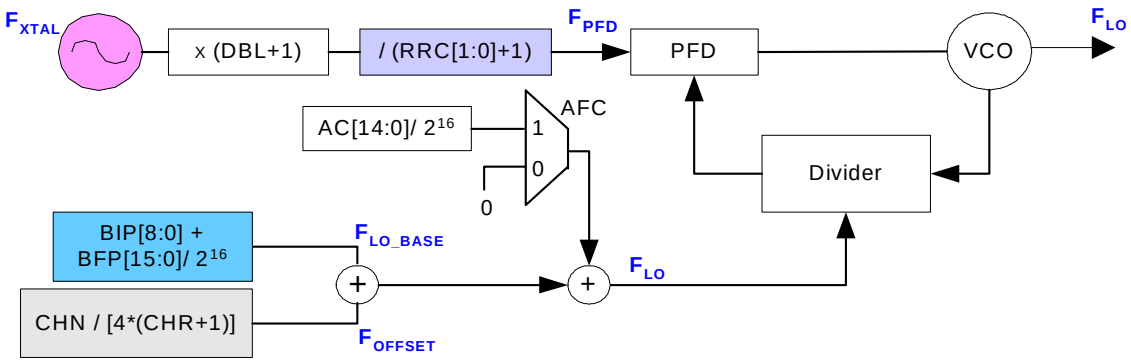


Fig 12.1 Frequency synthesizer block diagram

Relative Control Register

PLL Register I (Address: 0Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL I	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
Reset		0	0	0	0	0	0	0	0

PLL Register II (Address: 10h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL II	R	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IP8
	W	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	BIP8
Reset		1	0	0	1	1	1	1	0

PLL Register III (Address: 11h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL III	R	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
	W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
Reset		0	1	0	0	1	0	1	1

PLL Register IV (Address: 12h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL IV	R	SYNC/FP15	AC14/FP14	AC13/FP13	AC12/P12	AC11/ FP11	AC10/FP10	AC9/FP9	AC8/FP8
	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
Reset		0	0	0	0	0	0	0	0

PLL Register V (Address: 13h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL V	R	AC7/FP7	AC6/FP6	AC5/FP5	AC4/FP4	AC3/FP3	AC2/FP2	AC1/FP1	AC0/FP0
	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0

Reset		0	0	0	0	0	0	1	1

RX Register (Address: 18h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX	W	MSCRC	RXSM1	RXSM0	AFC	RXDI	DMG	BWS	ULS
Reset		0	1	0	0	0	0	1	0

Mode Control Register (Address: 01h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode Control I	R	DDPC	ARSSI	AIF	DFCD	WORE	FMT	FMS	ADCM
	W	DDPC	ARSSI	AIF	CD	WORE	FMT	FMS	ADCM
Reset		0	0	0	0	0	0	0	0

12.1 LO Frequency Setting

From Figure 12.1, F_{LO} is not only for TX radio frequency but also to be RX LO frequency. To set up $F_{LO,}$ it is easy to implement by below 7 steps.

1. Set the base frequency (**F_{LO_BASE}**) by PLL Register II, III, IV and V (0Fh, 10h, 11h and 12h).
   Recommend user to set **F_{LO_BASE} ~ 2400.001MHz**.
2. Set the channel step (F_{CHSP}) by PLL Register II (0Fh).
   $F_{CHSP} = F_{PFD}$ / (4*(CHR+1)) = F_{XTAL} * (DBL+1)/ (4*(CHR+1)), Recommend F_{CHSP} = 500 KHz.
3. Set CHN [7:0] to get offset frequency by PLL Register I (0Eh).
   F_{OFFSET} = CHN [7:0] x F_{CHSP}
4. LO frequency is equal to base frequency plus offset frequency.
   $F_{LO} = F_{LO\_BASE} + F_{OFFSET}$
5. For TX radio frequency (**F_{TXRF}**) is equal to **F_{LO}**.
   $F_{TXRF} = F_{LO}$
6. If disable AIF function (AIF=0),
   Channel frequency (or **F_{TXRF}**) shall be inserted F_{IF} offset because of low-IF architecture.

Channel Frequency (Need F_{IF} offset)	Mode Register [01h]	RX [18h]	RX LO Frequency	Note
F_{TXRF} − F_{IF}	AIF = 0	ULS = 1	**$F_{RXLO} = F_{LO}$**	Low side band (**$F_{CH} < F_{RXLO}$**)
F_{TXRF} + F_{IF}	AIF = 0	ULS = 0	**$F_{RXLO} = F_{LO}$**	Up side band (**$F_{CH} > F_{RXLO}$**)

   Where F_{IF}, the IF band pass filter center frequency is either 1MHz (BWS=0) or 2Mhz (BWS=0).

   RX LO frequency (**F_{RXLO}**) is equal to **F_{LO}**.
   $F_{RXLO} = F_{LO}$

7. If enable AIF function (AIF=1),
   Channel frequency (or **F_{TXRF}**) is no need to inserted F_{IF} offset (**F_{RXLO}** is auto-offset F_{IF} frequency internally).

Channel Frequency (No Need F_{IF} offset)	Mode Register [01h]	RX [18h]	RX LO Frequency (auto-offset)	Note
F_{TXRF}	AIF = 1	ULS = 0	**F_{RXLO}** = **F_{LO}** − F_{IF}	Up side band (**$F_{CH} > F_{RXLO}$**)
F_{TXRF}	AIF = 1	ULS = 1	**F_{RXLO}** = **F_{LO}** + F_{IF}	Low side band (**$F_{CH} < F_{RXLO}$**)

   Where F_{IF}, the IF band pass filter center frequency is either 500 KHz (BWS=1) or 250 KHz (BWS=0).

F_{LO_BASE}

$$F_{LO\_BASE} = F_{PFD} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}}) = (DBL + 1) \cdot \frac{F_{XTAL}}{RRC[1:0] + 1} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}})$$

Base on the above formula, for example, if select 16MHz crystal (F_{XTAL} = 16 MHz.) and set channel step F_{CHSP} = 500 KHz, To get **F_{LO_BASE} and F_{LO}**, see Table 12.1, 12.2, 12.3 and Figure 14.2 for details.

How to set F_{LO_BASE} ~ 2400.001 MHz

STEP	ITEMS	VALUE	NOTE

1	F_{XTAL}	16 MHz	Crystal Frequency
2	DBL	1	Disable double function
3	RRC	0	If so, F_{PFD}= 32MHz
4	BIP	0x4B	To get F_{LO_BASE} =2400 MHz
5	BFP	0x0002	To get F_{LO_BASE} ~ 2400.001 MHz
6	**F_{LO_BASE}**	**~2400.001 MHz**	LO Base frequency

Table 12.1 How to set F_{LO_BASE}

How to set F_{TXRF} = F_{LO} = F_{LO_BASE} + F_{OFFSET} ~ 2405.001 MHz

STEP	ITEMS	VALUE	NOTE
1	F_{LO_BASE}	~2400.001 MHz	After set up BIP and BFP
2	CHR	7	To get F_{CHSP}= 500 KHz
3	F_{CHSP}	500 KHz	Channel step = 500KHz
4	CHN	0x0A	Set channel number = 10
5	F_{OFFSET}	5 MHz	F_{OFFSET}= 500 KHz * (CHN) = 5MHz
6	F_{LO}	~2405.001 MHz	Get F_{LO}= F_{LO_BASE} + F_{OFFSET}
7	**F_{TXRF}**	**~2405.001 MHz**	F_{TXRF} = F_{LO}

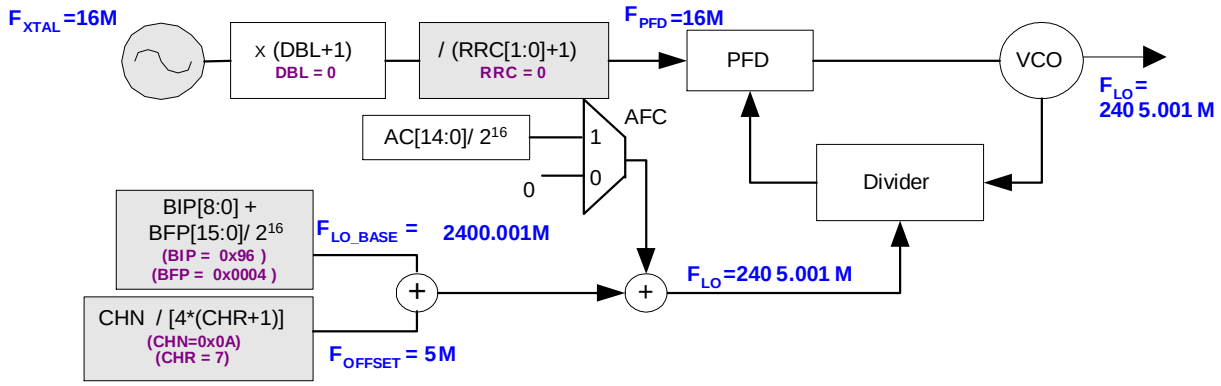
Table 12.2 How to set F_{TXRF}

How to set F_{RXLO} (If user set IF frequency = 1Mhz)

Register Setting	F_{RXLO}	NOTE
AIF=0 ULS=depends	~2405.001 MHz	F_{RXLO} = F_{LO}
AIF=0 ULS=depends	~2405.001 MHz	F_{RXLO} = F_{LO}
AIF=1 ULS=0	~2404.501 MHz	F_{RXLO} = F_{LO} − 1MHz
AIF=1 ULS=1	~2405.001 MHz	F_{RXLO} = F_{LO} + 1MHz

Table 12.3 How to set F_{RXLO}

Therefore, to get F_{LO} ~ 2405.001 MHz, see below block diagram for registers setting.



12.2 Auto IF exchange

Relative Control Register

Mode Control Register (Address: 01h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	DDPC	ARSSI	AIF	CD	WWSE	FMT	FMS	ADCM
	W	DDPC	ARSSI	AIF	DFCD	WWSE	FMT	FMS	ADCM
Reset		0	0	0	0	0	0	0	0

RX Register (Address: 18h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX	W	MSCRC	RXSM1	RXSM0	AFC	RXDI	DMG	BWS	ULS

Reset		0	1	0	0	0	0	1	0

A7107 has Auto IF offset function (AIF, 01h). Base on this, user has no need to change CHN [7:0] for insert F_{IF} offset while TRX exchanging because F_{LO} is changed automatically. See Table 12.1 for details.

Item	Role	AIF	ULS	CHN[10]	F_{CHSP} (KHz)	F_{TXRF} (KHz)	F_{RXLO} (MHz)	NOTE
Master	TX	1	0	**10**	500	2405.001	-	F_{TXRF}= F_{CH}
	RX	1	0	**10**	500	-	2404.001	Up side band (Slave F_{CH} > F_{RXLO})
Slave	TX	1	0	**10**	500	2405.001	-	F_{TXRF}= F_{CH}
	RX	1	0	**10**	500	-	2404.001	Up side band (Master F_{CH} > F_{RXLO})
Exchanging		While Master is doing TRX exchanging from TX to RX, F_{LO} is changed from 2405.001 MHz to 2404.001 MHz automatically. So does slave.						
On air occupied frequency		Master F_{TXRF} = 2405.001 MHz Slave F_{TXRF} = 2405.001 MHz						ONE occupied frequency.

Table 12.4 AIF function while TRX exchanging

13. Crystal Oscillator

A7107 needs external crystal or external clock that is either 16 MHz to generate internal wanted clock.

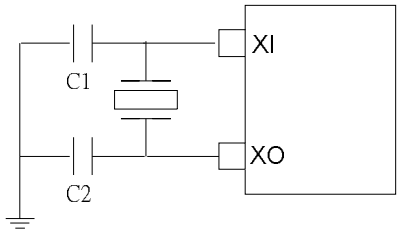
9.2.14 Clock Register (Address: 0Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Clock	R/W	GRC3	GRC2	GRC1	GRC0	-	CSC	CGS	XS
Reset		1	1	1	1	-	1	0	1

XS: Crystal oscillator select.
[0]: Use external clock. **[1]:** Use external crystal.

13.1 Use External Crystal

To use external crystal, user just sets XS= 1 (0Dh) to enable crystal oscillator. Figure 12.1 shows the connection of crystal network between XI and XO pins. For external capacitor select C1 and C2 capacitance are used to adjust different crystal loading but register VCOSC [5:0] need to set to 0. If using internal capacitor, VCOSC[5:0] need to setting the required crystal loading. A7107 support low cost crystal within ± 50ppm accuracy. Be noted that crystal accuracy requirement includes initial tolerance, temperature drift, aging and crystal loading.



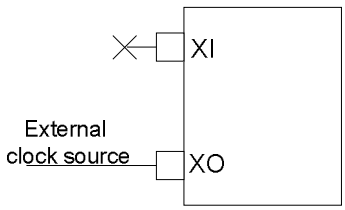
i.e., Crystal = 16MHz (Cload =20pF), C1=C2=33pF.

Figure12.1 Crystal network connection for using external crystal

13.2 Use External Clock

A7107 has built-in AC couple capacitor to support external clock input. Figure 12.2 shows how to connect. In such case, XI pin is left opened.

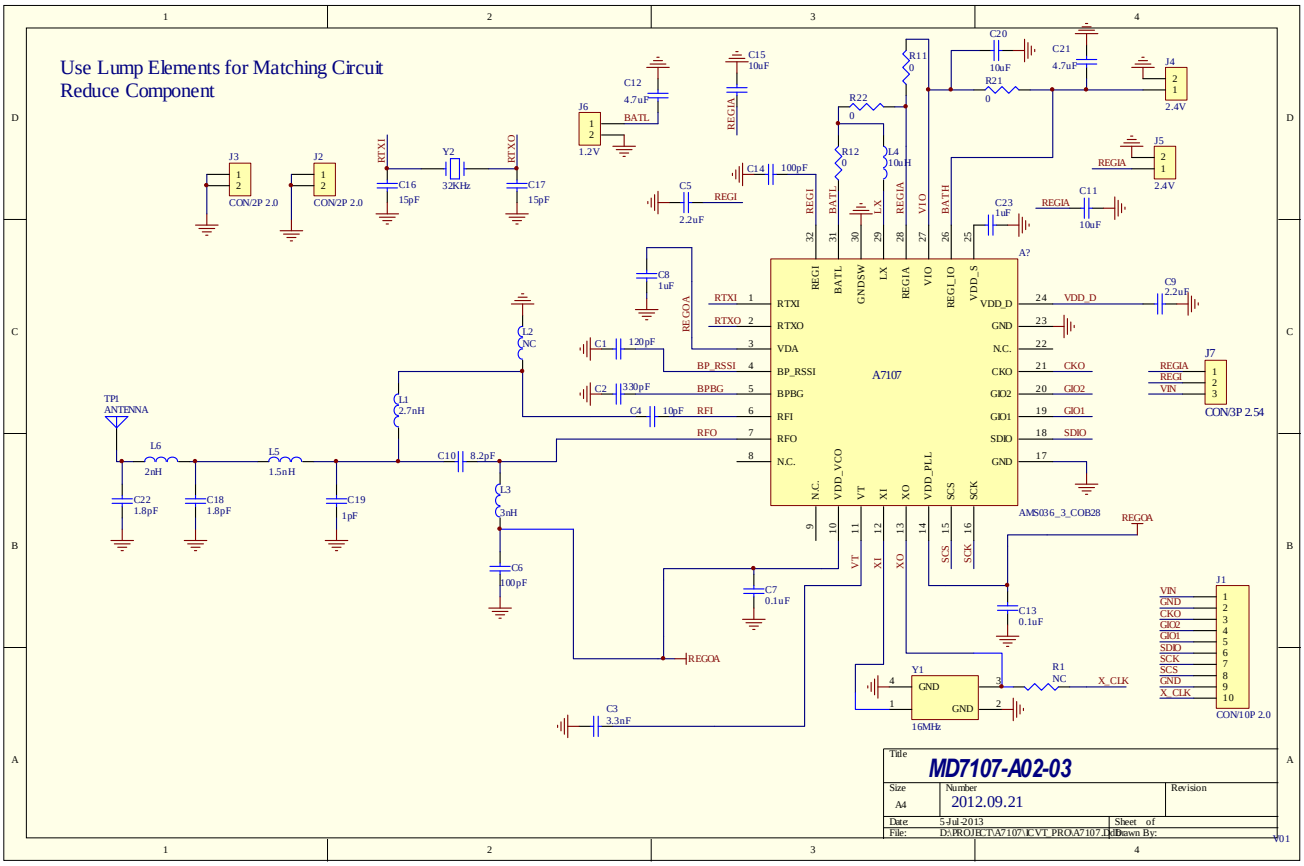
To use external clock from MCU instead of external crystal, user just sets XS= 0 (0Dh) to active AC couple capacitor. Be notice, the frequency accuracy of external clock shall be controlled within ± 50ppm and the clock swing (peak-to-peak) shall be larger than 1.5V.



(External clock is controlled within ± 50ppm and > 1.5Vpp.)

Figure 12.2 Connect to external clock source

14. Application Circuit (MD7107-A01)



Only LDO mode: Short Pin2 and Pin3 of J7 with a jump.
DC Converter (buck mode): Short Pin1 and Pin2 of J7 with a jump, R21 and R22 are 0 ohm; R11 and R12 are NO Load.
DC Converter (boost mode): Short Pin1 and Pin2 of J7 with a jump, R11 and R12 are 0 ohm; R21 and R22 are NO Load.

15. Ordering Information

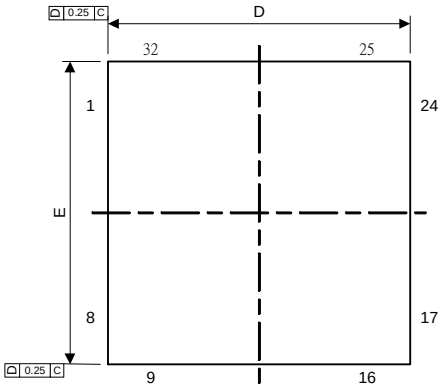
Part No.	Package	Units Per Reel / Tray
A71X07AQCI/Q	QFN32L, Tape & Reel, Pb free	3K
A71X07AQCI	QFN32L, Tray, Pb free	490EA
A71X07AH	Die form, Tray, Pb free	100EA

16. Package Information

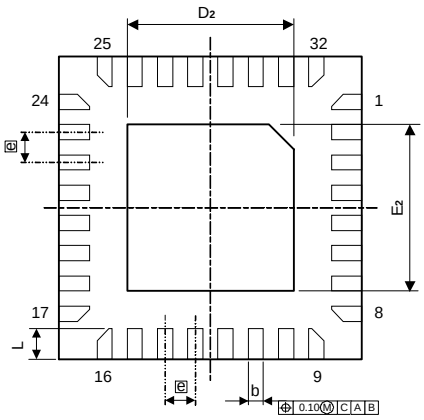
QFN 32L Saw Type Outline Dimensions

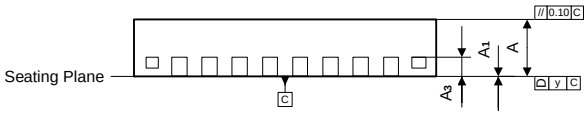
unit: inches/mm

Top View



Bottom View

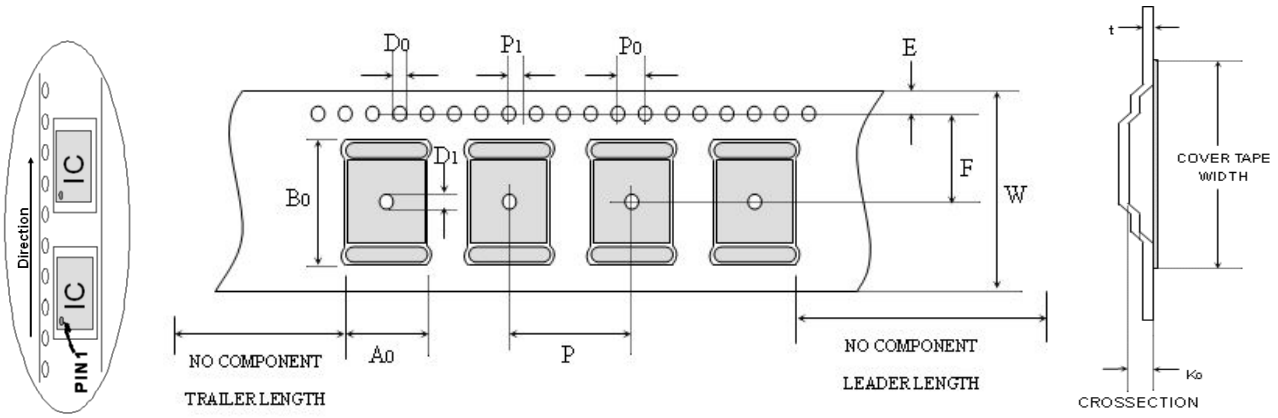




Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.032	0.70	0.75	0.80
A_1	0.000	0.001	0.002	0.00	0.02	0.05
A_3	0.010 REF			0.20 REF		
b	0.007	0.010	0.012	0.18	0.25	0.30
D	0.197 BSC			5.00 BSC		
D_2	0.049	0.106	0.128	1.25	2.70	3.25
E	0.197 BSC			5.00 BSC		
E_2	0.049	0.106	0.128	1.25	2.70	3.25
e	0.020 BSC			0.50 BSC		
L	0.012	0.016	0.020	0.30	0.40	0.50
y	0.004			0.10		

17. Tape Reel Information

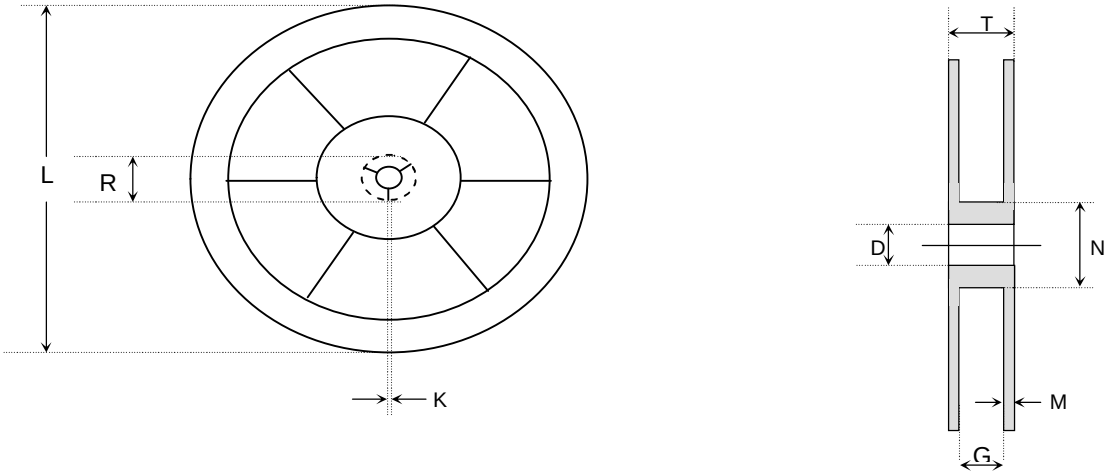
Cover / Carrier Tape Dimension



Unit: mm

TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W	K0	t	Cover tape width
QFN3*3	8±0.1	3.2 5±0.1	3.25 ±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75 ±0.1	5.5 ±0.05	12±0.3	1.25 ±0.1	0.3 ±0.05	9.3±0.1
QFN 4*4	8±0.1	4.35 ±0.1	4.35 ±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75 ±0.1	5.5 ±0.05	12±0.3	1.2 5±0.1	0.3 ±0.05	9.3±0.1
QFN 5*5	8±0.1	5.25 ±0.1	5.25 ±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75 ±0.1	5.5 ±0.05	12±0.3	1.25 ±0.1	0.3 ±0.05	9.3±0.1
SSOP	12±0.1	8.2±1	8.8±1.5	4.0±0.1	2.0±0.1	1.5±0.1	1.5±0.1	1.75 ±0.1	7.5±0.1	16±0.1	2.1±0.4	0.3 ±0.05	13.3 ±0.1

REEL DIMENSIONS



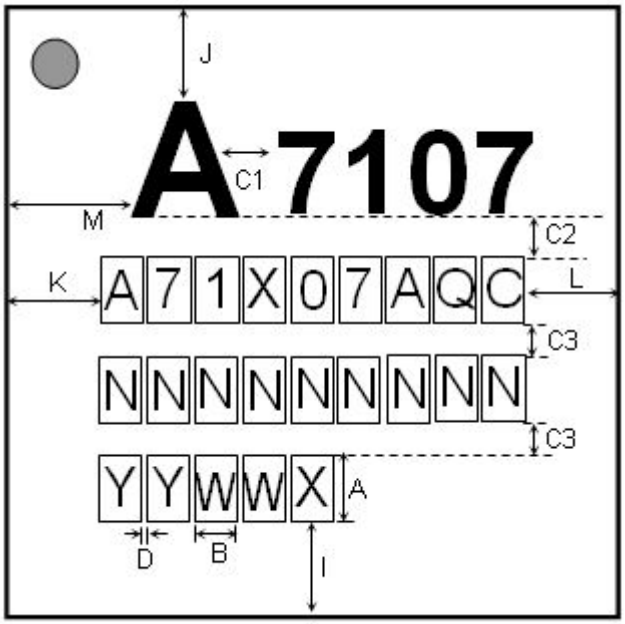
Unit: mm

TYPE	G	N	M	D	K	L	R
QFN	12.9±0.5	102 REF±2.0	2.3±0.2	13.15±0.35	2.0±0.5	330±3.0	19.6±2.9
SSOP	16.3±1	102 REF±2.0	2.3±0.2	13.15±0.35	2.0±0.5	330±3.0	19.6±2.9

18. Top Marking Information

- Part No. : **A71X07AQCI**
- Pin Count : **32**
- Package Type : **QFN**
- Dimension : **5*5 mm**
- Character Type : **Arial**

TOP MARKING LAYOUT:



❖ CHARACTER SIZE : (Unit in mm)

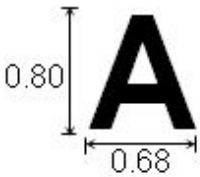
A : 0.55
B : 0.36
C1 : 0.25 C2 : 0.3 C3 : 0.2
D : 0.03
M : 1.5
A1 : 0.75 B2 : 0.7

Y Y W W : DATECODE

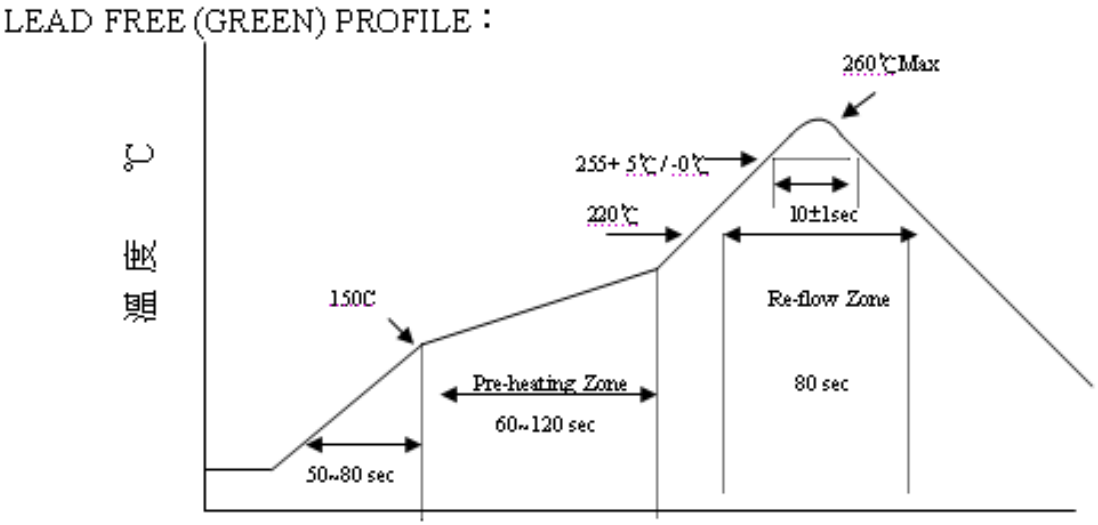
X : PKG HOUSE ID

N N N N N N N N N : LOT NO. (max. 9 characters)

I=J
K=L



19. Reflow Profile



20. Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date.AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only.

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