Document Title

A7103 Data Sheet

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial Issue	2007/7/19	
0.1	Modify specifications	2007/9/21	
0.2	Modify Logo and title	2007/10/5	
0.3	Modify register setting	2008/2/27	
0.4	Modify register setting for TX power control and Xtal start up time description	2008/3/28	

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1. General Description

A7103 is a highly integrated CMOS RF transceiver for sub 1GHz ISM band (315/434/868/915MHz). It futures both FSK and ASK capability.

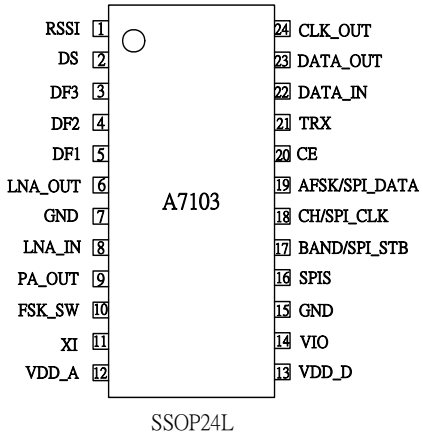
2. Typical Applications

- Remote Control.
- AMR (Auto Meter Reading).
- Security system.
- TPMS (Tire Pressure Measure System).

3. Features

- A7103A for 315/434MHz, A7103B for 868/ 915MHz.
- High link budget: Distance up to 1Km is possible. Typical Tx +10dBm @ 434MHz band.
- High sensitivity: -110dBm @ 434MHz band, IF bandwidth=100KHz.
- Very low current consumption: Typical Tx 15.5mA @ FSK, 9.5mA@ ASK; Rx: 8.8mA.
- Flexible control interface: Hardware pins or SPI.
- Support multi channels.
- High integration: VCO, PLL, LNA, Image Reject Mixer, IF Filter, Limiter, RSSI, Data Slicer, AFC, AGC…
- Very few external components: No need external filters.
- Build in image rejection mixer. Selectable IF band width (100, 200, 300 KHz).
- Wide operating range: VDD=2.2~3.3V (IO 2.0~4.2V). T=-40~+85/125℃.
- Auto ramp-up sequence control to optimize power consumption. Xtal→Auto Calibration→PLL→ RX.
- One receiver for different systems: Switching between ASK/FSK is possible.
- Auto calibration to compensate for process/temperature/voltage variation.
- Support typical 4/12/13.56/16MHz low cost crystal.

4. Pin Configuration



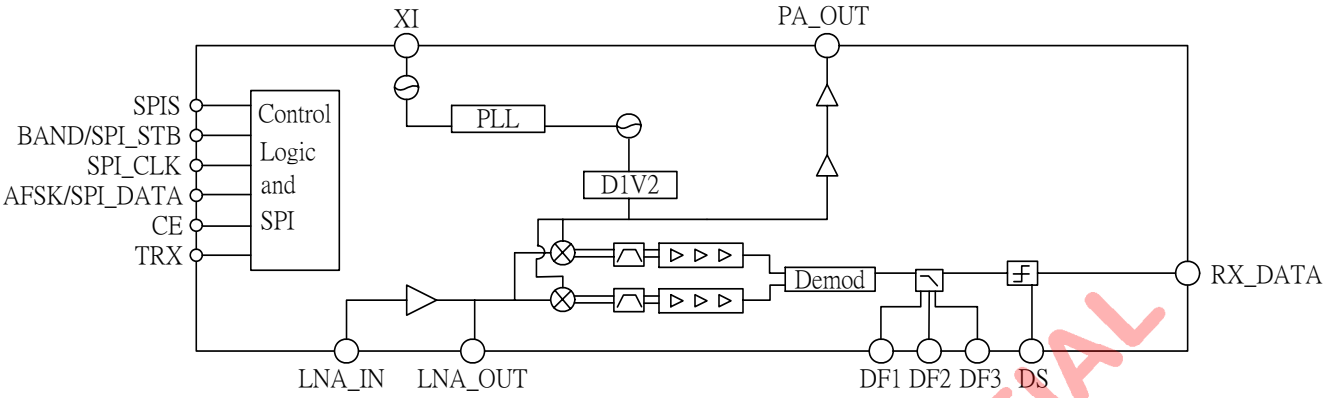
SSOP24L

5. Pin Description

Pin No.	Pin Name	Description
1	RSSI	Analog RSSI output. Connect a capacitor to GND.
2	DS	Data slicer bypass. Connect a capacitor to GND
3	DF3	Data filter capacitors.
4	DF2	
5	DF1	
6	LNA_OUT	LNA output matching.
7	GND	Connect to PCB ground.
8	LNA_IN	LNA input matching.
9	PA_OUT	Tx power amplifier output.
10	FSK_SW	FSK deviation setting. Connect to a capacitor.
11	XI	Crystal oscillator input.
12	VDD_A	Analog power input.
13	VDD_D	Digital power input.
14	VIO	Digital I/O voltage. For internal level shift VDD.
15	GND	Connect to PCB ground.
16	SPIS	SPI selection. Low→ disable SPI. Pin 17 will be configured as BAND and Pin 19 as AFSK. Pin 18 has to be tied to Low. High→ enable SPI. Pin 17 will be configured as SPI_STB and Pin 19 as SPI_DATA.
17	BAND	RF frequency band selection. Low→315MHz. High→ 434MHz.
	SPI_STB	SPI latch strobe.
18	SPI_CLK	SPI clock input. Tied to Low when SPIS is Low.
19	AFSK	Modulation selection. Low → FSK. High → ASK.
	SPI_DATA	SPI data input.
20	CE	Chip enable. Low→Sleep mode. High→Active mode.
21	TRX	TX/RX selection. Low→RX. High→TX. With internal 300KΩ pull low resistor.
22	TX_DATA	Transmitted data input. With internal 300KΩ pull low resistor.
23	RX_DATA	Received data output.
24	CLK_OUT	Clock output for micro controller. $F_{CLK\_OUT}=F_{xtal}/4$ or 16. Can be selected by SPI.

Notes: Please refer to page 4 "**Circuit Description**" for detail definitions.

6. Block Diagram



7. Specification

General Test Condition: Ta = 25ºC, Fin=434MHz, VDD=3.0V, Crystal=13.56MHz

Parameter	Description		Min.	Typ.	Max.	Unit
General						
Operating temperature			-40		85/125	°C
Supply voltage	VDD_A, VDD_D		2.2	2.8	3.3	V
Current consumption	OFF mode (all circuit off)		0.1	0.5		uA
	Rx mode			8.8		
	Tx mode (FSK), +10dBm output			15.5		
	Tx mode (ASK), +10dBm output, 50% duty.			9.5		
Crystal Frequency				4/12/13.56/16		MHz
Crystal Tolerance	Depends on application[1)]			+/-50	+/-100	ppm
Tx						
Frequency Range	A7103A			300~500		MHz
	A7103B			800~1000		
Data Rate	FSK		2		20	kbps
	ASK		2		20	
Output Power	f=314.8Hz. VDD=3.0V			10		dBm
	f=434MHz. VDD=3.0V			10		
	f=868.2MHz. VDD=3.0V			8		
	f=915MHz. VDD=3.0V			7		
Phase Noise	f=434MHz.	Offset=100KHz		-85		dBc/Hz
		Offset=1MHz		-98		
Reference Spur	f=434MHz			-45		
Rx						
Sensitivity	434MHz	FSK Bit rate=20K, Fdev=12KHz, BER<1E-3. IFBW=100KHz	-111	-109	-106	dBm
		ASK Bit rate=20K, BER<1E-3, IFBW=300KHz		-105	-102	
	314.8MHz	FSK Bit rate=20K, Fdev=12KHz, BER<1E-3. IFBW=100KHz		-108	-105	
		ASK Bit rate=20K, BER<1E-3, IFBW=300KHz		-105	-102	

	868.2MHz	FSK Bit rate=20K, Fdev=12KHz, BER<1E-3. IFBW=100KHz		-106	-103	
		ASK Bit rate=20K, BER<1E-3, IFBW=300KHz		-103	-101	
	915MHz	FSK Bit rate=20K, Fdev=12KHz, BER<1E-3. IFBW=100KHz		-105	-102	
		ASK Bit rate=20K, BER<1E-3, IFBW=300KHz		-102	-100	
IF bandwidth[2)]	FSK	IFB[1:0]=[11]	90	100		KHz
		IFB[1:0]=[10]	135	150		
		IFB[1:0]=[0X]	180	200		
	ASK	IFB[1:0]=[11]	135	150		
		IFB[1:0]=[10]	225	250		
		IFB[1:0]=[0X]	315	350		
IF frequency	Reference frequency =13.56MHz			423.75		KHz
	Reference frequency =4/12/16MHz			400		
Max input	Enable AGC, ASK			-20		dBm
	Enable AGC, FSK			0		
Image rejection	434MHz			20		dB
RSSI	Dynamic range			85		dB
	Lower level			-120		dBm
	Upper level			-35		dBm
Outband blocking	+/- 1.5MHz			45		dBc
	+/- 2MHz			45		
	+/- 3MHz			50		
	+/- 10MHz			55		
	+/- 20MHz			60		

1) Crystal tolerance is correlated to IF bandwidth setting as well as data rate. Refer to Section 9.5.2 for more details.
2) Different IF bandwidth setting results in different sensitivity. In general, better sensitivity can be obtained using narrower IF bandwidth, at the expense of tighter crystal tolerance.

8. Maximum Ratings

Characteristic	Pin name/symbol	Rating	Unit
Power supply voltage	All VDD	5.5	V
Input pin voltage		5	V
Storage temperature range	T_{stg}	-55~150	°C

9. Circuit Description

The A7103 is a highly integrated ASK/FSK transceiver featuring very low power consumption, flexible user interface and compact SSOP24 package. A built-in control sequence automatically brings A7103 into operation after a few settings, which makes this chip easy to use and power saving.

The receiving part features a low-IF architecture with high receiving sensitivity and few external components. The received signal is amplified and down-converted to the intermediate frequency. Signal is demodulated by demodulator and then low pass filtered for the decision circuit. The output data can be accessed on the RX_DATA pin.

The transmitting part features a crystal-based architecture with a highly efficient power amplifier. In the ASK mode, data on the TX_DATA pin controls the ON/OFF of the output power. In the FSK mode, data on the TX_DATA pin modulates the output frequency of the phase-lock-loop, which directly drives the power amplifier.

9.1 Control Interface:

A7103A (434/315MHz band) supports both SPI and hardware-pin controlled interface. A7103B (868/915MHz band) supports SPI only.

9.1.1 Hardware-pin interface:

For general performance 13.56MHz crystal based application, user can only set hardware pins to configure chip as following connection. In this mode, the transmitter is in max output operation; the receiver is in low-side band operation, auto gain control (AGC) is enabled, pin 19 CLK_OUT outputs crystal frequency/16, and IF bandwidth is max.

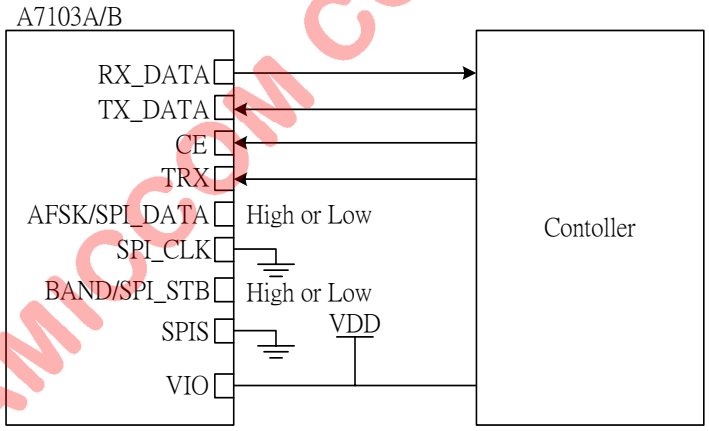


Fig 9.1.1

Pin No	Pin Name	Setting	Description
16	SPIS	0	Set to logic 0 to disable SPI
17	BAND/SPI_STB	0	RF band select to 315MHz band.
		1	RF band select to 434MHz band.
18	SPI_CLK	0	Set to logic 0 for normal operation.
19	ASK/SPI_DATA	0	Active mode select to FSK
		1	Active mode select to ASK

20	CE	0	Chip will into OFF mode.
		1	Chip will into Active mode.
21	TRX	0	Active mode select to RX
		1	Active mode select to TX

Table 9.1.1 Hardware pins setting

9.1.2 SPI interface:

User can control this chip through SPI to get more flexible configuration, such as multi RF channel, 4/12/13.56/16MHz crystal, IF bandwidth… The procedure includes only two steps:

Step 1: Write in RF and Crystal frequency to Register0.

Step 2: Write in Command (CEb, FASK, IFBW…) to Register1.

Please refer to section 9.2 SPI for full details.

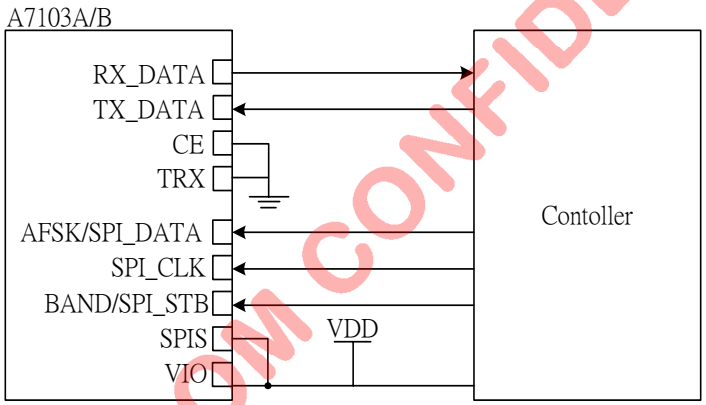


Fig 9.1.2

9.2 SPI

9.2.1 Registers

Register 0

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	R1	R0	NB7	NB6	NB5	NB4	NB3	NB2	NB1	NB0	NA3	NA2	NA1	NA0	1	1
Reset	0	1	1	0	1	1	1	1	0	0	0	0	1	0		

← Write in direction (D0 first)

Note: (1) D[1:0] are address bits.
(2) All bits will be reset to default value after VIO powered on.
(3) Address D[1:0]=[10] is reserved for internal test. Do not use for normal operation.
(4) Write in data (NA, NB) in 1's complement. For example, NA=15, NB=63.
Binary format NA=1111, NB=00111110.
Write in data should be 1's complement NA[3:0]=0000, NB[7:0]=11000001.

Register 0: Used for RF/Crystal frequency setting. $F_{RF} = F_{crystal}$ X N / 2R,

R[1:0]: Crystal reference frequency selection.

[11]: R=5 for 4MHz crystal.

[10]: R=15 for 12MHz crystal.

[01]: R=16 for 13.56MHz crystal.

[00]: R=20 for 16MHz crystal.

NB, NA: Binary format of PLL N counter. Used for RF frequency channel control.

For A7103A, N=(16XNB)+NA, NA=0~15; for A7103B, N=8X(NB+256)+NA, NA=0~7. Please refer to section 9.4 for detail calculation.

Register 1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	EAGC	TXP1	TXP0	ULS	CKS	ECK	X	IFB1	IFB0	BAND	FASK	CEb	RTX	CTLS	0	1
Reset	1	1	0	0	0	1	1	0	1	1	0	1	1	1		

Register 1: Used for command and parameters setting.

EAGC: Auto gain control (AGC) selection. 0: enable AGC, 1: disable AGC.

TXP[1:0]: TX output power control.

[11]: 10dBm (typ).

[10]: 7dBm (typ).

[01]: 3dBm (typ).

[00]: 0dBm (typ).

ULS: Receiver Up/Low side band selection. Used for TX/RX FDD application.

0: up side band .1:low side band.

CKS: Output clock (pin 24 CLK_OUT) divider ratio selection. 0: crystal frequency /4, 1: crystal frequency /16.

ECK: Output clock (pin 24 CLK_OUT) ON/OFF selection. 0: ON, 1: OFF.

X: Set to 1 for normal operation.

IFB[1:0]: IF filter bandwidth selection.

[11]: Min bandwidth.

[10]: Medium bandwidth.

[0X]: Max bandwidth.

BANDb: RF band selection.

For A7103A, 0: 434MHz band. 1: 315MHz band.

For A7103B, 0: 915MHz band. 1: 868MHz band.

FASK: ASK_FSK selection. 0: ASK. 1: FSK.

CEb: Chip enable. 0: enable. 1: disable.

TRX: Active mode (transmission/receiving) selection. 0: transmission 1: receiving.

CTLS: Control selection.

0: TRX and CE will be controlled by Register1 D3, D4. (IO pin 20, 21 will be don't cared.)

1: TRX and CE will be controlled by IO pin 20, 21. (Register1 D3, D4 will be don't cared.)

9.2.2 SPI timing

After STB turns high, data can be written in at the rising edge of CLK.

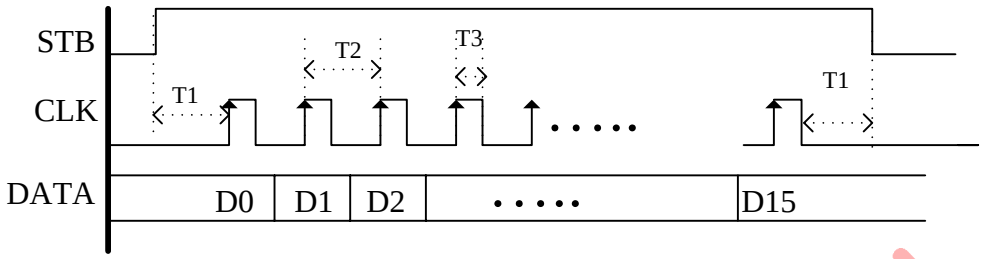


Fig 9.2.2 SPI timing

Name	Description	Min	Unit
T1	STB go high to first CLK rising edge	200	ns
T2	CLK period	200	
T3	CLK high hold time	40	

9.3 Operation Modes

9.3.1 OFF Mode.

All circuits will be turned off in this mode.

Pin		Register 1		Operation Mode
16 SPIS	20 CE	D2 CTLS	D4 CEb	
0	0	X	X	OFF
1	0	1	X	
1	X	0	1	

Table 9.3.1 OFF mode setting

9.3.2 Active Mode.

The chip enters either receiving or transmitting mode as described bellow.

SPI disabled (pin 16 SPIS =0). All register will be set to default values.

Pin		Operation Mode
20 CE	21 TRX	
0	X	OFF
1	0	Active, RX
1	1	Active, TX

Table 9.3.2.1 Active mode setting by hardware pins

SPI enabled (pin 16 SPIS =1).

Pin		Register 1			Operation Mode
20 CE	21 TRX	D2 CTLS	D3 RTX	D4 CEb	
1	0	1	X		Active, RX
1	1	1	X		Active, TX
X		0	1	0	Active, RX
X		0	0	0	Active, TX

Table 9.3.2.2 Active mode setting by SPI

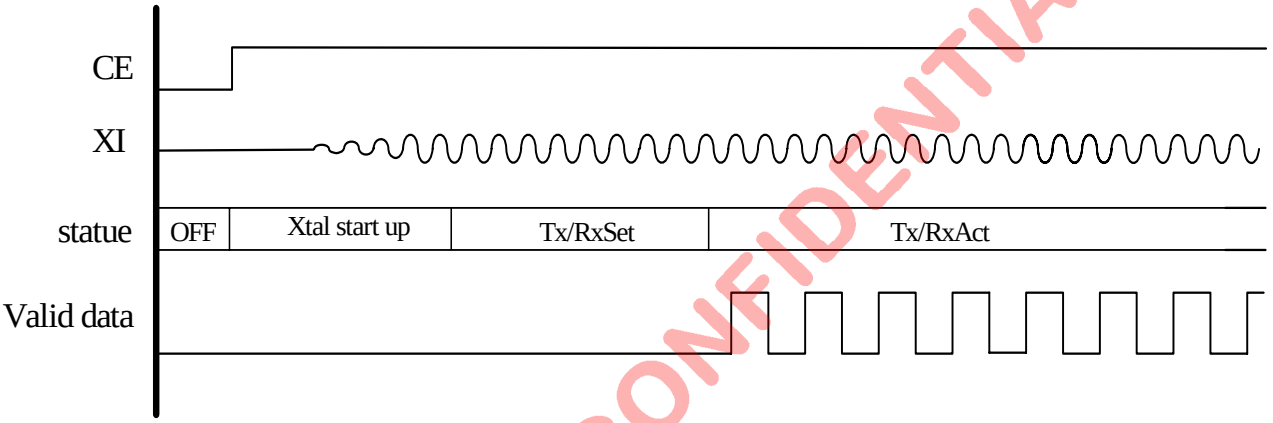


Fig 9.3.2 Start-up sequence

Name	Description	Time			Unit
		Mim	Typ	Max	
Xtal Start up[1)]	From OFF to Xtal stable		0.8		ms
Tx/RxSet	From Xtal stable to Tx/Rx circuit ready		1	1.8	

Table 9.3.2.3 Timing description

1) The stable time depends on the parallel capacitor (Ccomp) connected to XI, as shown in Fig 9.5.1. The time shown above assumes no parallel capacitor. For a 10pF capacitor, the stable time will be lengthened to 4ms typically.

9.3.4 Modulation and Band.

ASK/FSK modulation and 315/434MHz(A7103A), 868/915MHz(A7103B) frequency band can be set as following descriptions.

SPI disabled (pin 16 SPIS =0).

Pin		Operation Mode	Operation Mode
17 BAND/SPI_STB	19 AFSK/SPI_DATA	A7103A	A7103B
0	0	ASK, 315 band	ASK, 868 band
1	0	ASK, 434 band	ASK, 915 band
0	1	FSK, 315 band	FSK, 868 band
1	1	FSK, 434 band	FSK, 915 band

Table 9.3.4.1

SPI enabled (pin 16 SPIS =1).

Register 1		Operation Mode	Operation Mode
D6 BANDb	D5 AFSK	A7103A	A7103B
1	1	ASK, 315 band	ASK, 868 band
0	1	ASK, 434 band	ASK, 915 band
1	0	FSK, 315 band	FSK, 868 band
0	0	FSK, 434 band	FSK, 915 band

Table 9.3.4.2

9.4 RF and Reference Frequency Setting

A7103 supports multi RF frequency and up to four crystal frequencies, which can be set by different approach.

9.4.1 SPI disabled (A7103A only): $F_{RF} = F_{crystal}$ X N/32, Recommended crystal frequency is around 13.56MHz.

	315MHz	434MHz
N	743	1023
F_{RF} (MHz)[1)]	314.84625	433.49625

Table 9.4.1 RF channel frequency with SPI disabled

9.4.2 SPI enabled: $F_{RF} = F_{crystal}$ X N/(2XR), Recommended crystal can be 4[2)]/12/13.56/16MHz.

R could be 5, 15, 16 or 20.

Used crystal	4MHz	12MHz	13.56MHz	16MHz
Recommended R	5	15	16	20
SPI setting (R)	R[1:0]=[11]	R[1:0]=[10]	R[1:0]=[01]	R[1:0]=[00]

N could be 736~2319.

RF frequency band	315MHz	434MHz	868NHz	915MHz
Recommended N value	742~787	1022~1085	2171~2174	2256~2318
SPI setting (NA, NB)	N=(16XNB) + NA			

Table 9.4.2 RF channel frequency with SPI be enabled

For example:

4MHz crystal, 434MHz BAND, set N=1084→ F_{RF}=4X1084/(2X5)=433.6MHz.

12MHz crystal, 434MHz BAND, set N=1083→ F_{RF}=12X1083/(2X15)=433.2MHz.

13.56MHz crystal, 315MHz BAND, set N=787→ F_{RF} =13.56X743/(2X16)=314.846MHz.

16MHz crystal, 915MHz BAND, set N=2260→ F_{RF} =16X2260/(2X20)=904MHz.

1) F_{RF} is given for crystal=13.560000MHz.

2) 4MHz crystal has to be applied externally.

9.5 Reference Frequency Requirement

9.5.1 Crystal oscillator

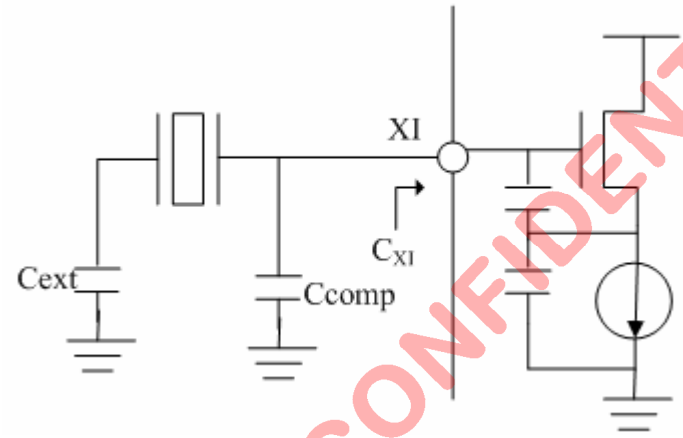


Fig 9.5.1

Crystal oscillator is Colpitts type oscillator with integrated feedback capacitors. Total input capacitance C_{XI} is about 10pF.

Cext is used to set the frequency align with transmitter for FSK application. It could be short to ground directly for ASK application.

Ccomp is an option used to compensate the load capacitance once the Cxi is too small for crystal default value.

9.5.2 Frequency tolerance

The crystal, RF, IF filter bandwidth and desired modulation signal bandwidth are all interrelated.

$\Delta RF_{TX} + \Delta RF_{RX} <$ Min IF filter bandwidth – Max Signal bandwidth

ΔRF_{TX} is total RF frequency tolerant of transmitter. Usually equal to F_{RF} × TX crystal ppm.

ΔRF_{RX} is total RF frequency tolerant of receiver. Usually equal to F_{RF} × RX crystal ppm.

For example:

F_{RF}=433.496MHz. ΔRF_{TX}= 100KHz (+/- 50KHz). Max Signal bandwidth 50KHz (FSK data rate 20Kbps with deviation 12.5KHz). Min IF filter bandwidth=180KHz.

Then $\Delta RF_{RX} <$ 180-50-100=30KHz. 30KHz/433.496MHz=70ppm (+/- 35ppm).

9.5.3 Sharing reference frequency with controller.

User can share RF and controller IC with one crystal as following two configurations. Reference clock can from RF side (divided by 4 or 16) to drive controller directly. Or from controller side send to RF

through an AC coupled capacitor.

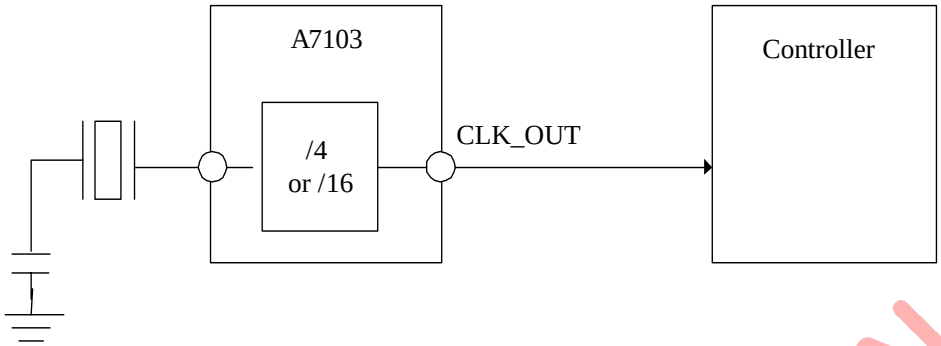


Fig 9.5.3.1 Crystal in RF side.

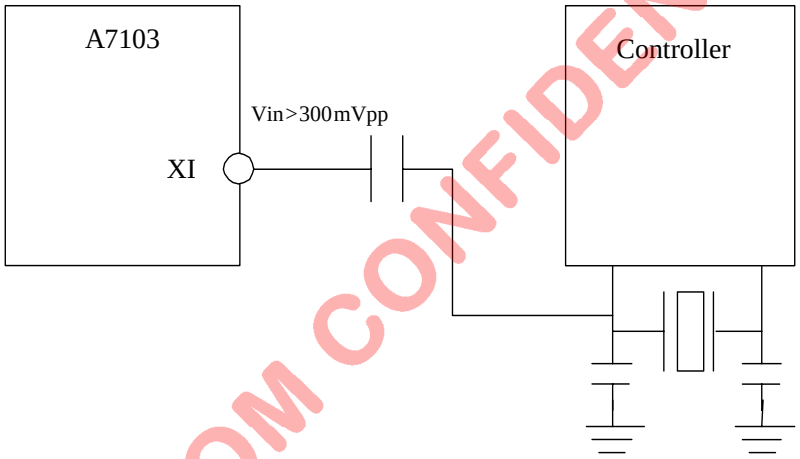


Fig 9.5.3.2 Crystal in controller side.

9.6 Data Filter

The data filter is composed of a second order multiple feedback low pass filter as shown in Fig 9.6. Two external capacitors can be adjusted for different data rates in order to obtain the best receiving sensitivity. Recommended component values are tabulated in Table 9.6 for 4.8, 9.6 and 20kbps application.

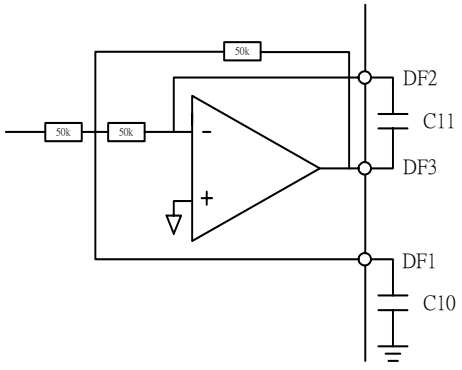


Fig 9.6

Data Rate (Kbps)	C10	C11
4.8	1nF	220pF
9.6	560pF	120pF
20	270pF	56pF

Table 9.6

Note: For other data rate, please contact AMICCOM's FAE for recommended values.

9.7 Transmitter

The power amplifier is composed of two stages with the input one directly driven by the internal divider-by-two circuit. The output stage, which dominates the overall power consumption, is carefully biased in class-C. An external inductor is required for the output matching of the power amplifier. Since A7103 has its input and output on the same port, the input matching for the low noise amplifier and the output matching for the power amplifier should be done simultaneously so that neither the receiving sensitivity not the transmitting power is severely sacrificed.

10. Application Circuit

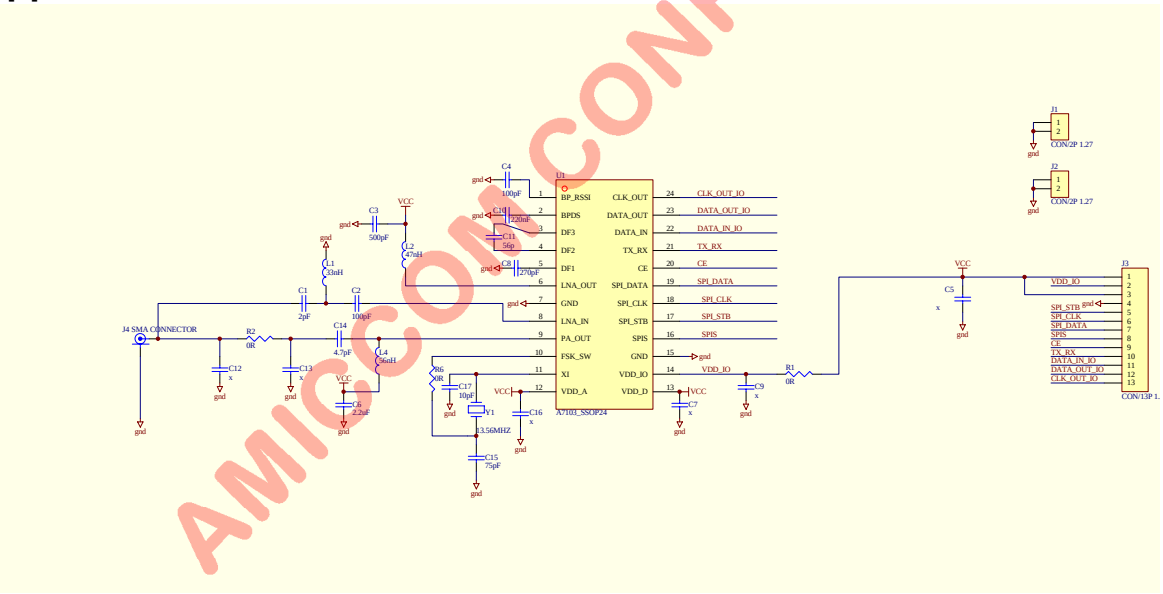


Fig 10.1 A7103A Application Circuit

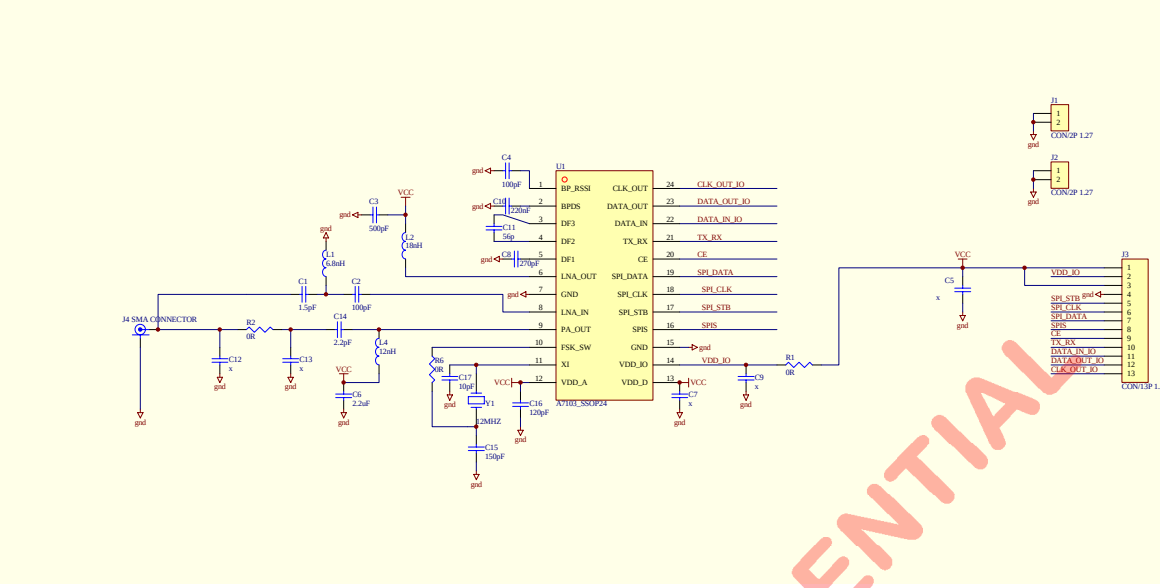


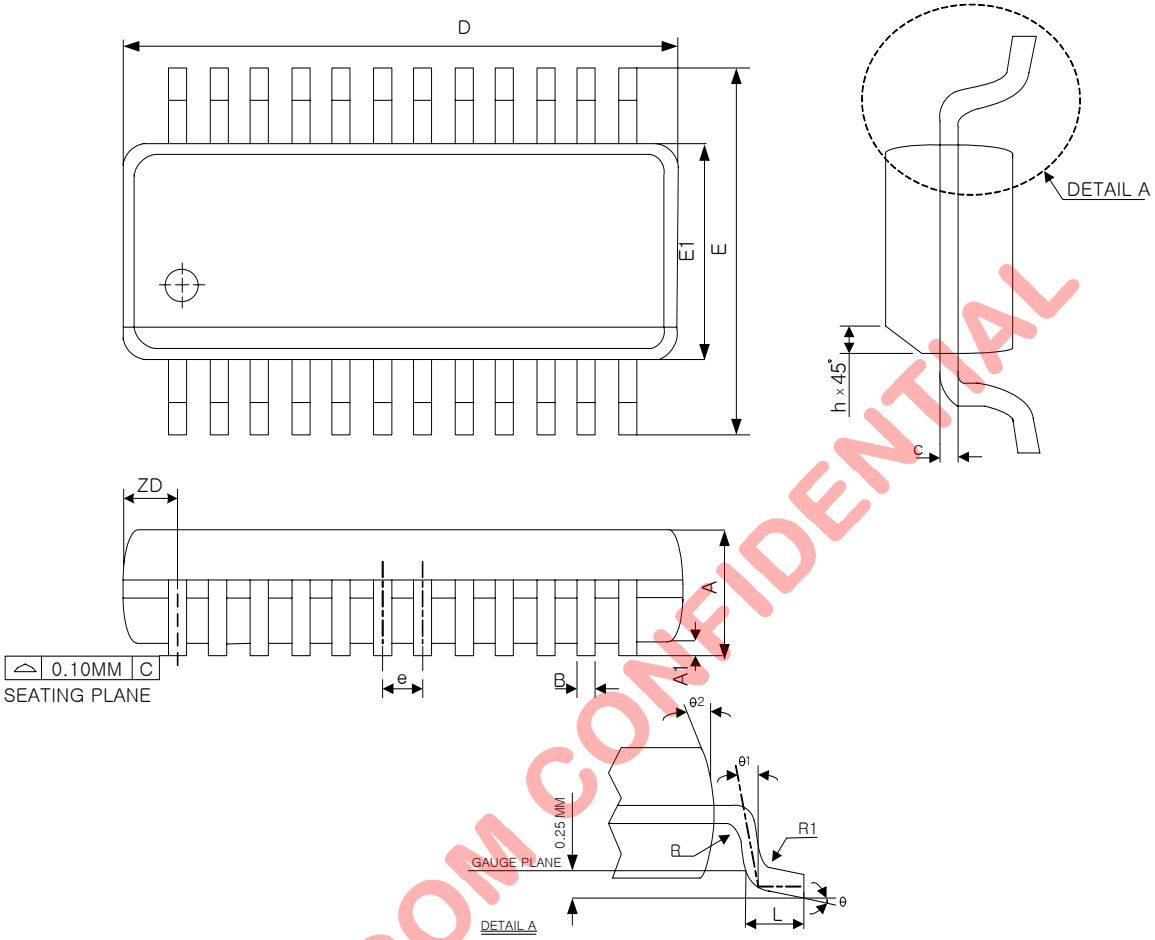
Fig 10.2 A7103B Application Circuit

11. Ordering Information

Part No.	Package	Units Per Reel / Tube
A71C03AUF/Q	SSOP 24L, Tape & Reel, Pb free, -40℃～85℃	3Kpcs
A71C03AUF	SSOP 24L, Tube, Pb free, -40℃～85℃	50pcs
A71C03BUF/Q	SSOP 24L, Tape & Reel, Pb free, -40℃～85℃	3Kpcs
A71C03BUF	SSOP 24L, Tube, Pb free, -40℃～85℃	50pcs

12. Package Information

SSOP24 Outline Dimensions



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NCM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			1.50			0.059
B	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e		0.635 BASIC			0.025 BASIC	
D	8.56	8.66	8.74	337	341	344
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
h	0.25		0.50	0.010		0.020
ZD		1.4732 REF			0.058 REF.	
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
θ	0°		8°	0°		8°
θ1	0°			0°		
θ2	5°	10°	15°	5°	10°	15°
JEOEC	M0-137 (AF)					