AMICCOM

A7102A

Preliminary ***315/433MHz FSK Transceiver***

Document Title

315/433 MHz FSK Transceiver

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue.	July 18th, 2007	Preliminary
0.1	Logo changed.	Nov. 5th, 2007	

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1. Typical Applications

- Wireless data communication
- Remote control
- Keyless entry
- Home automation
- Wireless toy

2. General Description

A7102A is a monolithic CMOS integrated circuit for wireless applications in 315/433MHz ISM band. The device is provided in a 32-lead plastic QFN5X5 packaging and is designed as a complete FSK transceiver up to 150kbps data rate.

3. Features

- Frequency bands: 315MHz/433MHz
- Programmable RF output power: up to 15dBm
- Low power consumption:
  RX:12mA, TX:20mA@0dBm
- Supply voltage 2.2 ~ 3.6V
- Programmable data rate up to 150kbps
- No external SAW Filter
- Optional RTC function
- On chip 8-bit ADC
- Integrated temperature sensor
- RSSI (Received Signal Strength Indicator)
- Programmable channel filter bandwidth
- Programmable carrier sense indicator
- RX clock recovery
- Frame synchronization recognition
- Optional FEC/CRC/data whitening
- Optional Manchester Data
- 64 bytes TX/RX FIFO buffer
- Extended FIFO up to 256 bytes
- Small 5x5 mm QFN32 package

4. Pin configuration

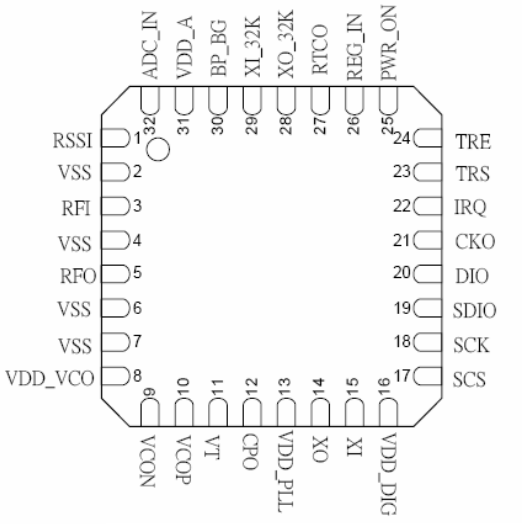

Fig.1 A7102 QFN package top view

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5. Block Diagram

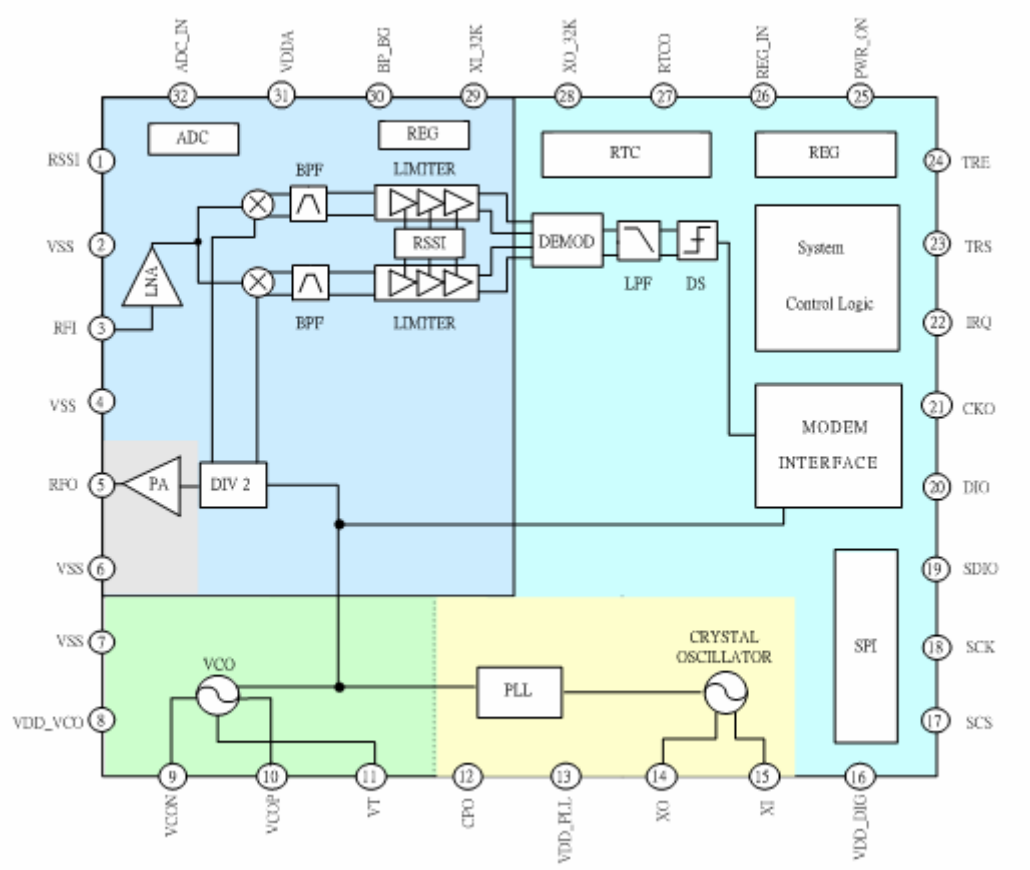


Fig.2 System Block Diagram

6. Specification (Ta=25℃, VDD=3.3V, data rate= 100kbps)

Parameter	Description	Minimum	Typical	Maximum	Unit
General					
Operating Temperature		-40		85	°C
Supply Voltage		2.2	3.3	3.6	V
Current Consumption Transceiver Circuit in 433MHz band	RX low gain mode		12		mA
	RX high gain mode		14		mA
	TX Mode @15dBm output		40		mA
	TX Mode @10dBm output		34		mA
	TX Mode @5dBm output		25		mA
	TX Mode @0dBm output		20		mA
	Synthesizer Mode		7.1		mA
	Standby Mode(x'tal on)		2.3		mA
	Standby Mode(x'tal off)		0.33		mA
	Sleep Mode			2	μA
Phase Locked Loop					
X'TAL Settling Time	couple=1, high current		0.45		ms
X'TAL frequency	@50K /100K Mode [1]		4/6/8/12.8		
	@150K Mode [1]		4/6/8/19.2		MHz
PLL Phase noise	PN @10k offset		75		dBc/Hz
	PN @100k offset		100		dBc/Hz
	PN @500k offset		115		dBc/Hz
Reference spur			65		dBc
PLL Settling Time @settle to 10Hz	C1=2.2nF,R2=820,C2=33nF,R3=22k, C3=33pF		70		μs
Transmitter					
TX Power	@ Maximum Power Setting		15		dBm
Power Control Range	0dBm ~15dBm		15		dB
TX Settling Time			60		μs
Receiver					
Sensitivity @BER=0.001, high gain mode	Data rate 50kbps@50K Mode [2]		-110		dBm
	Data rate 100kbps@100K Mode		-107		
	Data rate 150kbps@150K Mode		-104		
IF Frequency	@50K Mode		100		KHz
	@100K Mode		200		
	@150K Mode		300		
Receiver bandwidth	@50K Mode		50		KHz
	@100K Mode		100		
	@150K Mode		150		
Image Rejection			25		dB
RSSI Range	@RF input	-120		-70	dBm
RSSI linearity			-/+2		dB
RX Settling Time			150		μs

Note:

1. Crystal frequency can be chosen as 1 to 32X of 0.8MHz or 1 to 32X 1.2MHz.
2. Max Data rate= 50kbps @50K Mode, Max Data rate= 150kbps @150K Mode.

7. Pin Descriptions (I: input; O: output; OD: open drain output)

Pin No.	Symbol		Function Description
1	RSSI	O	RSSI bypass. Connect to external capacitor.
2	VSS	I	Analog ground.
3	RFI	I	RF input.
4	VSS	I	Analog ground.
5	RFO	O	RF output.
6	VSS	I	Analog ground.
7	VSS	I	Analog ground.
8	VDD_VCO	I	VCO Supply voltage.
9	VCON	I	VCO inductor negative connection pin
10	VCOP	I	VCO inductor positive connection pin
11	VT	I	Control voltage of VCO
12	CPO	O	Charge-pump output. This pin charges external capacitor to adjust VCO frequency.
13	VDD_PLL	I	PLL Supply voltage.
14	XO	I	Crystal oscillator node 2. Connect to external feedback capacitor.
15	XI	I	Crystal oscillator node 1. Connect to external feedback capacitor.
16	VDD_DIG	O	Digital supply voltage. Connect to bypass capacitor.
17	SCS	I	SPI chip select. Active low.
18	SCK	I	SPI/FIFO clock.
19	SDIO	IO	SPI/FIFO data.
20	DIO	IO	Bi-directional pin for direct mode. DATA input/output for TX/RX
21	CKO	O	Clock out. Can be configured to RCK (RX recovery clock) or DCK (TX data clock).
22	IRQ	O	Interrupt request. Can be configured to CD (carrier detect), SYNC (RX frame sync) or FP (FIFO packet).
23	TRS	I	TX/RX mode select. 0: RX, 1: TX.
24	TRE	I	TX/RX mode enable pin. Active high.
25	PWR_ON	I	Chip power on pin. Active high.
26	REG_IN	I	3.3V supply voltage input pin.
27	RTCO	O	32KHz clock output.
28	XO_32K	I	32KHz crystal oscillator node 2. Connect to external feedback capacitor.
29	XI_32K	I	32KHz crystal oscillator node 1. Connect to external feedback capacitor.
30	BP_BG	O	Bandgap bypass pin. Connect to external capacitor.
31	VDD_A	O	Analog Supply voltage. Connect to bypass capacitor.
32	ADC_IN	I	External input for on-chip ADC.

8. Absolute Maximum Ratings

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD)	GND	-0.3 ~ 3.6	Vdc
Other I/O pins range	GND	-0.3 ~ VDD+0.3	Vdc
Maximum input RF level		0	dBm
Storage Temperature range		-55 ~ 125	°C

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

9. Control Register

9.1 Control Register Summary

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h System clock	W	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
	R	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
01h PLL I	W				MDIV	RRC3	RRC2	RRC1	RRC0	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
02h PLL II	W	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
03h PLL III	W	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC34	MC24	MC1	MC0
	R	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC34	MC24	MC1	MC0
04h PLL IV	W					PDL2	PDL1	PDL0	HFB	VCS1	VCS0	CPS	CPC1	CPC0	SDPW	NSDO	EDI
05h Crystal	W							RTOE	RTCI	RTC1	RTC0	RTCE	XCC	XCP1	XCP0	CGS	XS
06h TX I	W				TME	GS	FDP2	FDP1	FDP0	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
07h TX II	W							TDL1	TDL0	TXDI	PAC1	PAC0	TDC1	TDC0	TBG2	TBG1	TBG0
08h RX I	W		DMT	MPL1	MPL0	SLF2	SLF1	SLF0	ETH1	ETH0	DMOS	DMG1	DMG0	BW1	BW0	ULS	HGM
09h RX II	W	RXDI	PMD1	PMD0	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0	DCL2	DCL1	DCL0	DCM1	DCM0
0Ah ADC	W							XADS	CDM	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
	R							VBD1	VBD0	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
0Bh FIFO	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
0Ch Code	W			WS6	WS5	WS4	WS3	WS2	WS1	WS0	MCS	WHTS	FECS	CRCS	IDL	PML1	PML0
0Dh Pin control	W							PCS	IRQI	IRQ1	IRQ0	IRQE	CKOI	CKO1	CKO0	CKOE	SCKI
0Eh Calibration	W		VTL2	VTL1	VTL0	VTH2	VTH1	VTH0	MVBS	MVB2	MVB1	MVB0	MIFS	MIF3	MIF2	MIF1	MIF0
	R	FCD4	FCD3	FCD2	FCD1	FCD0	DVT1	DVT0	VBCF	VB2	VB1	VB0	FBCF	FB3	FB2	FB1	FB0
0Fh Mode control	W								FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM
	R						FECF	CRCF	FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM

9.2 Control Register Description

Address 00h: System Clock Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

CSC [2:0]: Clock source counter. System clock = 64* IF clock= Clock source / (CSC[2:0]+1). Maximum divide ratio is 8.
GRC [4:0]: Clock generation reference counter. Clock generation reference= Crystal frequency / (GRC[4:0]+1). Maximum divide ratio is 32.
GRS: Clock generation reference frequency select. 0: 800 KHz, 1: 1.2 MHz.
SDR [6:0]: System clock to 128 data rate ratio. Data rate= System clock / (SDR[6:0]+1) / 128.

Address 01h: PLL (I)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MDIV	RRC3	RRC2	RRC1	RRC0	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
R/W				W	W	W	W	W	W	W	W	W	W	W	W	W
Reset				1	0	0	0	0	0	0	0	0	0	0	0	0

IP [7:0]: RF divider integer part setting. The divider number range is
If MDIV = 0, from 32 to 127.
If MDIV = 1, from 64 to 255.
RRC [3:0]: RF PLL reference counter. The divider range is from 1 to 16.
MDIV: RF divider range setting.

Address 02h: PLL (II)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FP [15:0]: PLL fractional part setting. The lock frequency is shown in the following
F = F_{xtal} / (RRC[4:0]+1) * (IP[7:0] + FP[15:0]/2**16), where F_{xtal} is crystal frequency.

Address 03h: PLL (III)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFC	FC14	FC13	FC12	FC11	FC10	FC9	FC8	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Reset																

MC [14:0]: PLL fractional part manual compensation value.
AFC: Auto frequency compensation. 0: Manual, 1: Auto.
FC [14:0]: PLL fractional part compensation value.

Address 04h: PLL (IV)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PDL2	PDL1	PDL0	HFB	VCS1	VCS0	CPS	CPC1	CPC0	SDPW	NSDO	EDI
R/W					W	W	W	W	W	W	W	W	W	W	W	W
Reset					0	0	0	0	0	0	0	0	0	0	0	0

EDI: EDI = 1, dither noise enable. DEDI = 0, dither noise disable.
NSDO: Mash sigma delta order setting, NSDO = 0, order 2. NSDO = 1, order 3.
SDPW: pulse width of sigma-delta modulator.
CPC [1:0]: Charge pump current setting.
[00]: 0.5mA.
[01]: 1.0mA.
[10]: 1.5mA.
[11]: 2.0mA.
CPS: Charge pump tri-state setting. 0: Tri-state, 1: Normal operation.
VCS [1:0]: VCO current setting.
HFB: Transceiver band selection. 0: low frequency band < 500 MHz, 1: high frequency band 500 MHz ~ 1 GHz.

PDL [2:0]: Delay for PLL settling. Delay= (PDL[2:0]+1)*(BW+1)*(RRC[3:0]+1)*(128/system clock).

Address 05h: Crystal Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RTOE	RTCI	RTC1	RTC0	RTCE	XCC	XCP1	XCP0	CGS	XS
R/W							W	W	W	W	W	W	W	W	W	W
Reset							0	0	0	0	0	0	0	0	0	0

XS: Crystal oscillator select. 0: disable, 1: Select.
CGS: Clock generation select. 0: disable, 1: Select.
XCP [1:0]: Crystal regulating couple setting.
XCC: Crystal current select. 1: high current, 0: low current
RTCE: RTC (real time clock). 1: Enable. The real time clock crystal is 32.768 KHz.
RTC [1:0]: RTC timer setting time. The RTC output toggles each setting time encountered.
[00]: 125 ms.
[01]: 500 ms.
[10]: 250 ms.
[11]: 1 s.
RTCI: RTC output invert. 0: normal, 1: Invert.
RTOE: RTC output enable. 0: High Z, 1: Enable.

Address 06h: TX (I)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TME	GS	FDP2	FDP1	FDP0	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
R/W				W	W	W	W	W	W	W	W	W	W	W	W	W
Reset				1	0	1	0	1	0	1	0	0	0	0	0	0

FD [7:0]: Frequency deviation setting.
If the Gaussain filter is off (GS = 0), the deviation is given by Fdev =0.5* F_{xtal} / (RRC[3:0]+1) * (FD[7:0]*$2^{FDP[2:0]}$/8/2^{16})
If the Gaussain filter is on (GS = 1), the deviation is given by Fdev =0.5* F_{xtal} / (RRC[3:0]+1) * (128*$2^{FDP[2:0]}$/8/2^{16})
FDP [2:0]: Frequency deviation exponential coefficient setting.
GS: Gaussain filter select. 1: Select.
TME: TX modulation enable. 1: Enable.

Address 07h: TX (II)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							TDL1	TDL0	TXDI	PAC1	PAC0	TDC1	TDC0	TBG2	TBG1	TBG0
R/W							W	W	W	W	W	W	W	W	W	W
Reset							0	0	0	0	1	1	0	1	1	1

TBG [2:0]: TX buffer gain setting.
TDC [1:0]: TX driver current setting.
PAC [1:0]: PA current setting.
TXDI: TX data inverted. 0: normal, 1: Invert.
TDL [1:0]: Delay for TX settling. Delay= (TDL[1:0]+1)*(BW+1)*(RRC[3:0]+1)*128/SYCK.

Address 08h: RX (I)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DMT	MLP1	MLP0	SLF2	SLF1	SLF0	ETH1	ETH0	DMOS	DMG1	DMG0	BW1	BW0	ULS	HGM
R/W		W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Reset		0	0	1	1	0	0	0	1	0	0	1	0	0	0	0

HGM: LNA high gain mode. 0: Normal, 1: High gain.
ULS: RX USB/LSB select. 0: USB, 1: LSB.
BW [1:0]: BPF Band-width selector.
[00]: 50 KHz.
[01]: 100 KHz.
[10]: 150 KHz.
[11]: Inhibit.
DMG [1:0]: Demodulator gain select.
[00]: x1.
[01]: x3.
[10]: x5.
[11]: x5.
DMOS: Demodulator over-sample select. 0: x64, 1: x32.
ETH [1:0]: Sync word error bit number threshold. [00]: 0 bit, [01]:1bit, [10]: 2bits, [11]:3 bits. Recommend value= [01].

SLF [2:0]: symbol recovery loop filter setting.
MLP [1:0]: symbol recovery loop filter setting after SYNC ok.
DMT: Reversed. It should be set to 0 for normal operation. 0: Normal, 1: Demodulator test.

Address 09h: RX (II)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXDI	PMD1	PMD0	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0	DCL2	DCL1	DCL0	DCM1	DCM0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	1	1	1

DCM [1:0]: the mode of dc average output setting.
[00]: DC set by DCV [7:0].
[01]: DC estimated by preamble.
[10]: DC estimated by ID.
[11]: DC estimated by data.
DCL [2:0]: the data length of dc average setting.
DCV [7:0]: the dc value setting by SPI.
PMD [1:0]: The length of preamble pattern detection. [00]: 0 bits, [01]: 4 bits, [10]: 8 bits, [11]: 16 bits. The detect length should be less than the preamble length PML.
RXDI: RX Data inverted. 1: Invert.

Address 0Ah: ADC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							XADS	CDM	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
R/W							W	W	W	W	W	W	W	W	W	W
Reset							0	0	0	0	1	1	0	1	1	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							VBD1	VBD0	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
R/W							R	R	R	R	R	R	R	R	R	R
Reset																

XADS: External ADC source. 0: internal, 1: external.
CDM: Carrier detector measurement. 0: RSS/T measurement mode, 1: CD measurement mode.
RTH [7:0]: RSSI threshold for carrier detector (CD).
CD=1 for ADC ≦ RTH, CD=0 for ADC ≧ RTH in RX mode.
ADC [7:0]: ADC output.
RX state: Digital RSSI output. PWR_{RSSI} = -110dbm + 40 * RSSI [7:0] / 8.
Non-RX state: Digital thermometer output. The temperature slope is around +2 ℃ / LSB.
VBD [1:0]: VCO bias detect.

Address 0Bh: FIFO

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Reset	0	1	0	0	0	0	0	0	0	0	1	1	0	1	1	1

FEP [7:0]: TX/RX FIFO end pointer in byte. FIFO mode packet stops when extended FIFO pointer= FEP [7:0]+1.
PSA [5:0]: TX FIFO packet start address in byte.
FPM [1:0]: TX/RX FIFO pointer margin threshold.

Setting	Bytes in TX FIFO	Bytes in RX FIFO
[00]	4	60
[01]	8	56
[10]	12	52
[11]	16	48

Address 0Ch: Code control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			WS6	WS5	WS4	WS3	WS2	WS1	WS0	MCS	WHTS	FECS	CRCS	IDL	PML1	PML0
R/W			W	W	W	W	W	W	W	W	W	W	W	W	W	W
Reset			0	1	0	1	0	1	0	0	0	0	0	1	0	1

PML [1:0]: Preamble length= PML+1 bytes.
IDL: ID length. 0: 2 bytes, 1: 4 bytes.

CRCS: CRC select. 1: Select. The CRC is CCITT-16 CRC.
FECS: FEC select. 1: Select. The FEC is (7, 4) Hamming code.
WHTS: Data whitening select. 1: Select. The data is whitening by multiplying PN7.
MCS: Manchester code select. 1: Select.
WS [6:0]: Whitening seed.

Address 0Dh: Pin Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							PCS	IRQI	IRQ1	IRQ0	IRQE	CKOI	CKO1	CKO0	CKOE	SCKI
R/W							W	W	W	W	W	W	W	W	W	W
Reset							0	0	0	0	0	0	0	1	0	1

SCKI: SPI clock invert. 1: Invert.
CKOE: CKO pin output enable. 0: High Z, 1: Enable.
CKO [1:0]: CKO select.
[00]: BCK (bit clock).
[01]: MRCK (modulation rate).
[10]: FPF (FIFO pointer flag).
[11]: Reversed.
When Manchester code is selected, BCK is the bit clock of Manchester code that equals half modulation rate. In such case, BCK will appear after TX modulation start in TX mode or internal frame sync in RX mode. On the other hand, BCK equals modulation rate.
When [11] selected, the output is the logic OR of EOP, EOVBC, EOFBC, EOADC and OKADC.
CKOI: CKO invert. 1: Invert.
IRQE: IRQ pin output enable. 0: High Z, 1: Enable.
IRQ [1:0]: IRQ function select.

	TX state	RX state
[00]	WPLL state & TX state(WTR)	WPLL state & RX state(WTR)
[01]	End of Access code (EOAC)	Access code matched (FSYNC)
[10]	TX modulation enable (TMEO)	carrier detected (CD)
[11]	None	External FSYNC input (for direct mode)

When IRQ set to [11] and direct mode is selected, the internal frame sync function will be disabled. In such case, it is recommended that user assure frame sync signal to this input to get better DC estimation of demodulation.
IRQI: IRQ output invert. 0: normal, 1: Invert.
PCS: TRE and TRS pin control. 0: Register control, 1: Pin control.

Address 0Eh: Calibration

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VTL2	VTL1	VTL0	VTH2	VTH1	VTH0	MVBS	MVB2	MVB1	MVB0	MFBS	MFB3	MFB2	MFB1	MFB0
R/W		W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Reset		0	0	0	0	0	0	0	1	0	0	0	0	1	1	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FCD4	FCD3	FCD2	FCD1	FCD0	DVT1	DVT0	VBCF	VB2	VB1	VB0	FBCF	FB3	FB2	FB1	FB0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Reset																

MFB [3:0]: Manual IF filter bank setting.
MFBS: Manual IF filter bank select. 0: FB, 1: MFB.
MVB [2:0]: Manual VCO bank setting. VCO frequency increases when MVB decreases.
MVBS: Manual VCO band select. 0: VB, 1: MVB.
VTH [2:0]: VT high threshold setting for VCO calibration.
[000]→ VTH=Vdd-0.1V　[100]→ VTH=Vdd-0.5V
[001]→ VTH=Vdd-0.2V　[101]→ VTH=Vdd-0.6V
[010]→ VTH=Vdd-0.3V　[110]→ VTH=Vdd-0.7V
[011]→ VTH=Vdd-0.4V　[111]→ VTH=Vdd-0.8V
VTL [2:0]: VT low threshold setting for VCO calibration.
[000]→ VTL=0.1V　[100]→ VTL=0.5V
[001]→ VTL=0.2V　[101]→ VTL=0.6V
[010]→ VTL=0.3V　[110]→ VTL=0.7V
[011]→ VTL=0.4V　[111]→ VTL=0.8V

FB [3:0]: IF filter bank.
FBCF: IF filter bank auto calibration flag. 0: Pass, 1: Fail.
VB [2:0]: VCO bank.
VBCF: VCO bank auto calibration flag. 0: Pass, 1: Fail.
DVT [1:0]: Digital VT output. VT of VCO will be compared with VT threshold set by VTH.
[00]: VT< VTL< VTH.
[01]: VTL< VT< VTH.
[10]: No used.
[11]: VTL< VTH< VT.
FCD [4:0]: IF filter calibration deviation from goal. 0: No deviation.

Address 0Fh: Mode Control

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name								FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM
R/W								W	W	W	W	W	W	W	W	W
Reset								0	0	0	0	0	0	0	0	0

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name						FECF	CRCF	FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM
R/W						R	R	R	R	R	R	R	R	R	R	R
Reset						0	0	0	0	0	0	0	0	0	0	0

ADCM: ADC measurement. 0: disable, 1: Measure. It will be cleared after measurement done in single mode.
RX state: RSSI measurement.
Non-RX state: Temperature measurement.
FBC: IF filter bank calibration. 1: Calibrate. It will be cleared after calibration done.
VBC: VCO bank calibration. 1: Calibrate. It will be cleared after calibration done.
TRER: TRX enable register. 1: Enable. It will be cleared after end of packet encountered in FIFO mode.
TRSR: TRX mode select register. 0: RX, 1: TX. When TRE register set, the chip will enter TX or RX mode by TRS register.
PLLE: PLL enable. 1: Enable.
CER: Chip enable register. 1: Enable.
FMS: FIFO mode select. 0: Direct mode, 1: FIFO mode.
FMT: Reserve. It should be set to 0 for normal operation.
0: Normal, 1: FIFO mode test. When test mode set, FIFO mode should be selected. It will be cleared after end of packet encountered in FIFO mode.
CRCF: CRC error flag. 0: normal, 1: Error.
FECF: FEC error flag. 0: normal, 1: Error.

10. 3 Wires Series Interface

A7102 RF chip can be control via 3-wires SPI-compatible interface. (SCS, SCK, SDIO).

During each write-cycle, 16 bits are sent on the SDIO line. *A7* is the MSB (Most Significant Bit) and is sent as the first bit. This bit is the R/W bit (high for write, low for read). The next seven bits of each data frame (*A6:0)* are the CMD and address-bits. The 16 data-bits are then transferred (*D15:0*). During address and data transfer the SCS must be kept low. The clocking of the data on SDIO is done on the positive edge of SCK. Data should be set up on the negative edge of SCK by the microcontroller. When the last bit, *D0*, of the 16 data-bits has been loaded, the data word is loaded into the internal configuration register. The configuration data will be retained during a programmed power down mode, but not when the power supply is turned off. The registers can be programmed in any order.

The configuration registers can also be read by the microcontroller via the same configuration interface. The R/W bit is set low to initiate the data read-back first then the seven address bits are sent. A7102 then returns the data from the addressed register. SDIO is used as the data output and must be configured as an input by the microcontroller. The SDIO is set at the negative edge of SCK and should be sampled at the negative edge.

10.1 SPI format:

RW/CMD/Address byte (8bits)								Data word (16 bits)															
R/W	Command			Address				Data															
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The address byte further contains three parts:
Bit 7: R/W command. 0: read from slave register, 1: write to slave register.
Bit [6:4]: Command.
[00x]: read/write control register.

[01x]: read/write ID code.
[10x]: read/write FIFO register.
[110]: reset TX/RX FIFO pointer.
[111]: reset RF register.

Bit [3:0]: Register address. It maps to register address [0000] ~ [1111].

Command table:

Address Byte								Description
b7	b6	b5	b4	b3	b2	b1	b0	
0	0	0	x	A3	A2	A1	A0	Write data to control register A[3:0]
1	0	0	x	A3	A2	A1	A0	Read out data A[3:0] from control register
0	0	1	x	x	x	x	x	Write ID code command
1	0	1	x	x	x	x	x	Read out ID code command
0	1	0	x	x	x	x	x	TX FIFO write command
1	1	0	x	x	x	x	x	RX FIFO read command
X	1	1	1	x	x	x	x	RF chip Reset command
0	1	1	0	x	x	x	x	TX FIFO address pointer reset command
1	1	1	0	x	x	x	x	RX FIFO address pointer reset command

Note：x – Don't care

Data words:
Bit [15:0]: data bits.

10.2 Series interface Timing chart:

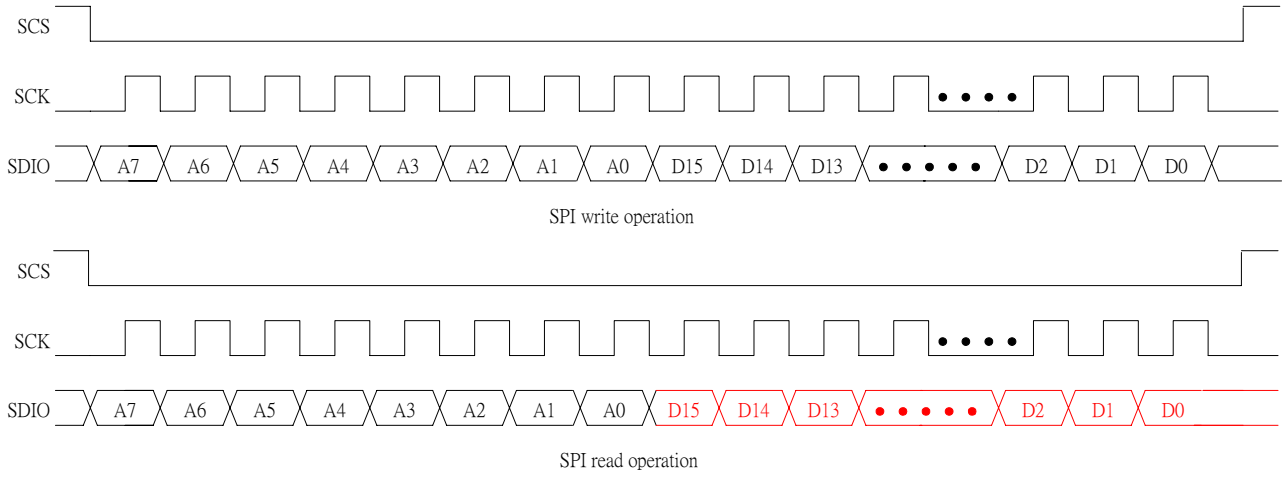


Fig3. 3 wires SPI read/write sequence

10.3 control register access

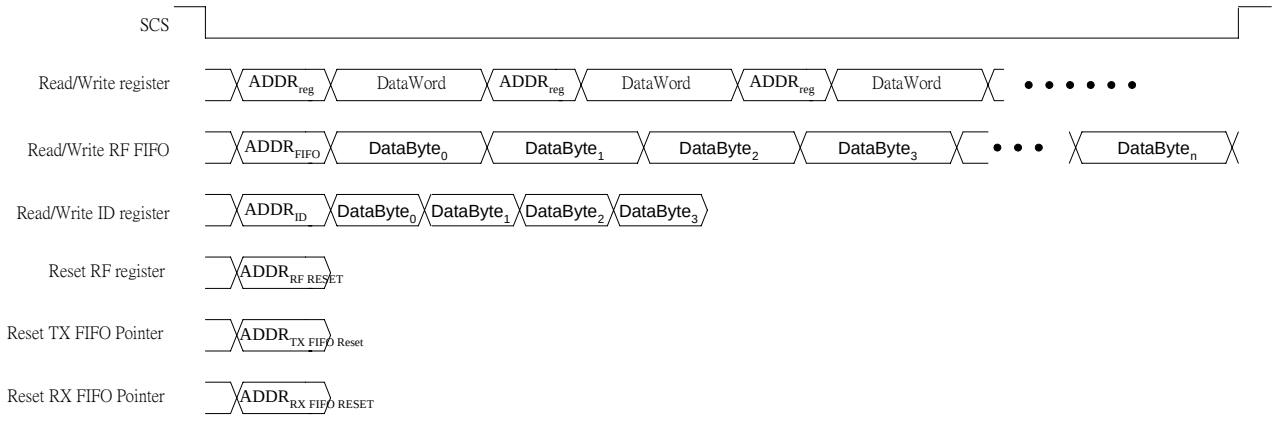
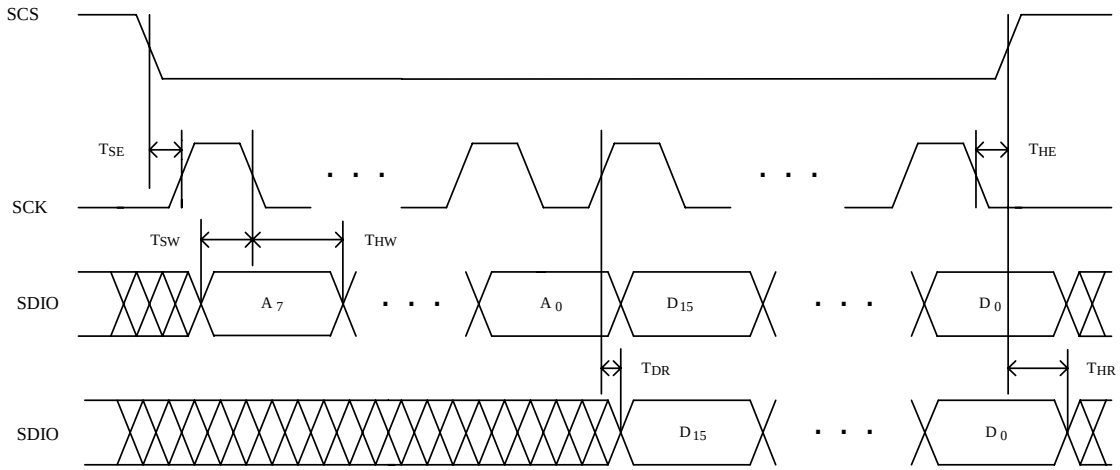


Fig4. Control register access type

10.4 Series Inetrface Timing Specification



Parameter	Description	Min.	Max.	Unit
F_C	SPI clock frequency.		10	MHz
T_{SE}	SCS setup time.	50		ns
T_{HE}	SCS hold time.	50		ns
T_{SW}	SDIO setup time.	50		ns
T_{HW}	SDIO hold time.	50		ns
T_{DR}	SDIO delay time.	0	100	ns
T_{HR}	SDIO hold time.	0		ns

10 .5 RF chip Reset Command

A7102 RF chip equipped a power on reset circuit to reset the register value when the chip is power on. Besides, users also can use RF chip reset command to reset the register content of the chip.

There are two ways to write the Reset Command via SPI interface, the timing sequences are shown as follows:
In both cases, chip is reset at the falling edge of SCK at bit A4.

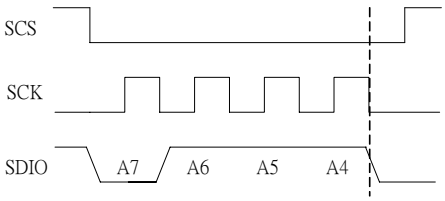


Fig. 5 Timing sequence of Reset Command 1

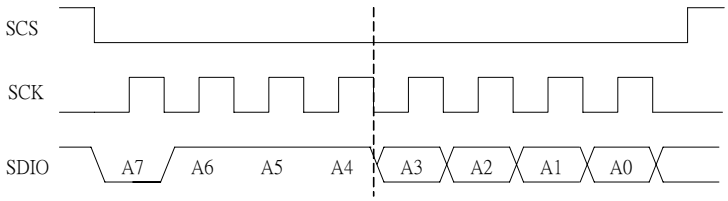
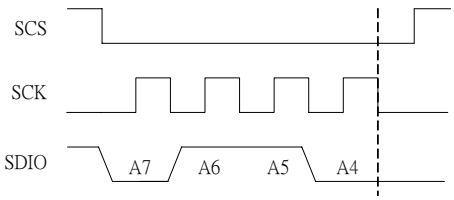


Fig.6 Timing sequence of Reset Command 2

10.6 TX FIFO Pointer Reset

There are two ways to reset the address pointer of TX FIFO via SPI interface, the timing sequences are shown as follows:
In both cases, address pointer of TX FIFO is reset to 0x00 at the falling edge of SCK at bit A4.



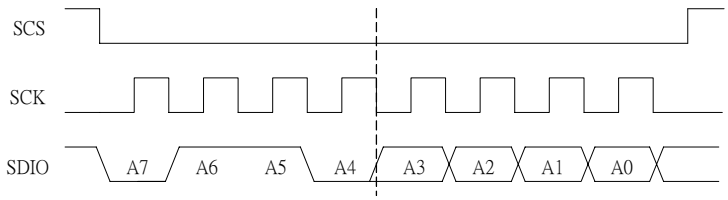


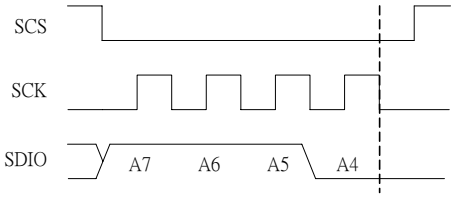
Fig.7 Timing sequence of TX FIFO pointer reset 1

Fig.8 Timing sequence of TX FIFO pointer reset 2

10.7 Rx FIFO Pointer Reset

There are two ways to reset the address pointer of RX FIFO via SPI interface, the timing sequences are shown as follows:

In both cases, address pointer of RX FIFO is reset to 0x00 at the falling edge of SCK at bit A4.



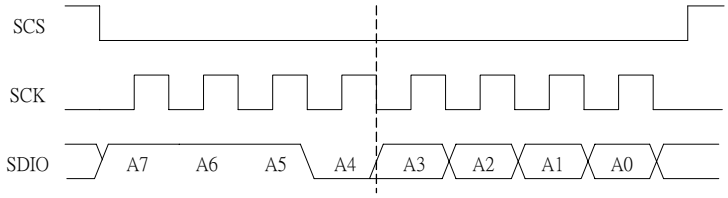


Fig.9 Timing sequence of RX FIFO pointer reset 1

Fig.10 Timing sequence of TX FIFO pointer reset 2

10.8 ID Read/Write Command

A7102 ID can be read or written via SPI interface, the timing sequences are shown as follows:

First execute the ID Red/write command in address byte, and then write data bytes with length of the 4 bytes.

IF the data length is only 2 bytes, user should set SCS=1 after Data Byte 1 to end the action of ID Read/ Write. Or after the completion of read/write Data Byte 0,1,2,3, the chip will end the read/write action automatically. Each ID code read/write action begins with DataByte0.

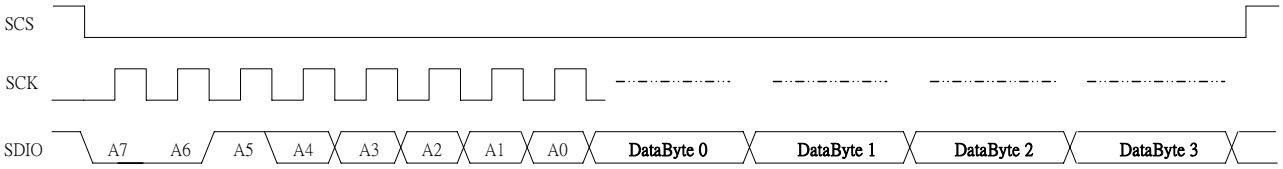


Fig.11 ID write command timing sequence

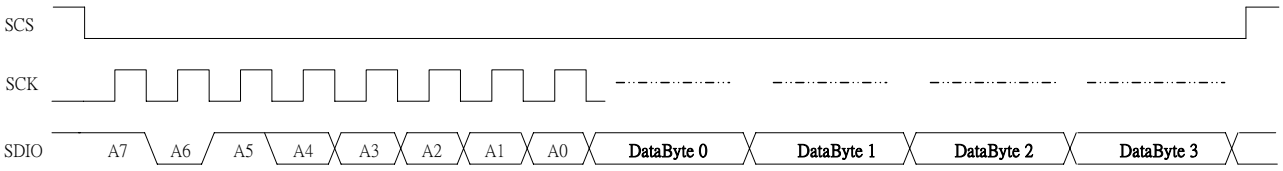


Fig.12 ID Read command timing sequence

11 Crystal oscillator

The internal crystal oscillator or an external clock signal can be used as the frequency reference of A7102 RF chip.

11.1 internal crystal oscillator

Crystal is connected to A7102 via pins XI and XO as shown in fig.13. Loading capacitors should be chosen properly for each crystal. The XS bit should set to 1 to enable the crystal oscillator. The oscillator circuit is amplitude regulated, user can set the bits XCP [1:0] to obtain the optimized crystal start-up time and current consumption.

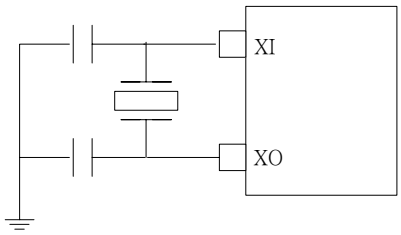


Fig.13 Crystal oscillator circuit

11.2 external clock source

An external clock source can be used as the reference clock of A7102, it should be connected to pin XO of A7102 and pin XI should be left open. AC coupling capacitor is integrated in A7102 so no capacitor is required on board, as shown in Fig.14.

Amplitude of clock source is about +2.0 ~ +2.5VPP. Note that the purity of clock source will affect the performance of RF chip. User should also set XS bit =0 to shut down the on-chip crystal oscillator to reduce the power consumption.

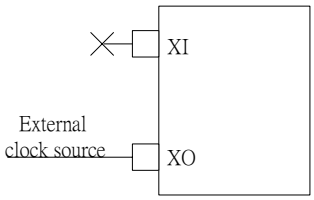


Fig.14 Connection of external clock source to A7102

12. System Clock

For A7102 to operate correctly, system clock must be set to correct value via the setting of related counters and clock generation circuit.

First consider the data rate used to determine the IF clock. If data rate <=50kbps, clock should set to 100 kHz. For 50kbps < data rate < 100kbps, the internal IF CLK should be set to 200 kHz. If 100kbps < data rate < 150kbps, the internal IF CLK should be set to 300 kHz. After determine the IF clock, the parameters on **System Clock Register** should be set as follows:

If crystal oscillator is used:

CSC = (Crystal frequency / 64*IF CLK) – 1
= (Crystal frequency / 12.8M) – 1　　for (data rate = 100kbps)
= (Crystal frequency / 19.2M) – 1　　for (data rate = 150kbps)

where CSC must be integral. The (CSC+1) is Crystal frequency to 64*IF frequency ratio (binary format).

To release the un-convenience restriction of specific crystal frequency, user can select the on-chip clock generation function to adopt other crystal frequency rather than 64*N*IF frequency. The clock generation circuit consists by counter GRCC and PLL circuit to generate a 38.4MHz clock source. The reference frequency of PLL can be chosen to be 0.8MHz or 1.2MHz by setting the GRCK bit. Then the crystal frequency can be determined by the following equation:

Crystal or external clock source = (GRC[4:0]+1)*GRCK

The above equation explains why the crystal frequency must choose a multiple of 800KHz for 100k mode and 1.2MHz for 150k mode, the tolerance within +/-20ppm of crystal frequency is recommended. This clock source is also used as the clock of on-chip ADC.

Please note that the TX data must be synchronized with chip's system clock (crystal frequency) when chip is operating in DIRECT mode. By setting the SDR counter value, the data rate clock can be divided from the system clock:

Data rate clock = (clock source)/(SDR[6:0]+1)/128

User can refer to the Fig.15 and Fig.16 for more detailed.

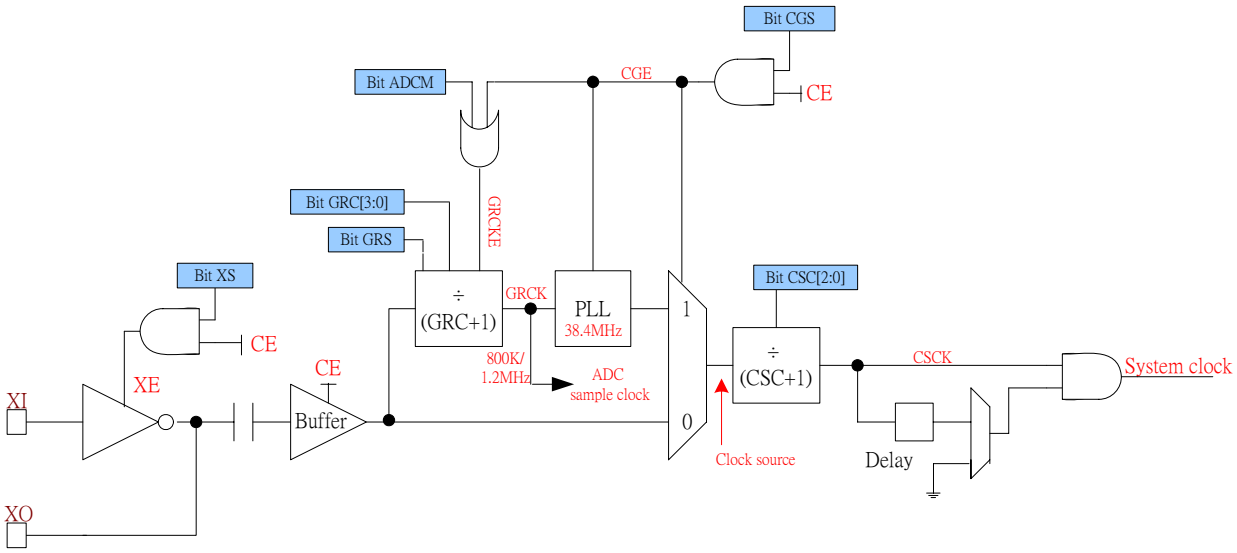


Fig.15 Block diagram of system clock

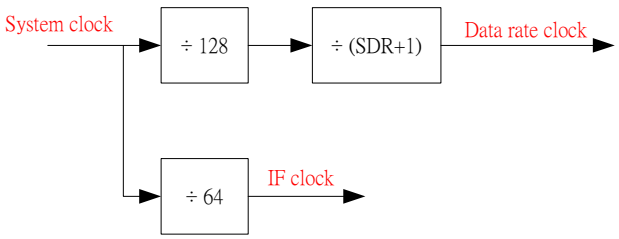


Fig.16 Relation of system clock to IF clock and data rate clock

12.1 clock generation

If 12.8MHz and/or 19.2MHz crystal are available, the clock source can be obtained directly from the output of crystal oscillator. The CGS bit in crystal register should set to 0. When 12.8MHz and 19.2MHz crystal are not available, user can enable the on-chip clock generation circuit to obtain the required clock source.

12.1.2 GRCK = 800KHz

If the frequencies of available crystal or the external clock source are 4, 8, 12, 16 and 20MHz etc, select the reference clock signal to 800KHz to generate the 38.4MHz clock source. Set CGS bit of crystal register to 1 and GRS bit to 0. Besides, user should set the correct counter value (GRC) to obtain the 800KHz GRCK.

11.1.3 GRCK = 1.2MHz

If the frequency of available crystal or the external clock source is 6MHz, select the reference clock signal to 1.2MHz to generate the 38.4MHz clock source. Set CGS bit of crystal register to 1 and GRS bit to 1. Besides, user should set the correct counter value (GRC) to obtain the 1.2MHz GRCK.

Table.1 Reference table for crystal source setting:

Crystal source	CGS	GRS	GRC[4:0]	description
12.8MHz	0	0	15	Clock-generation circuit disabled, GRCK=800KHz。
19.2MHz	0	0	23 or 15	Clock-generation circuit disabled, GRCK=00KHzor1.2MHz。
4MHz	1	0	4	Enable clock generation function, with GRCK=800KHz，generate 38.4MHz clock source。
8MHz	1	0	9	Enable clock generation function, with GRCK=800KHz，generate 38.4MHz clock source。
12MHz	1	0	14	Enable clock generation function, with GRCK=800KHz，generate 38.4MHz clock source。

16MHz	1	0	19	Enable clock generation function, with GRCK=800KHz，generate 38.4MHz clock source。
6MHz	1	1	4	Enable clock generation function, with GRCK=1.2MHz，generate 38.4MHz clock source。

13. Operation frequency setting

The system operation frequency of A7102 is set using the following characters:

Crystal: The external X'TAL frequency.
IP: The integer part of divider value.
FP: The fractional part of divider value.
PFD frequency: PLL phase frequency detector comparison frequency=crystal/(RRC+1).

A7102 RF chip can operate in any frequency in the ISM band. According to the formula listed below to calculate the values of IP, FP and R for the desired operating frequency, then set the corresponding contents of PLL I, II registers. The block diagram of A7102 system frequency is shown in Fig.17.

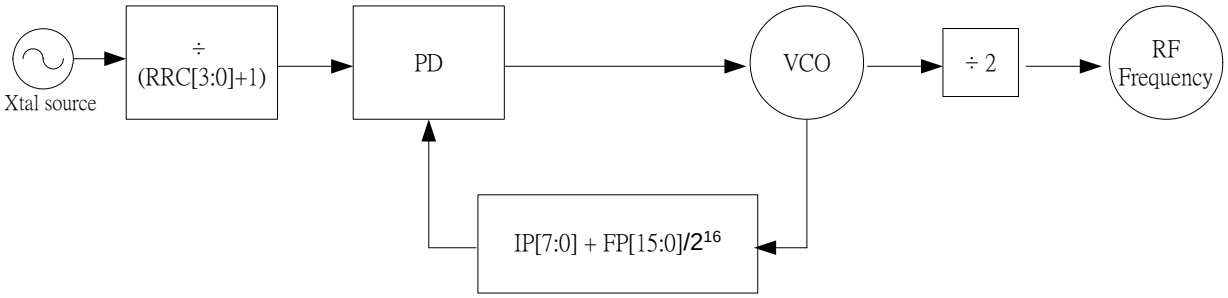


Fig.17 Frequency synthesizer block diagram

13.1 Setting of PLL I 及 PLL II

Formula: $$f_{RF} \cdot 2 = \frac{f_{xtal}}{RRC[3:0]+1} \cdot (IP[7:0] + \frac{FP[15:0]}{2^{16}})$$

For reference frequency(PD), suggested value is ≧ 40 *(data rate)
For example: RF freq=433.2MHz, X'tal=12.8MHz, PD=12.8MHz

$$PD = \frac{f_{xtal}}{RRC[3:0]+1}$$

=> RRC[3:0] = (f_{xtal} / PD) – 1
RRC[3:0] = (12.8 / 12.8) - 1 = 0

$$PD = \frac{2 \cdot f_{RF}}{IP[7:0] + \frac{FP[15:0]}{2^{16}}}$$

=> IP[7:0] + FP[15:0]/ 2^{16} =(2* f_{RF}) / PD
IP[7:0] + FP[15:0]/ 2^{16} = (2*433.2) / 12.8 = 67.6875

IP[7:0] = 67
FP[15:0] / 2^{16} = 0.6875,　　FP[15:0] = 0.6875 * 2^{16} = 45056

To determine the MDIV bit
32 ≤ IP[7:0] ≤ 67 , bit MDIV is set to 0
68 ≤ IP[7:0] ≤ 255 ,bit MDIV is set to 1

IP[7:0] = 67 ，so bit MDIV can be set to 0 or 1.

14. State machine

The A7102 have six main states: Sleep state, SB state(standby), WPLL(waiting PLL) state, TX state, RX state, CAL state, The state diagram of these states are shown in the figure 18.

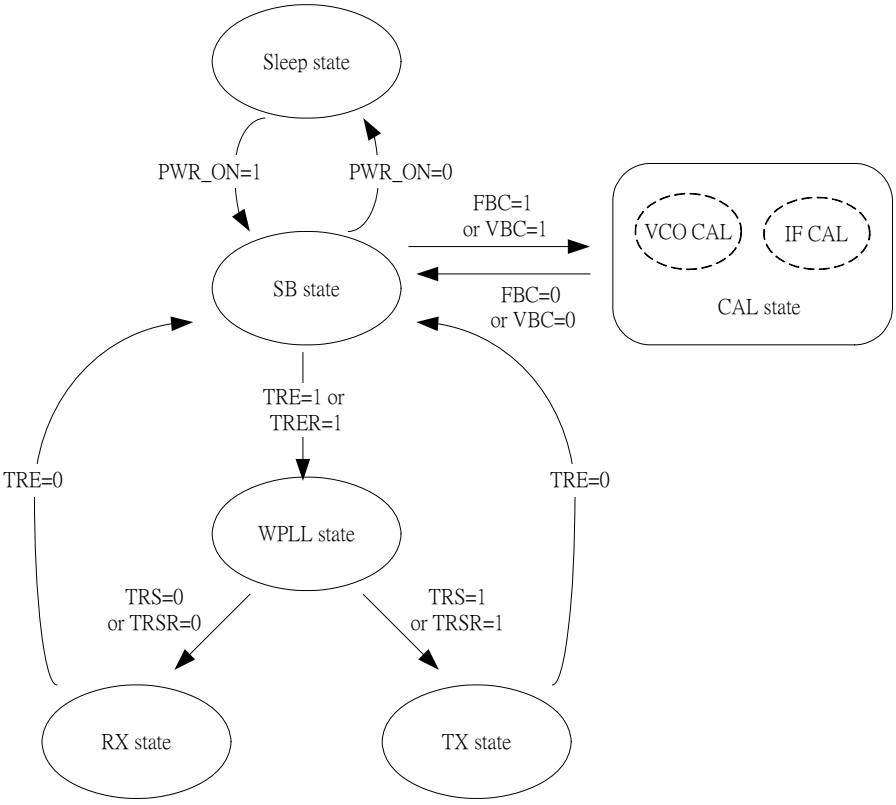


Fig.18 System state machine

Sleep state: when pin PWR_ON=0，RF chip enters sleep state。

SB state: when pin PWR_ON=1，RF chip will leaves from Sleep state and enters SB state. According to the value of bit CER and PLLE, RF chip will turn on or turn off the internal crystal oscillation circuit, bandgap reference circuit, and PLL circuit.
Ex. If bit CER=0, PLLE=0, on-chip band gap and crystal oscillator circuit will be off.
If bit CER=1, PLLE=0, on-chip band gap and crystal oscillator circuit will be on.
If bit CER=X, PLLE=1，PLL circuit is on.

WPLL(waiting PLL) state: in this state, according to the register contents of PLL (I), PLL(II), PLL(III), and PLL(IV) are changed or not, RF chip will determine the which state it will enter into, or to just stay on present state.

If the settings are changed, before RF chip enter TX/RX state, RF chip will automatically delay a period of time called PLL settling time. The length of PLL settling time is set by the PDL[2:0] in PLL register.
After this delay time, RF chip enter into TX/RX state.

TX/RX state: when pin TRE=1(or bit TRER=1), rf chip will enters TX or RX state according to the bit TRS (or bit TRSR). If use pin TRE and TRS to execute mode control, when pin TRS=1 and TRE=1，then enter into TX state, and RF power on, when pin TRS=0, and TRER=1, then enter into RX state.
In FIFO mode, after entering TX state, Rf chip will automatically delay a time called TX settling time. The length of PLL settling time is set by the TDL[1:0] in the TX II register. After this delay RF chip will transmit data in TX FIFO automatically.

CAL state: there are two independent calibration items in CAL state. Under the SB state, when bit FBC=1 or VBC=1, RF chip will execute IF filter calibration procedure or VCO band calibration procedure. When the calibration is complete, bit FBC or VBC will reset to 0 automatically and back to state.

A7102 RF chip state is determined by settings of pin PWR_ON, bit CER, PLLE, TRSR(or pin TRS), TRER(or pin TRS), as listed in the following table.

Table 2. State control bits

PWR_ON	CER	PLLE	TRS(TRSR)	TRE(TRER)	Operation mode
0	x	x	X	x	Sleep mode
1	0	0	X	0	SB mode, XOSC off, bandgap off, PLL off
1	1	0	X	0	SB mode, XOSC on, bandgap on, PLL off
1	x	1	X	0	SB mode, XOSC on, bandgap on, PLL on
1	x	x	1	1	TX mode
1	x	x	0	1	RX mode

Instead of controlling the chip via UI/O pins TRE/TRS, user can set the bits TRSR/TRER in control register to change the state of RF chip. The bit PCS in pin control register must set to 0. Pins TRS and TRE are suggested connecting to ground.

13.1 Auto Mode Back function

Under the FIFO mode, A7102 RF chip have auto mode back function, user can control the RF chip easily.
If RF chip is in the SB sate, after setting to enter TX/RX state, RF chip will automatically turn on crystal oscillation circuit and PLL circuit in sequence, and then enter TX/RX state. After completing the actions in TX/RX state, RF chip will back to SB state automatically. Step -by-step register setting is not needed for user.
Which state RF chip will back to is according the bit CER, and bit PLLE. If CER=1, and PLLE=0, then when exiting TX/RX state, RF chip will back to the corresponding state set by CER=1, PLLE=0.

15. Calibration

It is necessary to do the circuit calibration when A7102 is initialized. There are two type of calibration needed to perform: IF Filter calibration and VCO band calibration. IF CAL is to calibrate the IF filter bandwidth and center frequency. VCO band CAL(VCO band calibration) is to calibrate the VCO to operate in the proper frequency band.

15.1 IF Calibration Process

Under the Stand by state (XOSC is on), set bit MIFS=0(auto calibration). After setting the mode control register bit FBC=1,the chip will enter CAL state, and starts the calibration process. If RF chip is not in the SB state when bit FBC is set to 1, RF chip will not start the calibration process until entering SB state. When the calibration is completed, bit FBC will be cleared to 0 automatically, and chip will leave from CAL state and back to SB state.
If the mode control register bit TRER=1, FBC=1 or VBC=1are set simultaneously, RF chip will enter the CAL state first, and after completion of IF filter calibration or VCO band calibration process, RF chip can then enter into TX/RX state. The maximum time required for A7102 RF chip to perform IF Calibration process is about 16 * 256 * (1 / system clock).

15.2. VCO band Calibration Process

Before the VCO band calibration, user should set proper operating frequency first, meanwhile, the range of VT (VTH[2:0], VTL[2:0]) for VCO is also need to be set properly.

Under the Stand by state (XOSC is on), set bit MVBS=0(auto calibration). After setting the mode control register bit VBC=1, the chip will enter CAL state, and starts the calibration process. If RF chip is not in the SB state when bit VBC is set to 1, RF chip will not start the calibration process until it entering SB state. When the calibration is completed, bit VBC will be cleared to 0 automatically, and chip will leave from CAL state and back to SB state.

If the mode control register bit TRER=1, FBC=1 or VBC=1are set simultaneously, RF chip will enter the CAL state first, and after completion of IF filter calibration or VCO band calibration process, RF chip can then enter into TX/RX state. The maximum time required for A7102 RF chip to perform IF Calibration process is about 16 * 256 * (1 / system clock).

The maximum time required for A7102 RF chip to perform VCO band Calibration process is about 4 * PLL settling time.

16. FIFO (First In First Out)

A7102 RF chip has built-in TX and RX FIFO register, with 64 bytes, respectively. User can write data into TX FIFO and read out data from RX FIFO. Operation of data read /write was executed via SPI interface. In the FIFO mode, according to the defined data packet format, RF chip will transmit packet data or received packet data by itself.

16.1 packet format

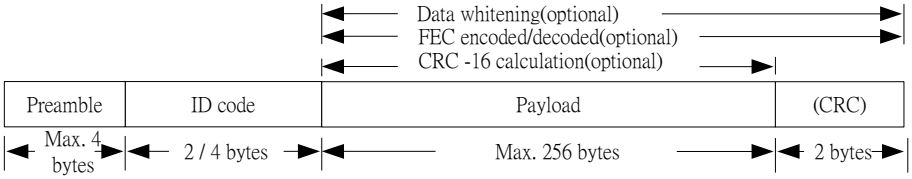


Fig.19 Data packet format

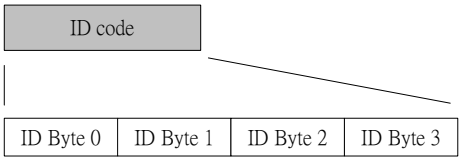


Fig.20 ID Code format

Preamble:

Preamble length can be set by bit PML[1:0] in code control register, the maximum length is 4 bytes. Chip will add the preamble as ”0101…0101”or ”1010…” automatically according to the first bit of ID code. If the first bit of ID code is 0, then preamble code will be ”0101…”. If first bit of ID code is 1, then the preamble code will be ”1010…”.

ID code:

The length of ID code can be set by bit IDL in code control register to 2/4 bytes. User can write/read ID code via SPI. If bit IDL set the length of ID code to 2 bytes, RF chip takes ID Byte 0 and ID Byte 1 as the ID code and ignores the ID Byte2, ID Byte 3. If bit IDL set the length of ID code to 4 bytes, RF chip takes from ID Byte 0 to ID Byte 4 as the ID code.

In FIFO mode, A702 RF chip compare the ID code received. If the ID code is correct, packet data will be written into RX FIFO automatically to reduce the loading of MCU. The number of error bit in ID code can be set by the bit ETH[1:0] in RX control register (I).

Payload:

The length of FIFO data packet is set by bits FEP[7:0] in FIFO control register 中 FEP[7:0]. The maximum length of packet in one transmit/receive action is 256 bytes. Data read/write into RX FIFO/TX FIFO via the pins of SPI interface.

CRC:

CRC is optional feature for A7102. If bit CRCS is set to 1 in the code control register, then when transmitting the data, 2 bytes CRC code will be added into packet in the Payload.

16.2 Packet Handling

A7102 RF chip provides 3 optional coding actions to packet data: CRC, FEC, and Data Whitening.

CRC:

If CRCS=1 in code control register, when transmitting packet data, chip will calculate the CRC code from the start to the end of data (not including preamble code, ID code), and added 2 bytes CRC code after payload. Upon receiving data packet, RF chip will check the CRC automatically, user can check bit CRCF in mode control register. If CRC checking is right, this bit will be set to 0. If CRC check fails, bit CRCF will be set to 1.

FEC(Forward Error Correction):

If bit FECS=1 in code control register, RF chip will perform FEC coding/decoding to data payload and CRC code before transmitting/receiving data packet. Once the data receiving data process is completed, RF chip will automatically check if FEC error occurs or not. User can check bit FECF in mode control register. If FEC error occurs, bit FECF will be set to 1.

Data Whitening:

If bit WHIT=1 in code control register, the XOR operation will be performed between payload data/CRC code and 7 bit pseudo random sequence. User can set the initial seed of data whitening by bits WS[6:0] in the code control register. When receiving data packet, data will be decoded according to the initial seed. If the initial seed is different for TX and RX terminals, RF chip will not decode the data correctly.

Manchester Code:

If bit MCS=1 in the code control register, packet data will be proceeded by Manchester encoding. When receiving, demodulation circuit will automatically decode the Manchester coded data to recover the original data.

16.3 Calculation of data transmission time

T =[[Preamble code] + [ID code] + [Payload + 16*K_{CRC}] * [1+3/4*K_{FEC}]] * [1 / Data rate] + ($K_{Gaussia}$n * [1 / Data rate])

K_{CRC} =0 @CRC Disable, K_{CRC} =1 @CRC Enable
K_{FEC} =0 @FEC Disable, K_{FEC} =1 @FEC Enable
$K_{Gaussian}$=2 @ Gaussian Disable, $K_{Gaussian}$=3 @ Gaussian Enable

16.4 TX/RX FIFO

A7102 contains one 64 bytes TX FIFO and one 64 bytes RX FIFO. Data can be written into TX FIFO and readout fom RX FIFO, respectively, via the SPI interface.

FIFO length and TX/RX pointer is set by bits FEP[7:0] in FIFO control register. Before writing TX FIFO data, user need to set the value of FEP[7:0], then A7102 will execute the writing action, if the pointer exceed the vale set by FEP[7:0], it will return to TX FIFO address 0x00, and overwrite the former data vale of address 0x00.

To write data into TXFIFO, MCU can write the data in batch mode. The data will be written into FIFO from the pointer address which was the end of last data writing process. When user write data into TX FIFO via SPI and bits FET[7:0] is set to 0x1F(data length 32byts), if the data length is larger than 32bytes，TX FIFO Pointer will return to address 0x00 automatically, and continue the data writing process. User should use TX FIFO reset command when he want to reset the TX FIFO pointer.

MCU can also read data from RX FIFO via SPI in batch mode. Data will be read out from the pointer address that was the end address of last read process. When user read data from RX FIFO via SPI and bits FET[7:0] is set to 0x1F(data length 32byts), if the data length is larger than 32bytes，RX FIFO Pointer will return to address 0x00 automatically, and continue the data reading process. User should use RX FIFO reset command when he want to reset the TX FIFO pointer.

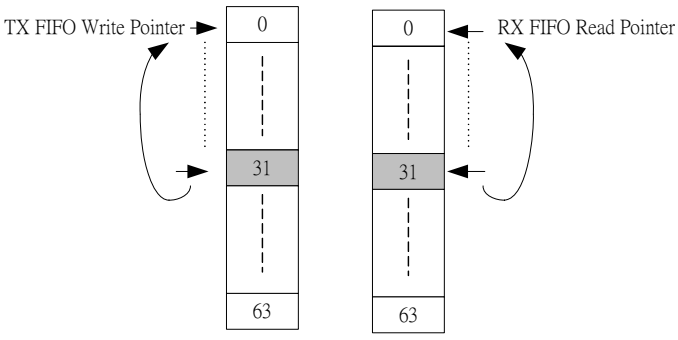


Fig.21 TX /RX FIFO Pointer

Bit PSA[5:0] in FIFO control register will determine the start pointer address when transmitting data. The default value is 0x00. If the data to be proceeded are simple and fixed, user can combine all the data and write them into TX FIFO in one time. Utilizing the start address pointer PSA[5:0] and end address pointer FEP[7:0] of data, user can re-sue the transmit data easily.

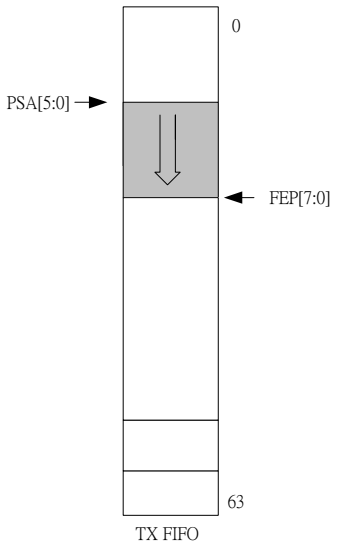


Fig.22 PSA and FEP relationship

16.5 FIFO pointer margin threshold

If packet data length is larger than 64 bytes, MCU must determine when the data is written into TX FIFO for transmitting the packet and when to read data from RX FIFO for receiving data packet. If there is error occurs in the write/read procedure, it will cause data overflow or data underflow.

A7102 RF chip provide programmable FIFO threshold value in FIFO control register. Bits FPM[1:0] and the pin CKO(FIFO pointer flag) are used to indicate the status of FIFO. Data underflow occurred in TX FIFO and data overflow occurred in RX FIFO can be detected. When writing data into TX FIFO, MCU must prevent the overflow in TX FIFO which will cause error in data transmitted. When reading data from RX FIFO, MCU must prevent the data underflow in RX FIFO which also cause error in data readed.

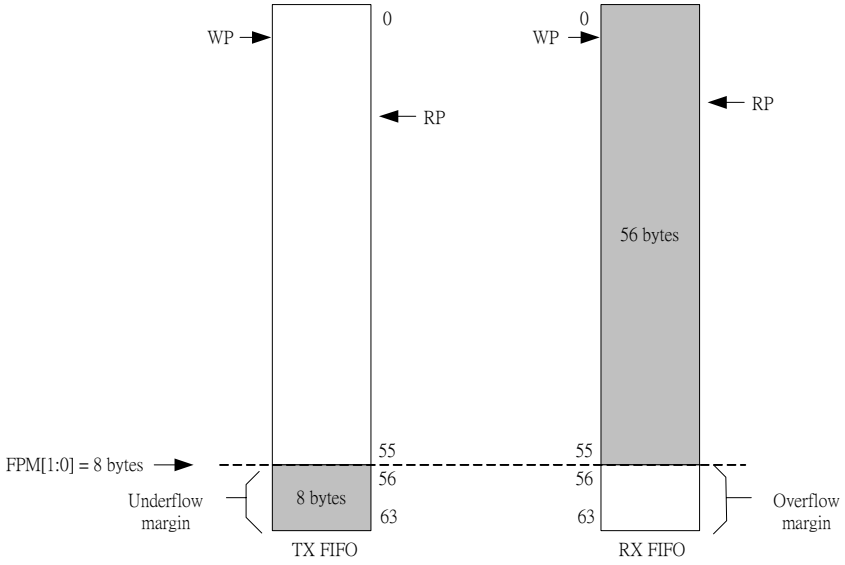


Fig.23 FIFO margin threshold

Condition for FIFO control auto indicator：

TX FIFO:

WP(write pointer) – RP(read pointer) ≦ FIFO threshold point

WP (write pointer) is the pointer when writing data into TX FIFO. RP (read pointer) is the pointer when read out data from TX FIFO and send to modulator.

RX FIFO:

WP (write pointer) – RP(read pointer) > FIFO threshold point

WP (write pointer) is the pointer when received data is writing into RX FIFO. RP (read pointer) is the pointer to readout data from RX FIFO.

Ex:
If FPM[1:0]=01, TX FIFO threshold pointer is 8 bytes, RX FIFO threshold pointer is 56 bytes,
When WP – RP ≦ 8 for TX FIFO, pin CKO(FIFO pointer flag) will be set to 1, else it will be 0
When WP – RP > 56 in RX FIFO, pin CKO(FIFO pointer flag) will be set to 1, else it will be 0.

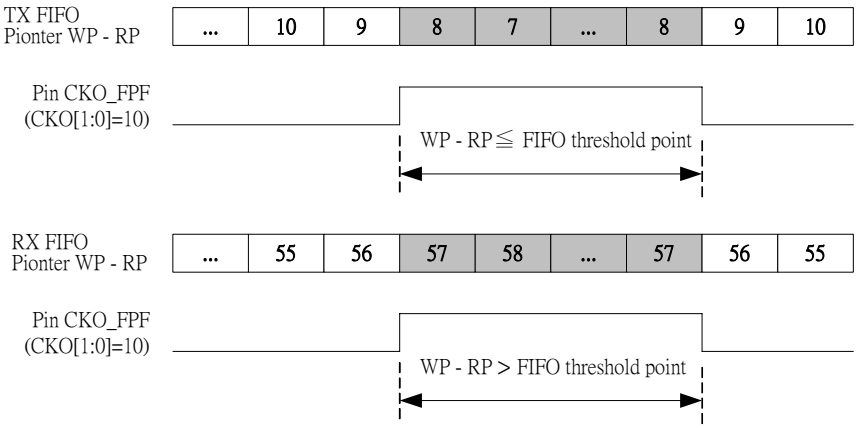


Fig.24 FMP[1:0]='01' vs. Pointer(WP-RP)

17. Mode of operation

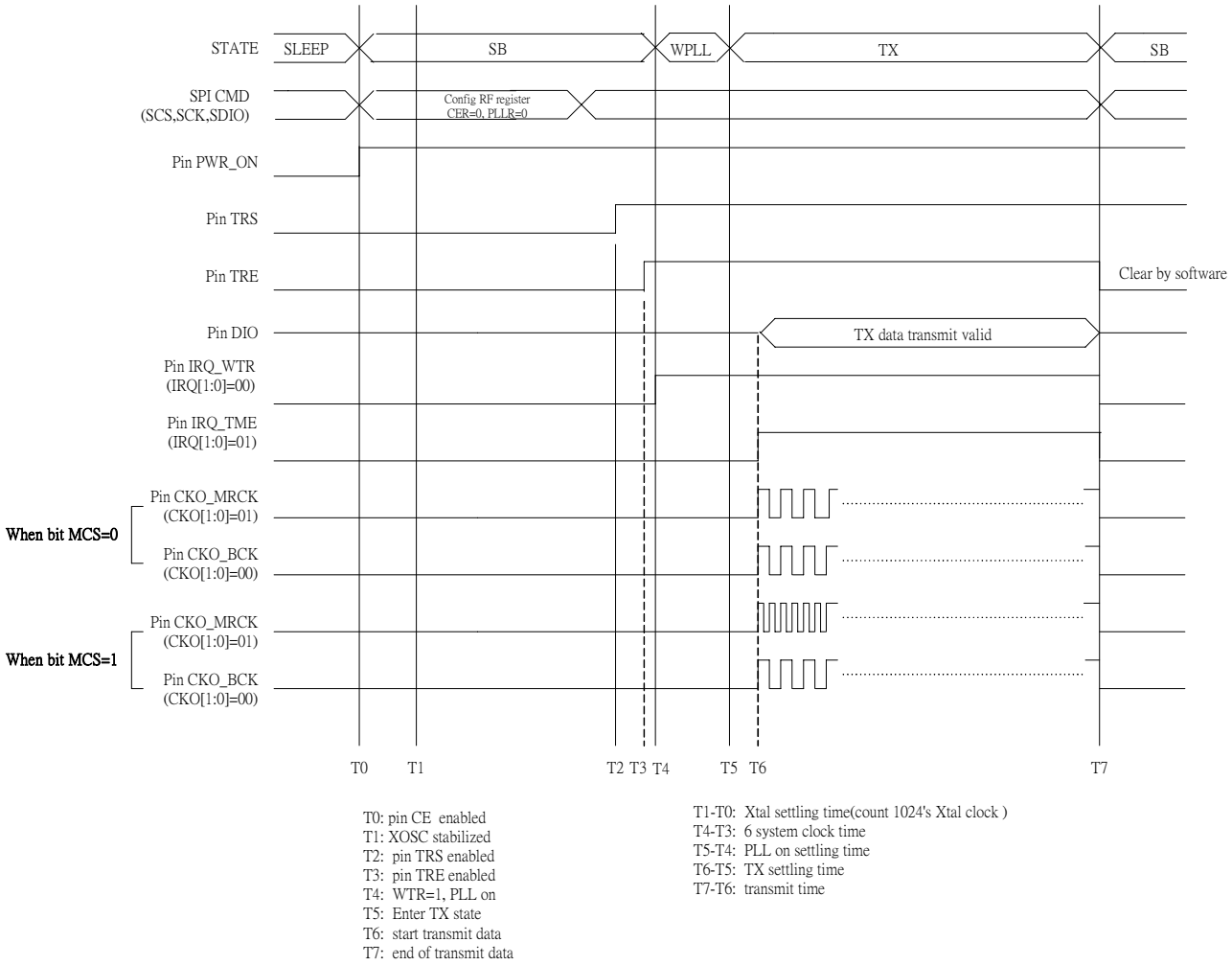
A7102 RF chip has two main operation modes: Direct mode and FIFO mode. User can set the operation mode by bit FMS in model control register. In DIRECT mode, the transceiver can communicate at data rate of 50k, 100k or 150kbps for maximum data throughput performance. For all low data rate applications, FIFO mode enables the on-chip FIFO to clock in data at a low data rate from a low speed micro-controller and transmit at high data rate 150kbps.

17.1 Direct mode

Direct mode provides user a RF channel. In TX terminal, Baseband or MCU send data to A7120 pin DIO, RF chip performs data modulation and then send out the data. In RX terminal, RF chip perform data demodulation to recovery the received data. Baseband or MCU need to find out the correct information form the data by itself.

17.1.1 TX timing sequence

Setting pin TRS=1, TRE=1 to enter TX state, data will be transmitted via Pin DIO. When data transmit finished, set pin TRE to 0, to exit TX state and back to SB state.



T0: pin CE enabled
T1: XOSC stabilized
T2: pin TRS enabled
T3: pin TRE enabled
T4: WTR=1, PLL on
T5: Enter TX state
T6: start transmit data
T7: end of transmit data

T1-T0: Xtal settling time(count 1024's Xtal clock)
T4-T3: 6 system clock time
T5-T4: PLL on settling time
T6-T5: TX settling time
T7-T6: transmit time

Fig.25 TX timing sequence in direct mode

17.1.2 RX timing sequence

Setting pin TRS=0, TRE=1 to enter RX state. Data will be received via Pin DIO. When data receiving action finished, set pin TRE to 0, to exit RX state and back to SB state.

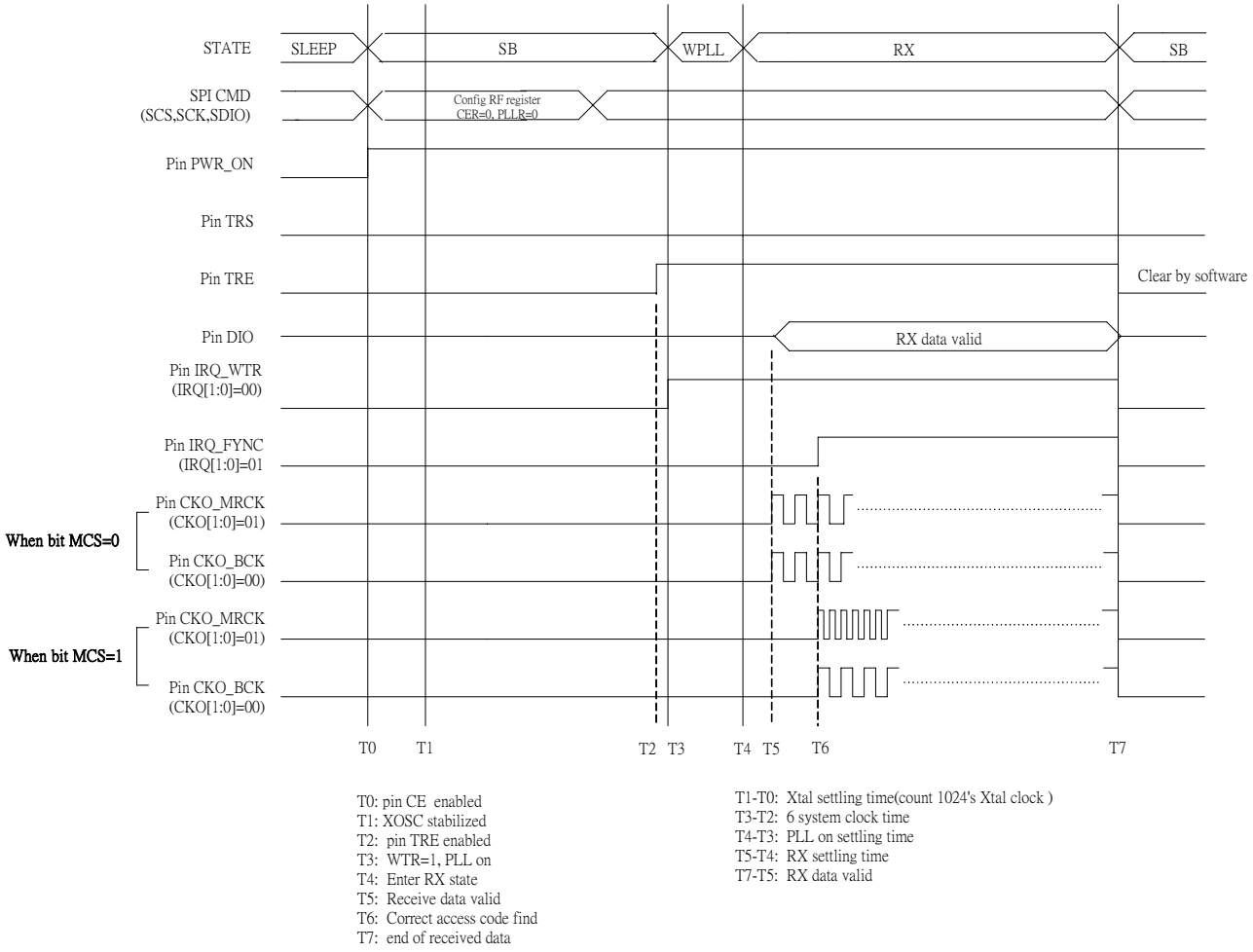


Fig.26 RX timing sequence in direct mode

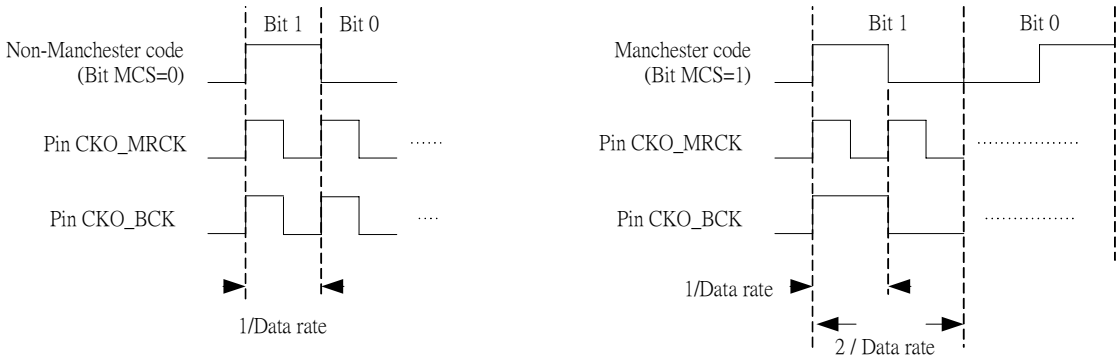


Fig.27 BCK, MRCK timing sequence when bit MCS=0 and 1

17.2 FIFO mode

The A7102 has two built-in 64 bytes FIFO, i.e. TX FIFO and RX FIFO, user can write the data into TX FIFO via SPI for transmit. After enabling RF chip, the circuit will transmit the data according to the data packet format. In receiving mode, circuit will detect the ID code automatically and then write the received data into RX FIFO so that the burden of MCU can be reduced. The FIFO can be enabled by set FMS bit to 1. A simplified FIFO block diagram is shown as follows.

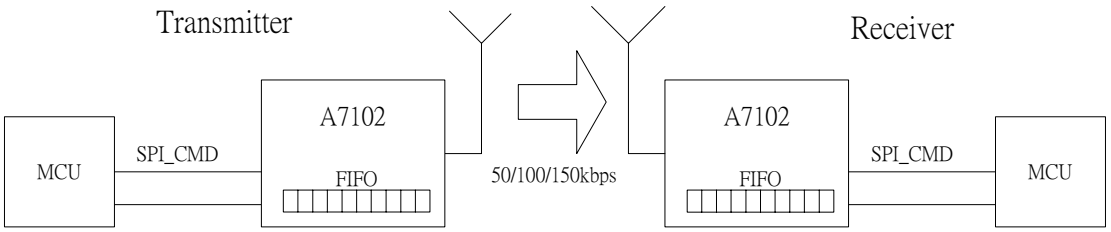
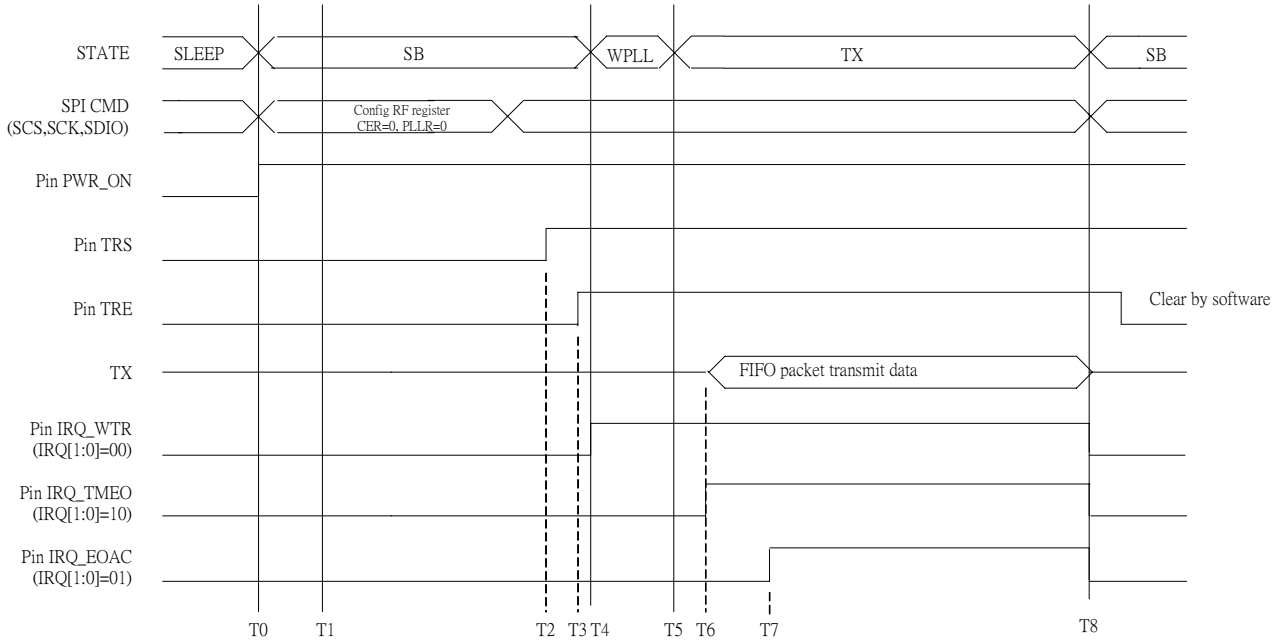


Fig.28 TX/RX in FIFO mode

17.2.1 TX

Data is written into TX FIFO via SPI. Setting pin TRS=1, TRE=1 to enter TX state. When data receiving action finished, set pin TRE to 0, to exit TX state and back to SB state.



T0: pin CE enabled
T1: XOSC stabilized
T2: pin TRS enabled
T3: pin TRE enabled
T4: WTR=1, PLL on
T5: Enter TX state
T6: start transmit data
T7: end of access code
T8: end of transmit data

T1-T0: Xtal settling time(count 1024's Xtal clock)
T4-T3: 6 system clock time
T5-T4: PLL on settling time
T6-T5: TX settling time
T7-T6: transmit time of access code & preamble
T8-T6: FIFO packet transmit data

Fig.29 TX timing sequence in FIFO mode

17.2.2 RX

Setting pin TRS=0, TRE=1 to enter RX state. When sync words are matched, pin RX_SYN will set to1, then received data starts to be written into RX FIFO. When data packet receiving action is completed , RF chip will exit RX state and back to SB state automatically. Then data received can then be read out via SPI.

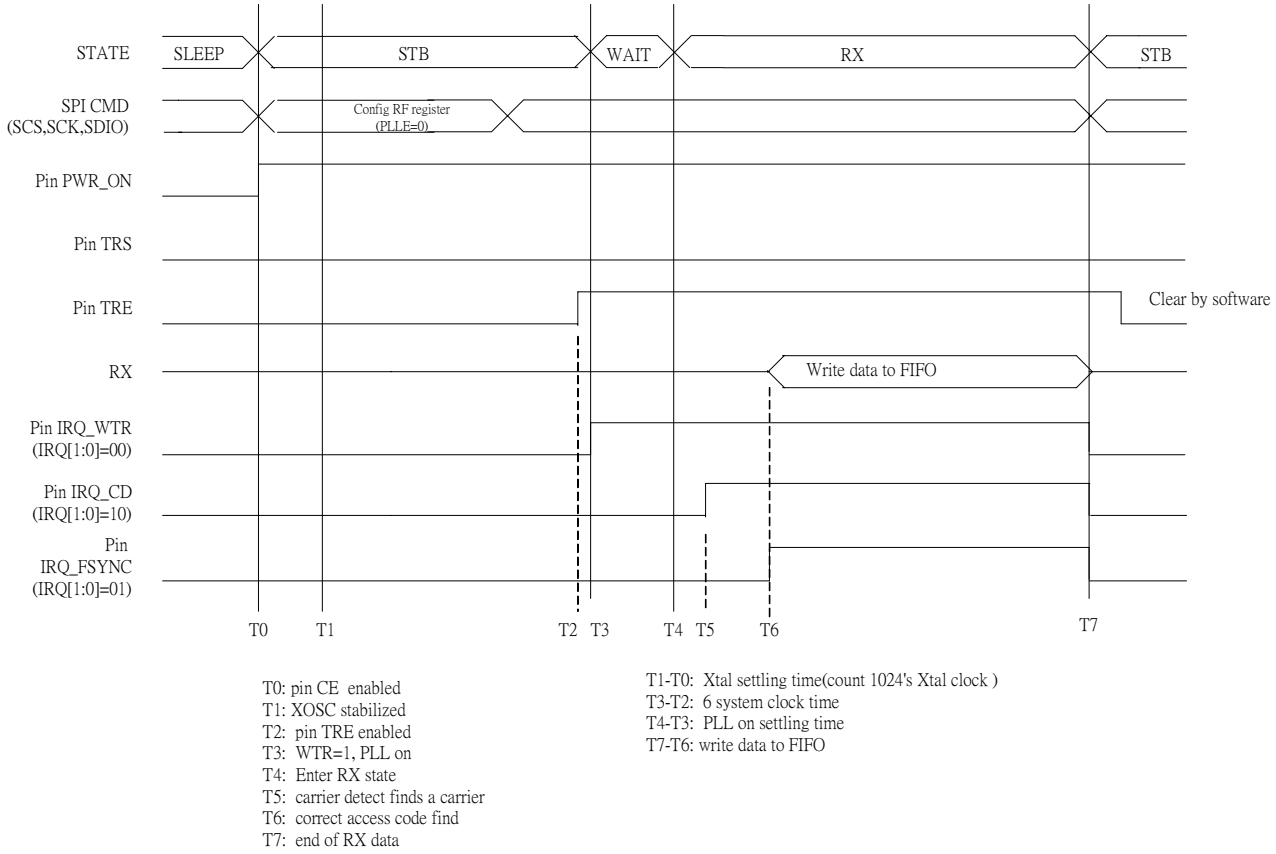


Fig.30 TX timing sequence in FIFO mode

17.3 pin TRE switch timing

A7102 provide pin control mode to change the RF chip into TX mode or RX mode. By setting the pins TRS, TRE, state ca be set properly. The switching time for setting pin TRE to 0 and reset to 1 should be larger than 2 period of system clock to ensure the state can switch correctly.

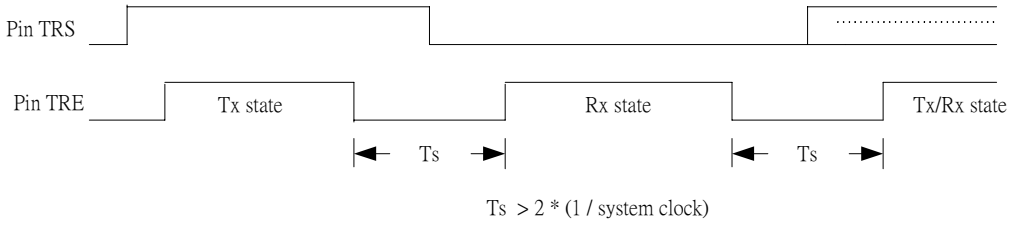


Fig.31 Mode switch timing for Pin TRE.

18. ADC (Analog Digital Converter)

A7102 RF chip contains a built-in 8-bit ADC for internal temperature measurement, RSSI measurement, and Carrier detect function. It also can perform external signal measurement through pin ADC_IN (pin32).
The conversion time of 8-bit ADC is depends on the clock input to ADC. It takes 20 cycles to complete the conversion. The clock source of ADC comes from Crystal oscillator, and according to the setting of bit GRC[4:0] in system clock register, select the ADC clock source to be 800KHz or 1.2MHz.

18.1 temperature measurement

A7102 RF chip has a simple on-chip temperature sensor, it can measure the variation of working temperature of RF chip.
Set bit CDM=0 in ADC register, then enable bit ADCM=1 in the mode control register to start the measurement of temperature. When the measurement is completed, the bit ADCM will be cleared to 0. User can then read the ADC[7:0] values from the ADC register.

Note: ADC value represent the temperature value in the non-RX state. In RX state, ADC value represents the RSSI value.

18.2 RSSI measurement

A7102 RF chip has a built-in RSSI (received signal strength indicator) to measure the RF signal strength. When the measurement procedure is completed, the RSSI value can be read form ADC register, the range of RSSI is 0~255. The larger for signal strength, the RSSI value is smaller, and vice versa. In RX state, set bit CDM=0 in ADC register, and then set bit ADCM=1 in mode control register to start the RSSI measurement. Once the measurement is completed, the bit ADCM will be cleared to 0. User can read the RSSI value from ADC[7:0] in ADC register.

18.3 CD (Carrier Detect)

A7102 RF chip provides an output pin IRQ to monitor that there is a carrier or not. If the carrier signal strength is greater than the value set by bit RTH[7:0] in ADC register, pin IRQ will go high, or it will go low. In RX state, set bit CDM=1 in ADC register, set bit ADCM to 1 in mode control register to start the carrier signal measurement. The value are stored in bit ADC[7:0] and it will be updated in each measurement period till the end of detection action.

18.4 External ADC measurement

A7102 RF chip provides an input pin ADC_IN for measurement of external signal. The measurable range for external signal is 0 ~ 1.28Vdc. In RX state, connect the signal to ADC_IN (RF chip pin 32), set bit XADS=1 in ADC register, and set bit CDM=0, then set bit ADCM=1 in mode control register to start the measurement for external signal. When the measurement is completed, bit ADCM will be cleared to 0. User can read the measurement values from bit ADC[7:0] in ADC register.

Table for ADC measurement setting：

Bit		description	
XADS	CDM	None Rx state	RX state
0	0	Temperature measurement	RSSI measurement
0	1	N/A	Carrier Detector
1	1	N/A	External signal measurement through pin ADC_IN

19. RTC(Real Time Clock)

A7102 RF chip has built-in Real Time Clock function. In order to save the power consumption, when RF chip enters sleep mode and MCU enter power down mode, user can set a proper periodical interrupt time to wake up the MCU for resumption, to manipulate the RF events.
Real time clock utilize an external low cost 32.768KHz crystal component, connected to A7102 via Pins XO3_32K and XI_32K, with two external 33pF capacitors, as shown in the following Figure.

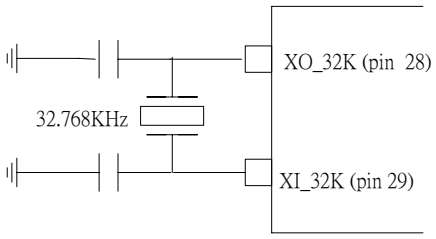


Fig.32 Connection of RTC oscillator

User should set bit RTCE in the crystal control register (Address 0x05) to 1 to enable the RTC circuit. Then Bit RTOE is set to 1, then RF chip will send out a periodical clock signal at pin RCTO (pin 27), the period is 250ms ~ 2S depends on the setting of bit RTC[1:0].

RTC[1:0]	Period
[00]	250ms
[01]	1s
[10]	500ms
[11]	2S

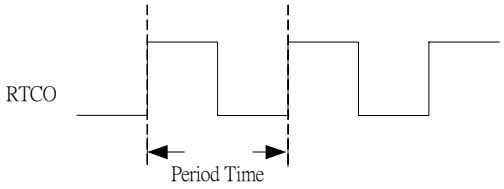


Fig.33 RTCO output timing diagram

20. Application Circuit

20.1 application circuit 1 (VDD > 2.5V)

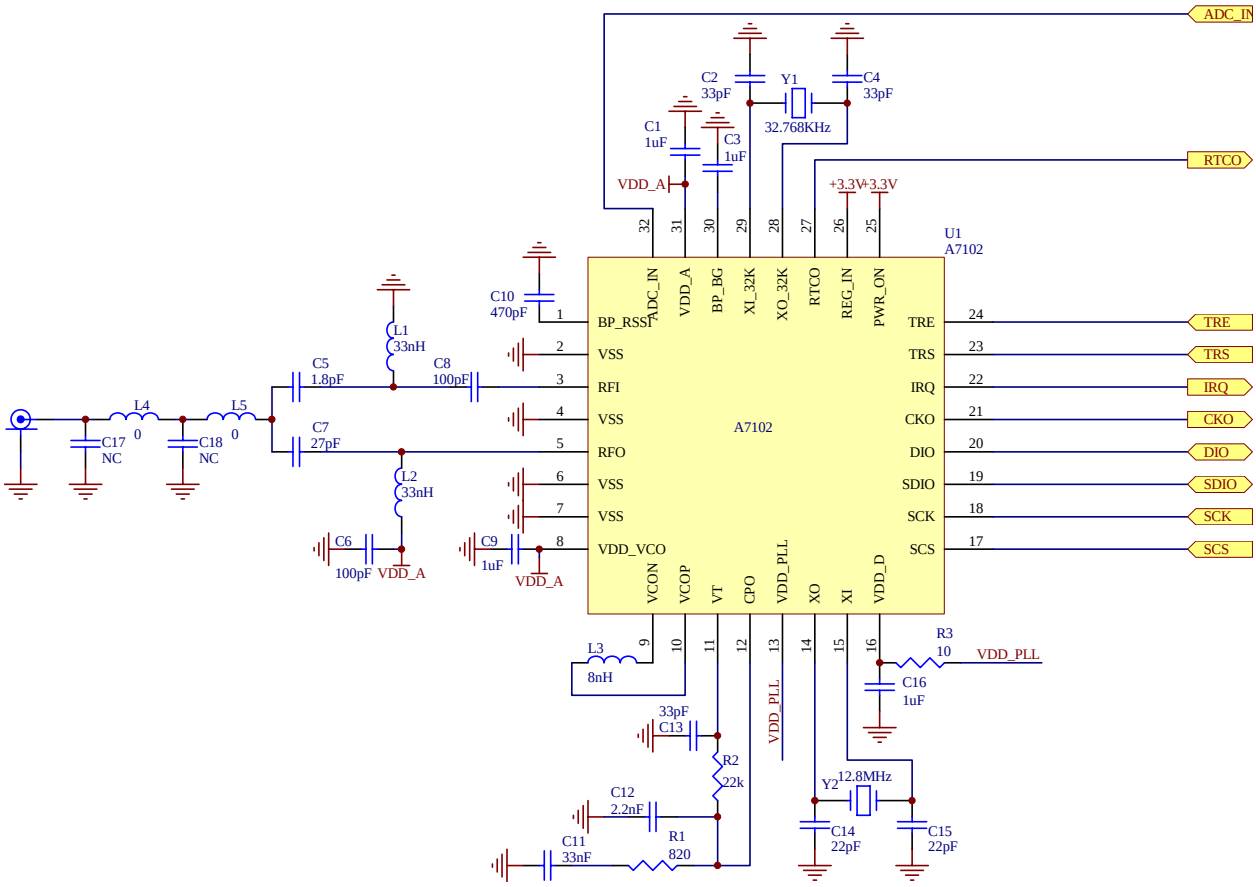


Fig.34 Application circuit 1

20.2 application circuit 2 (VDD = 2.5V)

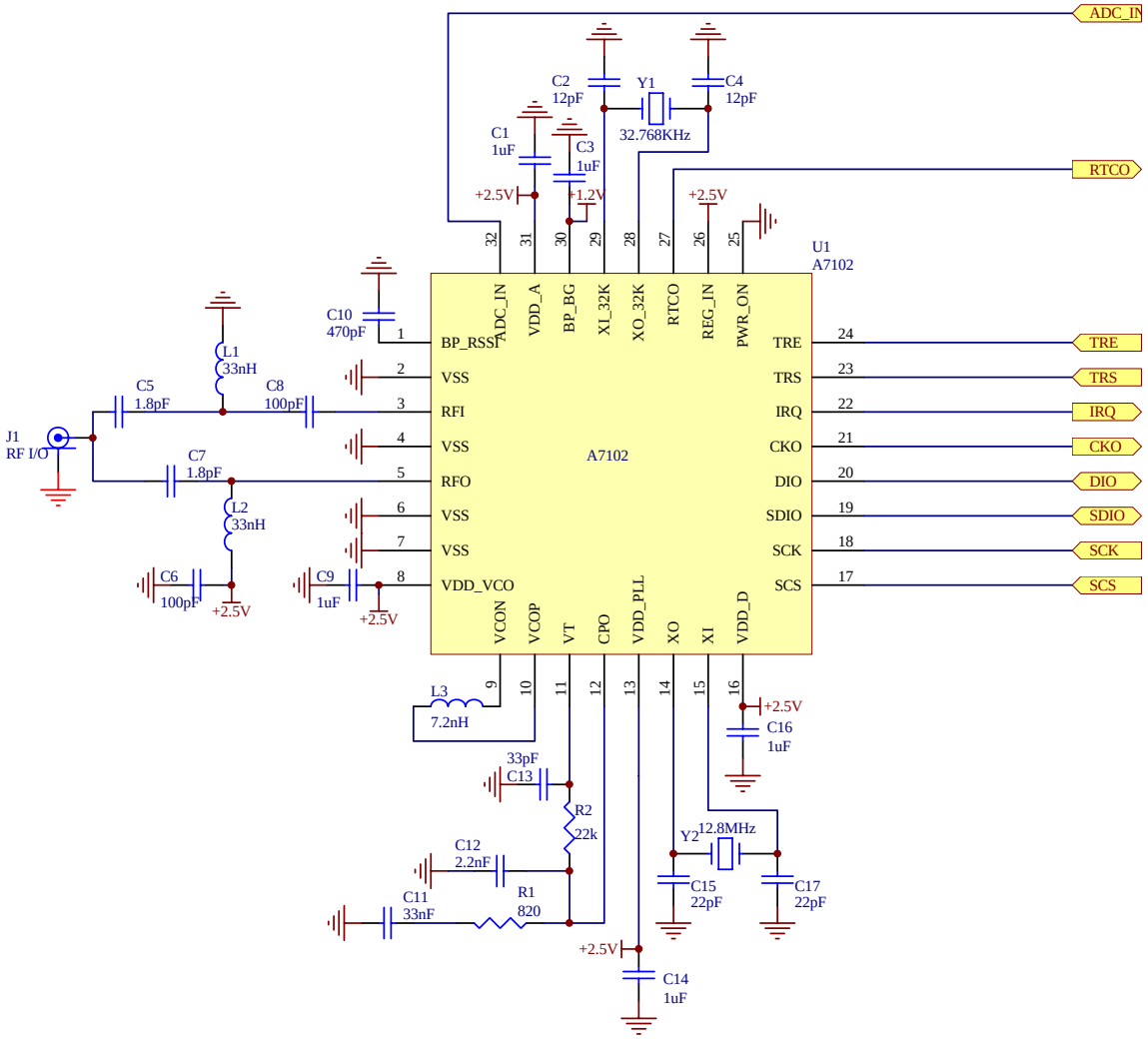
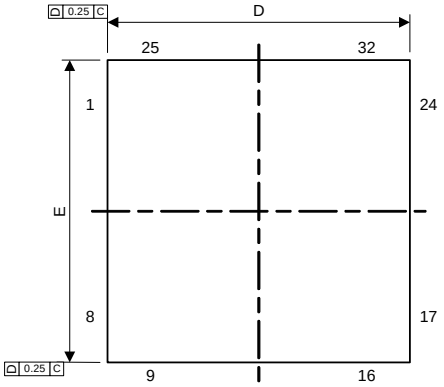


Fig.35 Application circuit 2

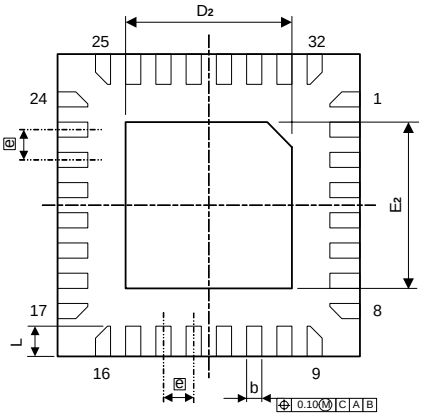
21. Package Information

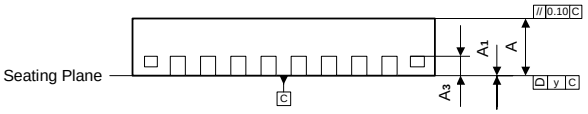
QFN 32L Saw Type Outline Dimensions　unit: inches/mm

Top View



Bottom View





Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.032	0.70	0.75	0.80
A_1	0.000	0.001	0.002	0.00	0.02	0.05
A_3	0.010 REF			0.20 REF		
b	0.007	0.010	0.012	0.18	0.25	0.30
D	0.197 BSC			5.00 BSC		
D_2	0.049	0.106	0.128	1.25	2.70	3.25
E	0.197 BSC			5.00 BSC		
E_2	0.049	0.106	0.128	1.25	2.70	3.25
e	0.020 BSC			0.50 BSC		
L	0.012	0.016	0.020	0.30	0.40	0.50
y	0.004			0.10		

22. Ordering Information

Part No.	Package	Units Per Reel / Tray
A71C02AQF/Q	QFN32L, Tape & Reel, Pb free, -40℃～85℃	3K
A71C02AQF	QFN32L, Tray, Pb free, -40℃～85℃	490EA