Switching Regulators

STR-A6251 AND STR-A6252

Data Sheet 28103.42c

Universal-Input/15 W 50 kHz Flyback Switching Regulators

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Control Supply Voltage, V_{CC} . . . . **36 V**
Drain-Source Voltage, V_{DSS} . . . . . **650 V**
Drain Switching Current, I_D
STR-A6251 . . . . . **2.5 A***
STR-A6252 . . . . . **3.0 A***
Peak Drain Switching Current, I_{DM}
STR-A6251 . . . . . **2.5 A**
STR-A6252 . . . . . **3.0 A**
Single-Pulse Avalanche Energy, E_{AS}
STR-A6251 . . . . . **72 mJ**
STR-A6252 . . . . . **123 mJ**
S/OCP Voltage Range,
V_{OCP} . . . . . **–0.3 V to +6 V**
FB/CC/OLP Voltage Range,
$V_{FB/OLP}$ . . . . . **–0.3 V to +12 V**
FM Voltage Range,
V_{FM} . . . . . **–0.3 V to +6 V**
Package Power Dissipation, P_D
control (V_{CC} × $I_{CC(ON)}$) . . . . . **0.15 W**
MOSFET (V_{DSS} × I_D) . . . . . **1.35 W**
total . . . . . **1.5 W**
MOSFET Channel Temp., T_J . **+150°C**
Internal Frame Temp., T_F . . . . **+125°C**
Storage Temperature Range,
T_S . . . . . **-40°C to +125°C**

* Drain switching current is limited by temperature (page 2) and safe operating area (page 4).

The STR-A6251 and STR-A6252 are 50 kHz PWM topology (with ±5% frequency jittering for minimum EMI) regulators specifically designed to satisfy the requirements for increased integration and reliability in flyback converters. They incorporate a primary control and drive circuit with avalanche-rated power MOSFETs. The STR-A6252 features higher allowable switching current and lower on-resistance. The STR-A6251 is also available for 67 kHz operation.

Covering the power range from below 21 watts or 24 watts for a 230 VAC input, or to 15 or 20 watts for a universal (85 to 264 VAC) input, these devices can be used in a wide range of applications, from DVD players and VCR player/recorders to ac adapters for cellular phones and digital cameras. An auto-burst standby function reduces power consumption at light load, while multiple protections, including the avalanche-energy guaranteed MOSFET, provide high reliability of system design.

Cycle-by-cycle current limiting, undervoltage lockout with hysteresis, overvoltage protection, and thermal shutdown protect the power supply during the normal overload and fault conditions. Overvoltage protection and thermal shutdown are latched after a short delay. The latch may be reset by cycling the input supply. Low start-up current and a low-power standby mode selected from the secondary circuit completes a comprehensive suite of features. Both devices are provided in an 8-pin mini-DIP plastic package with pin 6 removed.

FEATURES AND BENEFITS

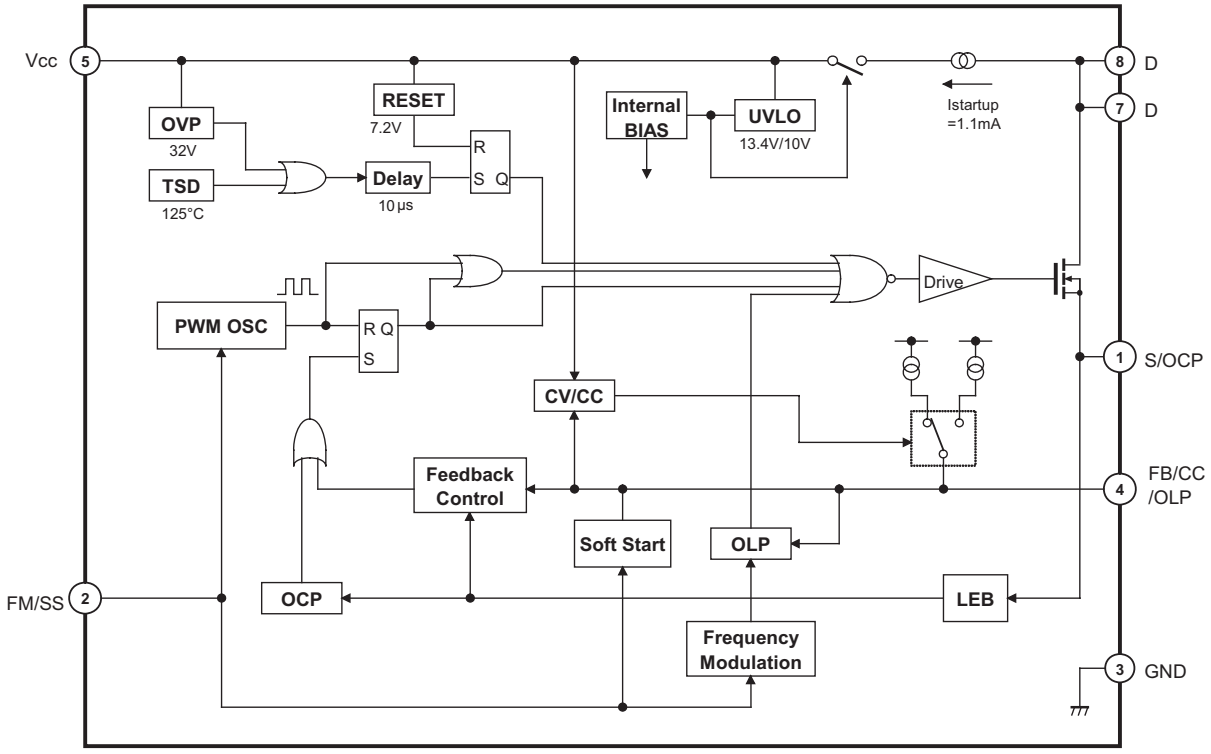
- 50 kHz PWM with ±5% Frequency Jittering
  Cost Reduction of EMI Noise Filtering
- Rugged 650 V Avalanche-Rated MOSFET
  Simplified Surge Absorption
  No V_{DSS} Derating Required
- Choice of $r_{DS(on)}$ (2.8 Ω or 3.95 Ω maximum)
- Auto-Burst Mode for Stand-By Operation or Light Loads
  Less Transformer Audible Noise
- Built-In Leading Edge Blanking
- Soft Start and Low Start-Up Current
  Start-Up Circuit Disabled in Operation
- Low Operating Current (4 mA max)

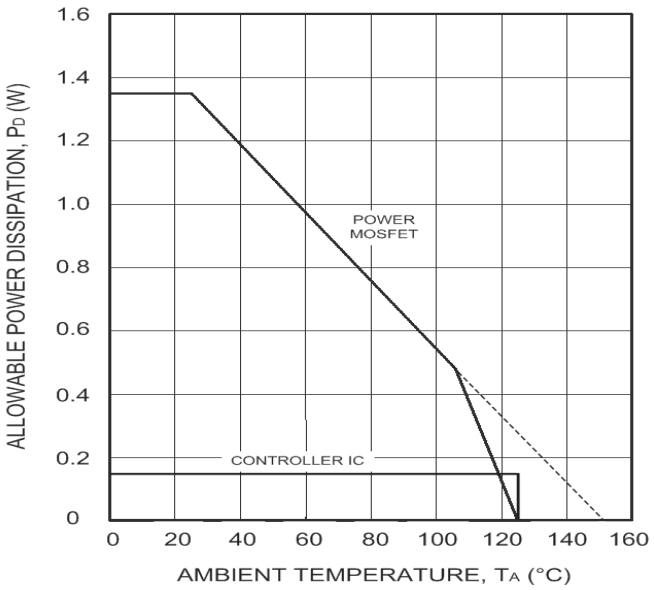
continued

Always order by complete part number, e.g., **STR-A6251** .

Sanken Power Devices from Allegro MicroSystems

FUNCTIONAL BLOCK DIAGRAM





FEATURES AND BENEFITS (cont'd)

- Automatic Burst Stand-By (intermittent operation)
  Input Power <0.1 W at No Load
- Auto-Bias Function
  Stable Burst Operation Without Generating Interference
- Internal Off-Timer Circuit
- Built-In Constant-Voltage/Constant Current
- Multiple Protections:
  Pulse-by-Pulse Overcurrent Protection (OCP)
  Overload Protection (OLP) with Auto Restart
  Latching Overvoltage Protection (OVP)
  Undervoltage Lockout (UVLO) with Hysteresis
  Latching Thermal Shutdown (TSD)
- Molded Small-Size 8-Pin Package
  For Low-Height SMPS

This data sheet is based on Sanken data sheet SSE-23297 and SSE-23298.

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ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{CC} = 18 V (unless otherwise specified).

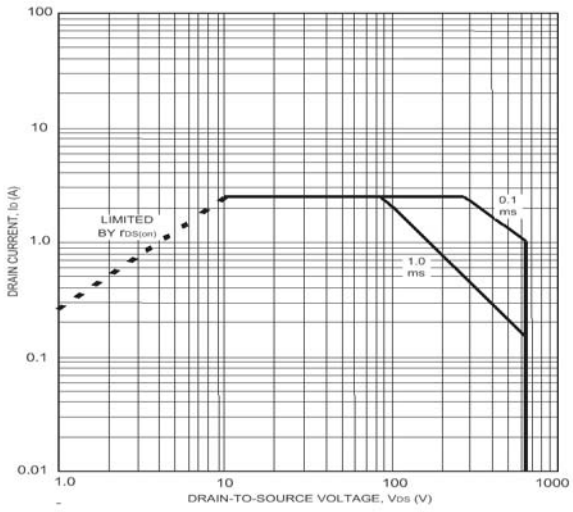
Characteristic	Pin No.	Symbol	Test Conditions	Ratings Min	Typ	Max	Units
Drain-to-Source Breakdown Volt.	8 - 1	$V_{(BR)DSS}$	I_D = 300 µA, $V_1 – V_3$ = 0 V (short)	650	-	-	V
Drain Leakage Current	8	I_{DSS}	V_{DS} = 650 V, $V_1 – V_3$ = 0 V (short)	-	-	300	µA
On-State Resistance	8 - 1	$r_{DS(on)}$	STR-A6251, I_D = 0.4 A	-	-	3.95	Ω
			STR-A6252, I_D = 0.4 A	-	-	2.8	Ω
MOSFET Switching Time	8 - 3	t_f	-	-	-	250	ns
Operation-Start Voltage	5 - 3	$V_{CC(ON)}$	V_{CC} = 0 → 15.7 V	12.9	14.3	15.7	V
Operation-Stop Voltage	5 - 3	$V_{CC(OFF)}$	V_{CC} = 15.7 → 9 V	9.0	10	11	V
Maximum Switching Frequency	8 - 3	$f_{osc(max)}$	-	45	50	55	kHz
Frequency-Jitter Deviation	8 - 3	Δf_{osc}	-	3.0	5.0	7.0	kHz
Maximum ON Duty Cycle	8 - 3	D max	-	70	76	82	%
Circuit Current in Operation	5	$I_{CC(ON)}$	-	-	-	4.0	mA
Circuit Current in Non-Operation	5	$I_{CC(OFF)}$	V_{CC} = 12 V	-	14	25	µA
FM Voltage	2 - 3	V_{FMH}	fosc = $f_{osc(max)}$	4.0	4.5	5.0	V
		V_{FML}	fosc < $f_{osc(max)}$	3.2	3.6	4.0	V
FM Current	2	I_{FMH}		-7.7	-11.0	-14.3	µA
		I_{FML}		7.7	11.0	14.3	µA
OCP Threshold Voltage	1 - 3	V_{OCP}	-	0.67	0.74	0.81	V
Leading Edge Blanking Time	8 - 3	t_{bw}	-	220	320	420	ns
Burst Threshold Voltage	4 - 3	V_{burst}	-	1.00	1.12	1.24	V
OLP Threshold Voltage	4 - 3	V_{OLP}	-	7.3	8.6	9.9	V
Current at OLP Operation	4	I_{OLP}	-	-12	-17	-22	µA
OLP Delay Time	4 - 3	t_{OLP}	-	0.84	1.20	1.56	s
Maximum FB Current	4	$I_{FB(MAX)}$	-	220	310	400	µA
CC Set Voltage	4 - 3	$V_{SET(CC)}$	-	4.9	5.8	6.7	V
CC Reset Voltage	4 - 3	$V_{RES(CC)}$	V_{CC} = 25 V	3.5	3.9	4.3	V
Start-Up Current	5	$I_{startup}$	V_{CC} = 13 V	0.77	1.10	1.43	mA
OVP Operation Voltage	5 - 3	$V_{CC(OVP)}$	V_{CC} = 18 → 35.2 V	28.8	32.0	35.2	V
OVP/TSD Latch Sustaining Current	5	$I_{CC(H)}$	V_{CC} =35.2 → 8.6 V	-	-	270	µA
OVP/TSD Latch Release Voltage	5 - 3	V_{CC}	V_{CC} =35.2 → 5.9 V	5.9	7.2	8.6	V
Thermal Shutdown	-	T_J	-	125	140	-	°C
Thermal Resistance	-	$R_{\theta JF}$	-	-	-	52	°C/W

Typical values are given for circuit design information only.

Negative current is defined as coming out of (sourcing) the specified terminal.

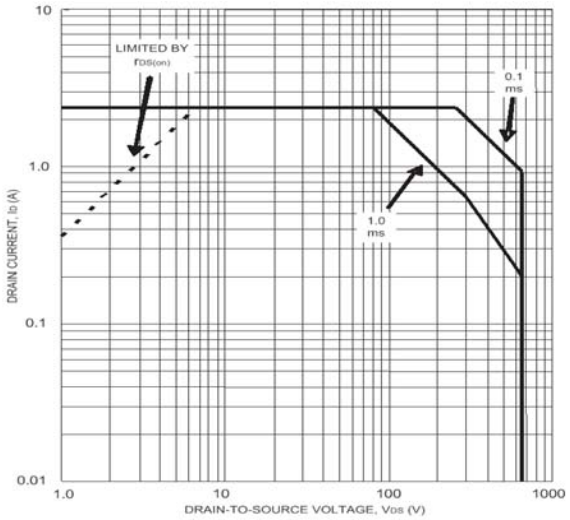
MOSFET TYPICAL CHARACTERISTICS

STR-A6251

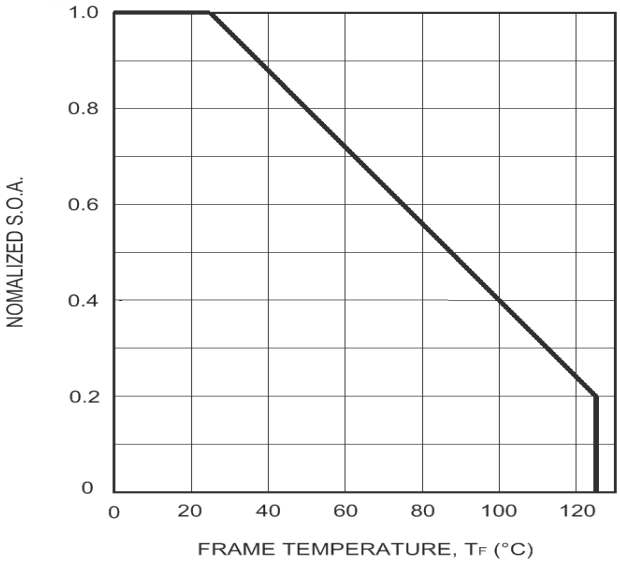


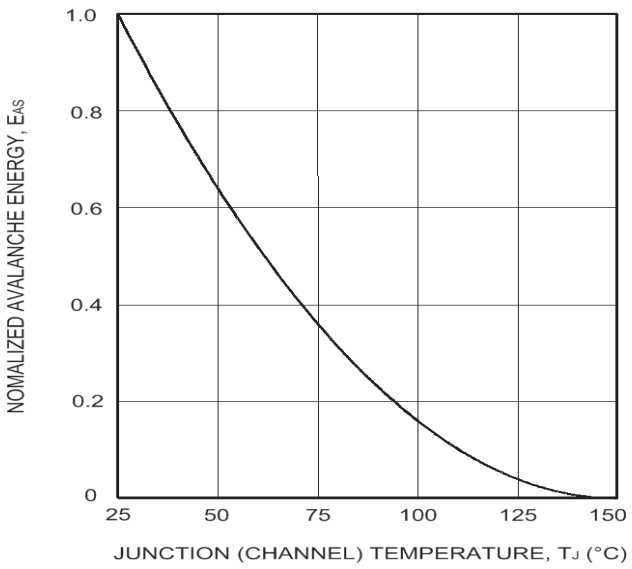
Avalanche energy is measured at V_{DD} = 99 V,
L = 20 mH, I_L = 2.5 A.

STR-A6252



Avalanche energy is measured at V_{DD} = 99 V,
L = 20 mH, I_L = 3.0 A.





Recommended Operating Conditions

Operating Ambient Temperature ..... -20°C to +100°C
Operating Junction Temperature ..... -20°C to +125°C
Maximum Frame Temperature ..... +115°C
For the availability of parts meeting -40°C requirements, contact Allegro's Sales Representative.

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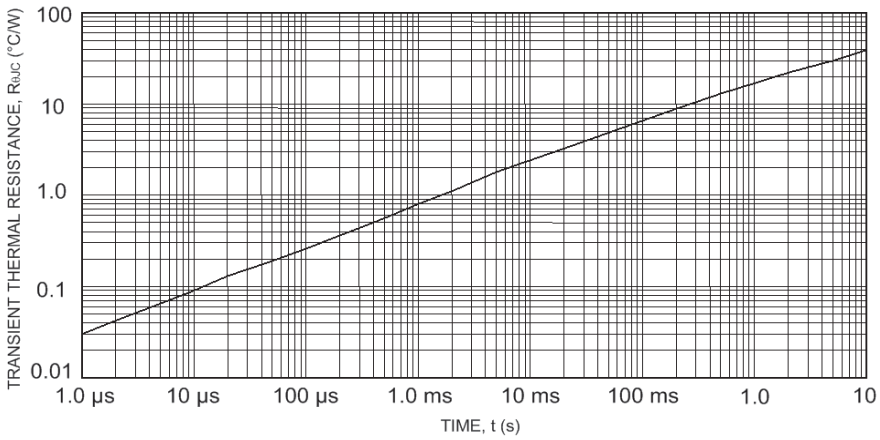
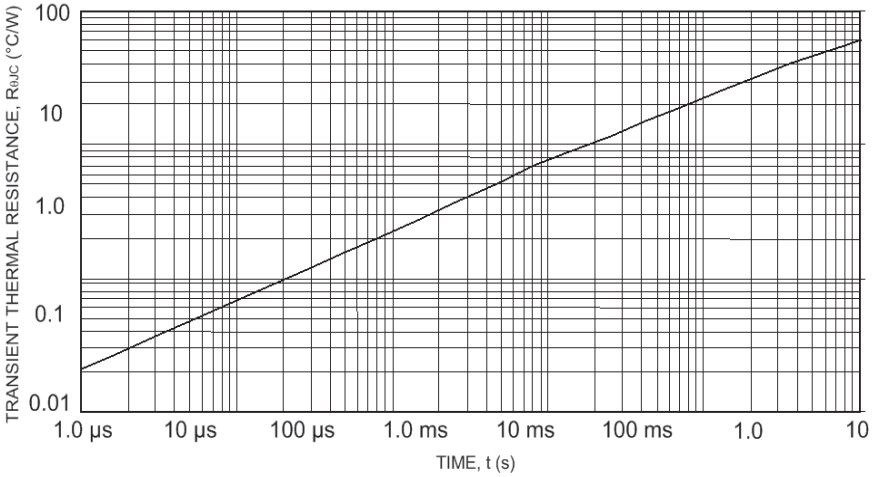
MOSFET TYPICAL CHARACTERISTICS (cont'd)

STR-A6251



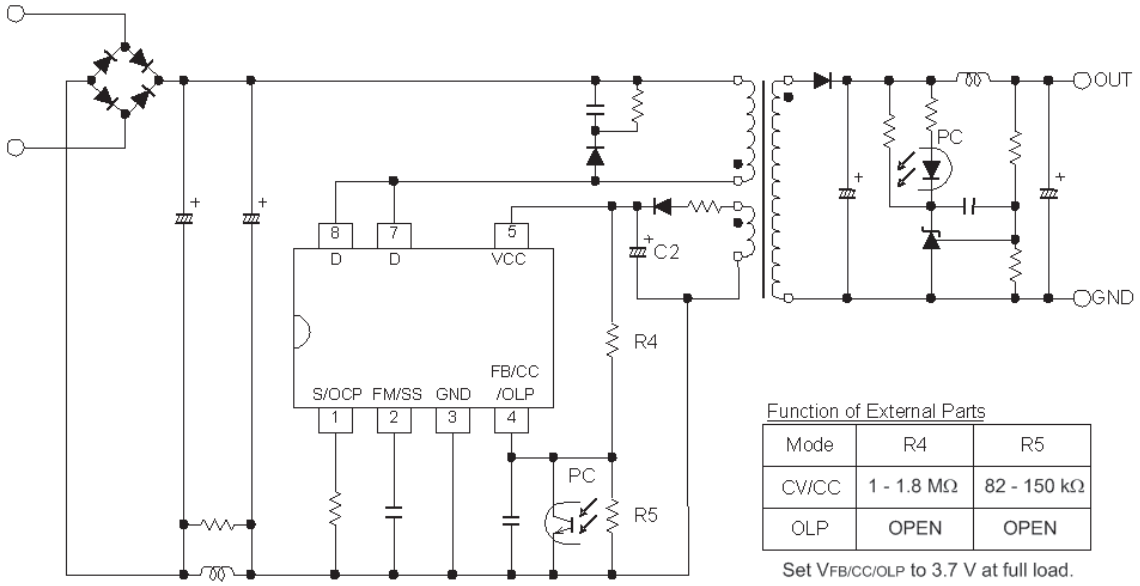
STR-A6252



WARNING — These devices are designed to be operated at lethal voltages and energy levels. Circuit designs that embody these components must conform with applicable safety requirements. Precautions must be taken to prevent accidental contact with power-line potentials. Do not connect grounded test equipment.

The use of an isolation transformer is recommended during circuit development and breadboarding.

APPLICATIONS INFORMATION



Function of External Parts

Mode	R4	R5
CV/CC	1 - 1.8 MΩ	82 - 150 kΩ
OLP	OPEN	OPEN

Set $V_{FB/CC/OLP}$ to 3.7 V at full load.

Typical Application

NOTE: The start-up performance of the IC can only be guaranteed for values of C2 greater than 22 µF. This value is required to keep the internal supply voltage within regulation during IC initialization.

Complete product description and applications information is provided in Application Note 28103.40, *Series STR-A6200 Flyback Switching Regulators*.

The products described herein are manufactured in Japan by Sanken Electric Co., Ltd. for sale by Allegro MicroSystems, Inc.

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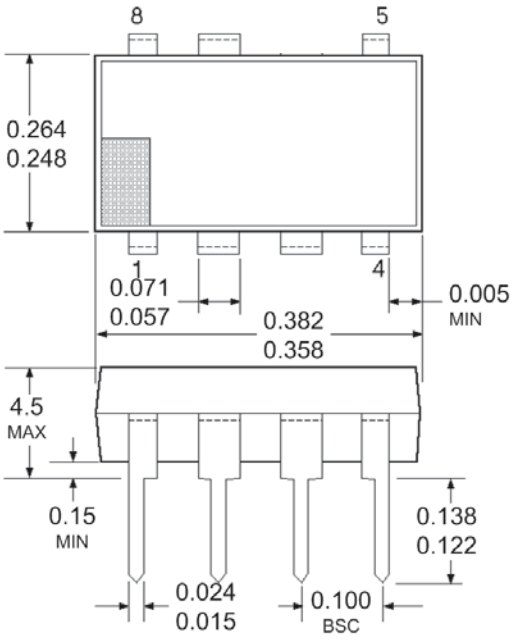
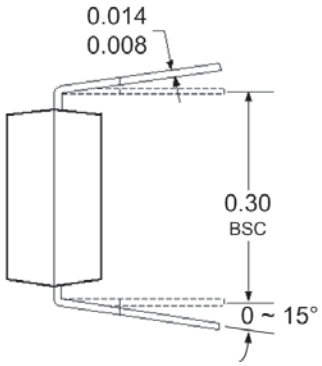
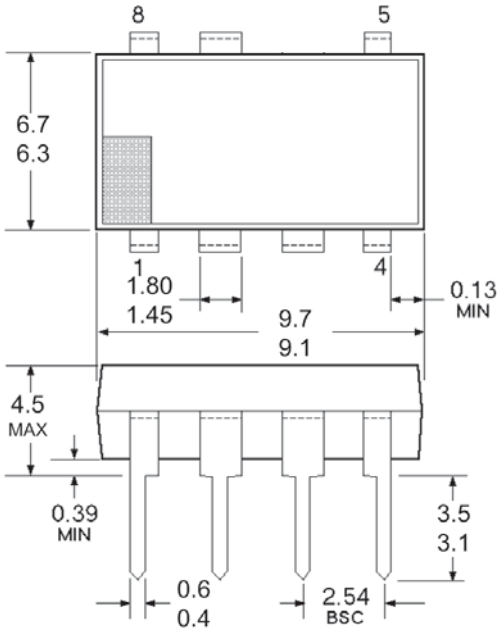
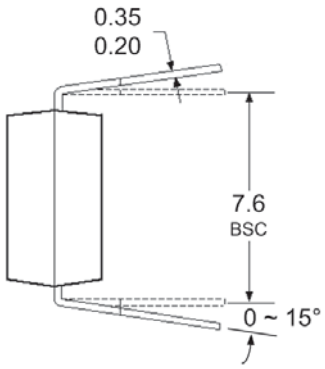
PACKAGE DIMENSIONS





Dimensions in Inches
(for reference only)





Dimensions in Millimeters
(controlling dimensions)

Terminal Finish: Pure Sn, 2nd level interconnect category (e3).
Product Weight: Approx. 0.51 g.
Frame temperature, T_F, is measured at the root of pin 3.
For more efficient heat radiation, connect a broad PCB pattern at pins 7 and 8.