A5M34TG140–TC

Airfast Power Amplifier Module

Rev. 0 — February 2023

Data Sheet: Technical Data

The A5M34TG140–TC is a fully integrated Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells and low power remote radio heads. The field–proven LDMOS and GaN on SiC power amplifiers are designed for TDD LTE and 5G systems.

3300–3670 MHz

- Typical LTE Performance: P_{out} = 10.7 W Avg., V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc, 1 × 20 MHz LTE, Input Signal PAR = 8 dB @ 0.01% Probability on CCDF. [(1)]

Carrier Center Frequency	Gain (dB)	ACPR (dBc)	PAE (%)
3310 MHz	31.2	–30.7	42.1
3500 MHz	31.0	–30.8	46.0
3660 MHz	30.7	–31.4	48.0

1. All data measured with device soldered in NXP reference circuit.

Features

- 2–stage module solution that includes an LDMOS integrated circuit as a driver and a GaN final stage amplifier
- Advanced high performance in–package Doherty
- Thermal path is separated from electrical/solder connection path for enhanced thermal dissipation
- Fully matched (50 ohm input/output, DC blocked)
- Designed for low complexity digital linearization systems
- Reduced memory effects for improved linearized error vector magnitude

A5M34TG140–TC

3300–3670 MHz, 31 dB, 10.7 W Avg.
AIRFAST POWER AMPLIFIER MODULE

14 mm × 10 mm Module

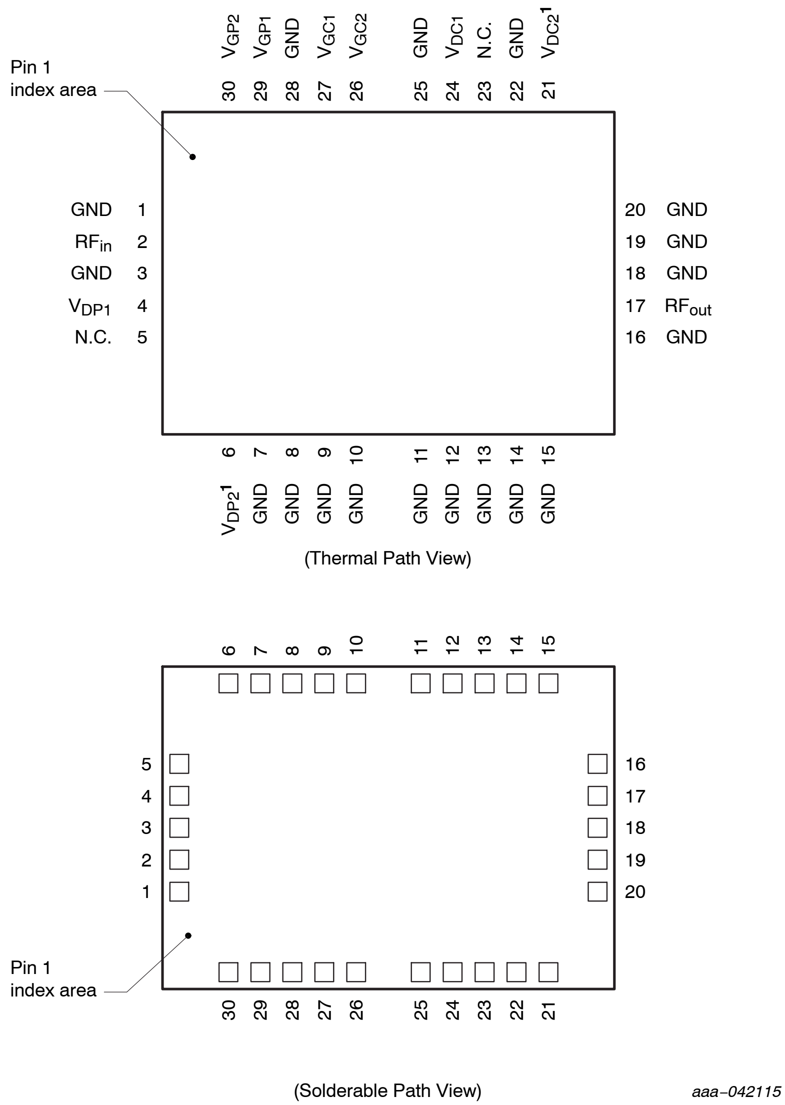


Figure 1. Pin Connections

1. V_{DP2} and V_{DC2} are DC coupled internal to the package and must be powered by a single DC power supply.

Table 1. Functional Pin Description

Pin Number	Pin Function	Pin Description
1, 3, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 18, 19, 20, 22, 25, 28	GND	Ground
2	RF_{in}	RF Input
4	V_{DP1}	Peaking Drain Supply, Stage 1
5, 23	N.C.	No Connection
6	V_{DP2}	Peaking Drain Supply, Stage 2
17	RF_{out}	RF Output
21	V_{DC2}	Carrier Drain Supply, Stage 2
24	V_{DC1}	Carrier Drain Supply, Stage 1
26	V_{GC2}	Carrier Gate Supply, Stage 2
27	V_{GC1}	Carrier Gate Supply, Stage 1
29	V_{GP1}	Peaking Gate Supply, Stage 1
30	V_{GP2}	Peaking Gate Supply, Stage 2

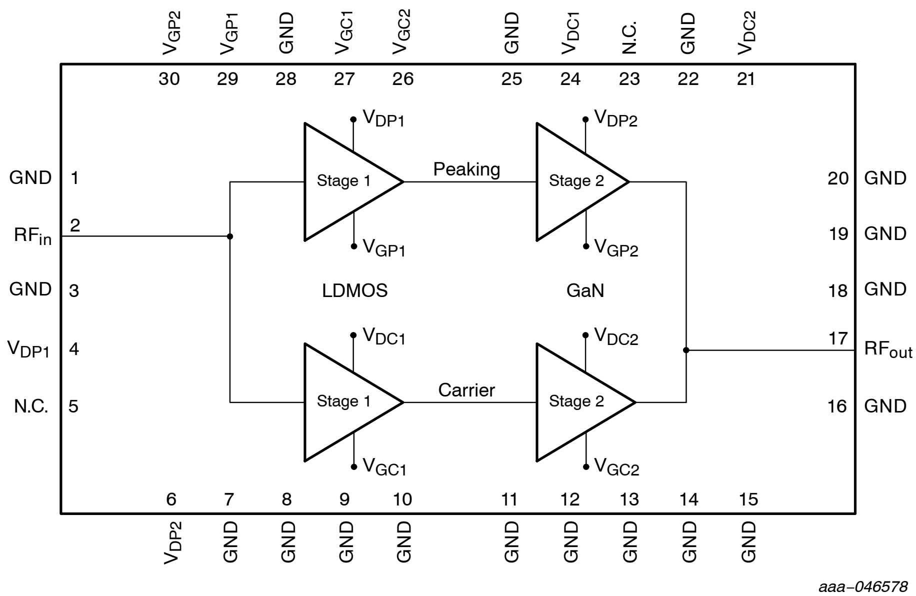


Figure 2. Functional Electrical Routing Diagram

Table 2. Maximum Ratings

Rating	Symbol	Value	Unit
Gate–Bias Voltage Range	V_{G1} V_{G2}	–0.5 to +10 –6, 0	Vdc
Operating Voltage Range	V_{DD1} V_{DD2}	4.75 to 5.25 +38 to +55	Vdc
Maximum Forward Gate Current, $I_{G\ (A+B)}$, @ T_C = 25°C	I_{GMAX}	11.3	mA
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature	T_C	125	°C
Maximum Channel Temperature	T_{CH}	225	°C
Peak Input Power (3500 MHz, Pulsed CW, 10 μsec(on), 10% Duty Cycle, V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc)	P_{in}	28	dBm

Table 3. Lifetime

Characteristic	Symbol	Value	Unit
Mean Time to Failure Case Temperature 125°C, 75% Duty Cycle, 10.7 W Avg., V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc	MTTF	> 10	Years

Table 4. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface–to–Case Case Temperature 125°C, P_D = 14.0 W	$R_{\theta JC}$ (IR)	4.4 (1)	°C/W
Thermal Resistance by Finite Element Analysis, Channel–to–Case Case Temperature 125°C, P_D = 12.7 W	$R_{\theta CHC}$ (FEA)	7.9 (2)	°C/W

Table 5. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS–001–2017)	2
Charge Device Model (per JS–002–2014)	C3

Table 6. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, EIA/IPC/JEDEC J–STD–020/JEDEC J–STD–075A	3/R6	250	°C

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955. High conductivity thermal interface used.
2. $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where *T* is the channel temperature in degrees Celsius, *A* = –11.6 and *B* = 9129.

Table 7. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Carrier + Peaking Stage 2, GaN — Off Characteristics					
Off−State Drain Leakage [(1)] (V_{DS} = 150 Vdc, V_{GS} = –8 Vdc)	$I_{D(BR)}$	—	—	5.0	mAdc
Off−State Gate Leakage (V_{DS} = 48 Vdc, V_{GS} = –7 Vdc)	I_{GLK}	–4.0	—	—	mAdc

Characteristic	Symbol	Typ	Range	Unit
Carrier Stage 1, LDMOS — On Characteristics				
Gate Threshold Voltage (V_{DS} = 5 Vdc, I_{DC1} = 120 μAdc)	$V_{GS(th)}$	1.4	±0.4	Vdc
Gate Quiescent Voltage (V_{DS} = 5 Vdc, I_{DQC1} = 145 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.0	±0.4	Vdc
Carrier Stage 2, GaN — On Characteristics				
Gate Threshold Voltage [(1)] (V_{DS} = 10 Vdc, I_D = 11.3 mAdc)	$V_{GS(th)}$	–2.7	±1.0	Vdc
Gate Quiescent Voltage (V_{DS} = 48 Vdc, I_{DQC2} = 35 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	–2.7	±1.0	Vdc
Peaking Stage 1, LDMOS — On Characteristics				
Gate Threshold Voltage (V_{DS} = 5 Vdc, I_{DP1} = 120 μAdc)	$V_{GS(th)}$	1.4	±0.4	Vdc
Gate Quiescent Voltage (V_{DS} = 5 Vdc, I_{DQP1} = 30 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.8	±0.4	Vdc
Peaking Stage 2, GaN — On Characteristics				
Gate Threshold Voltage [(1)] (V_{DS} = 10 Vdc, I_D = 11.3 mAdc)	$V_{GS(th)}$	–2.7	±1.0	Vdc
Gate Quiescent Voltage (V_{DS} = 48 Vdc, I_{DQP2} = 3 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	–2.9	±1.0	Vdc

1. Carrier side and Peaking side are tied together for these measurements.

(continued)

Table 7. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests — 3300 MHz (1) (In NXP Doherty Production ATE (2) Test Fixture, 50 ohm system) V_{DD1} = 5 Vdc, V_{DD2} = 48 Vdc, I_{DQC1} = 145 mA, I_{DQC2} = 35 mA, I_{DQP1} = 30 mA, V_{GP2} = (V_{BIAS} – 0.4) (3) Vdc, P_{out} = 10.7 W Avg., 1–tone CW, f = 3300 MHz.					
Gain	G	29.3	31.9	—	dB
Drain Efficiency	η_D	34.5	42.1	—	%
P_{out} @ 3 dB Compression Point	P3dB	48.0	49.1	—	dBm
Functional Tests — 3670 MHz (1) (In NXP Doherty Production ATE (2) Test Fixture, 50 ohm system) V_{DD1} = 5 Vdc, V_{DD2} = 48 Vdc, I_{DQC1} = 145 mA, I_{DQC2} = 35 mA, I_{DQP1} = 30 mA, V_{GP2} = (V_{BIAS} – 0.4) (3) Vdc, P_{out} = 10.7 W Avg., 1–tone CW, f = 3670 MHz.					
Gain	G	28.6	31.5	—	dB
Drain Efficiency	η_D	43.0	49.3	—	%
P_{out} @ 3 dB Compression Point	P3dB	48.4	49.7	—	dBm
Wideband Ruggedness (4) (In NXP Doherty Power Amplifier Module Reference Circuit, 50 ohm system) I_{DQC1} = 145 mA, I_{DQC2} = 35 mA, I_{DQP1} = 30 mA, V_{GP2} = (V_{BIAS} – 0.4) (3) Vdc, f = 3500 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR					
ISBW of 400 MHz at 55 Vdc, 3 dB Input Overdrive from 10.7 W Avg. Modulated Output Power	No Device Degradation				
Typical Performance (4) (In NXP Doherty Power Amplifier Module Reference Circuit, 50 ohm system) V_{DD1} = 5 Vdc, V_{DD2} = 48 Vdc, I_{DQC1} = 145 mA, I_{DQC2} = 35 mA, I_{DQP1} = 30 mA, V_{GP2} = (V_{BIAS} – 0.4) (2) Vdc, 3500 MHz					
VBW Resonance Point, 2–tone, 1 MHz Tone Spacing (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	230	—	MHz
1–carrier 20 MHz LTE, 8 dB Input Signal PAR					
Gain	G	—	31.0	—	dB
Power Added Efficiency	PAE	—	46.0	—	%
Adjacent Channel Power Ratio	ACPR	—	–30.8	—	dBc
Adjacent Channel Power Ratio	ALT1	—	–45.6	—	dBc
Adjacent Channel Power Ratio	ALT2	—	–52.0	—	dBc
Gain Flatness (5)	G_F	—	0.5	—	dB
Pulsed CW, 10% Duty Cycle					
P_{out} @ 3 dB Compression Point	P3dB	—	49.2	—	dBm
AM/PM @ P3dB	Φ	—	–16	—	°
Gain Variation @ Avg. Power over Temperature (–40°C to +125°C)	ΔG	—	0.034	—	dB/°C
P3dB Variation over Temperature (–40°C to +125°C)	ΔP3dB	—	0.005	—	dB/°C

Table 8. Ordering Information

Device	Tape and Reel Information	Package
A5M34TG140–TCT1	T1 Suffix = 1,000 Units, 24 mm Tape Width, 13–inch Reel	14 mm × 10 mm Module

1. Part input and output matched to 50 ohms.
2. ATE is a socketed test environment.
3. Increase V_{GP2} (peaking side) until I_{DQP2} = 40 mA current is attained, and then subtract 0.4 V for final V_{GP2} bias voltage.
4. All data measured in fixture with device soldered in NXP reference circuit.
5. Gain flatness = Max(G(f_{Low} to f_{High})) – Min(G(f_{Low} to f_{High}))

Correct Biasing Sequence

Turn ON:

Bias ON the GaN final stage first

1. Set gate voltage V_{GC2} and V_{GP2} to –5 V.
2. Set drain voltage V_{DC2} and V_{DP2} to nominal supply voltage (+48 V).
3. Increase V_{GP2} (peaking side) until I_{DQP2} = 40 mA current is attained, and then subtract 0.4 V for final V_{GP2} bias voltage.
4. Increase V_{GC2} (carrier side) until I_{DQC2} current is attained.

Bias ON the LDMOS driver stage second

5. Set drain voltage V_{DC1} and V_{DP1} to nominal supply voltage (+5 V).
6. Increase V_{GC1} (carrier side) until I_{DQC1} current is attained.
7. Increase V_{GP1} (peaking side) until I_{DQP1} current is attained.
8. Apply RF input power to desired level.

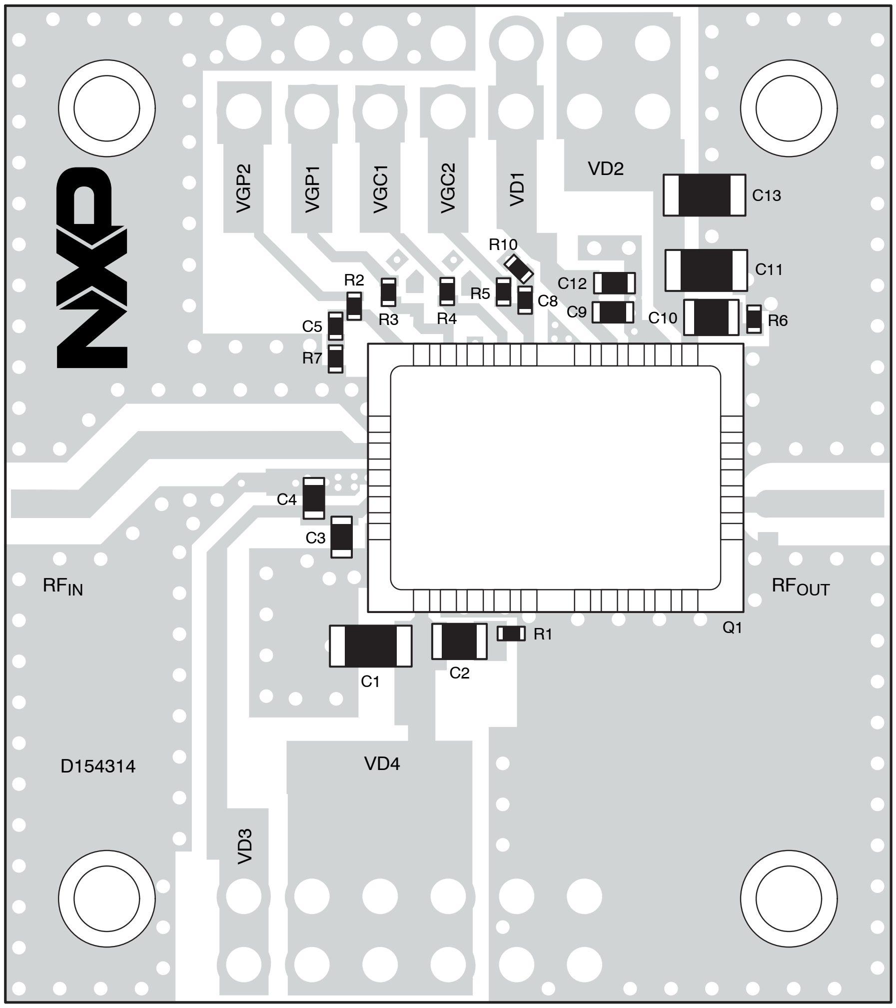
Turn OFF:

Bias OFF the GaN final stage first

1. Disable RF input power.
2. Adjust gate voltage V_{GC2} and V_{GP2} to –5 V.
3. Adjust drain voltage V_{DC2} and V_{DP2} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Disable V_{GC2} and V_{GP2}.

Bias OFF the LDMOS driver stage second

5. Adjust gate voltage V_{GC1} and V_{GP1} to 0 V.
6. Adjust drain voltage V_{DC1} and V_{DP1} to 0 V.



Board Label	Pin Description	Pin Function
VD1	Carrier Drain Supply, Stage 1	V_{DC1}
VD2	Carrier Drain Supply, Stage 2	V_{DC2}
VD3	Peaking Drain Supply, Stage 1	V_{DP1}
VD4	Peaking Drain Supply, Stage 2	V_{DP2}

Figure 3. A5M34TG140−TC Reference Circuit Component Layout

Table 9. A5M34TG140−TC Reference Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C11, C13	4.7 μF Chip Capacitor	GRM31CC72A475KE11L	Murata
C2, C10	1 μF Chip Capacitor	GRM21BC72A105KE01L	Murata
C3, C9	1 μF Chip Capacitor	GRT188R61H105KE13D	Murata
C4, C12	10 μF Chip Capacitor	GRM188R61E106KA73D	Murata
C5	0.1 μF Chip Capacitor	GRM155R61H104KE19D	Murata
C8	10 nF Chip Capacitor	GRM155R71E103KA01D	Murata
Q1	Power Amplifier Module	A5M34TG140−TC	NXP
R1, R6	2 Ω, 1/10 W Chip Resistor	ERJ−2GEJ2R0X	Panasonic
R2, R3, R5	1 Ω, 1/10 W Chip Resistor	ERJ−2GEJ1R0X	Panasonic
R4, R10	10 Ω, 1/10 W Chip Resistor	ERJ−2GEJ100X	Panasonic
R7	0 Ω, 1/20 W Chip Resistor	ERJ−1GN0R00C	Panasonic
PCB	Megtron R−5575, 0.020″, ε_r = 3.67	D154314	MTL

Note: Component numbers C6, C7, R8 and R9 are intentionally omitted.

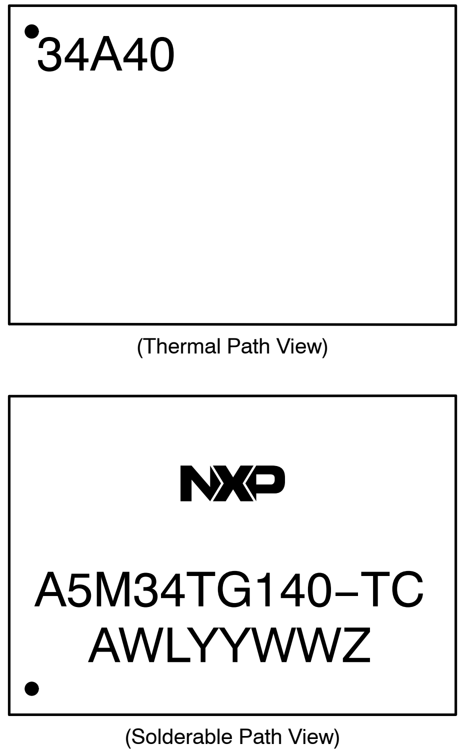


Figure 4. Product Marking

Package Information

H–PLGA–30 I/O
14 X 10 X 1.97 PKG, 1 PITCH

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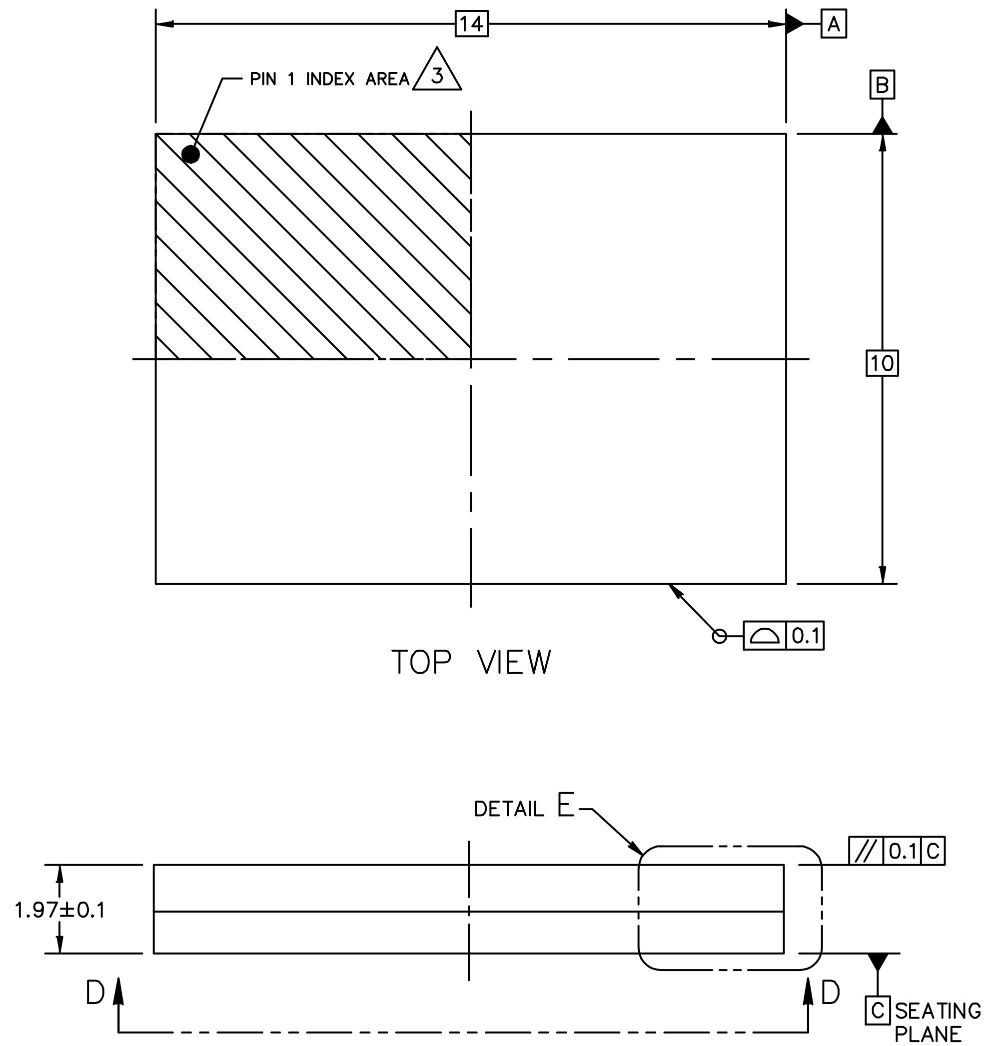
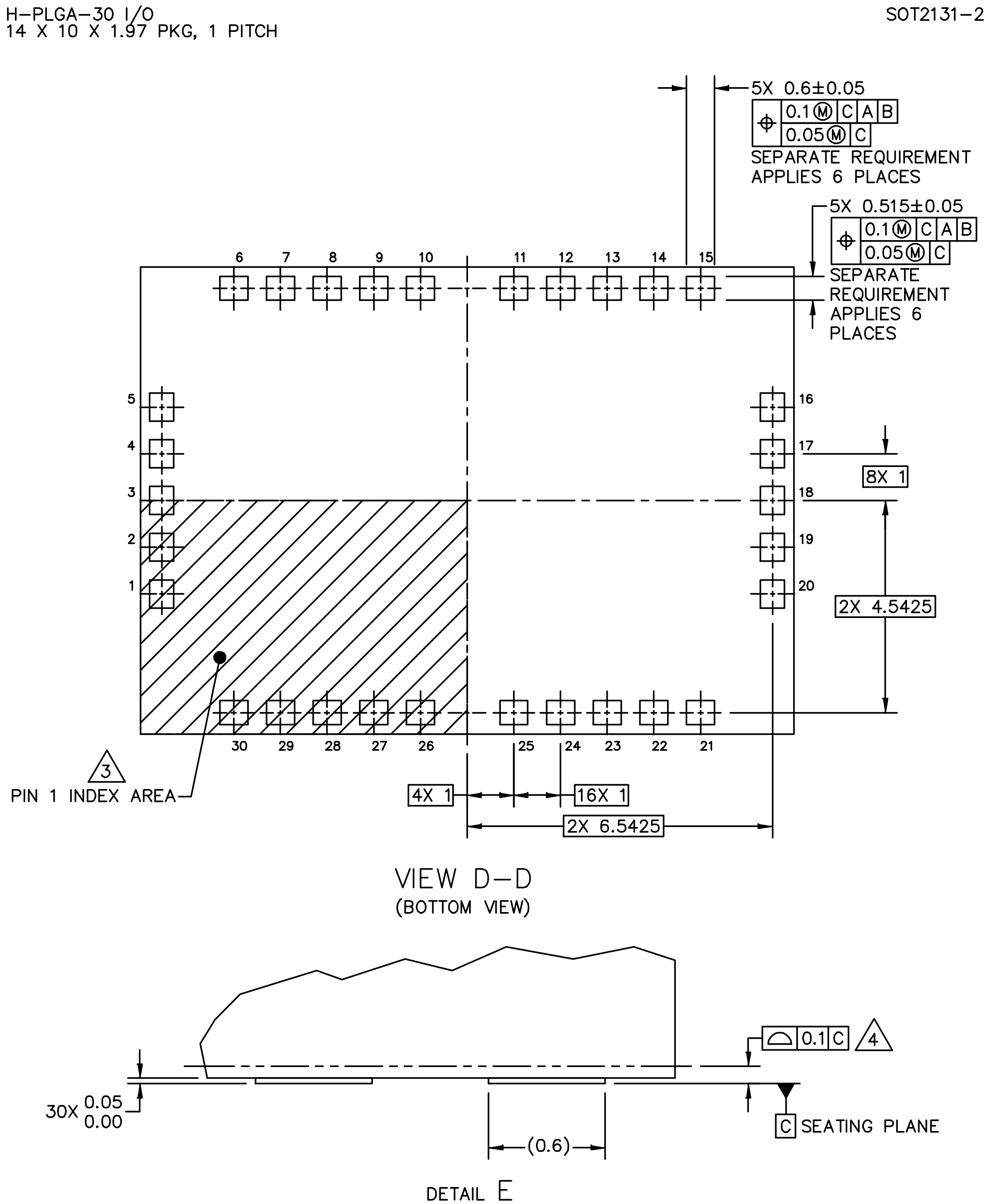


DATE: 28 SEP 2022

MECHANICAL OUTLINE	STANDARD:	DRAWING NUMBER:	REVISION:	PAGE:
PRINT VERSION NOT TO SCALE	NON–JEDEC	98ASA01864D	A	1 OF 6



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H–PLGA–30 I/O
14 X 10 X 1.97 PKG, 1 PITCH

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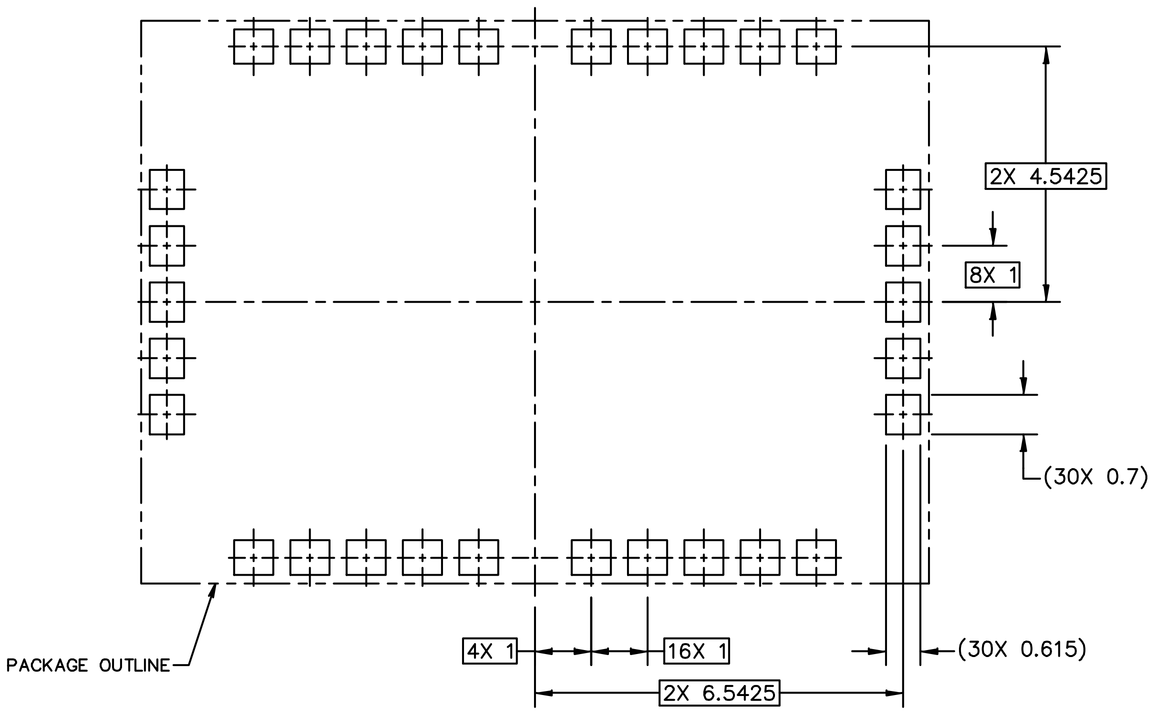

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H–PLGA–30 I/O
14 X 10 X 1.97 PKG, 1 PITCH

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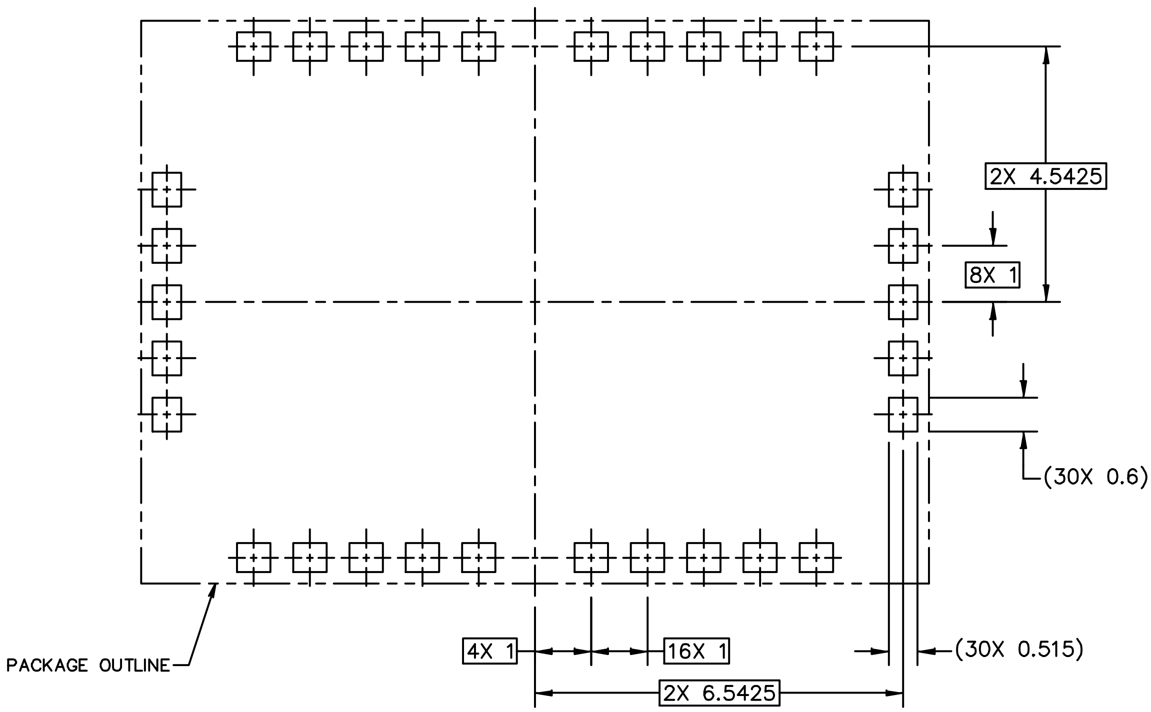

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H–PLGA–30 I/O
14 X 10 X 1.97 PKG, 1 PITCH

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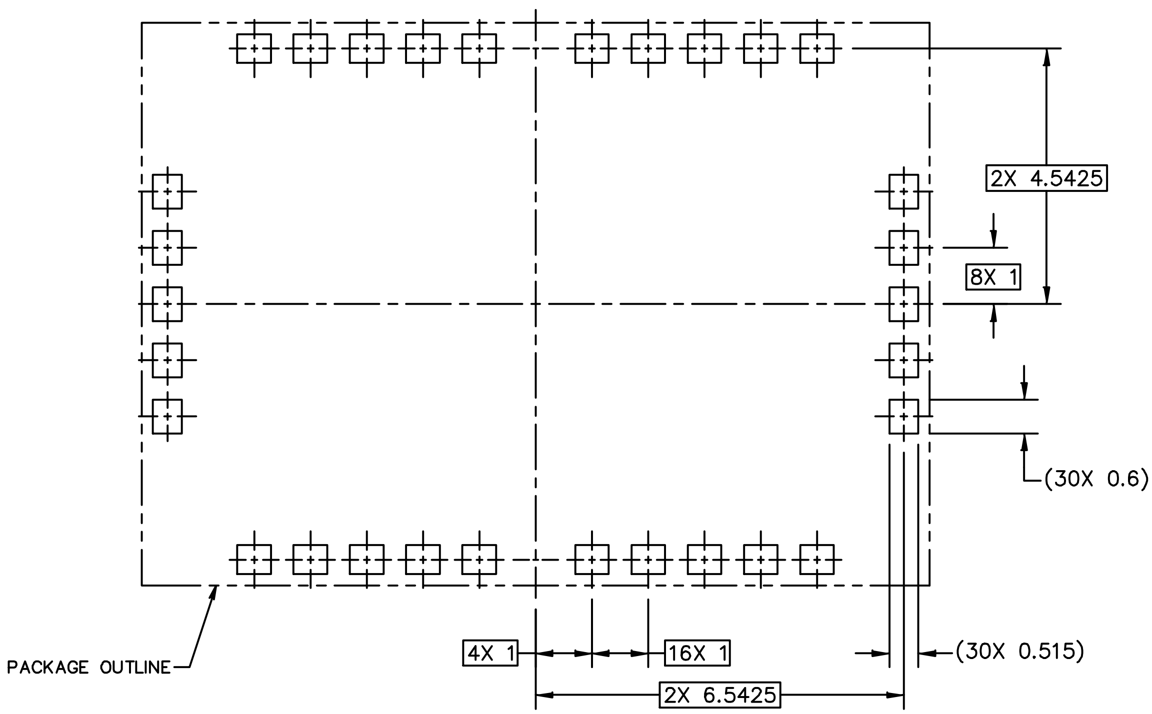

RECOMMENDED STENCIL THICKNESS 0.125 OR 0.150

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H-PLGA-30 I/O
14 X 10 X 1.97 PKG, 1 PITCH

SOT2131-2

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO ALL LEADS.

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	NON-JEDEC	98ASA01864D	A	6

Product Documentation and Tools

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Development Tools

- Printed Circuit Boards

Revision History

The following table summarizes revisions to this document.

Revision	Date	Description
0	Feb. 2023	• Initial release of data sheet

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