ProASIC3E Flash Family FPGAs

with Optional Soft ARM® Support

FlashLock

Features and Benefits

High Capacity
- 600 k to 3 Million System Gates
- 108 to 504 kbits of True Dual-Port SRAM
- Up to 620 User I/Os

Reprogrammable Flash Technology
- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Live at Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off

On-Chip User Nonvolatile Memory
- 1 kbit of FlashROM with Synchronous Interfacing

High Performance
- 350 MHz System Performance
- 3.3 V, 66 MHz 64-Bit PCI

In-System Programming (ISP) and Security
- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532–compliant)
- FlashLock® to Secure FPGA Contents

Low Power
- Core Voltage for Low Power
- Support for 1.5-V-Only Systems
- Low-Impedance Flash Switches

High-Performance Routing Hierarchy
- Segmented, Hierarchical Routing and Clock Structure
- Ultra-Fast Local and Long-Line Network
- Enhanced High-Speed, Very-Long-Line Network
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

Pro (Professional) I/O
- 700 Mbps DDR, LVDS-Capable I/Os

- 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 8 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS
- Voltage-Referenced I/O Standards: GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Programmable Input Delay
- Schmitt Trigger Option on Single-Ended Inputs
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the ProASIC®3E Family

Clock Conditioning Circuit (CCC) and PLL
- Six CCC Blocks, Each with an Integrated PLL
- Configurable Phase-Shift, Multiply/Divide, Delay Capabilities and External Feedback
- Wide Input Frequency Range (1.5 MHz to 200 MHz)

SRAMs and FIFOs
- Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations available)
- True Dual-Port SRAM (except ×18)
- 24 SRAM and FIFO Configurations with Synchronous Operation up to 350 MHz

ARM® Processor Support in ProASIC3E FPGAs
- M1 ProASIC3E Devices—Cortex-M1 Soft Processor Available with or without Debug

Table 1-1 • ProASIC3E Product Family

ProASIC3E Devices	A3PE600	A3PE1500	A3PE3000
Cortex-M1 Devices[1]		M1A3PE1500	M1A3PE3000
System Gates	600 k	1.5 M	3 M
VersaTiles (D-flip-flops)	13,824	38,400	75,264
RAM kbits (1,024 bits)	108	270	504
4,608-Bit Blocks	24	60	112
FlashROM Bits	1 k	1 k	1 k
Secure (AES) ISP	Yes	Yes	Yes
CCCs with Integrated PLLs[2]	6	6	6
VersaNet Globals[3]	18	18	18
I/O Banks	8	8	8
Maximum User I/Os	270	444	620

Package Pins
  PQFP
  FBGA
	PQ208
	FG256, FG484
		PQ208
		FG484, FG676
			PQ208
			FG324, FG484, FG896

Notes:
1. *Refer to the Cortex-M1 product brief for more information.*
2. *The PQ208 package has six CCCs and two PLLs.*
3. *Six chip (main) and three quadrant global networks are available.*
4. *For devices supporting lower densities, refer to the ProASIC3 Flash Family FPGAs handbook.*
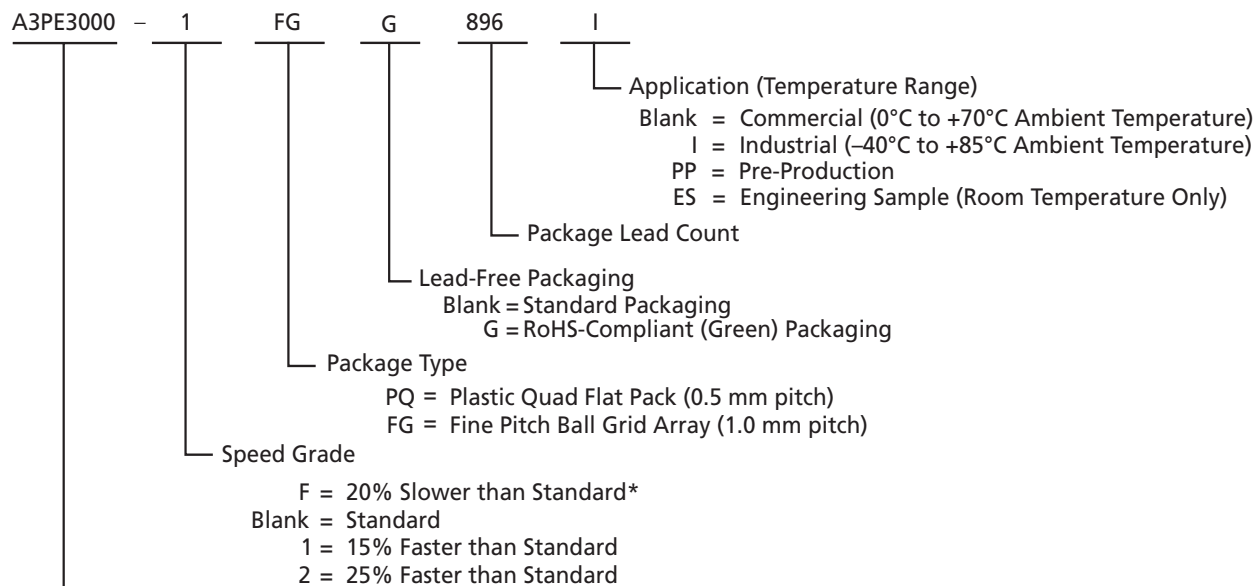
I/Os Per Package[1]

ProASIC3E Devices	A3PE600		A3PE1500 [3]		A3PE3000 [3]	
Cortex-M1 Devices[2]			M1A3PE1500		M1A3PE3000	
	I/O Types					
Package	Single-Ended I/O[1]	Differential I/O Pairs	Single-Ended I/O[1]	Differential I/O Pairs	Single-Ended I/O[1]	Differential I/O Pairs
PQ208	147	65	147	65	147	65
FG256	165	79	–	–	–	–
FG324	–	–	–	–	221	110
FG484	270	135	280	139	341	168
FG676	–	–	444	222	–	–
FG896	–	–	–	–	620	310

Notes:

1. When considering migrating your design to a lower- or higher-density device, refer to the ProASIC3E Flash Family FPGAs handbook to ensure compliance with design and board migration requirements.

2. Each used differential I/O pair reduces the number of single-ended I/Os available by two.

3. For A3PE1500 and A3PE3000 devices, the usage of certain I/O standards is limited as follows:
   – SSTL3(I) and (II): up to 40 I/Os per north or south bank
   – LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
   – SSTL2(I) and (II) / GTL+ 2.5 V/ GTL 2.5 V: up to 72 I/Os per north or south bank

4. FG256 and FG484 are footprint-compatible packages.

5. When using voltage-referenced I/O standards, one I/O pin should be assigned as a voltage-referenced pin (V_{REF}) per minibank (group of I/Os).

6. "G" indicates RoHS-compliant packages. Refer to the "ProASIC3E Ordering Information" on page III for the location of the "G" in the part number.

ProASIC3E Ordering Information

A3PE3000 – 1 FG G 896 I

Application (Temperature Range)
Blank = Commercial (0°C to +70°C Ambient Temperature)
I = Industrial (–40°C to +85°C Ambient Temperature)
PP = Pre-Production
ES = Engineering Sample (Room Temperature Only)

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS-Compliant (Green) Packaging

Package Type
PQ = Plastic Quad Flat Pack (0.5 mm pitch)
FG = Fine Pitch Ball Grid Array (1.0 mm pitch)

Speed Grade
F = 20% Slower than Standard*
Blank = Standard
1 = 15% Faster than Standard
2 = 25% Faster than Standard

Part Number
ProASIC3E Devices
A3PE600 = 600,000 System Gates
A3PE1500 = 1,500,000 System Gates
A3PE3000 = 3,000,000 System Gates

ProASIC3E Devices with Cortex-M1
M1A3PE1500 = 1,500,000 System Gates
M1A3PE3000 = 3,000,000 System Gates

* The DC and switching characteristics for the –F speed grade targets are based only on simulation. The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

Temperature Grade Offerings

Package	A3PE600	A3PE1500	A3PE3000
Cortex-M1 Devices		M1A3PE1500	M1A3PE3000
PQ208	C, I	C, I	C, I
FG256	C, I	–	–
FG324	–	–	C, I
FG484	C, I	C, I	C, I
FG676	–	C, I	–
FG896	–	–	C, I

Note: *C = Commercial temperature range: 0°C to 70°C ambient temperature*
I = Industrial temperature range: –40°C to 85°C ambient temperature

Speed Grade and Temperature Grade Matrix

Temperature Grade	–F [1]	Std.	–1	–2
C [2]	✓	✓	✓	✓
I [3]	–	✓	✓	✓

Notes:

1. *The DC and switching characteristics for the –F speed grade targets are based only on simulation.*
   The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

2. *C = Commercial temperature range: 0°C to 70°C ambient temperature*

3. *I = Industrial temperature range: –40°C to 85°C ambient temperature*

References made to ProASIC3E devices also apply to ARM-enabled ProASIC3E devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

Contact your local Actel representative for device availability:
http://www.actel.com/contact/default.aspx.

1 – ProASIC3E Device Family Overview

General Description

ProASIC3E, the third-generation family of Actel flash FPGAs, offers performance, density, and features beyond those of the ProASIC^PLUS® family. Nonvolatile flash technology gives ProASIC3E devices the advantage of being a secure, low-power, single-chip solution that is live at power-up (LAPU). ProASIC3E is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3E devices offer 1 kbit of on-chip, programmable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on six integrated phase-locked loops (PLLs). ProASIC3E devices have up to three million system gates, supported with up to 504 kbits of true dual-port SRAM and up to 620 user I/Os.

Several ProASIC3E devices support the Cortex-M1 soft IP cores, and the ARM-Enabled devices have Actel ordering numbers that begin with M1A3PE.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based ProASIC3E devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3E family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3E family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/ communications, computing, and avionics markets.

Security

The nonvolatile, flash-based ProASIC3E devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC3E devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

ProASIC3E devices utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in ProASIC3E devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC3E devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3E devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed ProASIC3E device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3E family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The ProASIC3E family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your

valuable IP is protected and secure, making remote ISP possible. A ProASIC3E device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based ProASIC3E FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Live at Power-Up

The Actel flash-based ProASIC3E devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based ProASIC3E devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs that are used for these purposes in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC3E device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC3E devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC3E flash-based FPGAs. Once it is programmed, the flash cell configuration element of ProASIC3E FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based ProASIC3E devices exhibit power characteristics similar to an ASIC, making them an ideal choice for power-sensitive applications. ProASIC3E devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

ProASIC3E devices also have low dynamic power consumption to further maximize power savings.

Advanced Flash Technology

The ProASIC3E family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary ProASIC3E architecture provides granularity comparable to standard-cell ASICs. The ProASIC3E device consists of five distinct and programmable architectural features (Figure 1-1 on page 3):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Pro I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3E core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC family of third-generation architecture Flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of ProASIC3E devices via an IEEE 1532 JTAG interface.
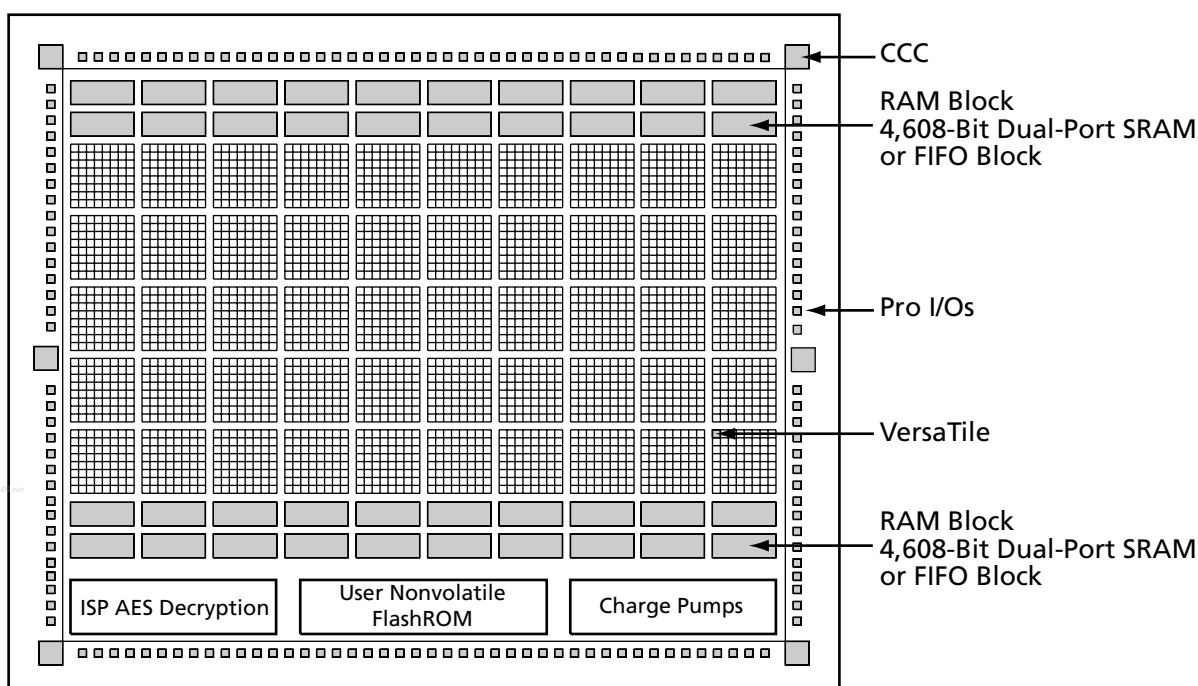

Figure 1-1 • **ProASIC3E Device Architecture Overview**

VersaTiles

The ProASIC3E core consists of VersaTiles, which have been enhanced beyond the ProASIC^PLUS® core tiles. The ProASIC3E VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set
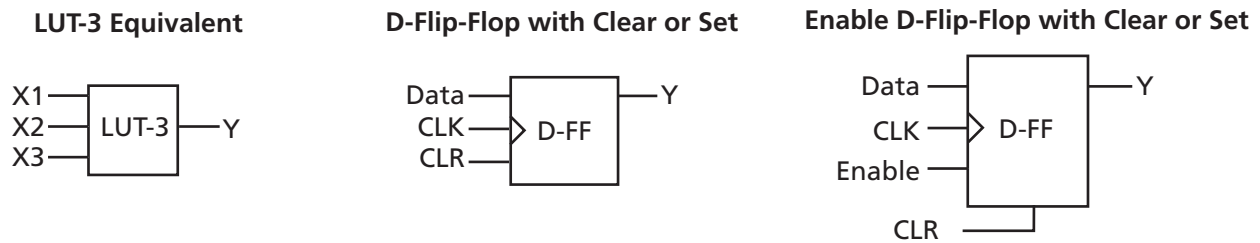
Refer to Figure 1-2 for VersaTile configurations.

LUT-3 Equivalent   **D-Flip-Flop with Clear or Set**   **Enable D-Flip-Flop with Clear or Set**

Figure 1-2 • **VersaTile Configurations**

User Nonvolatile FlashROM

Actel ProASIC3E devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3E IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel ProASIC3E development software solutions, Libero® Integrated Design Environment (IDE) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

ProASIC3E devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

ProASIC3E devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3E family contains six CCCs, each with an integrated PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

To maximize user I/Os, only the center east and west PLLs are available in devices using the PQ208 package. However, all six CCC blocks are still usable; the four corner CCCs allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time = 300 μs
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × (350 MHz / f_{OUT_CCC})

Global Clocking

ProASIC3E devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.

Pro I/Os with Advanced I/O Standards

The ProASIC3E family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3E FPGAs support 19 different I/O standards, including single-ended, differential, and voltage-referenced. The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported. Each I/O bank is subdivided into V_{REF} minibanks, which are used by voltage-referenced I/Os. V_{REF} minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common V_{REF} line. Therefore, if any I/O in a given V_{REF} minibank is configured as a V_{REF} pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-Data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II)

ProASIC3E banks support M-LVDS with 20 multi-drop points.

Part Number and Revision Date

Part Number 51700098-001-1

Revised March 2008

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v1.0)	Page
51700098-001-1	This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
51700098-001-0 (January 2008)	The FG324 package was added to the "ProASIC3E Product Family" table, the "I/Os Per Package1" table, and the "Temperature Grade Offerings" table for A3PE3000.	I, II, IV
v2.1 (July 2007)	This document was previously in datasheet v2.1. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700098-001-0.	N/A
v2.0 (April 2007)	CoreMP7 information was removed from the "Features and Benefits" section.	i
	The M1 device part numbers have been updated in Table 4 • ProASIC3E Product Family, "Packaging Tables", "Temperature Grade Offerings", "Speed Grade and Temperature Grade Matrix", and "Speed Grade and Temperature Grade Matrix".	iii, ii, iii, iv, iv
	The words "ambient temperature" were added to the temperature range in the "Temperature Grade Offerings", "Speed Grade and Temperature Grade Matrix", and "Speed Grade and Temperature Grade Matrix" sections.	iii, iv, iv
	The "Clock Conditioning Circuit (CCC) and PLL" section was updated.	i
Advance v0.6 (January 2007)	In the "Temperature Grade Offerings" section, Ambient was deleted.	iii
	Ambient was deleted from "Temperature Grade Offerings".	iii
	Ambient was deleted from the "Speed Grade and Temperature Grade Matrix".	iv

Previous Version	Changes in Current Version (v1.0)	Page
Advance v0.5 (April 2006)	In the "Packaging Tables" table, the number of I/Os for the A3PE1500 was changed for the FG484 and FG676 packages.	ii
Advance v0.4 (October 2005)	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
Advance v0.2	The "Packaging Tables" table was updated.	ii

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," "Preliminary," and "Production." The definition of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Actel Safety Critical, Life Support, and High-Reliability Applications Policy

The Actel products described in this advance status document may not have completed Actel's qualification process. Actel may amend or enhance products during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any Actel product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult Actel's Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of Actel's products is available on the Actel website at http://www.actel.com/documents/ORT_Report.pdf. Actel also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local Actel sales office for additional reliability information.

2 – ProASIC3E DC and Switching Characteristics

General Specifications

DC and switching characteristics for –F speed grade targets are based only on simulation.

The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 •   Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
V_{CC}	DC core supply voltage	–0.3 to 1.65	V
V_{JTAG}	JTAG DC voltage	–0.3 to 3.75	V
V_{PUMP}	Programming voltage	–0.3 to 3.75	V
V_{CCPLL}	Analog power supply (PLL)	–0.3 to 1.65	V
V_{CCI}	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VMV	DC I/O input buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (V_{CCI} + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [2]	Storage temperature	–65 to +150	°C
T_J [2]	Junction temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-3 on page 2-2.*

2. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-2, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

Table 2-2 • **Recommended Operating Conditions** [1]

Symbol	Parameter		Commercial	Industrial	Units
T_A	Ambient temperature		0 to +70 [4,6]	–40 to +85 [5,6]	°C
V_{CC}	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
V_{JTAG}	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
V_{PUMP}	Programming voltage	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation[3]	0 to 3.6	0 to 3.6	V
V_{CCPLL}	Analog power supply (PLL)		1.4 to 1.6	1.4 to 1.6	V
V_{CCI} and VMV [2]	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS/B-LVDS/M-LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*

2. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in* *VMV and V_{CCI} should be at the same voltage within a given I/O bank.*

3. *V_{PUMP} can be left floating during normal operation (not programming mode).*

4. *Maximum $T_J = 85$ °C.*

5. *Maximum $T_J = 100$ °C.*

6. *To ensure targeted reliability standards are met across ambient and junction operating temperatures, Actel recommends that the user follow best design practices using Actel's timing and power simulation tools.*

Table 2-3 • **Flash Programming Limits – Retention, Storage and Operating Temperature**[1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*

2. *These limits apply for program/data retention only. Refer to* *and* *for device operating conditions and absolute limits.*

Table 2-4 • **Overshoot and Undershoot Limits** [1]

V_{CCI} and VMV	Average V_{CCI}–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*

2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*

3. *The device meets overshoot/undershoot specification requirements for PCI inputs with V_{CCI} 3.45 V at 85°C maximum, whereas the average toggling of inputs at one-sixth of PCI frequency is considered.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC®3E device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4.

There are five regions to consider during power-up.

ProASIC3E I/Os are activated only if ALL of the following three conditions are met:

1. V_{CC} and V_{CCI} are above the minimum specified trip points (Figure 2-1 on page 2-4).
2. $V_{CCI} > V_{CC} - 0.75$ V (typical)
3. Chip is in the operating mode.

V_{CCI} Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

V_{CC} Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

V_{CC} and V_{CCI} ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to V_{CCI}.
- JTAG supply, PLL power supplies, and charge pump V_{PUMP} supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Actel recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until V_{CC} and V_{CCPLXL} exceed brownout activation levels. The V_{CC} activation level is specified as 1.1 V worst-case (see Figure 2-1 on page 2-4 for more details).

When PLL power supply voltage and/or V_{CC} levels drop below the V_{CC} brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the *Power-Up/-Down Behavior of Low-Power Flash Devices* chapter of the handbook for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation
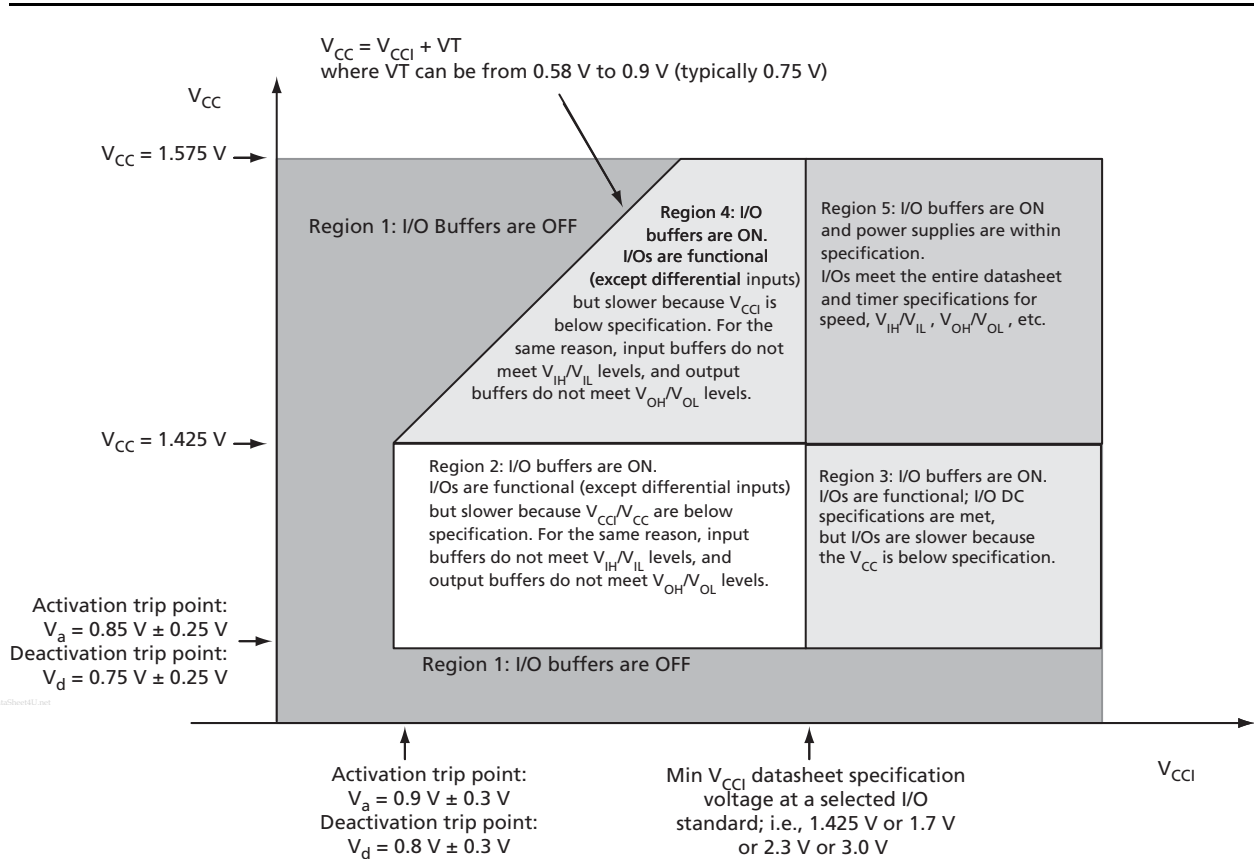
Figure 2-1 • **I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in Actel Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 2-1 can be used to calculate junction temperature.

T_J = Junction Temperature = $\Delta T + T_A$

EQ 2-1

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 2-2 shows a sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{110\text{°C} - 70\text{°C}}{13.6\text{°C/W}} = 5.88 \text{ W}$$

EQ 2-2

Table 2-5 •   **Package Thermal Resistivities**

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	200 ft./min.	500 ft./min.	
Plastic Quad Flat Package (PQFP)	208	8.0	26.1	22.5	20.8	C/W
Plastic Quad Flat Package (PQFP) with embedded heat spreader	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.9	22.8	21.5	C/W
	484	3.2	20.5	17.0	15.9	C/W
	676	3.2	16.4	13.0	12.0	C/W
	896	2.4	13.6	10.4	9.4	C/W

Temperature and Voltage Derating Factors

Table 2-6 •   **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, V_{CC} = 1.425 V)**

Array Voltage V_{CC} (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.87	0.92	0.95	1.00	1.02	1.05
1.500	0.83	0.88	0.90	0.95	0.97	1.00
1.575	0.80	0.85	0.87	0.92	0.94	0.96

Calculating Power Dissipation

Quiescent Supply Current

Table 2-7 •   **Quiescent Supply Current Characteristics**

	A3PE600	A3PE1500	A3PE3000
Typical (25°C)	5 mA	12 mA	25 mA
Maximum (Commercial)	30 mA	70 mA	150 mA
Maximum (Industrial)	45 mA	105 mA	225 mA

Notes:

1. *I_{DD} Includes V_{CG}, V_{PUMP}, V_{CCI}, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-8 and Table 2-9 on page 2-7.*

2. *–F speed grade devices may experience higher standby I_{DD} of up to five times the standard I_{DD} and higher I/O leakage.*

Power per I/O Pin

Table 2-8 •   **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings**

	VMV (V)	Static Power P_{DC2} (mW)[1]	Dynamic Power P_{AC9} (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	17.39
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	25.51
2.5 V LVCMOS	2.5	–	5.76
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.16
1.8 V LVCMOS	1.8	–	2.72
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.80
1.5 V LVCMOS (JESD8-11)	1.5	–	2.08
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	2.00
3.3 V PCI	3.3	–	18.82
3.3 V PCI – Schmitt trigger	3.3	–	20.12
3.3 V PCI-X	3.3	–	18.82
3.3 V PCI-X – Schmitt trigger	3.3	–	20.12
Voltage-Referenced			
3.3 V GTL	3.3	2.90	8.23
2.5 V GTL	2.5	2.13	4.78
3.3 V GTL+	3.3	2.81	4.14
2.5 V GTL+	2.5	2.57	3.71
HSTL (I)	1.5	0.17	2.03
HSTL (II)	1.5	0.17	2.03
SSTL2 (I)	2.5	1.38	4.48
SSTL2 (II)	2.5	1.38	4.48
SSTL3 (I)	3.3	3.21	9.26
SSTL3 (II)	3.3	3.21	9.26

Notes:

1. *P_{DC2} is the static power (where applicable) measured on VMV.*

2. *P_{AC9} is the total dynamic power measured on V_{CC} and VMV.*

Table 2-8 •   **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings (continued)**

	VMV (V)	Static Power P_{DC2} (mW)[1]	Dynamic Power P_{AC9} (µW/MHz)[2]
Differential			
LVDS/B-LVDS/M-LVDS	2.5	2.26	1.50
LVPECL	3.3	5.71	2.17

Notes:

1. *P_{DC2} is the static power (where applicable) measured on VMV.*

2. *P_{AC9} is the total dynamic power measured on V_{CC} and VMV.*

Table 2-9 •   **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1]**

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC3} (mW)[2]	Dynamic Power P_{AC10} (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL/LVCMOS	35	3.3	–	474.70
2.5 V LVCMOS	35	2.5	–	270.73
1.8 V LVCMOS	35	1.8	–	151.78
1.5 V LVCMOS (JESD8-11)	35	1.5	–	104.55
3.3 V PCI	10	3.3	–	204.61
3.3 V PCI-X	10	3.3	–	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	–	24.08
2.5 V GTL	10	2.5	–	13.52
3.3 V GTL+	10	3.3	–	24.10
2.5 V GTL+	10	2.5	–	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
Differential				
LVDS/B-LVDS/M-LVDS	–	2.5	7.70	89.62
LVPECL	–	3.3	19.42	168.02

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*

2. *P_{DC3} is the static power (where applicable) measured on V_{CCI}.*

3. *P_{AC10} is the total dynamic power measured on V_{CC} and V_{CCI}.*

Power Consumption of Various Internal Resources

Table 2-10 • **Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices**

Parameter	Definition	Device-Specific Dynamic Contributions (µW/MHz)		
		A3PE600	A3PE1500	A3PE3000
P_{AC1}	Clock contribution of a Global Rib	12.77	16.21	19.7
P_{AC2}	Clock contribution of a Global Spine	1.85	3.06	4.16
P_{AC3}	Clock contribution of a VersaTile row	0.88		
P_{AC4}	Clock contribution of a VersaTile used as a sequential module	0.12		
P_{AC5}	First contribution of a VersaTile used as a sequential module	0.07		
P_{AC6}	Second contribution of a VersaTile used as a sequential module	0.29		
P_{AC7}	Contribution of a VersaTile used as a combinatorial module	0.29		
P_{AC8}	Average contribution of a routing net	0.70		
P_{AC9}	Contribution of an I/O input pin (standard-dependent)	See Table 2-8 on page 2-6.		
P_{AC10}	Contribution of an I/O output pin (standard-dependent)	See Table 2-9 on page 2-7		
P_{AC11}	Average contribution of a RAM block during a read operation	25.00		
P_{AC12}	Average contribution of a RAM block during a write operation	30.00		
P_{AC13}	Static PLL contribution	2.55 mW		
P_{AC14}	Dynamic contribution for PLL	2.60		

Note: For a different output load, drive strength, or slew rate, Actel recommends using the Actel power calculator or SmartPower in Actel Libero® Integrated Design Environment (IDE).

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-11 on page 2-11.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-12 on page 2-11.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-12 on page 2-11. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

$P_{STAT} = P_{DC1} + N_{INPUTS} * P_{DC2} + N_{OUTPUTS} * P_{DC3}$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S-CELL} * P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in Table 2-11 on page 2-11.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in Table 2-11 on page 2-11.

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

P_{AC1}, P_{AC2}, P_{AC3}, and P_{AC4} are device-dependent.

Sequential Cells Contribution—P_{S-CELL}

$P_{S-CELL} = N_{S-CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-11 on page 2-11.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-11 on page 2-11.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-11 on page 2-11.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-12 on page 2-11.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 2-12 on page 2-11.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-12 on page 2-11.

PLL Contribution—P_{PLL}

$P_{PLL} = P_{AC13} + P_{AC14} * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[1]

---

1. *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% as all flip-flop outputs toggle at half of the clock frequency.

- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1   = 50%
  - Bit 2   = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-11 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-12 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

User I/O Characteristics

Timing Model
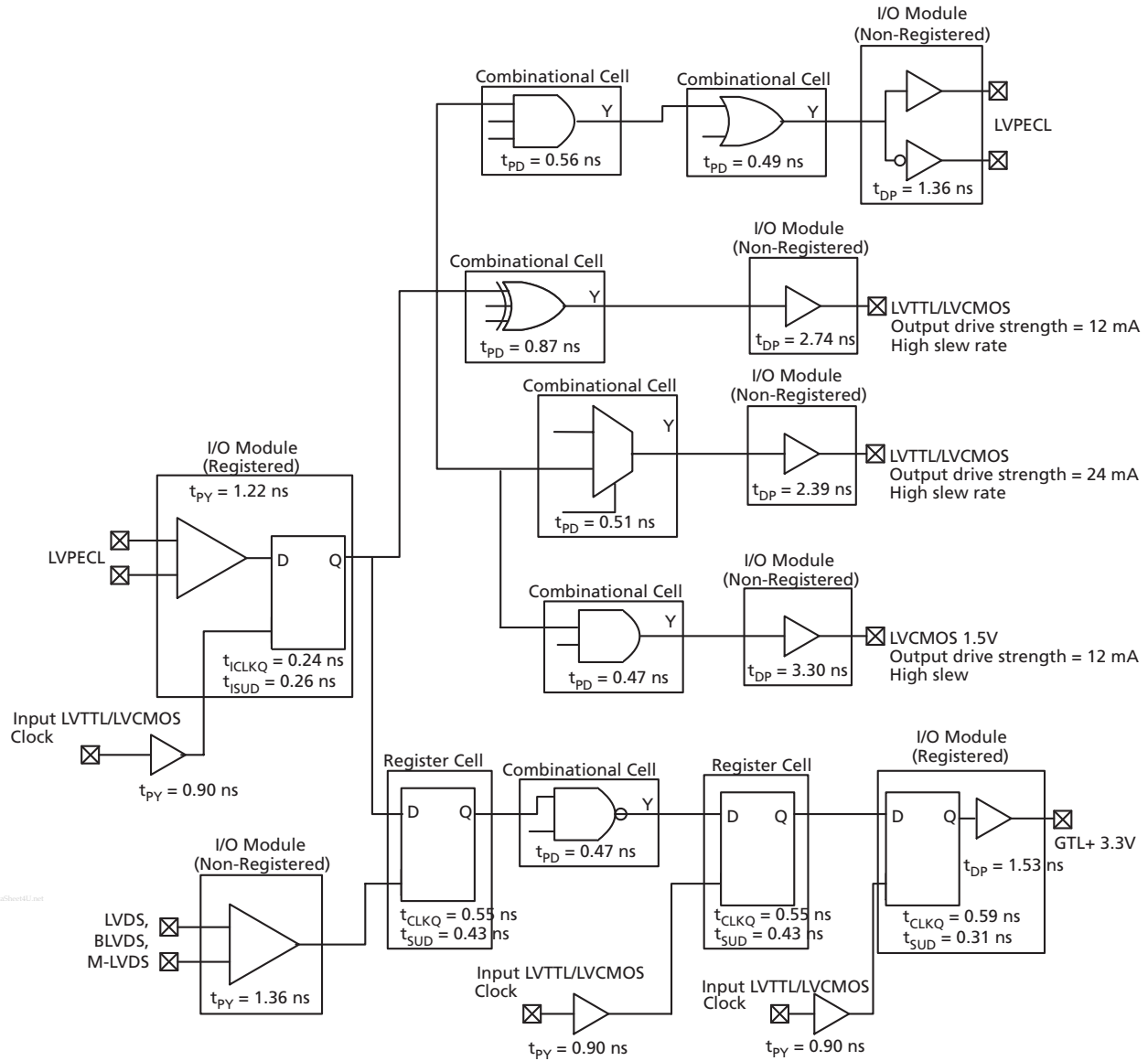
Figure 2-2 • **Timing Model**
Operating Conditions: –2 Speed, Commercial Temperature Range (T$_J$ = 70°C), Worst-Case V$_{CC}$ = 1.425 V

$$t_{PY} = MAX(t_{PY}(R), t_{PY}(F))$$

$$t_{DIN} = MAX(t_{DIN}(R), t_{DIN}(F))$$
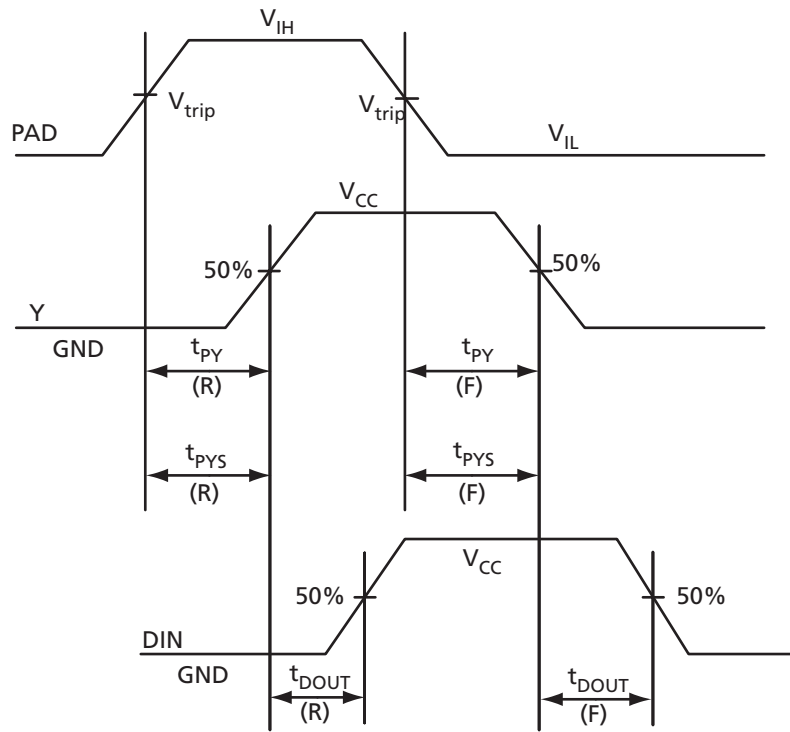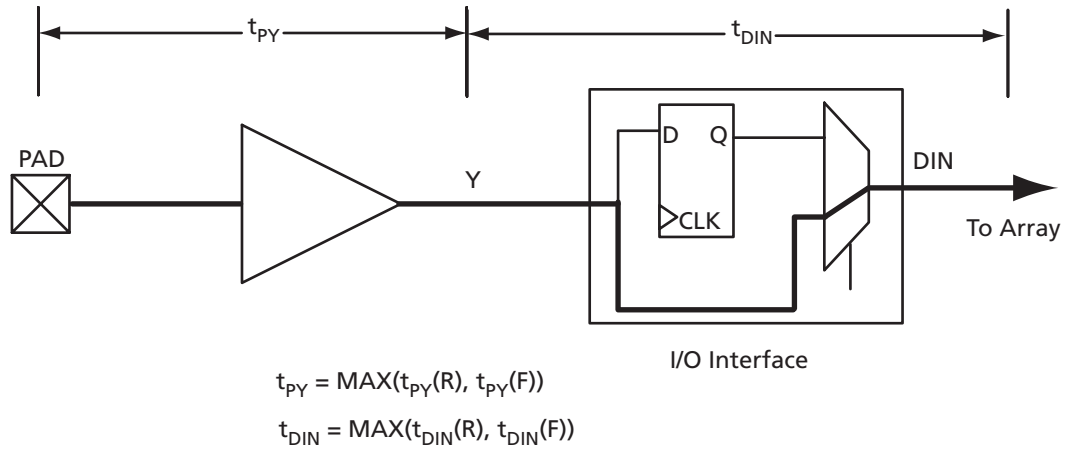
Figure 2-3 • **Input Buffer Timing Model and Delays (example)**

$$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$$
$$t_{DOUT} = MAX(t_{DOUT}(R), t_{DOUT}(F))$$
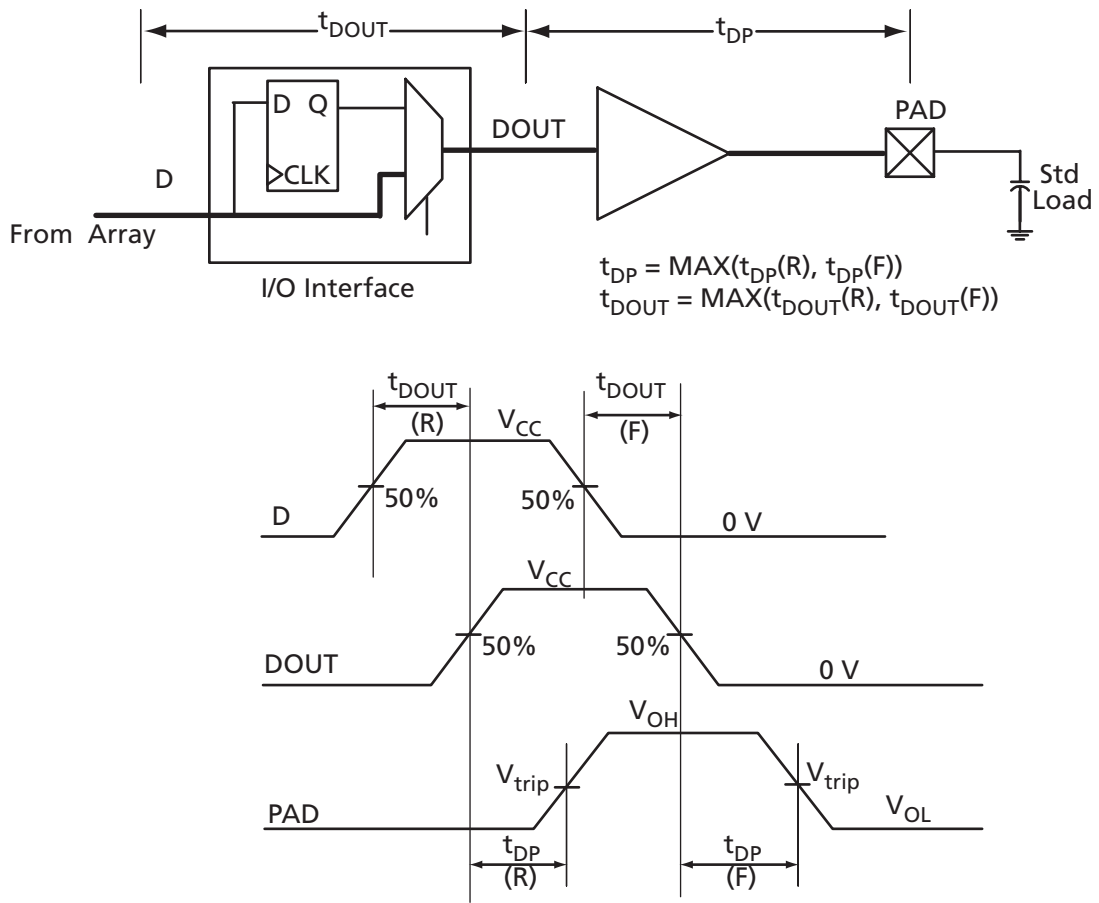
Figure 2-4 • **Output Buffer Model and Delays (example)**

$$t_{EOUT} = MAX(t_{EOUT}(r), t_{EOUT}(f))$$
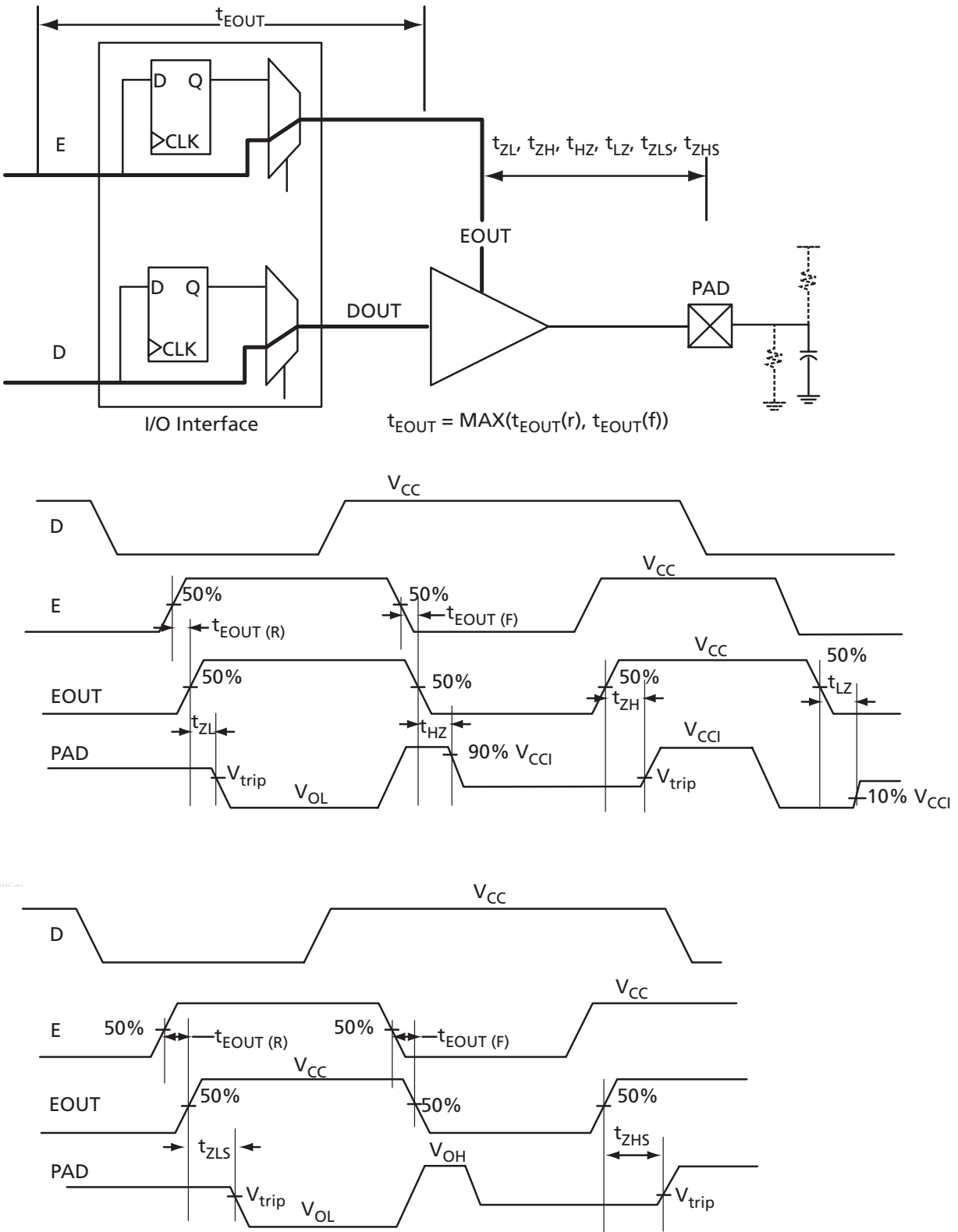
Figure 2-5 • **Tristate Output Buffer Timing Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-13 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions**

I/O Standard	Drive Strength	Slew Rate	V_{IL} Min, V	V_{IL} Max, V	V_{IH} Min, V	V_{IH} Max, V	V_{OL} Max, V	V_{OH} Min, V	I_{OL} mA	I_{OH} mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	12	12
1.5 V LVCMOS	12 mA	High	–0.3	$0.30 * V_{CCI}$	$0.7 * V_{CCI}$	3.6	$0.25 * V_{CCI}$	$0.75 * V_{CCI}$	12	12
3.3 V PCI	Per PCI Specification									
3.3 V PCI-X	Per PCI-X Specification									
3.3 V GTL	25 mA[2]	High	–0.3	$V_{REF} - 0.05$	$V_{REF} + 0.05$	3.6	0.4	–	25	25
2.5 V GTL	25 mA[2]	High	–0.3	$V_{REF} - 0.05$	$V_{REF} + 0.05$	3.6	0.4	–	25	25
3.3 V GTL+	35 mA	High	–0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.6	–	51	51
2.5 V GTL+	33 mA	High	–0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.6	–	40	40
HSTL (I)	8 mA	High	–0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCI} - 0.4$	8	8
HSTL (II)	15 mA[2]	High	–0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCI} - 0.4$	15	15
SSTL2 (I)	15 mA	High	–0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.54	$V_{CCI} - 0.62$	15	15
SSTL2 (II)	18 mA	High	–0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.35	$V_{CCI} - 0.43$	18	18
SSTL3 (I)	14 mA	High	–0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCI} - 1.1$	14	14
SSTL3 (II)	21 mA	High	–0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCI} - 0.9$	21	21

Notes:

1. *Currents are measured at 85°C junction temperature.*

2. *Output drive strength is below JEDEC specification.*

3. *Output Slew Rates can be extracted from IBIS Models, located at http://www.actel.com/download/ibis/default.aspx.*

Table 2-14 • **Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions**

	Commercial[1]		Industrial[2]	
	I_{IL}	I_{IH}	I_{IL}	I_{IH}
DC I/O Standards	µA	µA	µA	µA
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15
3.3 V GTL	10	10	15	15
2.5 V GTL	10	10	15	15
3.3 V GTL+	10	10	15	15
2.5 V GTL+	10	10	15	15
HSTL (I)	10	10	15	15
HSTL (II)	10	10	15	15
SSTL2 (I)	10	10	15	15
SSTL2 (II)	10	10	15	15
SSTL3 (I)	10	10	15	15
SSTL3 (II)	10	10	15	15

Notes:

1. *Commercial range (0°C < T_A < 70°C)*

2. *Industrial range (–40°C < T_A < 85°C)*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-15 • **Summary of AC Measuring Points**

Standard	Input Reference Voltage (V_{REF_TYP})	Board Termination Voltage (V_{TT_REF})	Measuring Trip Point (V_{trip})
3.3 V LVTTL / 3.3 V LVCMOS	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
3.3 V PCI	–	–	$0.285 * V_{CCI}$ (RR) $0.615 * V_{CCI}$ (FF))
3.3 V PCI-X	–	–	$0.285 * V_{CCI}$ (RR) $0.615 * V_{CCI}$ (FF)
3.3 V GTL	0.8 V	1.2 V	V_{REF}
2.5 V GTL	0.8 V	1.2 V	V_{REF}
3.3 V GTL+	1.0 V	1.5 V	V_{REF}
2.5 V GTL+	1.0 V	1.5 V	V_{REF}
HSTL (I)	0.75 V	0.75 V	V_{REF}
HSTL (II)	0.75 V	0.75 V	V_{REF}
SSTL2 (I)	1.25 V	1.25 V	V_{REF}
SSTL2 (II)	1.25 V	1.25 V	V_{REF}
SSTL3 (I)	1.5 V	1.485 V	V_{REF}
SSTL3 (II)	1.5 V	1.485 V	V_{REF}
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

Table 2-16 • **I/O AC Parameter Definitions**

Parameter	Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{PYS}	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t_{HZ}	Enable to Pad delay through the Output Buffer—HIGH to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to HIGH
t_{LZ}	Enable to Pad delay through the Output Buffer—LOW to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to LOW

Table 2-16 • **I/O AC Parameter Definitions**

Parameter	Definition
t$_{ZHS}$	Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH
t$_{ZLS}$	Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW

Table 2-17 • **Summary of I/O Timing Characteristics—Software Default Settings**
–2 Speed Grade, Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case V$_{CC}$ = 1.425 V, Worst-Case V$_{CCI}$ = 3.0 V

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t$_{DOUT}$ (ns)	t$_{DP}$ (ns)	t$_{DIN}$ (ns)	t$_{PY}$ (ns)	t$_{PYS}$ (ns)	t$_{EOUT}$ (ns)	t$_{ZL}$ (ns)	t$_{ZH}$ (ns)	t$_{LZ}$ (ns)	t$_{HZ}$ (ns)	t$_{ZLS}$ (ns)	t$_{ZHS}$ (ns)
3.3 V LVTTL / 3.3 V LVCMOS	12	High	35	–	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81
2.5 V LVCMOS	12	High	35	–	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28
1.8 V LVCMOS	12	High	35	–	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98
1.5 V LVCMOS	12	High	35	–	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37
3.3 V PCI	Per PCI spec	High	10	25 [2]	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V PCI-X	Per PCI-X spec	High	10	25 [2]	0.49	2.09	0.03	0.78	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16
3.3 V GTL	25	High	10	25	0.45	1.55	0.03	2.19	–	0.32	1.52	1.55	–	–	3.19	3.22
2.5 V GTL	25	High	10	25	0.45	1.59	0.03	1.83	–	0.32	1.61	1.59	–	–	3.28	3.26
3.3 V GTL+	35	High	10	25	0.45	1.53	0.03	1.19	–	0.32	1.56	1.53	–	–	3.23	3.20
2.5 V GTL+	33	High	10	25	0.45	1.65	0.03	1.13	–	0.32	1.68	1.57	–	–	3.35	3.24
HSTL (I)	8	High	20	50	0.49	2.37	0.03	1.59	–	0.32	2.42	2.35	–	–	4.09	4.02
HSTL (II)	15	High	20	25	0.49	2.26	0.03	1.59	–	0.32	2.30	2.03	–	–	3.97	3.70
SSTL2 (I)	15	High	30	50	0.49	1.59	0.03	1.00	–	0.32	1.62	1.38	–	–	3.29	3.05
SSTL2 (II)	18	High	30	25	0.49	1.62	0.03	1.00	–	0.32	1.65	1.32	–	–	3.32	2.99
SSTL3 (I)	14	High	30	50	0.49	1.72	0.03	0.93	–	0.32	1.75	1.37	–	–	3.42	3.04
SSTL3 (II)	21	High	30	25	0.49	1.54	0.03	0.93	–	0.32	1.57	1.25	–	–	3.24	2.92
LVDS/B-LVDS/ M-LVDS	24	High	–	–	0.49	1.40	0.03	1.36	–	–	–	–	–	–	–	–
LVPECL	24	High	–	–	0.49	1.36	0.03	1.22	–	–	–	–	–	–	–	–

Notes:

1. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-10 on page 2-35 for connectivity. This resistor is not required during normal operation.

Detailed I/O DC Characteristics

Table 2-18 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	$V_{IN} = 0$, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	$V_{IN} = 0$, f = 1.0 MHz		8	pF

Table 2-19 • **I/O Output Buffer Maximum Resistances[1]**

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω)[2]	$R_{PULL-UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	25 mA	11	–
2.5 V GTL	25 mA	14	–
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–
HSTL (I)	8 mA	50	50

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at* http://www.actel.com/techdocs/models/ibis.html*.*

2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$

3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-19 • **I/O Output Buffer Maximum Resistances[1] (continued)**

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω)[2]	$R_{PULL-UP}$ (Ω)[3]
HSTL (II)	15 mA	25	25
SSTL2 (I)	15 mA	27	31
SSTL2 (II)	18 mA	13	15
SSTL3 (I)	14 mA	44	69
SSTL3 (II)	21 mA	18	32

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at *http://www.actel.com/techdocs/models/ibis.html.*

2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$

3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-20 • **I/O Weak Pull-Up/Pull-Down Resistances**
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

V_{CCI}	$R_{(WEAK\ PULL-UP)}$[1] (Ω)		$R_{(WEAK\ PULL-DOWN)}$[2] (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK\ PULL-DOWN-MAX)} = (V_{OLspec}) / I_{WEAK\ PULL-DOWN-MIN}$

2. $R_{(WEAK\ PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{WEAK\ PULL-UP-MIN}$

Table 2-21 • I/O Short Currents I_{OSH}/I_{OSL}

	Drive Strength	I_{OSH} (mA)*	I_{OSL} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55

* $T_J = 100°C$

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-22 • **Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months

Table 2-23 • **Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

Table 2-24 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability***

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns *	20 years (110°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (110°C)
HSTL/SSTL/GTL	No requirement	10 ns *	10 years (100°C)
LVDS/B-LVDS/M-LVDS/ LVPECL	No requirement	10 ns *	10 years (100°C)

* For clock signals and similar edge-generating signals, refer to ProASIC3/E SSO and Pin Placement Guidelines. *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTL support.

Table 2-25 • **Minimum and Maximum DC Input and Output Levels**

3.3 V LVTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	−0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*

2. *Currents are measured at 85°C junction temperature.*

3. *Software default selection highlighted in gray.*
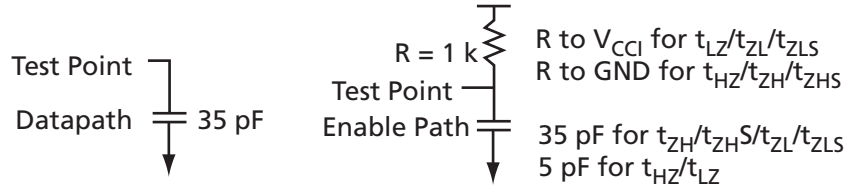
Figure 2-6 • **AC Loading**

Table 2-26 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	35

 * *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-27 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–F	0.79	9.47	0.05	1.44	1.88	0.51	9.64	8.05	3.23	3.11	12.33	10.74	ns
	Std.	0.66	7.88	0.04	1.20	1.57	0.43	8.03	6.70	2.69	2.59	10.26	8.94	ns
	–1	0.56	6.71	0.04	1.02	1.33	0.36	6.83	5.70	2.29	2.20	8.73	7.60	ns
	–2	0.49	5.89	0.03	0.90	1.17	0.32	6.00	5.01	2.01	1.93	7.67	6.67	ns
8 mA	–F	0.79	6.10	0.05	1.44	1.88	0.51	6.21	4.98	3.66	3.86	8.90	7.66	ns
	Std.	0.66	5.08	0.04	1.20	1.57	0.43	5.17	4.14	3.05	3.21	7.41	6.38	ns
	–1	0.56	4.32	0.04	1.02	1.33	0.36	4.40	3.52	2.59	2.73	6.30	5.43	ns
	–2	0.49	3.79	0.03	0.90	1.17	0.32	3.86	3.09	2.28	2.40	5.53	4.76	ns
12 mA	–F	0.79	4.41	0.05	1.44	1.88	0.51	4.49	3.45	3.93	4.34	7.17	6.13	ns
	Std.	0.66	3.67	0.04	1.20	1.57	0.43	3.74	2.87	3.28	3.61	5.97	5.11	ns
	–1	0.56	3.12	0.04	1.02	1.33	0.36	3.18	2.44	2.79	3.07	5.08	4.34	ns
	–2	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
16 mA	–F	0.79	4.16	0.05	1.44	1.88	0.51	4.24	3.13	4.00	4.47	6.92	5.82	ns
	Std.	0.66	3.46	0.04	1.20	1.57	0.43	3.53	2.61	3.33	3.72	5.76	4.84	ns
	–1	0.56	2.95	0.04	1.02	1.33	0.36	3.00	2.22	2.83	3.17	4.90	4.12	ns
	–2	0.49	2.59	0.03	0.90	1.17	0.32	2.63	1.95	2.49	2.78	4.30	3.62	ns
24 mA	–F	0.79	3.85	0.05	1.44	1.88	0.51	3.92	2.59	4.07	4.96	6.61	5.28	ns
	Std.	0.66	3.21	0.04	1.20	1.57	0.43	3.27	2.16	3.39	4.13	5.50	4.39	ns
	–1	0.56	2.73	0.04	1.02	1.33	0.36	2.78	1.83	2.88	3.51	4.68	3.74	ns
	–2	0.49	2.39	0.03	0.90	1.17	0.32	2.44	1.61	2.53	3.08	4.11	3.28	ns

Notes:

1. *Software default selection highlighted in gray.*

2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

Table 2-28 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–F	0.79	13.22	0.05	1.44	1.88	0.51	13.47	10.87	3.23	2.93	16.16	13.56	ns
	Std.	0.66	11.01	0.04	1.20	1.57	0.43	11.21	9.05	2.69	2.44	13.45	11.29	ns
	–1	0.56	9.36	0.04	1.02	1.33	0.36	9.54	7.70	2.29	2.08	11.44	9.60	ns
	–2	0.49	8.22	0.03	0.90	1.17	0.32	8.37	6.76	2.01	1.82	10.04	8.43	ns
8 mA	–F	0.79	9.45	0.05	1.44	1.88	0.51	9.62	7.74	3.65	3.68	12.31	10.42	ns
	Std.	0.66	7.86	0.04	1.20	1.57	0.43	8.01	6.44	3.04	3.06	10.24	8.68	ns
	–1	0.56	6.69	0.04	1.02	1.33	0.36	6.81	5.48	2.58	2.61	8.71	7.38	ns
	–2	0.49	5.87	0.03	0.90	1.17	0.32	5.98	4.81	2.27	2.29	7.65	6.48	ns
12 mA	–F	0.79	7.24	0.05	1.44	1.88	0.51	7.37	6.03	3.93	4.17	10.06	8.72	ns
	Std.	0.66	6.03	0.04	1.20	1.57	0.43	6.14	5.02	3.28	3.47	8.37	7.26	ns
	–1	0.56	5.13	0.04	1.02	1.33	0.36	5.22	4.27	2.79	2.95	7.12	6.17	ns
	–2	0.49	4.50	0.03	0.90	1.17	0.32	4.58	3.75	2.45	2.59	6.25	5.42	ns
16 mA	–F	0.79	6.75	0.05	1.44	1.88	0.51	6.87	5.68	3.99	4.30	9.56	8.36	ns
	Std.	0.66	5.62	0.04	1.20	1.57	0.43	5.72	4.72	3.32	3.58	7.96	6.96	ns
	–1	0.56	4.78	0.04	1.02	1.33	0.36	4.87	4.02	2.83	3.04	6.77	5.92	ns
	–2	0.49	4.20	0.03	0.90	1.17	0.32	4.27	3.53	2.48	2.67	5.94	5.20	ns
24 mA	–F	0.79	6.30	0.05	1.44	1.88	0.51	6.42	5.64	4.07	4.76	9.10	8.32	ns
	Std.	0.66	5.24	0.04	1.20	1.57	0.43	5.34	4.69	3.39	3.96	7.58	6.93	ns
	–1	0.56	4.46	0.04	1.02	1.33	0.36	4.54	3.99	2.88	3.37	6.44	5.89	ns
	–2	0.49	3.92	0.03	0.90	1.17	0.32	3.99	3.50	2.53	2.96	5.66	5.17	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications. It uses a 5 V–tolerant input buffer and push-pull output buffer.

Table 2-29 • **Minimum and Maximum DC Input and Output Levels**

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

2. Currents are measured at 85°C junction temperature.

3. Software default selection highlighted in gray.
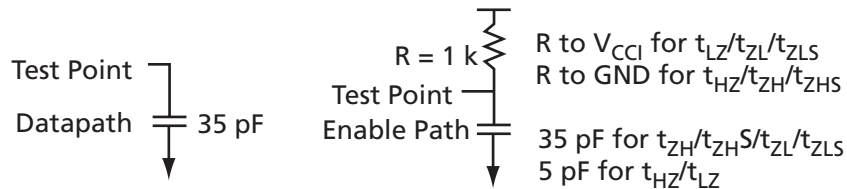
Figure 2-7 • **AC Loading**

Table 2-30 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

* *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-31 • **2.5 V LVCMOS High Slew**
   Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–F	0.79	10.59	0.05	1.82	1.99	0.51	9.77	10.59	3.26	2.75	12.45	13.28	ns
	Std.	0.66	8.82	0.04	1.51	1.66	0.43	8.13	8.82	2.72	2.29	10.37	11.05	ns
	–1	0.56	7.50	0.04	1.29	1.41	0.36	6.92	7.50	2.31	1.95	8.82	9.40	ns
	–2	0.49	6.58	0.03	1.13	1.24	0.32	6.07	6.58	2.03	1.71	7.74	8.25	ns
8 mA	–F	0.79	6.33	0.05	1.82	1.99	0.51	6.33	6.33	3.73	3.64	9.02	9.02	ns
	Std.	0.66	5.27	0.04	1.51	1.66	0.43	5.27	5.27	3.10	3.03	7.50	7.51	ns
	–1	0.56	4.48	0.04	1.29	1.41	0.36	4.48	4.48	2.64	2.58	6.38	6.38	ns
	–2	0.49	3.94	0.03	1.13	1.24	0.32	3.93	3.94	2.32	2.26	5.60	5.61	ns
12 mA	–F	0.79	4.50	0.05	1.82	1.99	0.51	4.58	4.19	4.04	4.20	7.27	6.88	ns
	Std.	0.66	3.74	0.04	1.51	1.66	0.43	3.81	3.49	3.37	3.49	6.05	5.73	ns
	–1	0.56	3.18	0.04	1.29	1.41	0.36	3.24	2.97	2.86	2.97	5.15	4.87	ns
	–2	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28	ns
16 mA	–F	0.79	4.24	0.05	1.82	1.99	0.51	4.32	3.75	4.11	4.35	7.00	6.43	ns
	Std.	0.66	3.53	0.04	1.51	1.66	0.43	3.59	3.12	3.42	3.62	5.83	5.35	ns
	–1	0.56	3.00	0.04	1.29	1.41	0.36	3.06	2.65	2.91	3.08	4.96	4.55	ns
	–2	0.49	2.63	0.03	1.13	1.24	0.32	2.68	2.33	2.56	2.71	4.35	4.00	ns
24 mA	–F	0.79	3.92	0.05	1.82	1.99	0.51	3.99	2.98	4.20	4.93	6.68	5.67	ns
	Std.	0.66	3.26	0.04	1.51	1.66	0.43	3.32	2.48	3.49	4.11	5.56	4.72	ns
	–1	0.56	2.77	0.04	1.29	1.41	0.36	2.83	2.11	2.97	3.49	4.73	4.01	ns
	–2	0.49	2.44	0.03	1.13	1.24	0.32	2.48	1.85	2.61	3.07	4.15	3.52	ns

Notes:

1. *Software default selection highlighted in gray.*

2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

Table 2-32 • **2.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case V$_{CC}$ = 1.425 V, Worst-Case V$_{CCI}$ = 2.3 V

Drive Strength	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{PYS}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	t$_{ZLS}$	t$_{ZHS}$	Units
4 mA	−F	0.79	14.42	0.05	1.82	1.99	0.51	14.69	13.95	3.26	2.64	17.37	16.63	ns
	Std.	0.66	12.00	0.04	1.51	1.66	0.43	12.23	11.61	2.72	2.20	14.46	13.85	ns
	−1	0.56	10.21	0.04	1.29	1.41	0.36	10.40	9.88	2.31	1.87	12.30	11.78	ns
	−2	0.49	8.96	0.03	1.13	1.24	0.32	9.13	8.67	2.03	1.64	10.80	10.34	ns
8 mA	−F	0.79	10.49	0.05	1.82	1.99	0.51	10.68	9.62	3.73	3.52	13.37	12.31	ns
	Std.	0.66	8.73	0.04	1.51	1.66	0.43	8.89	8.01	3.10	2.93	11.13	10.25	ns
	−1	0.56	7.43	0.04	1.29	1.41	0.36	7.57	6.82	2.64	2.49	9.47	8.72	ns
	−2	0.49	6.52	0.03	1.13	1.24	0.32	6.64	5.98	2.32	2.19	8.31	7.65	ns
12 mA	−F	0.79	8.14	0.05	1.82	1.99	0.51	8.29	7.34	4.04	4.08	10.97	10.02	ns
	Std.	0.66	6.77	0.04	1.51	1.66	0.43	6.90	6.11	3.37	3.39	9.14	8.34	ns
	−1	0.56	5.76	0.04	1.29	1.41	0.36	5.87	5.20	2.86	2.89	7.77	7.10	ns
	−2	0.49	5.06	0.03	1.13	1.24	0.32	5.15	4.56	2.51	2.53	6.82	6.23	ns
16 mA	−F	0.79	7.58	0.05	1.82	1.99	0.51	7.72	6.88	4.11	4.23	10.40	9.57	ns
	Std.	0.66	6.31	0.04	1.51	1.66	0.43	6.42	5.73	3.42	3.52	8.66	7.96	ns
	−1	0.56	5.37	0.04	1.29	1.41	0.36	5.46	4.87	2.91	3.00	7.37	6.77	ns
	−2	0.49	4.71	0.03	1.13	1.24	0.32	4.80	4.28	2.56	2.63	6.47	5.95	ns
24 mA	−F	0.79	7.13	0.05	1.82	1.99	0.51	7.26	6.85	4.20	4.80	9.94	9.54	ns
	Std.	0.66	5.93	0.04	1.51	1.66	0.43	6.04	5.70	3.49	4.00	8.28	7.94	ns
	−1	0.56	5.05	0.04	1.29	1.41	0.36	5.14	4.85	2.97	3.40	7.04	6.75	ns
	−2	0.49	4.43	0.03	1.13	1.24	0.32	4.51	4.26	2.61	2.99	6.18	5.93	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-33 • **Minimum and Maximum DC Input and Output Levels**

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	μA^2	μA^2
2 mA	−0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} − 0.45	2	2	11	9	10	10
4 mA	−0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} − 0.45	4	4	22	17	10	10
6 mA	−0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} − 0.45	6	6	44	35	10	10
8 mA	−0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} − 0.45	8	8	51	45	10	10
12 mA	−0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} − 0.45	12	12	74	91	10	10
16 mA	−0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} − 0.45	16	16	74	91	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*

2. *Currents are measured at 85°C junction temperature.*

3. *Software default selection highlighted in gray.*

Test Point
Datapath — 35 pF

R = 1 k
Test Point
Enable Path

R to V_{CCI} for $t_{LZ}/t_{ZL}/t_{ZLS}$
R to GND for $t_{HZ}/t_{ZH}/t_{ZHS}$

35 pF for $t_{ZH}/t_{ZH}S/t_{ZL}/t_{ZLS}$
5 pF for t_{HZ}/t_{LZ}

Figure 2-8 • **AC Loading**

Table 2-34 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	35

* *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-35 • **1.8 V LVCMOS High Slew**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case V$_{CC}$ = 1.425 V, Worst-Case V$_{CCI}$ = 1.7 V

Drive Strength	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{PYS}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	t$_{ZLS}$	t$_{ZHS}$	Units
2 mA	–F	0.79	14.54	0.05	1.74	2.29	0.51	11.52	14.54	3.34	1.97	14.21	17.23	ns
	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	–1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	–2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4 mA	–F	0.79	8.47	0.05	1.74	2.29	0.51	7.45	8.47	3.90	3.44	10.14	11.16	ns
	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	–1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	–2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
6 mA	–F	0.79	5.43	0.05	1.74	2.29	0.51	5.36	5.43	4.29	4.17	8.05	8.12	ns
	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	–1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	–2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
8 mA	–F	0.79	4.95	0.05	1.74	2.29	0.51	5.04	4.80	4.36	4.35	7.73	7.48	ns
	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	–1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	–2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
12 mA	–F	0.79	4.56	0.05	1.74	2.29	0.51	4.64	3.71	4.48	5.09	7.33	6.40	ns
	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns
16 mA	–F	0.79	4.56	0.05	1.74	2.29	0.51	4.64	3.71	4.48	5.09	7.33	6.40	ns
	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to *Table 2-6 on page 2-5* for derating values.
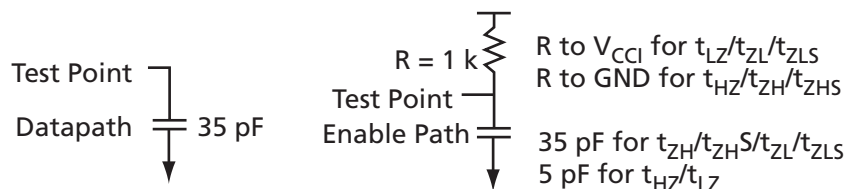
Table 2-36 • **1.8 V LVCMOS Low Slew**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case V$_{CC}$ = 1.425 V, Worst-Case V$_{CCI}$ = 1.7 V

Drive Strength	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{PYS}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	t$_{ZLS}$	t$_{ZHS}$	Units
2 mA	–F	0.79	19.03	0.05	1.74	2.29	0.51	18.80	19.03	3.34	1.90	21.49	21.71	ns
	Std.	0.66	15.84	0.04	1.45	1.91	0.43	15.65	15.84	2.78	1.58	17.89	18.07	ns
	–1	0.56	13.47	0.04	1.23	1.62	0.36	13.31	13.47	2.37	1.35	15.22	15.37	ns
	–2	0.49	11.83	0.03	1.08	1.42	0.32	11.69	11.83	2.08	1.18	13.36	13.50	ns
4 mA	–F	0.79	13.68	0.05	1.74	2.29	0.51	13.94	12.92	3.91	3.33	16.62	15.61	ns
	Std.	0.66	11.39	0.04	1.45	1.91	0.43	11.60	10.76	3.26	2.77	13.84	12.99	ns
	–1	0.56	9.69	0.04	1.23	1.62	0.36	9.87	9.15	2.77	2.36	11.77	11.05	ns
	–2	0.49	8.51	0.03	1.08	1.42	0.32	8.66	8.03	2.43	2.07	10.33	9.70	ns
6 mA	–F	0.79	10.78	0.05	1.74	2.29	0.51	10.98	9.73	4.29	4.03	13.66	12.41	ns
	Std.	0.66	8.97	0.04	1.45	1.91	0.43	9.14	8.10	3.57	3.36	11.37	10.33	ns
	–1	0.56	7.63	0.04	1.23	1.62	0.36	7.77	6.89	3.04	2.86	9.67	8.79	ns
	–2	0.49	6.70	0.03	1.08	1.42	0.32	6.82	6.05	2.66	2.51	8.49	7.72	ns
8 mA	–F	0.79	10.03	0.05	1.74	2.29	0.51	10.22	9.11	4.37	4.23	12.90	11.80	ns
	Std.	0.66	8.35	0.04	1.45	1.91	0.43	8.50	7.59	3.64	3.52	10.74	9.82	ns
	–1	0.56	7.10	0.04	1.23	1.62	0.36	7.23	6.45	3.10	3.00	9.14	8.35	ns
	–2	0.49	6.24	0.03	1.08	1.42	0.32	6.35	5.66	2.72	2.63	8.02	7.33	ns
12 mA	–F	0.79	9.54	0.05	1.74	2.29	0.51	9.72	9.08	4.50	4.93	12.40	11.77	ns
	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns
16 mA	–F	0.79	9.54	0.05	1.74	2.29	0.51	9.72	9.08	4.50	4.93	12.40	11.77	ns
	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-37 • **Minimum and Maximum DC Input and Output Levels**

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	μA^2	μA^2
2 mA	−0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	16	13	10	10
4 mA	−0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4	33	25	10	10
6 mA	−0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	6	6	39	32	10	10
8 mA	−0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	8	8	55	66	10	10
12 mA	−0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12	55	66	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*

2. *Currents are measured at 85°C junction temperature.*

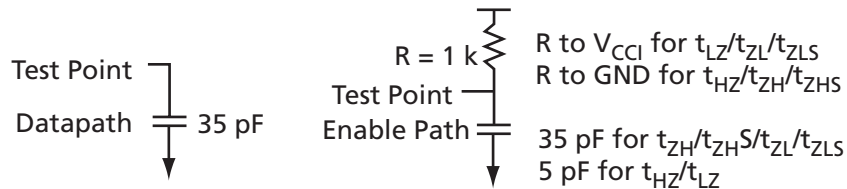3. *Software default selection highlighted in gray.*

Figure 2-9 • **AC Loading**

Table 2-38 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	1.5	0.75	–	35

* *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-39 • **1.5 V LVCMOS High Slew**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case V$_{CC}$ = 1.425 V, Worst-Case V$_{CCI}$ = 1.4 V

Drive Strength	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{PYS}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	t$_{ZLS}$	t$_{ZHS}$	Units
2 mA	−F	0.79	10.25	0.05	2.04	2.58	0.51	8.72	10.25	4.08	3.35	11.41	12.94	ns
	Std.	0.66	8.53	0.04	1.70	2.14	0.43	7.26	8.53	3.39	2.79	9.50	10.77	ns
	−1	0.56	7.26	0.04	1.44	1.82	0.36	6.18	7.26	2.89	2.37	8.08	9.16	ns
	−2	0.49	6.37	0.03	1.27	1.60	0.32	5.42	6.37	2.53	2.08	7.09	8.04	ns
4 mA	−F	0.79	6.50	0.05	2.04	2.58	0.51	6.27	6.50	4.51	4.18	8.95	9.19	ns
	Std.	0.66	5.41	0.04	1.70	2.14	0.43	5.22	5.41	3.75	3.48	7.45	7.65	ns
	−1	0.56	4.60	0.04	1.44	1.82	0.36	4.44	4.60	3.19	2.96	6.34	6.50	ns
	−2	0.49	4.04	0.03	1.27	1.60	0.32	3.89	4.04	2.80	2.60	5.56	5.71	ns
6 mA	−F	0.79	5.77	0.05	2.04	2.58	0.51	5.88	5.70	4.60	4.41	8.56	8.39	ns
	Std.	0.66	4.80	0.04	1.70	2.14	0.43	4.89	4.75	3.83	3.67	7.13	6.98	ns
	−1	0.56	4.09	0.04	1.44	1.82	0.36	4.16	4.04	3.26	3.12	6.06	5.94	ns
	−2	0.49	3.59	0.03	1.27	1.60	0.32	3.65	3.54	2.86	2.74	5.32	5.21	ns
8 mA	−F	0.79	5.31	0.05	2.04	2.58	0.51	5.41	4.35	4.76	5.25	8.09	7.04	ns
	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	−1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	−2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns
12 mA	−F	0.79	5.31	0.05	2.04	2.58	0.51	5.41	4.35	4.76	5.25	8.09	7.04	ns
	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	−1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	−2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns

Notes:

1. *Software default selection highlighted in gray.*

2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

Table 2-40 • **1.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case V$_{CC}$ = 1.425 V, Worst-Case V$_{CCI}$ = 1.4 V

Drive Strength	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{PYS}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	t$_{ZLS}$	t$_{ZHS}$	Units
2 mA	–F	0.79	16.95	0.05	2.04	2.58	0.51	17.26	15.78	4.09	3.22	19.95	18.47	ns
	Std.	0.66	14.11	0.04	1.70	2.14	0.43	14.37	13.14	3.40	2.68	16.61	15.37	ns
	–1	0.56	12.00	0.04	1.44	1.82	0.36	12.22	11.17	2.90	2.28	14.13	13.08	ns
	–2	0.49	10.54	0.03	1.27	1.60	0.32	10.73	9.81	2.54	2.00	12.40	11.48	ns
4 mA	–F	0.79	13.49	0.05	2.04	2.58	0.51	13.74	11.85	4.53	4.03	16.43	14.54	ns
	Std.	0.66	11.23	0.04	1.70	2.14	0.43	11.44	9.87	3.77	3.36	13.68	12.10	ns
	–1	0.56	9.55	0.04	1.44	1.82	0.36	9.73	8.39	3.21	2.86	11.63	10.29	ns
	–2	0.49	8.39	0.03	1.27	1.60	0.32	8.54	7.37	2.81	2.51	10.21	9.04	ns
6 mA	–F	0.79	12.56	0.05	2.04	2.58	0.51	12.79	11.10	4.62	4.26	15.48	13.79	ns
	Std.	0.66	10.45	0.04	1.70	2.14	0.43	10.65	9.24	3.84	3.55	12.88	11.48	ns
	–1	0.56	8.89	0.04	1.44	1.82	0.36	9.06	7.86	3.27	3.02	10.96	9.76	ns
	–2	0.49	7.81	0.03	1.27	1.60	0.32	7.95	6.90	2.87	2.65	9.62	8.57	ns
8 mA	–F	0.79	12.04	0.05	2.04	2.58	0.51	12.26	11.09	4.77	5.07	14.94	13.77	ns
	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	–1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	–2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns
12 mA	–F	0.79	12.04	0.05	2.04	2.58	0.51	12.26	11.09	4.77	5.07	14.94	13.77	ns
	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	–1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	–2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-41 • **Minimum and Maximum DC Input and Output Levels**

3.3 V PCI/PCI-X	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
Per PCI specification	Per PCI curves										10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*

2. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Actel loadings for enable path characterization are described in Figure 2-10.
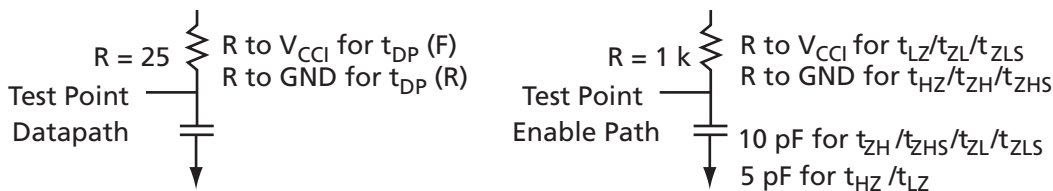
Figure 2-10 • **AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; Actel loading for tristate is described in Table 2-42.

Table 2-42 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	0.285 * V_{CCI} for $t_{DP(R)}$ 0.615 * V_{CCI} for $t_{DP(F)}$	–	10

 * *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-43 • **3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	3.37	0.05	1.26	2.01	0.51	3.43	2.40	3.93	4.34	6.12	5.08	ns
Std.	0.66	2.81	0.04	1.05	1.67	0.43	2.86	2.00	3.28	3.61	5.09	4.23	ns
–1	0.56	2.39	0.04	0.89	1.42	0.36	2.43	1.70	2.79	3.07	4.33	3.60	ns
–2	0.49	2.09	0.03	0.78	1.25	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Voltage-Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 3.3 V.

Table 2-44 • **Minimum and Maximum DC Input and Output Levels**

3.3 V GTL	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
25 mA[3]	−0.3	$V_{REF} - 0.05$	$V_{REF} + 0.05$	3.6	0.4	–	25	25	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*

2. *Currents are measured at 85°C junction temperature.*

3. *Output drive strength is below JEDEC specification.*

Figure 2-11 • **AC Loading**

Table 2-45 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
$V_{REF} - 0.05$	$V_{REF} + 0.05$	0.8	0.8	1.2	10

* *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-46 • **3.3 V GTL**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 3.0 V V_{REF} = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.72	2.49	0.05	3.52	0.51	2.45	2.49			5.13	5.18	ns
Std.	0.60	2.08	0.04	2.93	0.43	2.04	2.08			4.27	4.31	ns
–1	0.51	1.77	0.04	2.50	0.36	1.73	1.77			3.63	3.67	ns
–2	0.45	1.55	0.03	2.19	0.32	1.52	1.55			3.19	3.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

Table 2-47 • **Minimum and Maximum DC Input and Output Levels**

2.5 GTL	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	μA^2	μA^2
25 mA[3]	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*

2. *Currents are measured at 85°C junction temperature.*

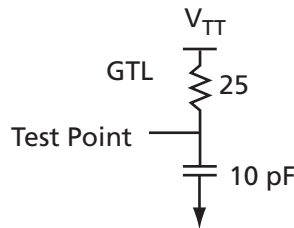3. *Output drive strength is below JEDEC specification.*
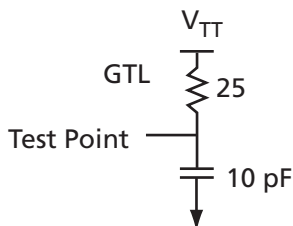
Figure 2-12 • **AC Loading**

Table 2-48 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.05	V_{REF} + 0.05	0.8	0.8	1.2	10

 * *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-49 • **2.5 V GTL**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V V_{REF} = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.72	2.56	0.05	2.95	0.51	2.60	2.56			5.28	5.24	ns
Std.	0.60	2.13	0.04	2.46	0.43	2.16	2.13			4.40	4.36	ns
–1	0.51	1.81	0.04	2.09	0.36	1.84	1.81			3.74	3.71	ns
–2	0.45	1.59	0.03	1.83	0.32	1.61	1.59			3.28	3.26	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 3.3 V.

Table 2-50 • **Minimum and Maximum DC Input and Output Levels**

3.3 V GTL+	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
35 mA	−0.3	V_{REF} − 0.1	V_{REF} + 0.1	3.6	0.6	–	35	35	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*

2. *Currents are measured at 85°C junction temperature.*

Figure 2-13 • **AC Loading**

Table 2-51 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} − 0.1	V_{REF} + 0.1	1.0	1.0	1.5	10

* *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-52 • **3.3 V GTL+**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 3.0 V, V_{REF} = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
−F	0.72	2.47	0.05	1.91	0.51	2.51	2.47			5.20	5.15	ns
Std.	0.60	2.06	0.04	1.59	0.43	2.09	2.06			4.33	4.29	ns
−1	0.51	1.75	0.04	1.35	0.36	1.78	1.75			3.68	3.65	ns
−2	0.45	1.53	0.03	1.19	0.32	1.56	1.53			3.23	3.20	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

Table 2-53 • **Minimum and Maximum DC Input and Output Levels**

2.5 V GTL+	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
33 mA	−0.3	V_{REF} − 0.1	V_{REF} + 0.1	3.6	0.6	–	33	33	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
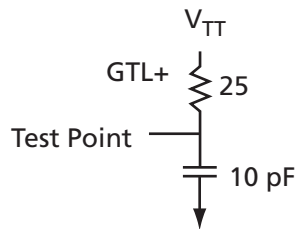
2. *Currents are measured at 85°C junction temperature.*
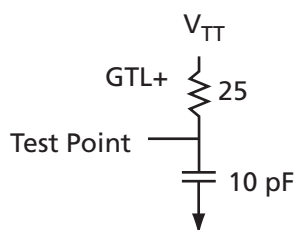
Figure 2-14 • **AC Loading**

Table 2-54 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} − 0.1	V_{REF} + 0.1	1.0	1.0	1.5	10

 * *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-55 • **2.5 V GTL+**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 2.3 V, V_{REF} = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
−F	0.72	2.65	0.05	1.82	0.51	2.70	2.52			5.38	5.21	ns
Std.	0.60	2.21	0.04	1.51	0.43	2.25	2.10			4.48	4.34	ns
−1	0.51	1.88	0.04	1.29	0.36	1.91	1.79			3.81	3.69	ns
−2	0.45	1.65	0.03	1.13	0.32	1.68	1.57			3.35	3.24	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-56 • **Minimum and Maximum DC Input and Output Levels**

HSTL Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
8 mA	–0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCI} - 0.4$	8	8	39	32	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*

2. *Currents are measured at 85°C junction temperature.*
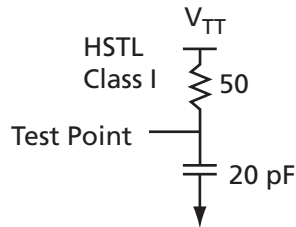
Figure 2-15 • **AC Loading**

Table 2-57 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
$V_{REF} - 0.1$	$V_{REF} + 0.1$	0.75	0.75	0.75	20

* Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-58 • **HSTL Class I**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = .4 V, V_{REF} = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	3.82	0.05	2.55	0.51	3.89	3.78			6.58	6.46	ns
Std.	0.66	3.18	0.04	2.12	0.43	3.24	3.14			5.47	5.38	ns
–1	0.56	2.70	0.04	1.81	0.36	2.75	2.67			4.66	4.58	ns
–2	0.49	2.37	0.03	1.59	0.32	2.42	2.35			4.09	4.02	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-59 • **Minimum and Maximum DC Input and Output Levels**

HSTL Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
15 mA[3]	–0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	V_{CCI}-0.4	15	15	55	66	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*

2. *Currents are measured at 85°C junction temperature.*

3. *Output drive strength is below JEDEC specification.*
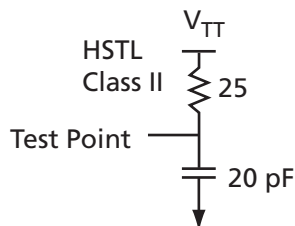
Figure 2-16 • **AC Loading**

Table 2-60 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
$V_{REF} - 0.1$	$V_{REF} + 0.1$	0.75	0.75	0.75	20

* Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-61 • **HSTL Class II**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 1.4 V, V_{REF} = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	3.63	0.05	2.55	0.51	3.70	3.26			6.39	5.95	ns
Std.	0.66	3.02	0.04	2.12	0.43	3.08	2.71			5.32	4.95	ns
–1	0.56	2.57	0.04	1.81	0.36	2.62	2.31			4.52	4.21	ns
–2	0.49	2.26	0.03	1.59	0.32	2.30	2.03			3.97	3.70	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-62 • **Minimum and Maximum DC Input and Output Levels**

SSTL2 Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA**[1]	**Max., mA**[1]	**µA**[2]	**µA**[2]
15 mA	–0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.54	$V_{CCI} - 0.62$	15	15	87	83	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*

2. *Currents are measured at 85°C junction temperature.*
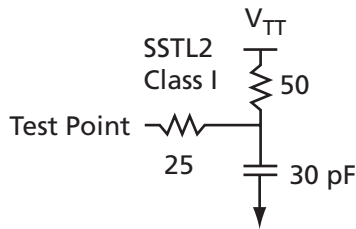
Figure 2-17 • **AC Loading**

Table 2-63 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
$V_{REF} - 0.2$	$V_{REF} + 0.2$	1.25	1.25	1.25	30

* *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-64 • **SSTL 2 Class I**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 2.3 V, V_{REF} = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	2.56	0.05	1.60	0.51	2.60	2.22			5.29	4.90	ns
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
–1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
–2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-65 • **Minimum and Maximum DC Input and Output Levels**

SSTL2 Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
18 mA	−0.3	$V_{REF} − 0.2$	$V_{REF} + 0.2$	3.6	0.35	$V_{CCI} − 0.43$	18	18	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*

2. *Currents are measured at 85°C junction temperature.*
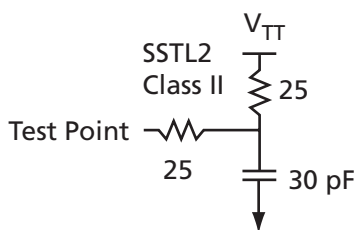
Figure 2-18 • **AC Loading**

Table 2-66 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
$V_{REF} − 0.2$	$V_{REF} + 0.2$	1.25	1.25	1.25	30

* *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-67 • **SSTL 2 Class II**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 2.3 V, V_{REF} = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
−F	0.79	0.79	2.60	0.05	1.60	0.51	2.65	2.13			5.34	ns
Std.	0.66	0.66	2.17	0.04	1.33	0.43	2.21	1.77			4.44	ns
−1	0.56	0.56	1.84	0.04	1.14	0.36	1.88	1.51			3.78	ns
−2	0.49	0.49	1.62	0.03	1.00	0.32	1.65	1.32			3.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-68 • **Minimum and Maximum DC Input and Output Levels**

SSTL3 Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
14 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCI} – 1.1	14	14	54	51	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*

2. *Currents are measured at 85°C junction temperature.*
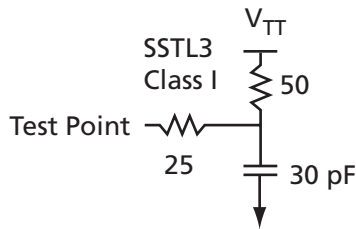
Figure 2-19 • **AC Loading**

Table 2-69 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.5	1.5	1.485	30

* *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-70 • **SSTL3 Class I**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 3.0 V, V_{REF} = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	2.77	0.05	1.50	0.51	2.82	2.21			5.51	4.89	ns
Std.	0.66	2.31	0.04	1.25	0.43	2.35	1.84			4.59	4.07	ns
–1	0.56	1.96	0.04	1.06	0.36	2.00	1.56			3.90	3.46	ns
–2	0.49	1.72	0.03	0.93	0.32	1.75	1.37			3.42	3.04	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-71 • **Minimum and Maximum DC Input and Output Levels**

SSTL3 Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
21 mA	−0.3	V_{REF} − 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCI} − 0.9	21	21	109	103	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*

2. *Currents are measured at 85°C junction temperature.*
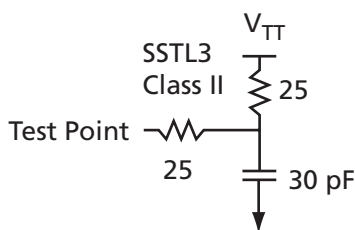
Figure 2-20 • **AC Loading**

Table 2-72 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} − 0.2	V_{REF} + 0.2	1.5	1.5	1.485	30

* *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-73 • **SSTL3 Class II**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 3.0 V, V_{REF} = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
−F	0.79	2.48	0.05	1.50	0.51	2.53	2.01			5.21	4.69	ns
Std.	0.66	2.07	0.04	1.25	0.43	2.10	1.67			4.34	3.91	ns
−1	0.56	1.76	0.04	1.06	0.36	1.79	1.42			3.69	3.32	ns
−2	0.49	1.54	0.03	0.93	0.32	1.57	1.25			3.24	2.92	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by the Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and DDR. However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-21. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3E also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

Figure 2-21 • **LVDS Circuit Diagram and Board-Level Implementation**

Table 2-74 • **LVDS Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
V_{CCI}	Supply Voltage [1]	2.375	2.5	2.625	V
V_{OL}	Output Low Voltage	0.9	1.075	1.25	V
V_{OH}	Output High Voltage	1.25	1.425	1.6	V
I_{OL} [4]	Output Lower Current	0.65	0.91	1.16	mA
I_{OH} [4]	Output High Current	0.65	0.91	1.16	mA
V_I	Input Voltage	0		2.925	V
I_{IH} [3]	Input High Leakage Current			10	µA
I_{IL} [3]	Input Low Leakage Current			10	µA
V_{ODIFF}	Differential Output Voltage	250	350	450	mV
V_{OCM}	Output Common Mode Voltage	1.125	1.25	1.375	V
V_{ICM}	Input Common Mode Voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input Differential Voltage [2]	100	350		mV

Notes:

1. ±5%

2. *Differential input voltage = ±350 mV.*

3. *Currents are measured at 85°C junction temperature.*

4. I_{OL}/I_{OH} *defined by* $V_{ODIFF}/(Resistor\ Network)$.

Table 2-75 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.075	1.325	Cross point	–

* Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.

Timing Characteristics

Table 2-76 • **LVDS**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case V$_{CC}$ = 1.425 V, Worst-Case V$_{CCI}$ = 2.3 V

Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	Units
–F	0.79	2.25	0.05	2.18	ns
Std.	0.66	1.87	0.04	1.82	ns
–1	0.56	1.59	0.04	1.55	ns
–2	0.49	1.40	0.03	1.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Actel LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-22. The input and output buffer delays are available in the LVDS section in Table 2-76.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: R$_S$ = 60 Ω and R$_T$ = 70 Ω, given Z$_0$ = 50 Ω (2") and Z$_{stub}$ = 50 Ω (~1.5").
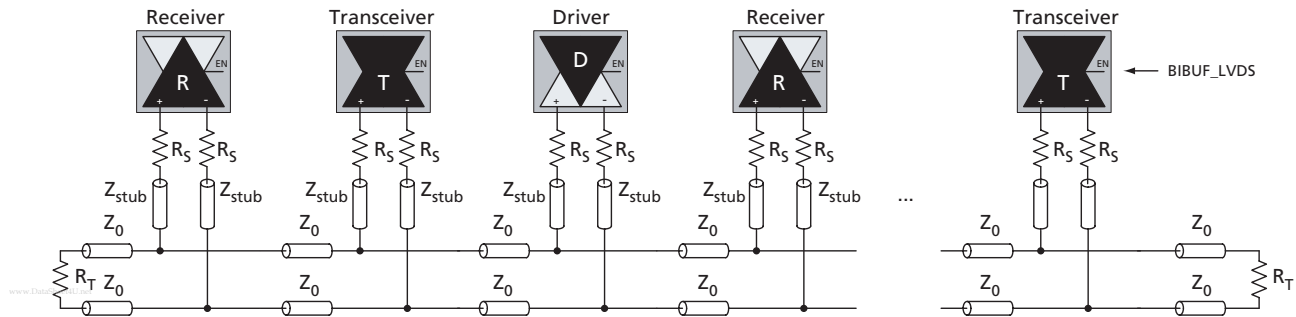
Figure 2-22 • **B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-23. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.
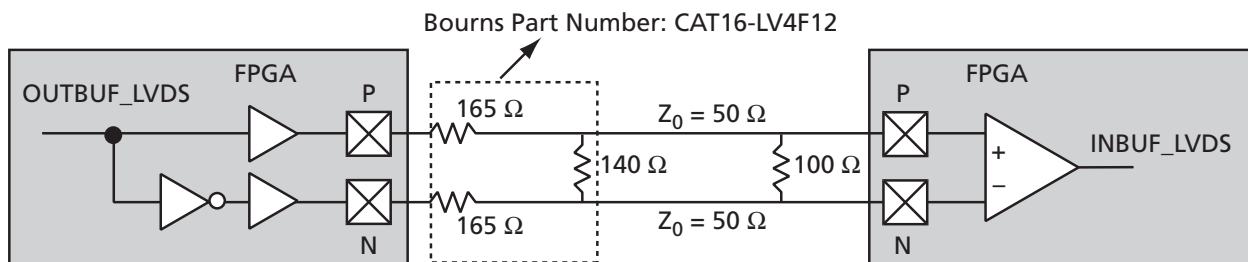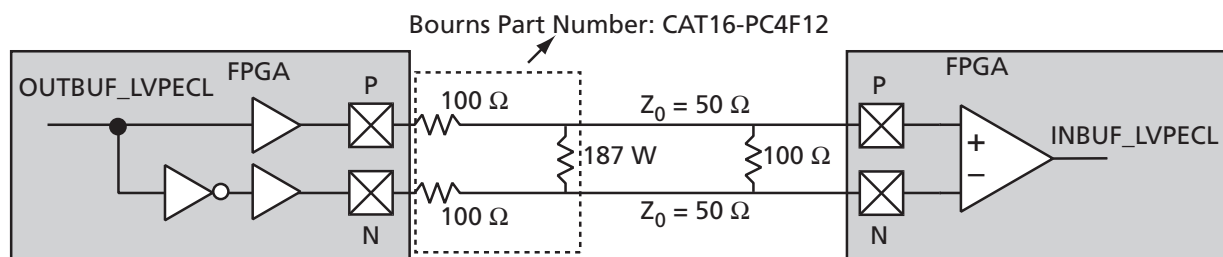

Figure 2-23 • **LVPECL Circuit Diagram and Board-Level Implementation**

Table 2-77 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{CCI}	Supply Voltage	3.0		3.3		3.6		V
V_{OL}	Output LOW Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{OH}	Output HIGH Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{IL}, V_{IH}	Input LOW, Input HIGH Voltages	0	3.3	0	3.6	0	3.9	V
V_{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V_{OCM}	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V_{ICM}	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V_{IDIFF}	Input Differential Voltage	300		300		300		mV

Table 2-78 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.64	1.94	Cross point	–

 * *Measuring point = V_{trip}. See Table 2-15 on page 2-18 for a complete table of trip points.*

Timing Characteristics

Table 2-79 • **LVPECL**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
–F	0.79	2.19	0.05	1.96	ns
Std.	0.66	1.83	0.04	1.63	ns
–1	0.56	1.55	0.04	1.39	ns
–2	0.49	1.36	0.03	1.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset
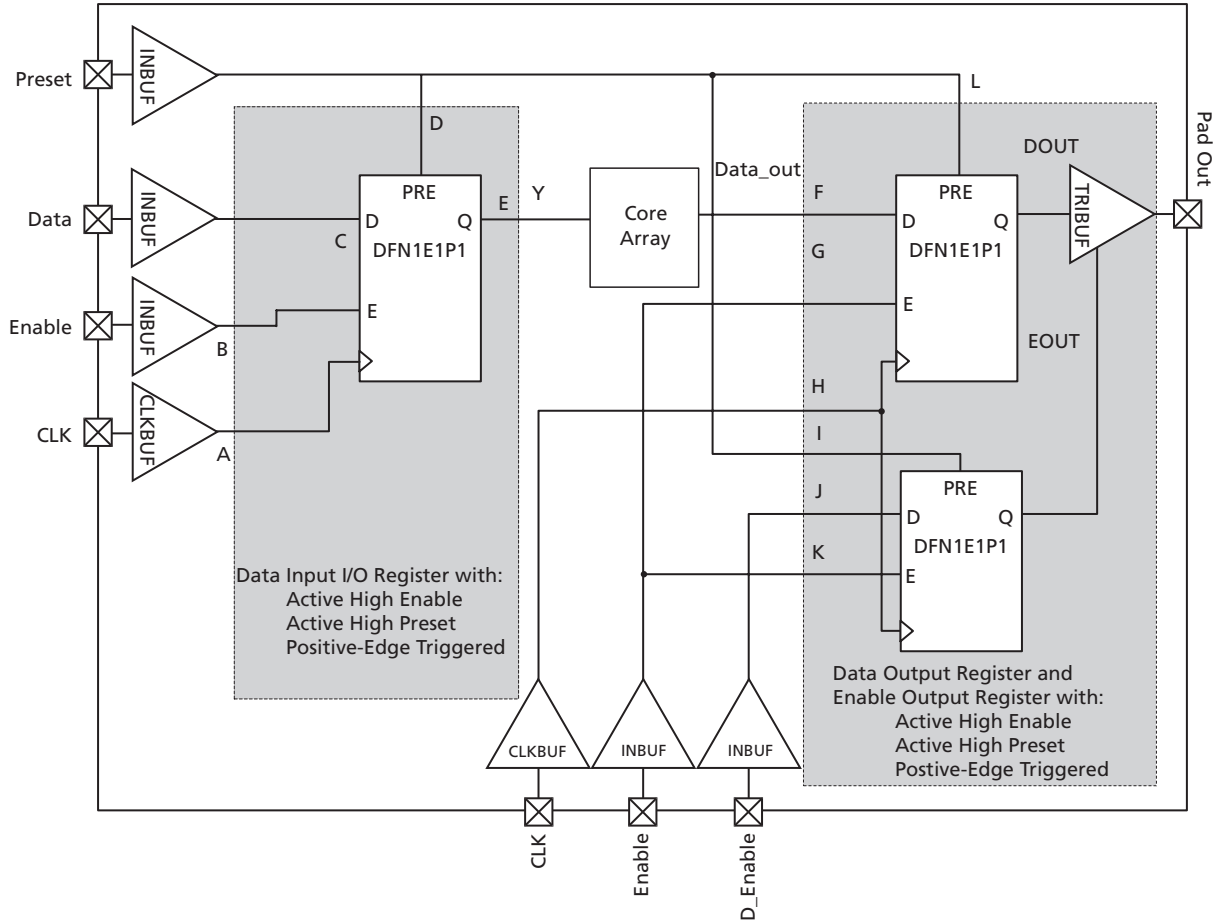
Figure 2-24 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Table 2-80 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

* See *Figure 2-24 on page 2-50* for more information.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear
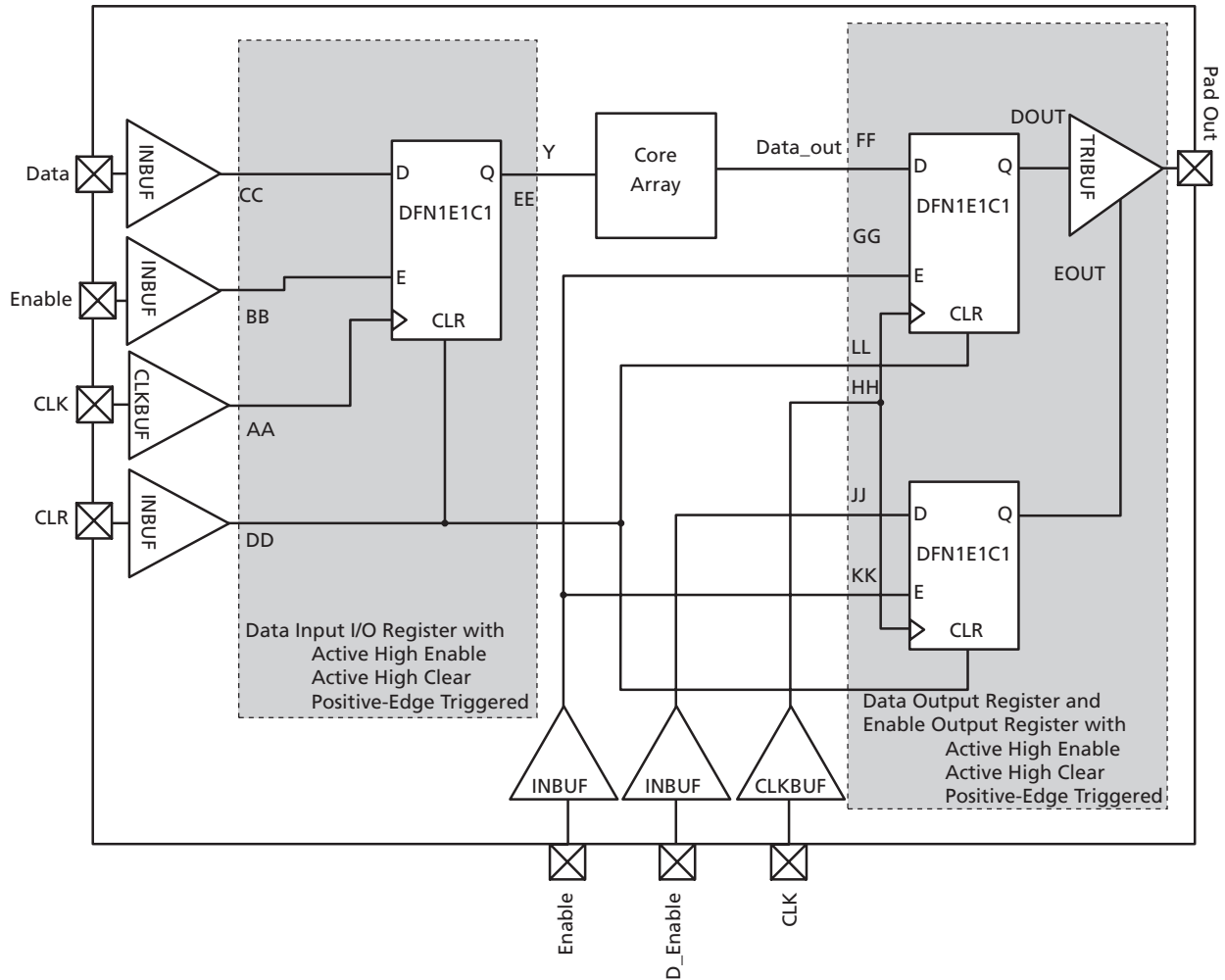
Figure 2-25 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Table 2-81 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

* *See Figure 2-25 on page 2-52 for more information.*

Input Register

Figure 2-26 • **Input Register Timing Diagram**

Timing Characteristics

Table 2-82 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.27	0.32	0.38	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.26	0.30	0.35	0.42	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.37	0.42	0.50	0.60	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.45	0.52	0.61	0.73	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.52	0.61	0.73	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.22	0.25	0.30	0.36	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.22	0.25	0.30	0.36	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	0.36	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	0.36	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.36	0.41	0.48	0.57	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.32	0.37	0.43	0.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Output Register
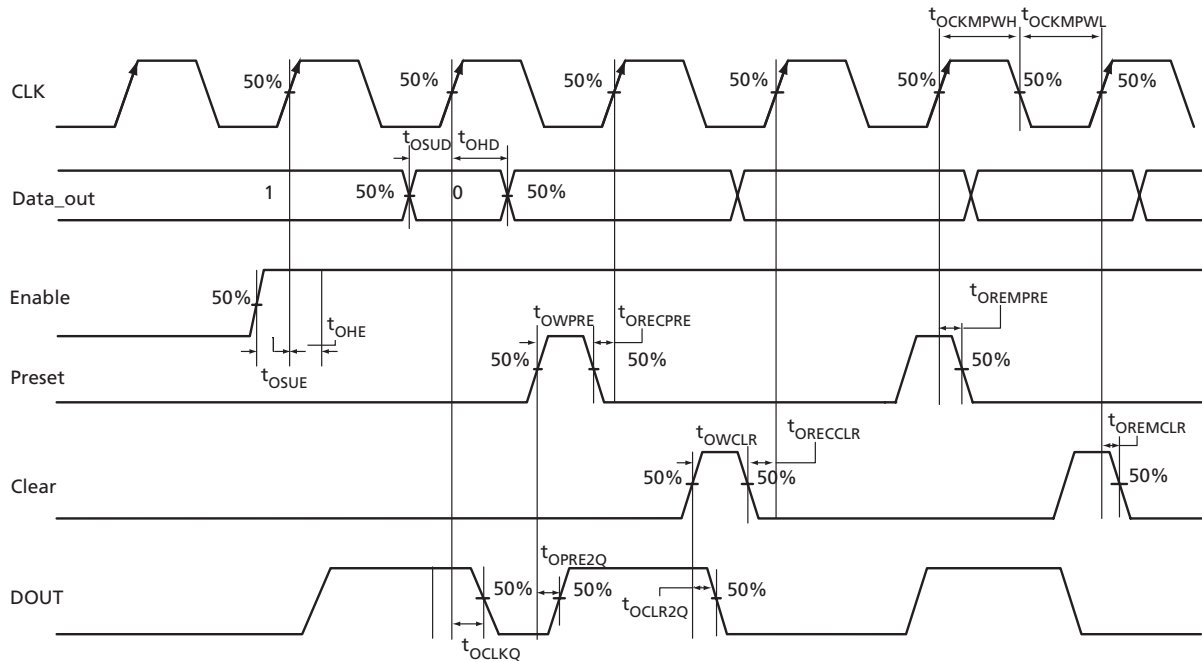
Figure 2-27 • **Output Register Timing Diagram**

Timing Characteristics

Table 2-83 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case V$_{CC}$ = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t$_{OCLKQ}$	Clock-to-Q of the Output Data Register	0.59	0.67	0.79	0.95	ns
t$_{OSUD}$	Data Setup Time for the Output Data Register	0.31	0.36	0.42	0.50	ns
t$_{OHD}$	Data Hold Time for the Output Data Register	0.00	0.00	0.00	0.00	ns
t$_{OSUE}$	Enable Setup Time for the Output Data Register	0.44	0.50	0.59	0.70	ns
t$_{OHE}$	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	0.00	ns
t$_{OCLR2Q}$	Asynchronous Clear-to-Q of the Output Data Register	0.80	0.91	1.07	1.29	ns
t$_{OPRE2Q}$	Asynchronous Preset-to-Q of the Output Data Register	0.80	0.91	1.07	1.29	ns
t$_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	0.00	ns
t$_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.22	0.25	0.30	0.36	ns
t$_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	0.00	ns
t$_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.22	0.25	0.30	0.36	ns
t$_{OWCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	0.36	ns
t$_{OWPRE}$	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	0.36	ns
t$_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.36	0.41	0.48	0.57	ns
t$_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.32	0.37	0.43	0.52	ns

Note: *For specific junction temperature and voltage supply levels, refer to* Table 2-6 on page 2-5 *for derating values.*
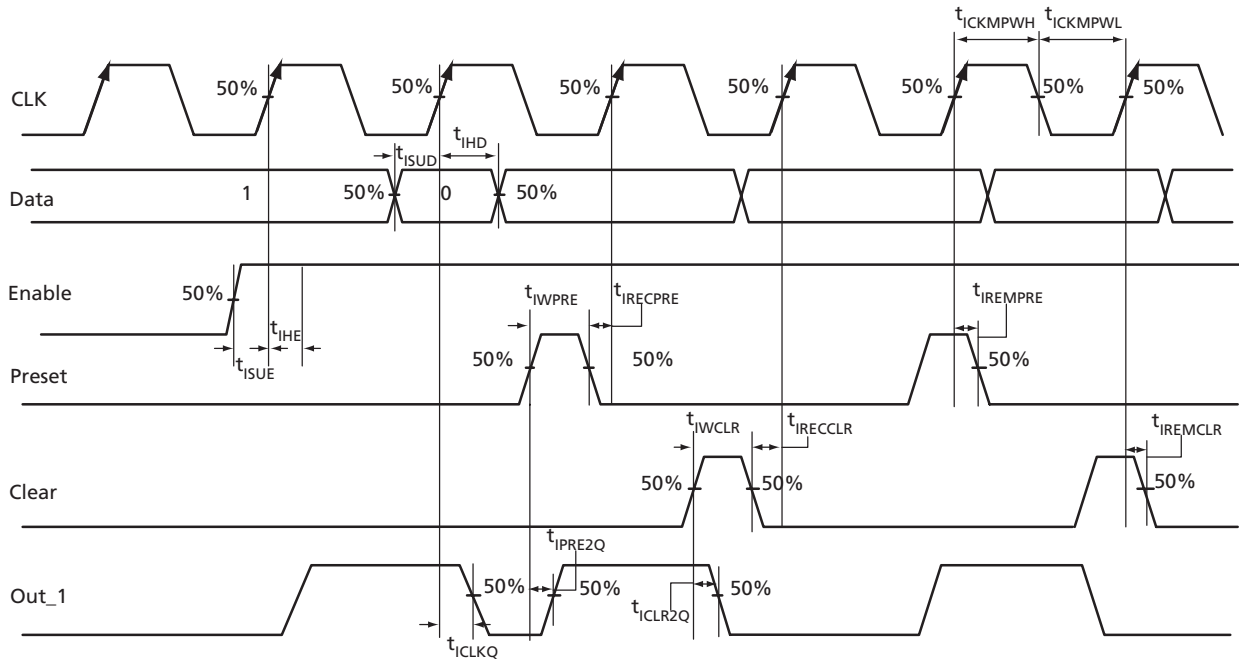
Output Enable Register
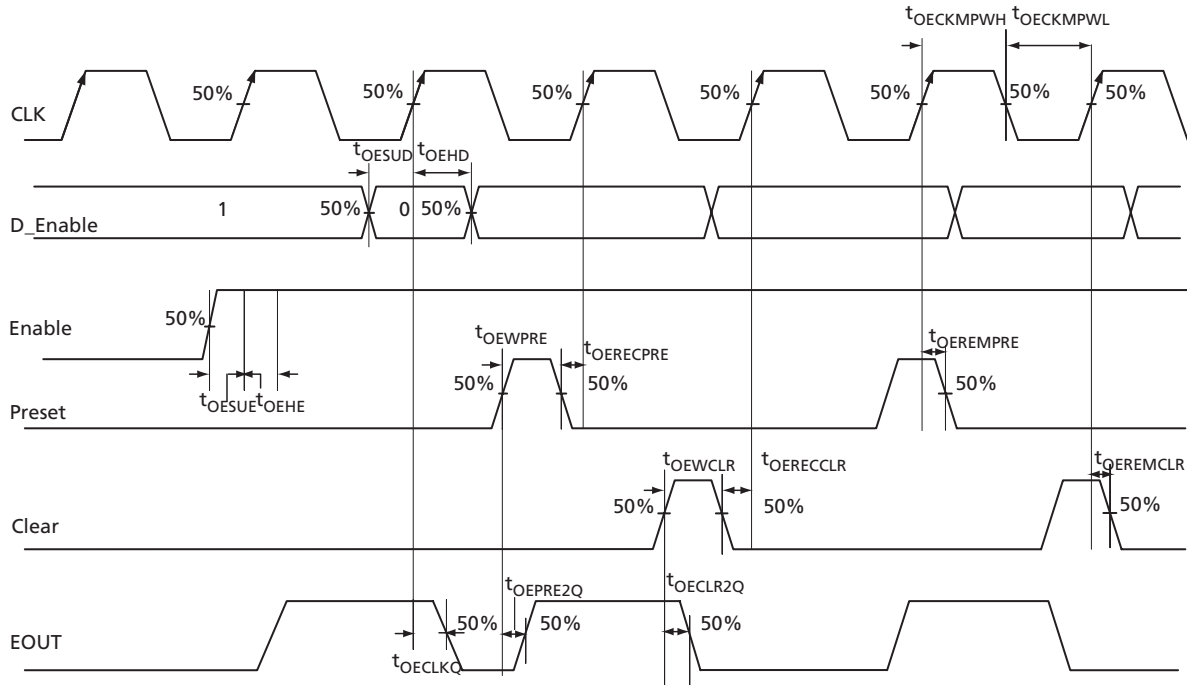
Figure 2-28 • **Output Enable Register Timing Diagram**

Timing Characteristics

Table 2-84 • **Output Enable Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.59	0.67	0.79	0.95	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.31	0.36	0.42	0.50	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.50	0.58	0.70	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.67	0.76	0.89	1.07	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.67	0.76	0.89	1.07	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.22	0.25	0.30	0.36	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.22	0.25	0.30	0.36	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	0.36	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	0.36	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.36	0.41	0.48	0.57	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.32	0.37	0.43	0.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

DDR Module Specifications

Input DDR Module
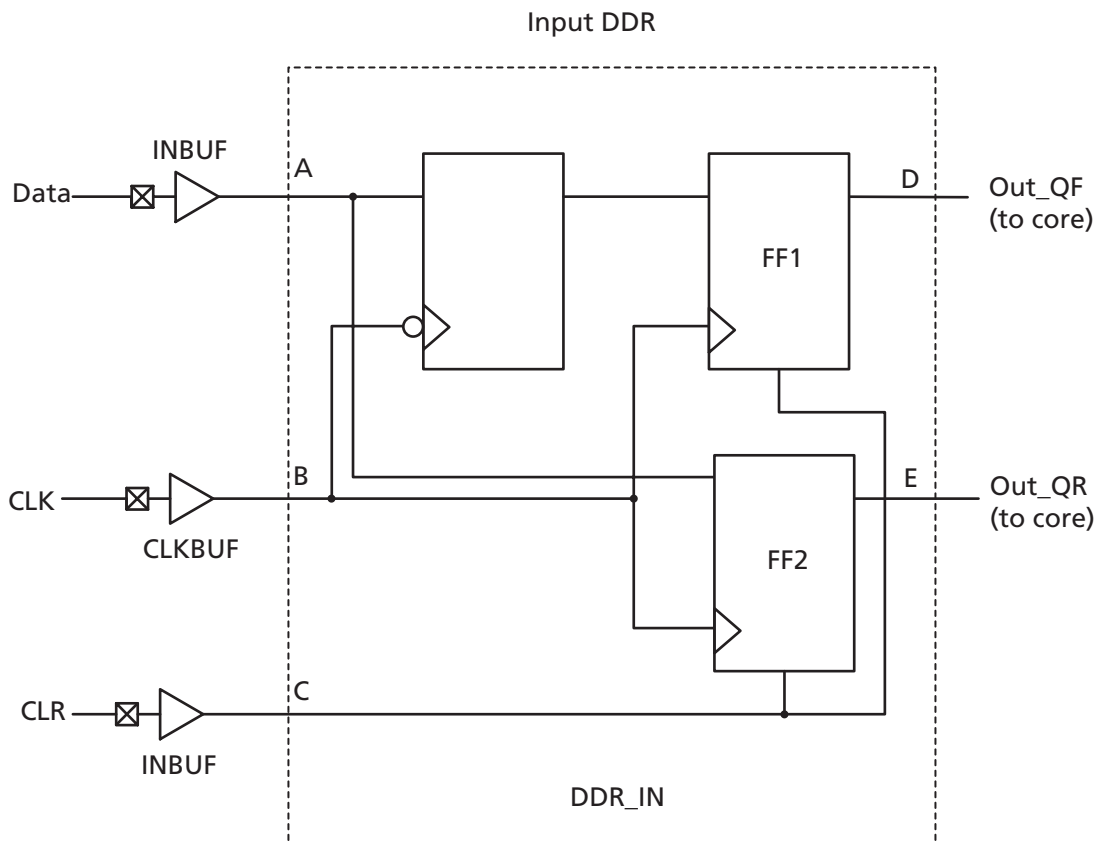
Figure 2-29 • **Input DDR Timing Model**

Table 2-85 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B
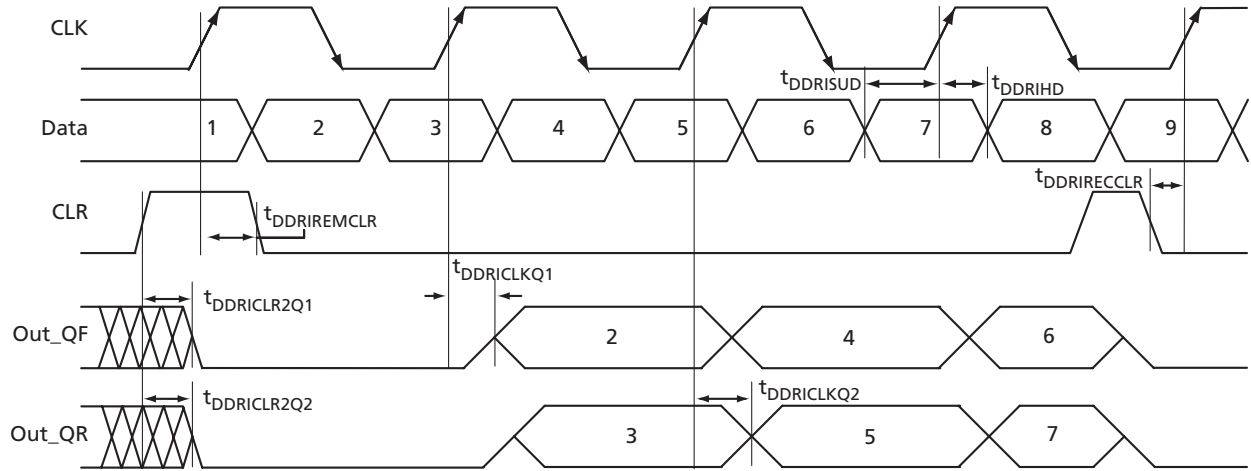
Figure 2-30 • **Input DDR Timing Diagram**

Timing Characteristics

Table 2-86 • **Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.39	0.44	0.52	0.62	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.27	0.31	0.37	0.44	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.28	0.32	0.38	0.45	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	0.00	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear to Out Out_QR for Input DDR	0.57	0.65	0.76	0.92	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.46	0.53	0.62	0.74	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.22	0.25	0.30	0.36	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	0.25	0.30	0.36	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.36	0.41	0.48	0.57	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.32	0.37	0.43	0.52	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	1404	1232	1048	871	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

Output DDR Module
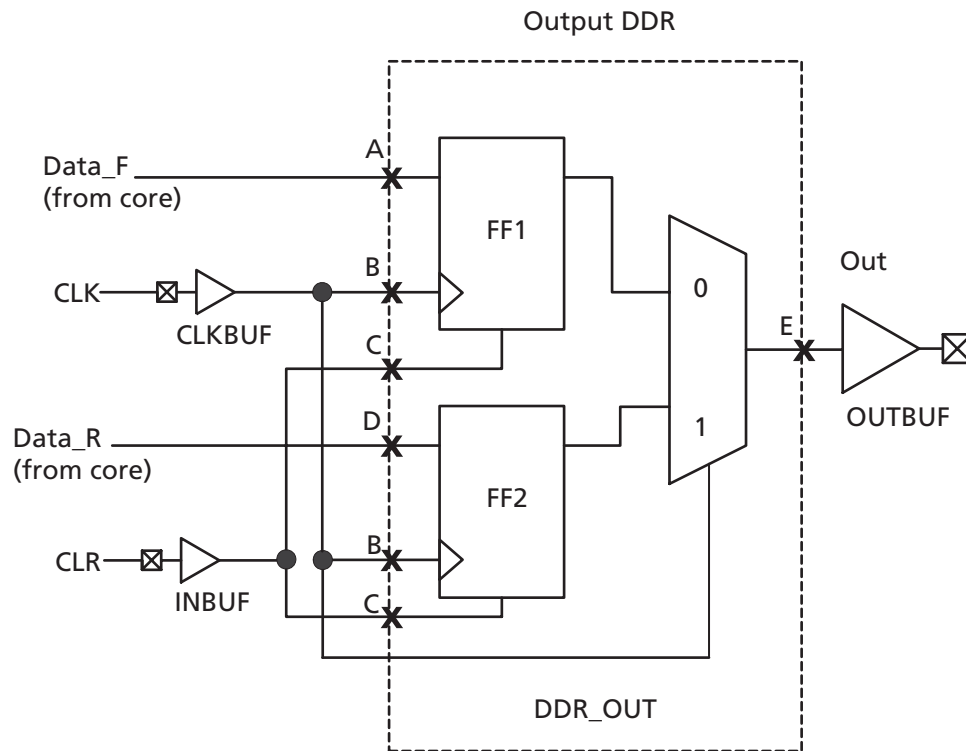
*Figure 2-31 •* **Output DDR Timing Model**

Table 2-87 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B
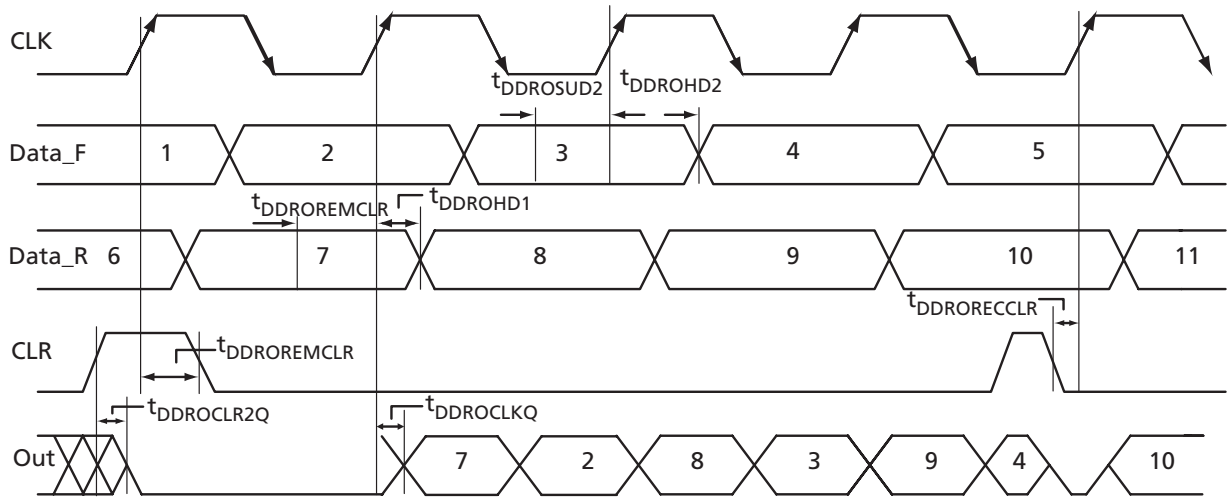
Figure 2-32 • **Output DDR Timing Diagram**

Timing Characteristics

Table 2-88 • **Output DDR Propagation Delays**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case V$_{CC}$ = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t$_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.70	0.80	0.94	1.13	ns
t$_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.38	0.43	0.51	0.61	ns
t$_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.38	0.43	0.51	0.61	ns
t$_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	0.00	0.00	ns
t$_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	0.00	0.00	ns
t$_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.80	0.91	1.07	1.29	ns
t$_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	0.00	0.00	ns
t$_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.22	0.25	0.30	0.36	ns
t$_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.25	0.30	0.36	ns
t$_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.36	0.41	0.48	0.57	ns
t$_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.32	0.37	0.43	0.52	ns
F$_{DDOMAX}$	Maximum Frequency for the Output DDR	1404	1232	1048	871	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

VersaTile Characteristics

## VersaTile Specifications as a Combinatorial Module

The ProASIC3E library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO®/e, and ProASIC3/E Macro Library Guide*.
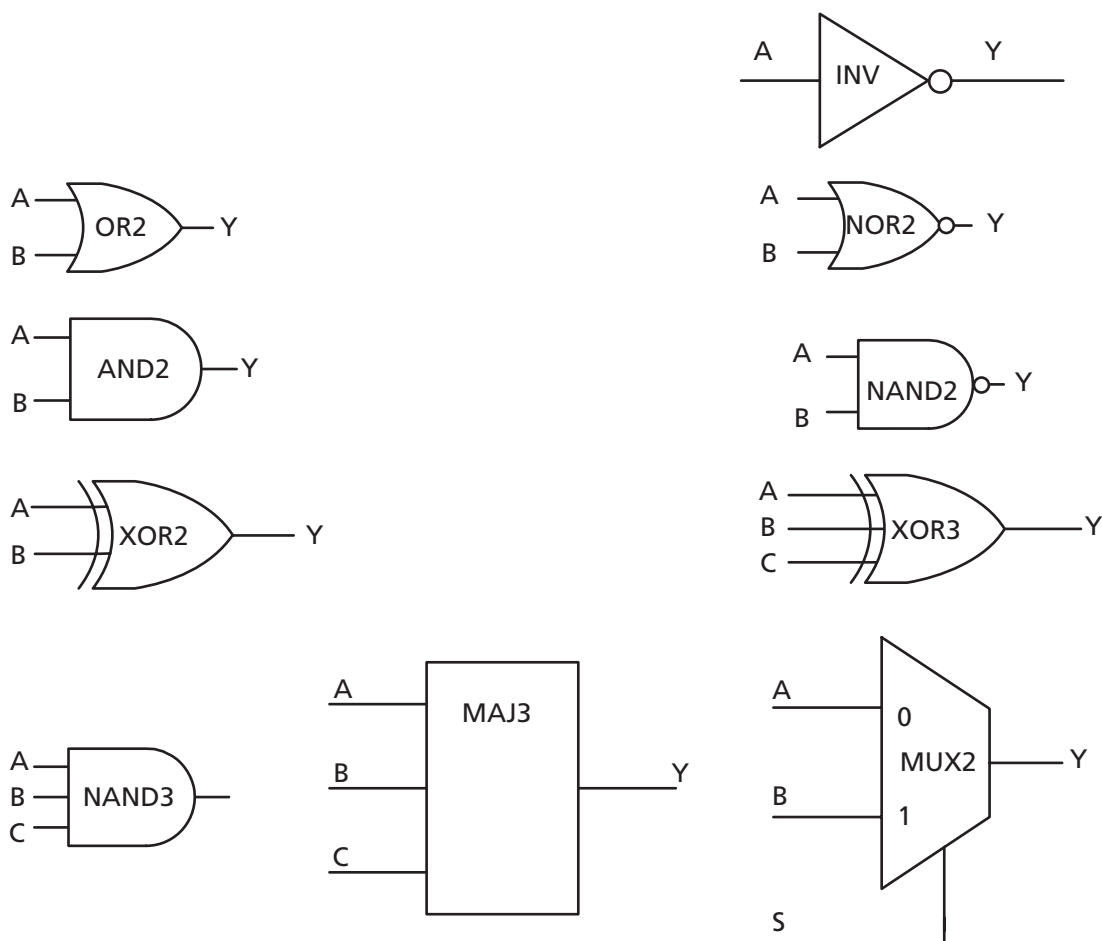
Figure 2-33 • **Sample of Combinatorial Cells**

$t_{PD} = MAX(t_{PD(RR)}, t_{PD(RF)}, t_{PD(FF)}, t_{PD(FR)})$ where edges are applicable for the particular combinatorial cell
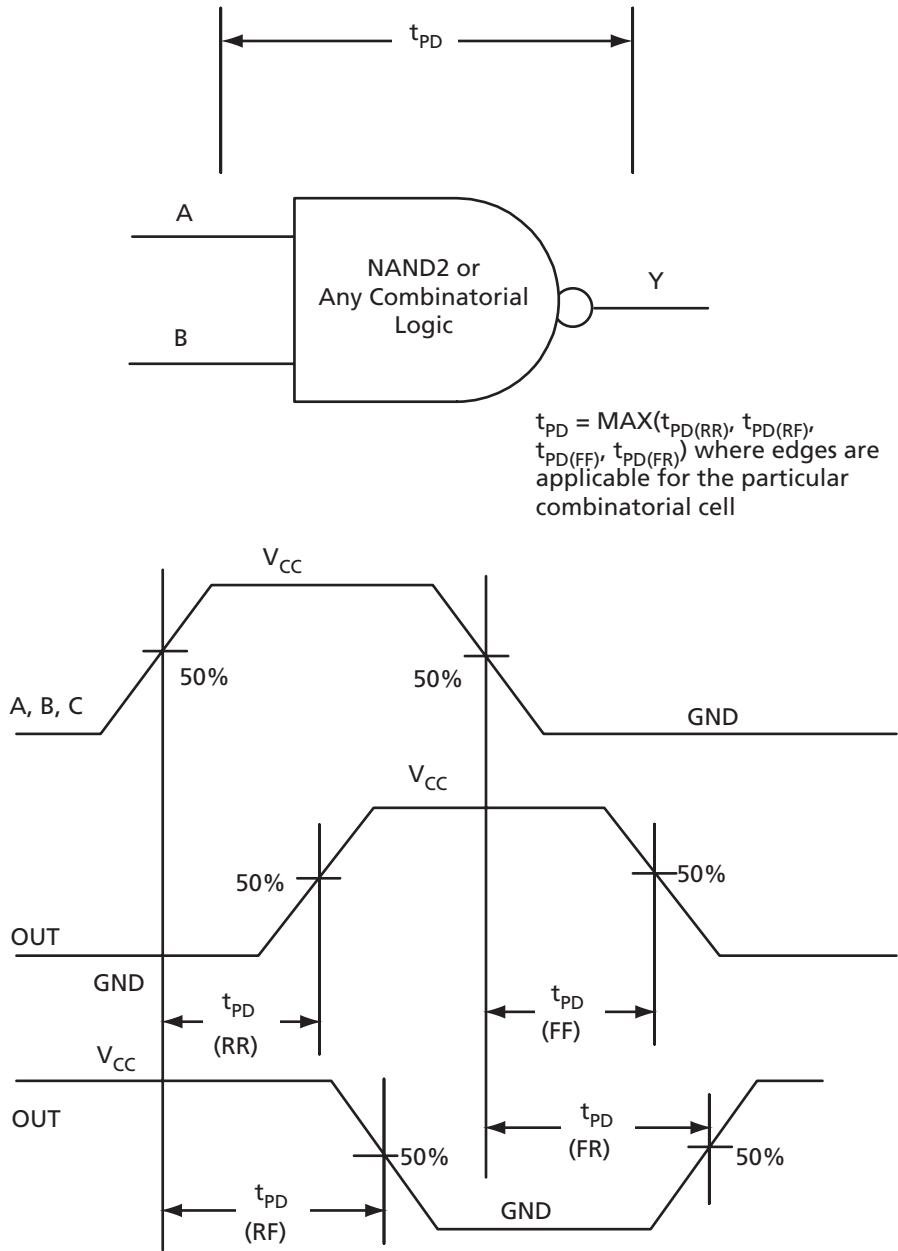
Figure 2-34 • **Timing Model and Waveforms**

Timing Characteristics

Table 2-89 • **Combinatorial Cell Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Combinatorial Cell	Equation	Parameter	–2	–1	Std.	–F	Units
INV	Y = !A	t_{PD}	0.40	0.46	0.54	0.65	ns
AND2	Y = A · B	t_{PD}	0.47	0.54	0.63	0.76	ns
NAND2	Y = !(A · B)	t_{PD}	0.47	0.54	0.63	0.76	ns
OR2	Y = A + B	t_{PD}	0.49	0.55	0.65	0.78	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.55	0.65	0.78	ns
XOR2	Y = A $\oplus$ B	t_{PD}	0.74	0.84	0.99	1.19	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	0.70	0.79	0.93	1.12	ns
XOR3	Y = A $\oplus$ B $\oplus$ C	t_{PD}	0.87	1.00	1.17	1.41	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.58	0.68	0.81	ns
AND3	Y = A · B · C	t_{PD}	0.56	0.64	0.75	0.90	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

VersaTile Specifications as a Sequential Module

The ProASIC3E library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.
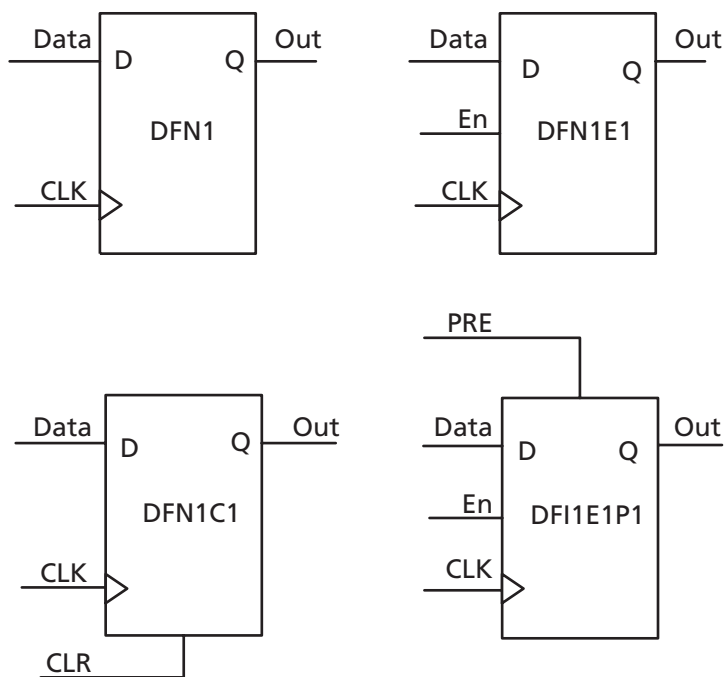
Figure 2-35 • **Sample of Sequential Cells**
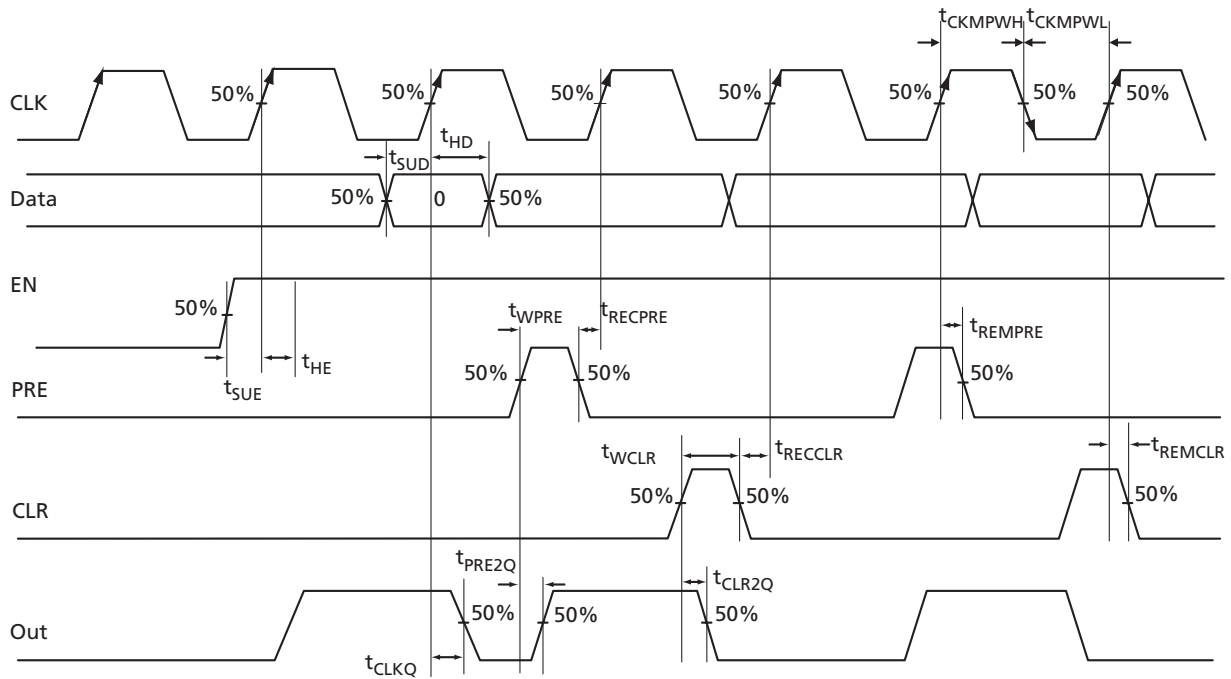
Figure 2-36 • **Timing Model and Waveforms**

Timing Characteristics

Table 2-90 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.55	0.63	0.74	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.43	0.49	0.57	0.69	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.45	0.52	0.61	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.40	0.45	0.53	0.64	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.40	0.45	0.53	0.64	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.22	0.25	0.30	0.36	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.22	0.25	0.30	0.36	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	0.25	0.30	0.36	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	0.25	0.30	0.36	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.32	0.37	0.43	0.52	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.36	0.41	0.48	0.57	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Global Resource Characteristics

A3PE600 Clock Tree Topology

Clock delays are device-specific. Figure 2-37 is an example of a global tree used for clock routing. The global tree presented in Figure 2-37 is driven by a CCC located on the west side of the A3PE600 device. It is used to drive all D-flip-flops in the device.
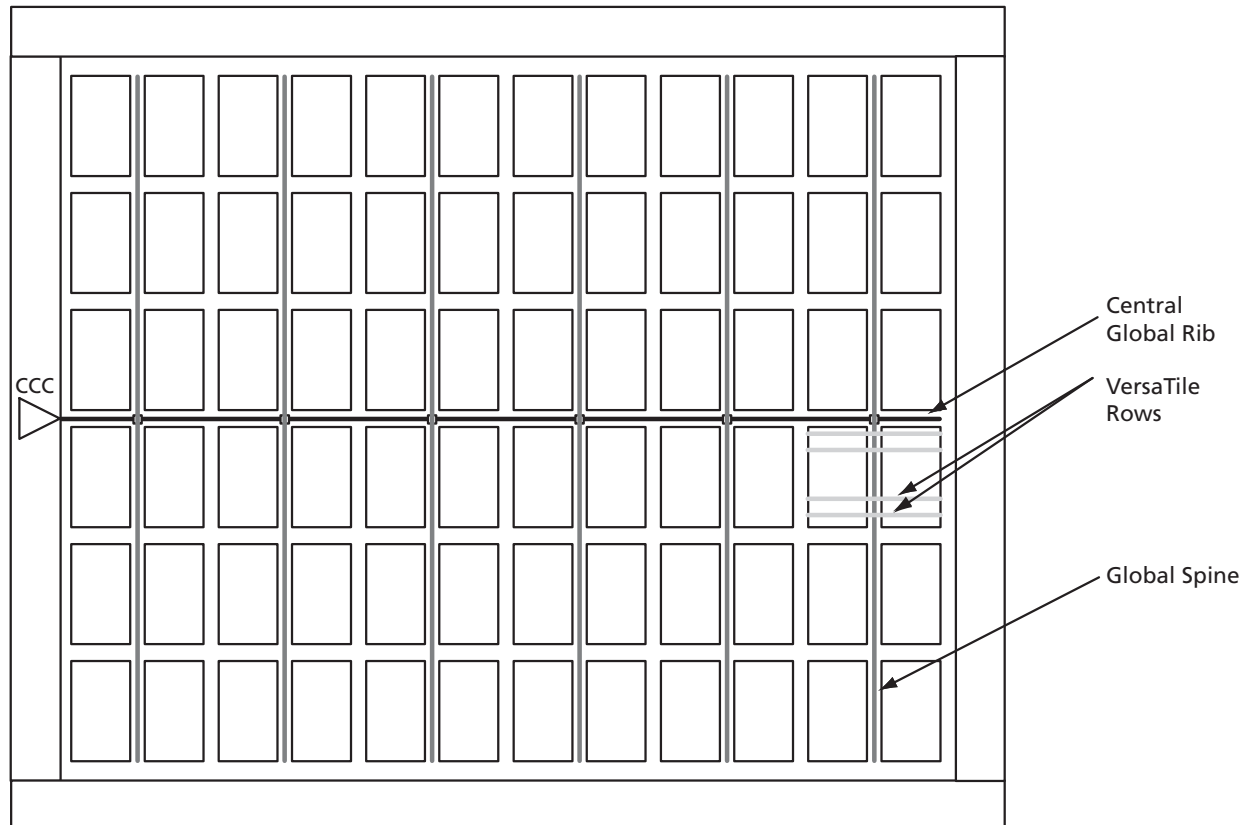
Figure 2-37 • **Example of Global Tree Use in an A3PE600 Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-68. Table 2-91 on page 2-66, Table 2-92 on page 2-66, and Table 2-93 on page 2-67 present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

Table 2-91 • **A3PE600 Global Resource**
Commercial-Case Conditions: $T_J = 70°C$, $V_{CC} = 1.425$ V

Parameter	Description	−2		−1		Std.		−F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	0.83	1.04	0.94	1.18	1.11	1.39	1.33	1.67	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.81	1.06	0.93	1.21	1.09	1.42	1.31	1.71	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock									ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock									ns
t_{RCKSW}	Maximum Skew for Global Clock		0.25		0.28		0.33		0.40	ns
F_{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*

2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*

3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

Table 2-92 • **A3PE1500 Global Resource**
Commercial-Case Conditions: $T_J = 70°C$, $V_{CC} = 1.425$ V

Parameter	Description	−2		−1		Std.		−F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.07	1.29	1.22	1.47	1.43	1.72	1.72	2.07	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.06	1.32	1.21	1.50	1.42	1.76	1.71	2.12	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock									ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock									ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34		0.41	ns
F_{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*

2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*

3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

Table 2-93 • **A3PE3000 Global Resource**
Commercial-Case Conditions: T$_J$ = 70°C, V$_{CC}$ = 1.425 V

Parameter	Description	−2		−1		Std.		−F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t$_{RCKL}$	Input LOW Delay for Global Clock	1.41	1.62	1.60	1.85	1.88	2.17	2.26	2.61	ns
t$_{RCKH}$	Input HIGH Delay for Global Clock	1.40	1.66	1.59	1.89	1.87	2.22	2.25	2.66	ns
t$_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock									ns
t$_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock									ns
t$_{RCKSW}$	Maximum Skew for Global Clock		0.26		0.29		0.35		0.41	ns
F$_{RMAX}$	Maximum Frequency for Global Clock									MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*

2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*

3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

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Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-94 • **ProASIC3E CCC/PLL Specification**

Parameter	Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350	MHz
Delay Increments in Programmable Delay Blocks[2, 3]		160		ps
Serial Clock (SCLK) for Dynamic PLL[1]			125	MHz
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max Peak-to-Peak Period Jitter			
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%		0.70%	
24 MHz to 100 MHz	1.00%		1.20%	
100 MHz to 250 MHz	1.75%		2.00%	
250 MHz to 350 MHz	2.50%		5.60%	
Acquisition Time LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[4] LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1[2, 3]	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2[2, 3]	0.025		5.56	ns
Delay Range in Block: Fixed Delay[1, 2]		2.2		ns

Notes:

1. *Maximum value obtained for a –2 speed-grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.*

2. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-5 for deratings.*

3. *$T_J = 25°C$, $V_{CC} = 1.5$ V.*

4. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
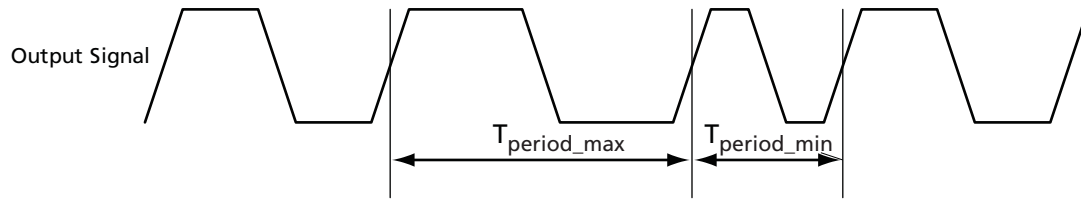
Note: *Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.*

Figure 2-38 • **Peak-to-Peak Jitter Definition**

Embedded SRAM and FIFO Characteristics

SRAM

RAM4K9

ADDRA11	DOUTA8
ADDRA10	DOUTA7
•	•
ADDRA0	DOUTA0
DINA8	
DINA7	
•	
DINA0	
WIDTHA1	
WIDTHA0	
PIPEA	
WMODEA	
BLKA	
WENA	
CLKA	

ADDRB11	DOUTB8
ADDRB10	DOUTB7
•	•
ADDRB0	DOUTB0
DINB8	
DINB7	
•	
DINB0	
WIDTHB1	
WIDTHB0	
PIPEB	
WMODEB	
BLKB	
WENB	
CLKB	

RESET

RAM512X18

RADDR8	RD17
RADDR7	RD16
•	•
RADDR0	RD0
RW1	
RW0	
PIPE	
REN	
RCLK	

WADDR8	
WADDR7	
•	
WADDR0	
WD17	
WD16	
•	
WD0	
WW1	
WW0	
WEN	
WCLK	

RESET
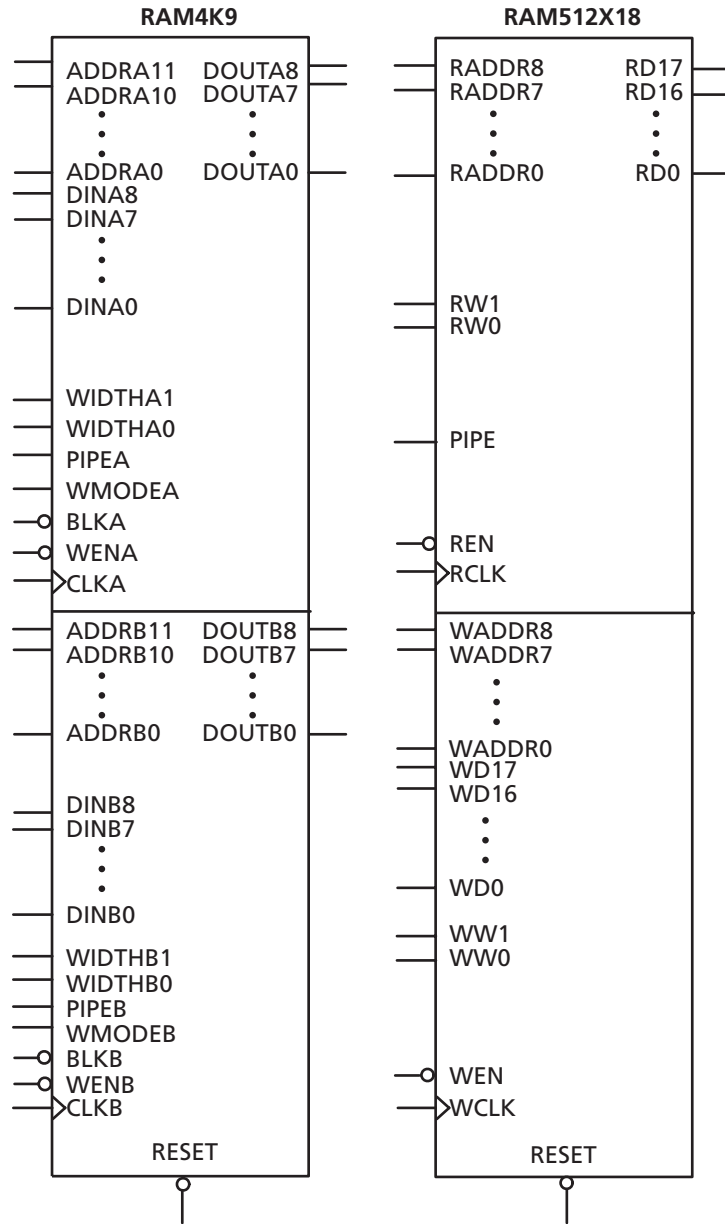
Figure 2-39 • **RAM Models**

Timing Waveforms
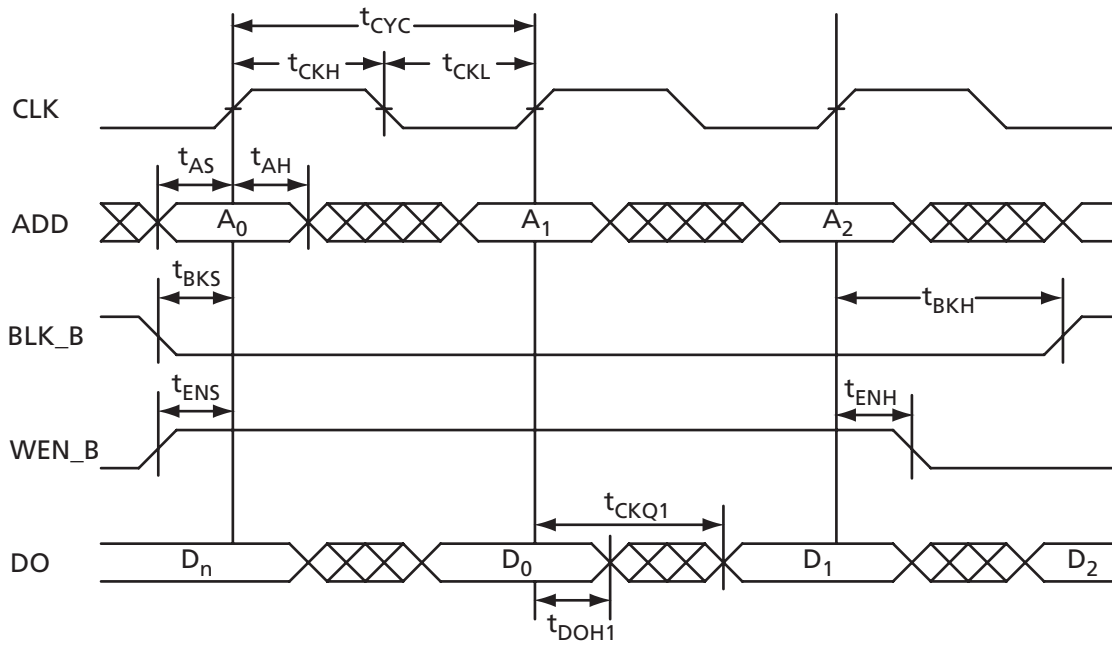
Figure 2-40 • RAM Read for Pass-Through Output
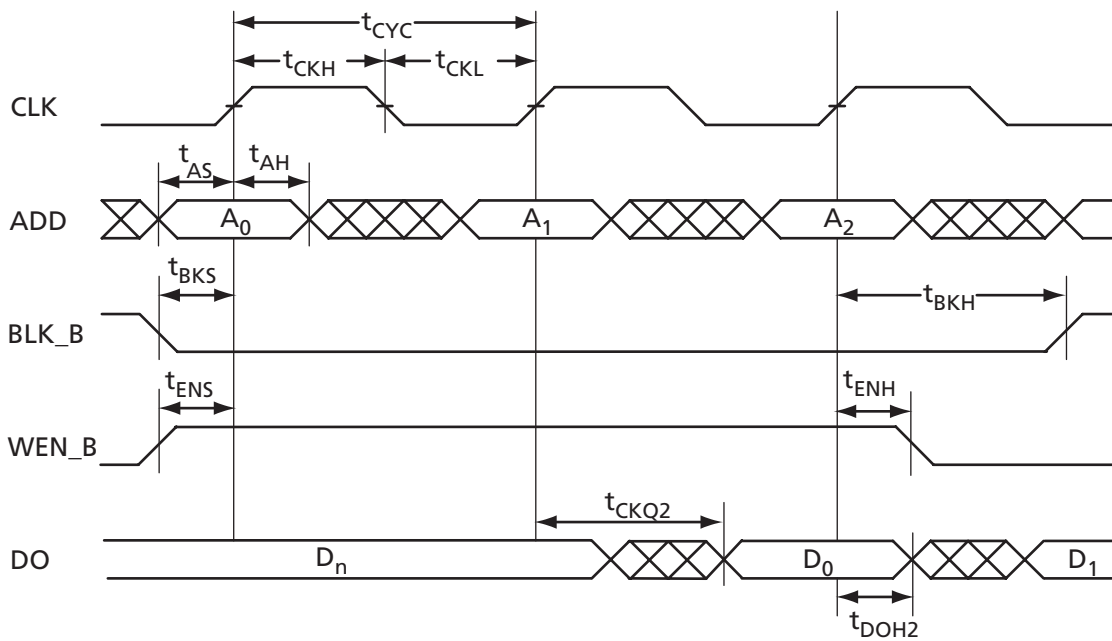
Figure 2-41 • RAM Read for Pipelined Output
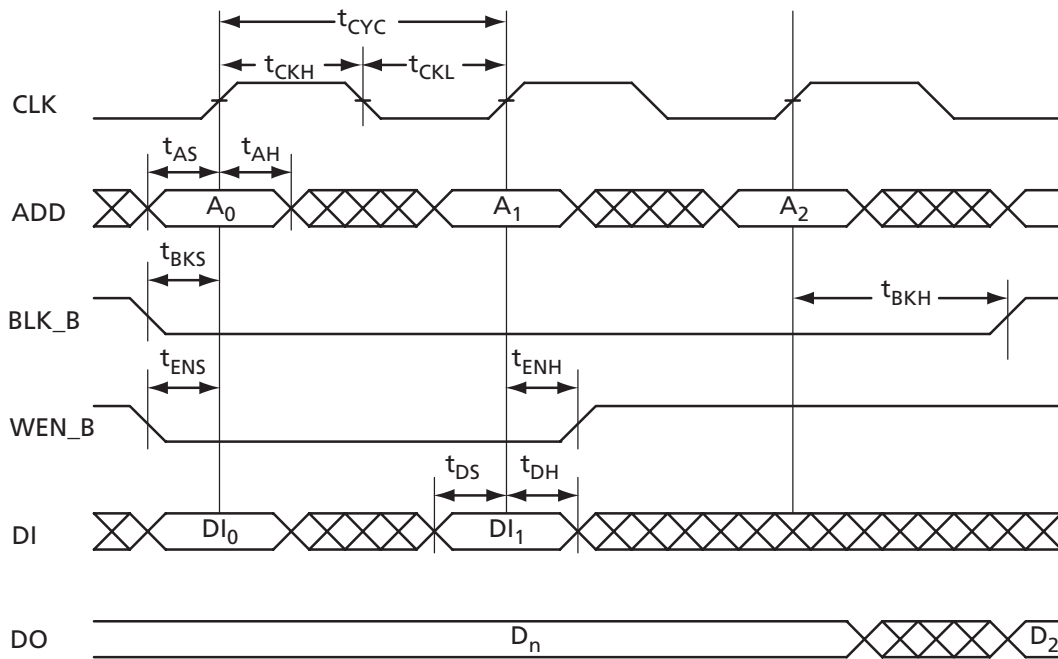
Figure 2-42 • **RAM Write, Output Retained (WMODE = 0)**
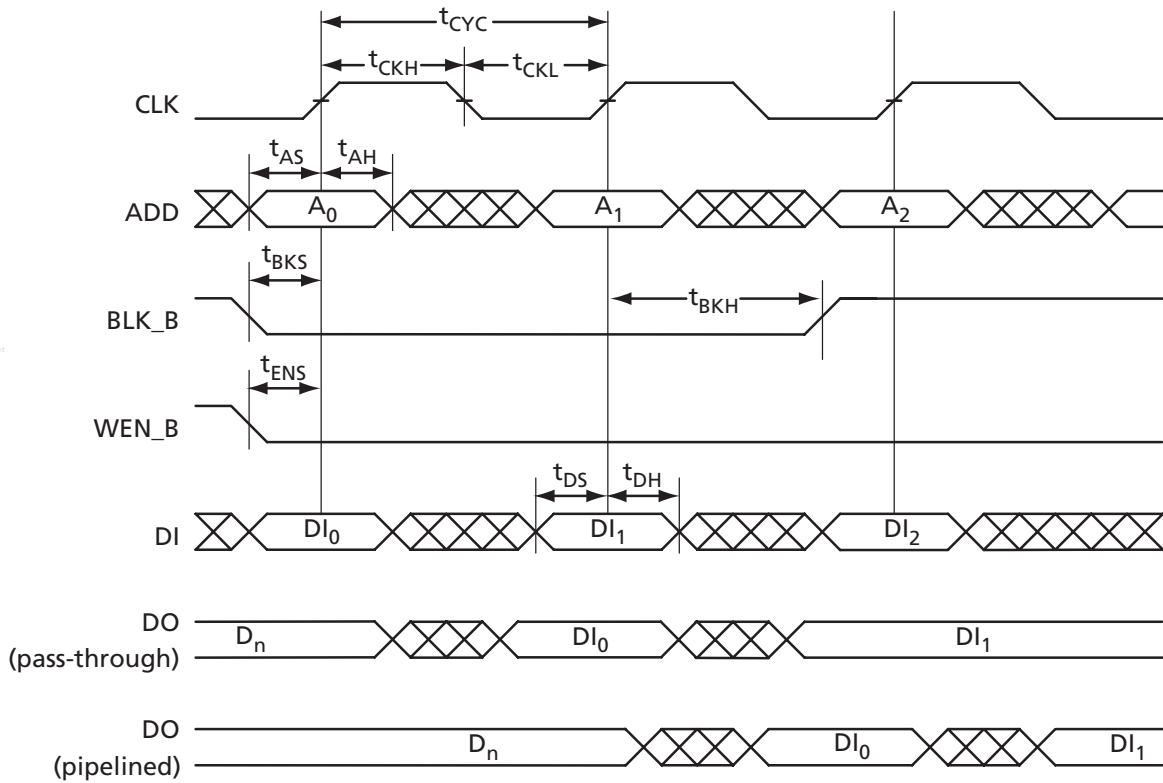
Figure 2-43 • **RAM Write, Output as Write Data (WMODE = 1)**
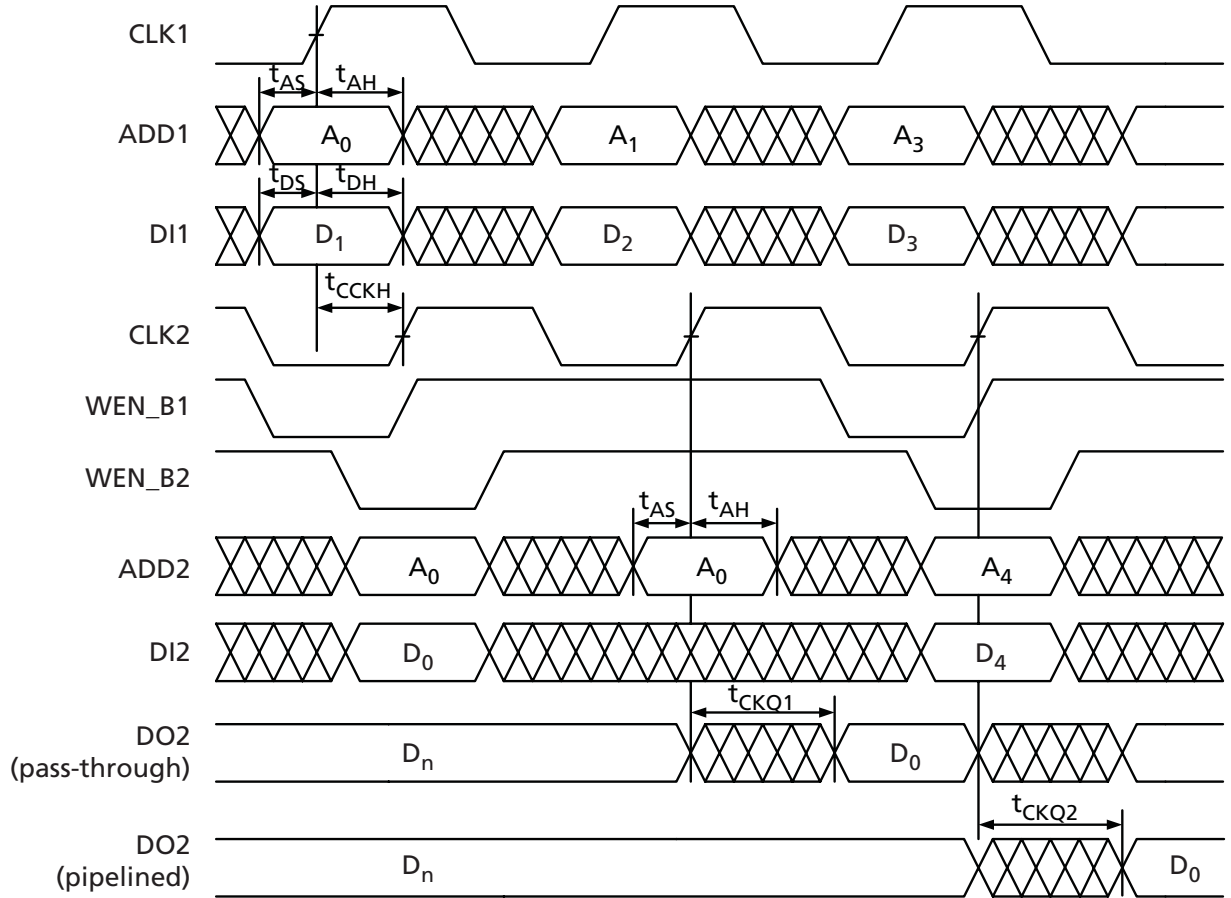
Figure 2-44 • **Write Access after Write onto Same Address**
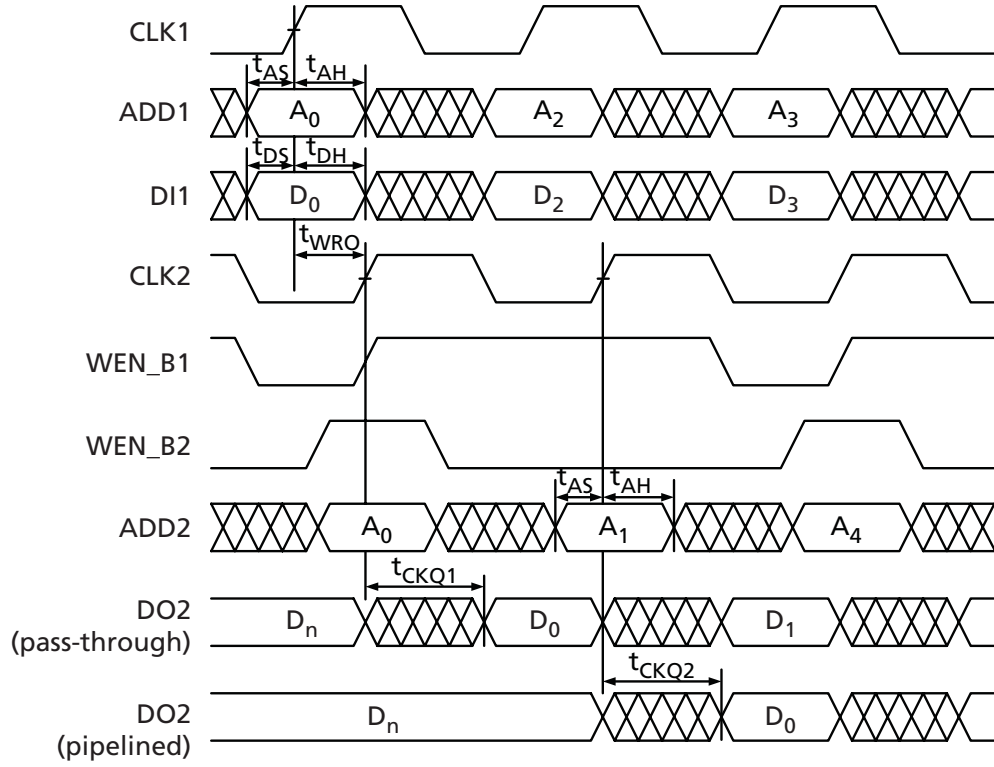
Figure 2-45 • **Read Access after Write onto Same Address**
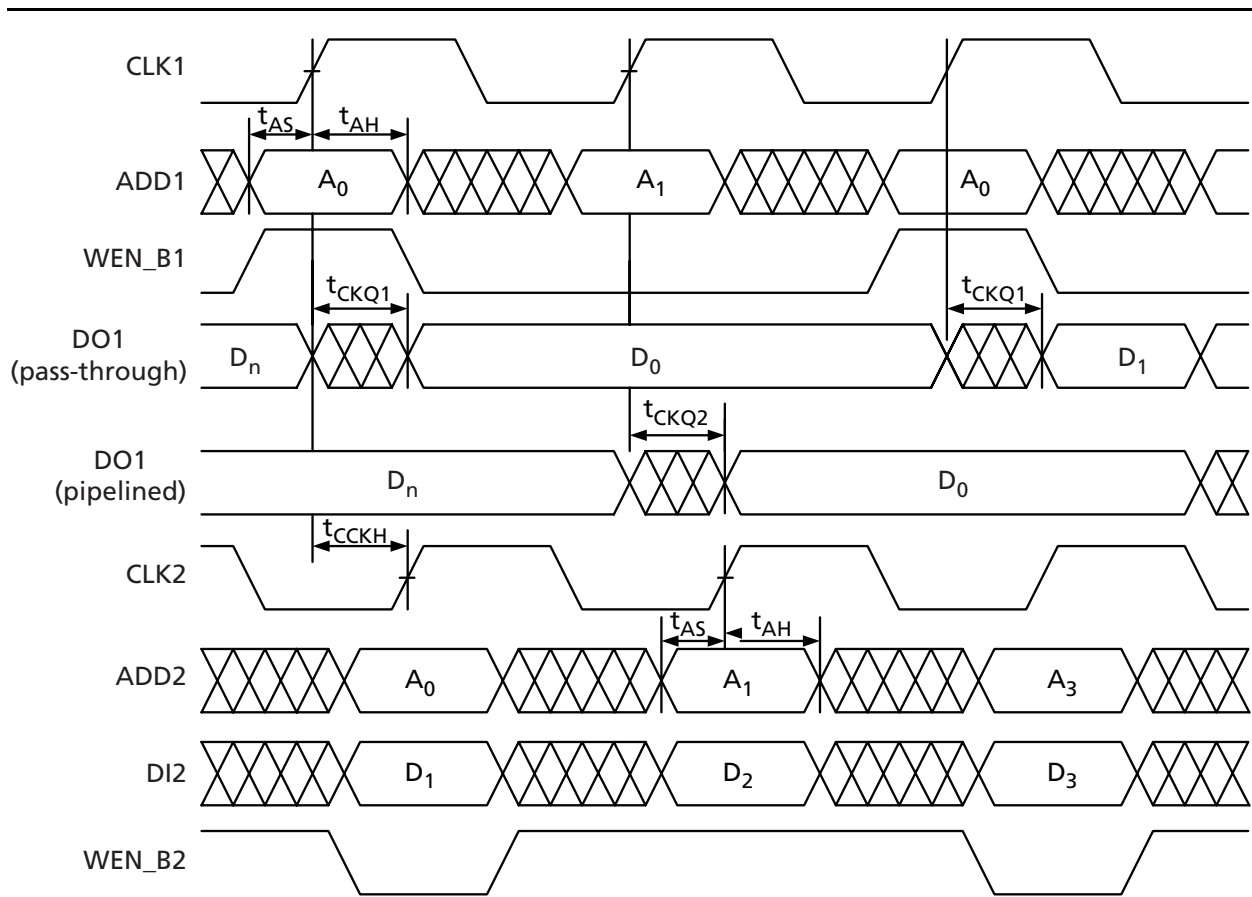
Figure 2-46 • Write Access after Read onto Same Address
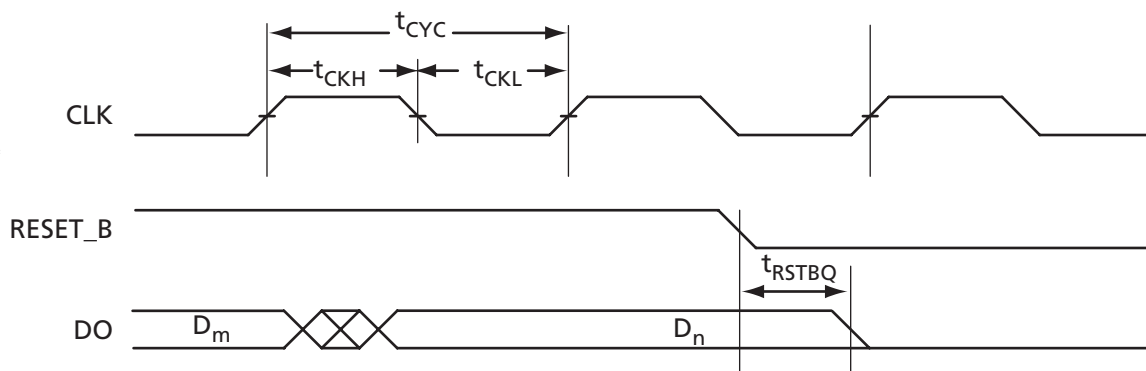
Figure 2-47 • RAM Reset

Timing Characteristics

Table 2-95 • **RAM4K9**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case V$_{CC}$ = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t$_{AS}$	Address Setup Time	0.25	0.28	0.33	0.40	ns
t$_{AH}$	Address Hold Time	0.00	0.00	0.00	0.00	ns
t$_{ENS}$	REN_B, WEN_B Setup Time	0.14	0.16	0.19	0.23	ns
t$_{ENH}$	REN_B, WEN_B Hold Time	0.10	0.11	0.13	0.16	ns
t$_{BKS}$	BLK_B Setup Time	0.23	0.27	0.31	0.37	ns
t$_{BKH}$	BLK_B Hold Time	0.02	0.02	0.02	0.03	ns
t$_{DS}$	Input Data (DI) Setup Time	0.18	0.21	0.25	0.29	ns
t$_{DH}$	Input Data (DI) Hold Time	0.00	0.00	0.00	0.00	ns
t$_{CKQ1}$	Clock HIGH to New Data Valid on DO (output retained, WMODE = 0)	1.79	2.03	2.39	2.87	ns
	Clock HIGH to New Data Valid on DO (pass-through, WMODE = 1)	2.36	2.68	3.15	3.79	ns
t$_{CKQ2}$	Clock HIGH to New Data Valid on DO (pipelined)	0.89	1.02	1.20	1.44	ns
t$_{WRO}$	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	TBD	TBD	ns
t$_{CCKH}$	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	TBD	TBD	ns
t$_{RSTBQ}$	RESET_B LOW to Data Out LOW on DO (pass-through)	0.92	1.05	1.23	1.48	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	0.92	1.05	1.23	1.48	ns
t$_{REMRSTB}$	RESET_B Removal	0.29	0.33	0.38	0.46	ns
t$_{RECRSTB}$	RESET_B Recovery	1.50	1.71	2.01	2.41	ns
t$_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.21	0.24	0.29	0.34	ns
t$_{CYC}$	Clock Cycle Time	3.23	3.68	4.32	5.19	ns
F$_{MAX}$	Maximum Frequency	310	272	231	193	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Table 2-96 • **RAM512X18**
        Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case V$_{CC}$ = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t$_{AS}$	Address Setup Time	0.25	0.28	0.33	0.40	ns
t$_{AH}$	Address Hold Time	0.00	0.00	0.00	0.00	ns
t$_{ENS}$	REN_B, WEN_B Setup Time	0.18	0.20	0.24	0.28	ns
t$_{ENH}$	REB_B, WEN_B Hold Time	0.06	0.07	0.08	0.09	ns
t$_{DS}$	Input Data (DI) Setup Time	0.18	0.21	0.25	0.29	ns
t$_{DH}$	Input Data (DI) Hold Time	0.00	0.00	0.00	0.00	ns
t$_{CKQ1}$	Clock HIGH to New Data Valid on DO (output retained, WMODE = 0)	2.16	2.46	2.89	3.47	ns
t$_{CKQ2}$	Clock HIGH to New Data Valid on DO (pipelined)	0.90	1.02	1.20	1.44	ns
t$_{WRO}$	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	TBD	TBD	ns
t$_{CCKH}$	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	TBD	TBD	ns
t$_{RSTBQ}$	RESET_B LOW to Data Out LOW on DO (pass-through)	0.92	1.05	1.23	1.48	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	0.92	1.05	1.23	1.48	ns
t$_{REMRSTB}$	RESET_B Removal	0.29	0.33	0.38	0.46	ns
t$_{RECRSTB}$	RESET_B Recovery	1.50	1.71	2.01	2.41	ns
t$_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.21	0.24	0.29	0.34	ns
t$_{CYC}$	Clock Cycle Time	3.23	3.68	4.32	5.19	ns
F$_{MAX}$	Maximum Frequency	310	272	231	193	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

FIFO

Figure 2-48 • **FIFO Model**

Timing Waveforms
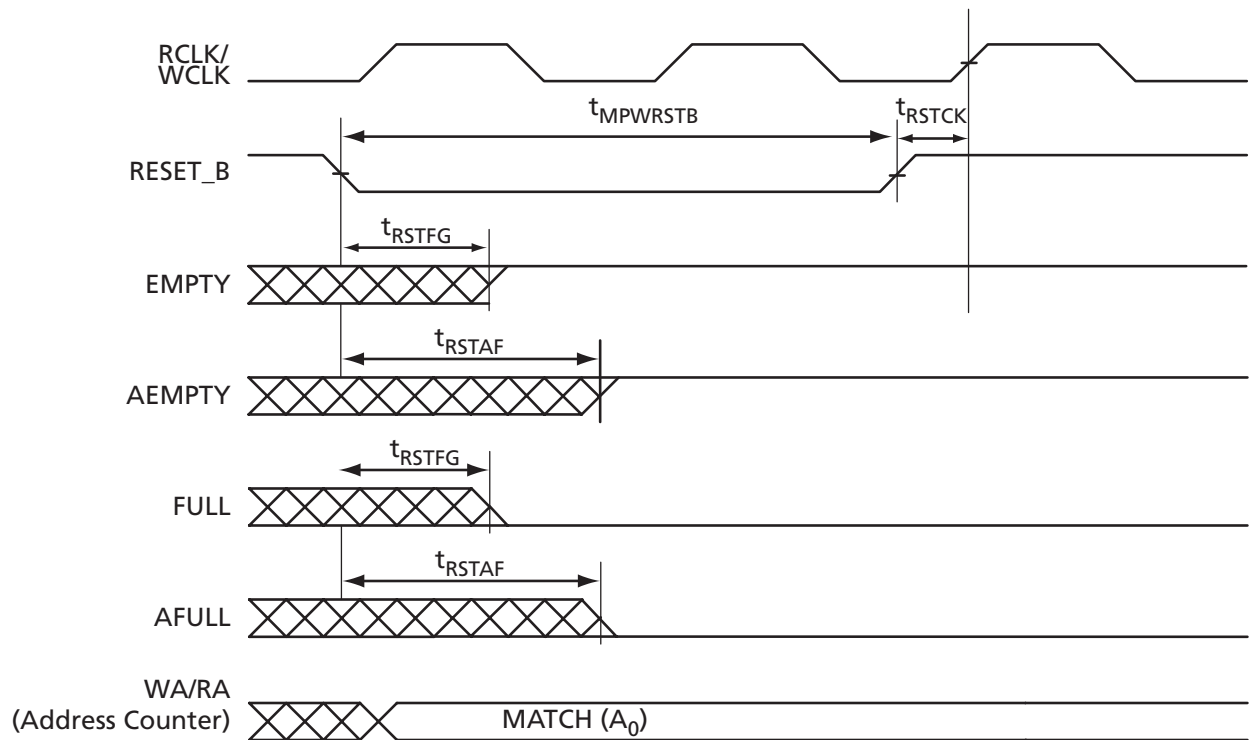
Figure 2-49 • FIFO Reset
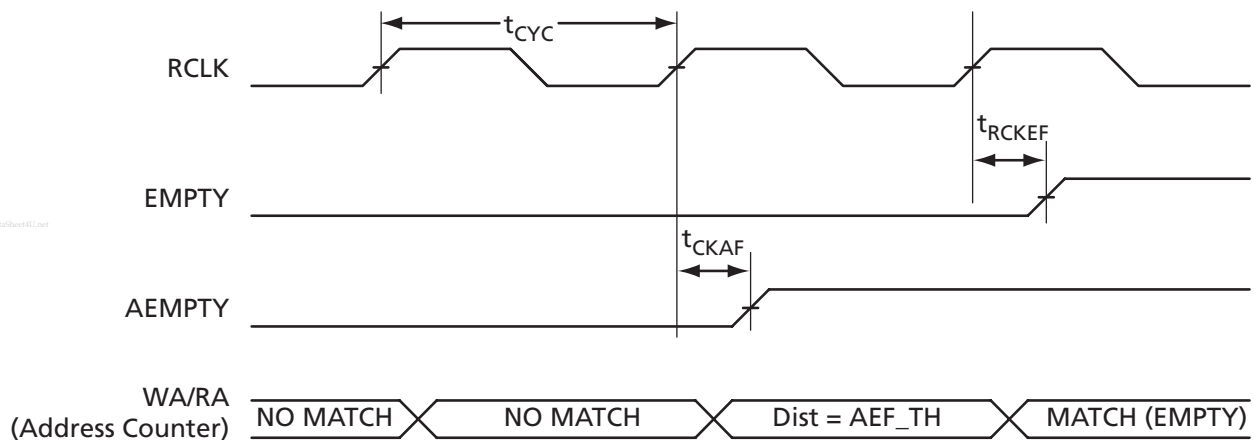
Figure 2-50 • FIFO EMPTY Flag and AEMPTY Flag Assertion
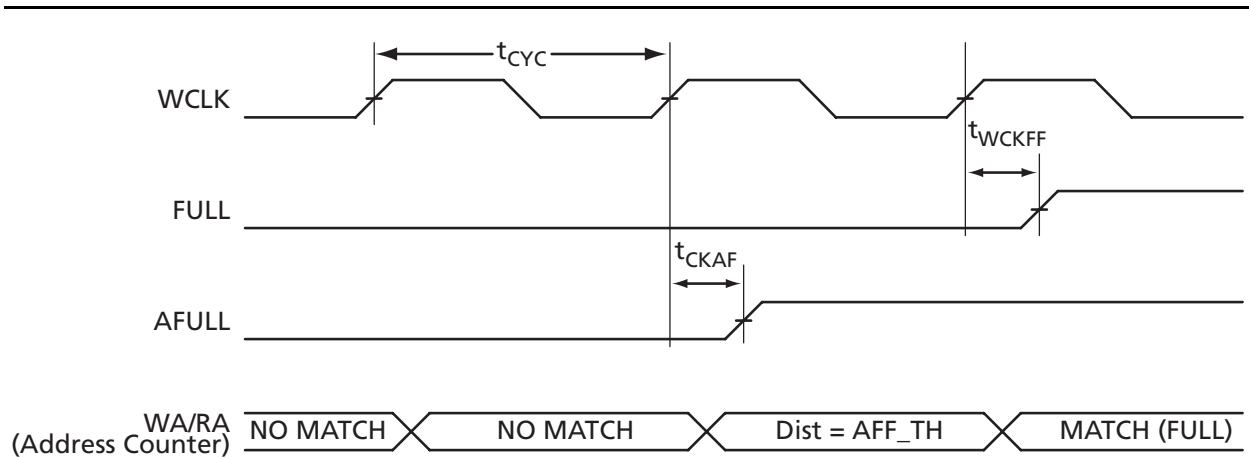
Figure 2-51 • **FIFO FULL Flag and AFULL Flag Assertion**
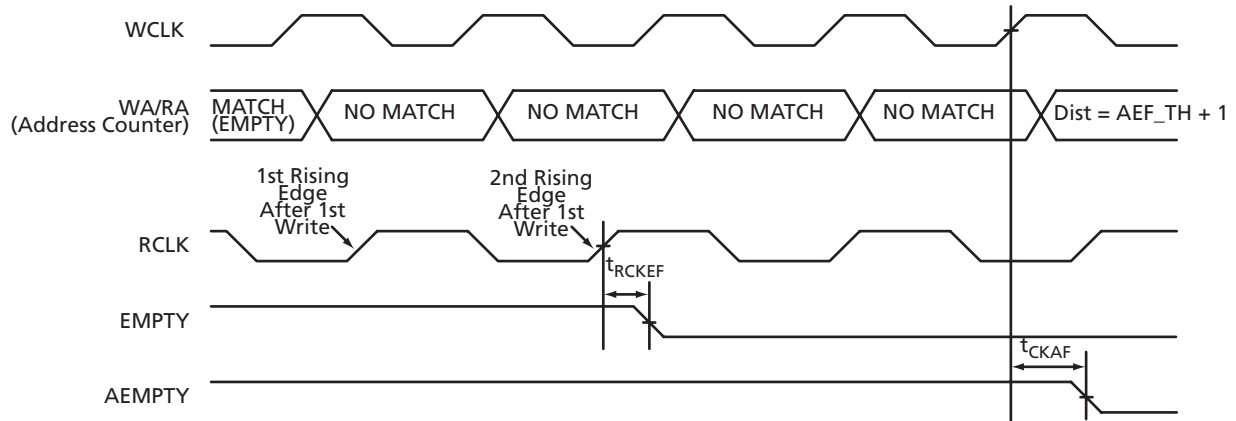
Figure 2-52 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**
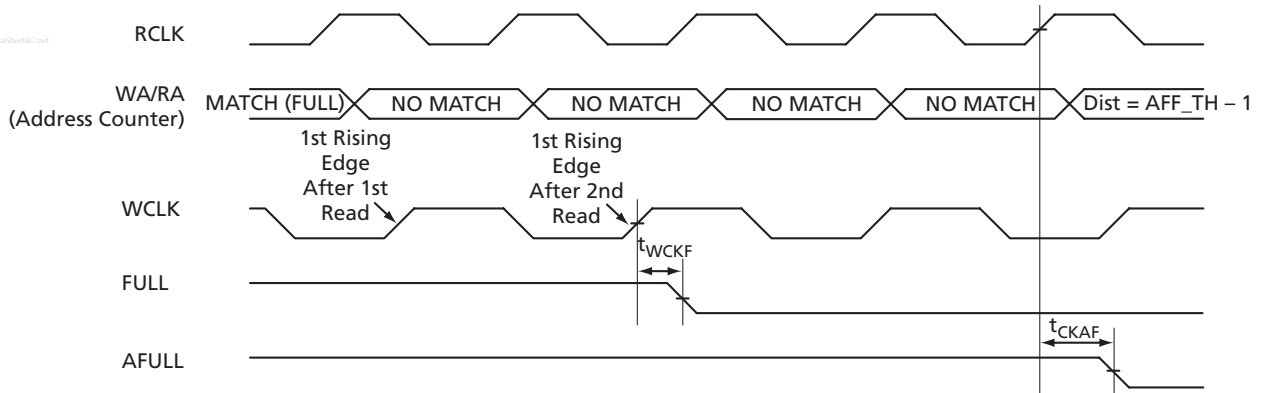
Figure 2-53 • **FIFO FULL Flag and AFULL Flag Deassertion**

Timing Characteristics

Table 2-97 • **FIFO**
Commercial-Case Conditions: T$_J$ = 70°C, V$_{CC}$ = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t$_{ENS}$	REN_B, WEN_B Setup Time	1.38	1.57	1.84	2.21	ns
t$_{ENH}$	REN_B, WEN_B Hold Time	0.02	0.02	0.02	0.03	ns
t$_{BKS}$	BLK_B Setup Time	0.19	0.22	0.26	0.31	ns
t$_{BKH}$	BLK_B Hold Time	0.00	0.00	0.00	0.00	ns
t$_{DS}$	Input Data (DI) Setup Time	0.18	0.21	0.25	0.29	ns
t$_{DH}$	Input Data (DI) Hold Time	0.00	0.00	0.00	0.00	ns
t$_{CKQ1}$	Clock HIGH to New Data Valid on DO (pass-through)	2.36	2.68	3.15	3.79	ns
t$_{CKQ2}$	Clock HIGH to New Data Valid on DO (pipelined)	0.89	1.02	1.20	1.44	ns
t$_{RCKEF}$	RCLK HIGH to Empty Flag Valid	1.72	1.96	2.30	2.76	ns
t$_{WCKFF}$	WCLK HIGH to Full Flag Valid	1.63	1.86	2.18	2.62	ns
t$_{CKAF}$	Clock HIGH to Almost Empty/Full Flag Valid	6.19	7.05	8.29	9.96	ns
t$_{RSTFG}$	RESET_B LOW to Empty/Full Flag Valid	1.69	1.93	2.27	2.72	ns
t$_{RSTAF}$	RESET_B LOW to Almost Empty/Full Flag Valid	6.13	6.98	8.20	9.85	ns
t$_{RSTBQ}$	RESET_B LOW to Data Out LOW on DO (pass-through)	0.92	1.05	1.23	1.48	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	0.92	1.05	1.23	1.48	ns
t$_{REMRSTB}$	RESET_B Removal	0.29	0.33	0.38	0.46	ns
t$_{RECRSTB}$	RESET_B Recovery	1.50	1.71	2.01	2.41	ns
t$_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.21	0.24	0.29	0.34	ns
t$_{CYC}$	Clock Cycle Time	3.23	3.68	4.32	5.19	ns
F$_{MAX}$	Maximum Frequency	310	272	231	193	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

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Embedded FlashROM Characteristics
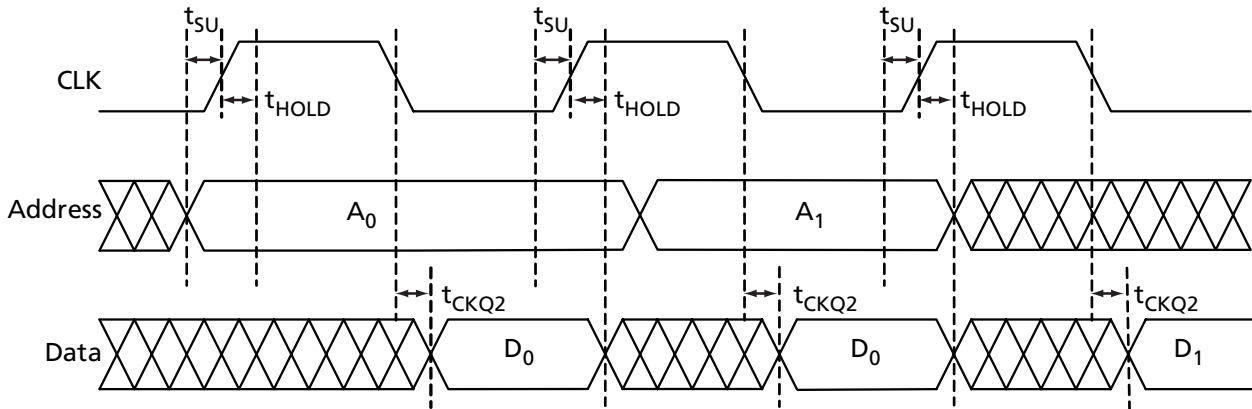
Figure 2-54 • **Timing Diagram**

Timing Characteristics

Table 2-98 • **Embedded FlashROM Access Time**

Parameter	Description	–2	–1	Std.	Units
t_{SU}	Address Setup Time	0.53	0.61	0.71	ns
t_{HOLD}	Address Hold Time	0.00	0.00	0.00	ns
t_{CK2Q}	Clock to Out	16.23	18.48	21.73	ns
F_{MAX}	Maximum Clock Frequency	15	15	15	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-12 for more details.

Timing Characteristics

Table 2-99 • **JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.50	0.57	0.67	ns
t_{DIHD}	Test Data Input Hold Time	1.00	1.13	1.33	ns
t_{TMSSU}	Test Mode Select Setup Time	0.50	0.57	0.67	ns
t_{TMDHD}	Test Mode Select Hold Time	1.00	1.13	1.33	ns
t_{TCK2Q}	Clock to Q (data out)	6.00	6.80	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	20.00	22.67	26.67	ns
F_{TCKMAX}	TCK Maximum Frequency	25.00	22.00	19.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.00	0.00	0.00	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.20	0.23	0.27	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-5 for derating values.

Part Number and Revision Date

Part Number 51700098-002-2
Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.2)	Page
v1.1 (January 2008)	The title of Table 2-4 · Overshoot and Undershoot Limits 1 was modified to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.	2-3
	Table 2-74 · LVDS Minimum and Maximum DC Input and Output Levels was updated.	2-47
v1.0 (January 2008)	In Table 2-3 · Flash Programming Limits – Retention, Storage and Operating Temperature1, Maximum Operating Junction Temperature was changed from 110°C to 100°C for both commercial and industrial grades.	2-2
	The "PLL Behavior at Brownout Condition" section is new.	2-4
	In the "PLL Contribution—PPLL" section, the following was deleted: FCLKIN is the input clock frequency.	2-10
	In Table 2-14 · Summary of Maximum and Minimum DC Input Levels, the note was incorrect. It previously said T_J and it was corrected and changed to T_A.	2-17
	In Table 2-94 · ProASIC3E CCC/PLL Specification, the SCLK parameter and note 1 are new.	2-68
	Table 2-99 · JTAG 1532 was populated with the parameter data, which was not in the previous version of the document.	2-82
v2.1 (July 2007)	This document was previously in datasheet v2.1. As a result of moving to the handbook format, Actel has restarted the version numbers so the new version number is v1.0.	N/A
v2.0 (April 2007)	The caption "Main (chip)" in Figure 2-9 • Overview of Automotive ProASIC3 VersaNet Global Network was changed to "Chip (main)."	2-9
	The T_J parameter in Table 3-2 • Recommended Operating Conditions was changed to T_A, ambient temperature, and table notes 4–6 were added.	3-2
	The "PLL Macro" section was updated to add information on the VCO and PLL outputs during power-up.	2-15
Advance v0.6 (January 2007)	The "PLL Macro" section was updated to include power-up information.	2-15
	Table 2-13 • ProASIC3E CCC/PLL Specification was updated.	2-30
	Figure 2-19 • Peak-to-Peak Jitter Definition is new.	2-18
	The "SRAM and FIFO" section was updated with operation and timing requirement information.	2-21
	The "RESET" section was updated with read and write information.	2-25
	The "RESET" section was updated with read and write information.	2-25
	The "Introduction" in the "Advanced I/Os" section was updated to include information on input and output buffers being disabled.	2-28
	In the Table 2-15 • Levels of Hot-Swap Support, the ProASIC3 compliance descriptions were updated for levels 3 and 4.	2-34

Previous Version	Changes in Current Version (v1.2)	Page
Advance v0.6 (continued)	Table 2-45 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices was updated.	2-64
	Notes 3, 4, and 5 were added to Table 2-17 • Comparison Table for 5 V–Compliant Receiver Scheme. 5 x 52.72 was changed to 52.7 and the Maximum current was updated from 4 x 52.7 to 5 x 52.7.	2-40
	The "V_{CCPLF} PLL Supply Voltage" section was updated.	2-50
	The "V_{PUMP} Programming Supply Voltage" section was updated.	2-50
	The "GL Globals" section was updated to include information about direct input into quadrant clocks.	2-51
	V_{JTAG} was deleted from the "TCK Test Clock" section.	2-51
	In Table 2-22 • Recommended Tie-Off Values for the TCK and TRST Pins, TSK was changed to TCK in note 2. Note 3 was also updated.	2-51
	Ambient was deleted from Table 3-2 • Recommended Operating Conditions. V_{PUMP} programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45".	3-2
	Note 3 is new in Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os).	3-2
	In EQ 3-2, 150 was changed to 110 and the result changed to 5.88.	3-5
	Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays was updated.	3-5
	Table 3-5 • Package Thermal Resistivities was updated.	3-5
	Table 3-10 • Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices was updated.	3-8
	t_{WRO} and t_{CCKH} were added to Table 3-94 • RAM4K9 and Table 3-95 • RAM512X18.	3-74 to 3-74
	The note in Table 3-24 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated.	3-23
	Figure 3-43 • Write Access After Write onto Same Address, Figure 3-44 • Read Access After Write onto Same Address, and Figure 3-45 • Write Access After Read onto Same Address are new.	3-71 to 3-73
	Figure 3-53 • Timing Diagram was updated.	3-80
Advance v0.4 (October 2005)	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-8 • Very-Long-Line Resources was updated.	2-8
	The footnotes in Figure 2-27 • CCC/PLL Macro were updated.	2-28
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21
	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25
	The "RESET" section was updated.	2-25
	The "RESET" section was updated.	2-27
	The "Introduction" of the "Introduction" section was updated.	2-28

Previous Version	Changes in Current Version (v1.2)	Page
Advance v0.4 (continued)	PCI-X 3.3 V was added to the Compatible Standards for 3.3 V in Table 2-11 • VCCI Voltages and Compatible Standards	2-29
	Table 2-35 • ProASIC3E I/O Features was updated.	2-54
	The "Double Data Rate (DDR) Support" section was updated to include information concerning implementation of the feature.	2-32
	The "Electrostatic Discharge (ESD) Protection" section was updated to include testing information.	2-35
	Level 3 and 4 descriptions were updated in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices.	2-64
	The notes in Table 2-45 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices were updated.	2-64
	The "Simultaneous Switching Outputs (SSOs) and Printed Circuit Board Layout" section is new.	2-41
	A footnote was added to Table 2-37 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in ProASIC3E Devices (maximum drive strength and high slew selected).	2-55
	Table 2-48 • ProASIC3E I/O Attributes vs. I/O Standard Applications	2-81
	Table 2-55 • ProASIC3 I/O Standards—SLEW and Output Drive (OUT_DRIVE) Settings	2-85
	The "x" was updated in the "Pin Descriptions" section.	2-50
	The "V_{CC} Core Supply Voltage" pin description was updated.	2-50
	The "VMVx I/O Supply Voltage (quiet)" pin description was updated to include information concerning leaving the pin unconnected.	2-50
	EXTFB was removed from Figure 2-24 • ProASIC3E CCC Options.	2-24
	The CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} was updated in Table 2-13 • ProASIC3E CCC/PLL Specification.	2-30
	EXTFB was removed from Figure 2-27 • CCC/PLL Macro.	2-28
	The LVPECL specification in Table 2-45 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3E Devices was updated.	2-64
	Table 2-15 • Levels of Hot-Swap Support was updated.	2-34
	The "Cold-Sparing Support" section was updated.	2-34
	"Electrostatic Discharge (ESD) Protection" section was updated.	2-35
	The VJTAG and I/O pin descriptions were updated in the "Pin Descriptions" section.	2-50
	The "VJTAG JTAG Supply Voltage" pin description was updated.	2-50
	The "V_{PUMP} Programming Supply Voltage" pin description was updated to include information on what happens when the pin is tied to ground.	2-50
	The "I/O User Input/Output" pin description was updated to include information on what happens when the pin is unused.	2-50
	The "JTAG Pins" section was updated to include information on what happens when the pin is unused.	2-51
	The "Programming" section was updated to include information concerning serialization.	2-53
	The "JTAG 1532" section was updated to include SAMPLE/PRELOAD information.	2-54

Previous Version	Changes in Current Version (v1.2)	Page
Advance v0.4 (continued)	The "DC and Switching Characteristics" chapter was updated with new information.	Starting on page 3-1
	Table 3-6 was updated.	3-5
	In Table 3-10, PAC4 was updated.	3-8
	Table 3-19 was updated.	3-20
	The note in Table 3-24 was updated.	3-23
	All Timing Characteristics tables were updated from LVTTL to Register Delays	3-26 to 3-64
	The Timing Characteristics for RAM4K9, RAM512X18, and FIFO were updated.	3-74 to 3-79
	F_{TCKMAX} was updated in Table 3-98.	3-80
Advance v0.2	Figure 2-11 was updated.	2-9
	The "Clock Resources (VersaNets)" section was updated.	2-9
	The "VersaNet Global Networks and Spine Access" section was updated.	2-9
	The "PLL Macro" section was updated.	2-15
	Figure 2-27 was updated.	2-28
	Figure 2-20 was updated.	2-19
	Table 2-5 was updated.	2-25
	Table 2-6 was updated.	2-25
	The "FIFO Flag Usage Considerations" section was updated.	2-27
	Table 2-33 was updated.	2-51
	Figure 2-24 was updated.	2-31
	The "Cold-Sparing Support" section is new.	2-34
	Table 2-45 was updated.	2-64
	Table 2-48 was updated.	2-81
	Pin descriptions in the "JTAG Pins" section were updated.	2-51
	The "Pin Descriptions" section was updated.	2-50
	Table 3-7 was updated.	3-6
	The "Methodology" section was updated.	3-9

Actel Safety Critical, Life Support, and High-Reliability Applications Policy

The Actel products described in this advance status datasheet may not have completed Actel's qualification process. Actel may amend or enhance products during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any Actel product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult Actel's Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of Actel's products is available on the Actel website at http://www.actel.com/documents/ORT_Report.pdf. Actel also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local Actel sales office for additional reliability information.

3 – Package Pin Assignments

208-Pin PQFP
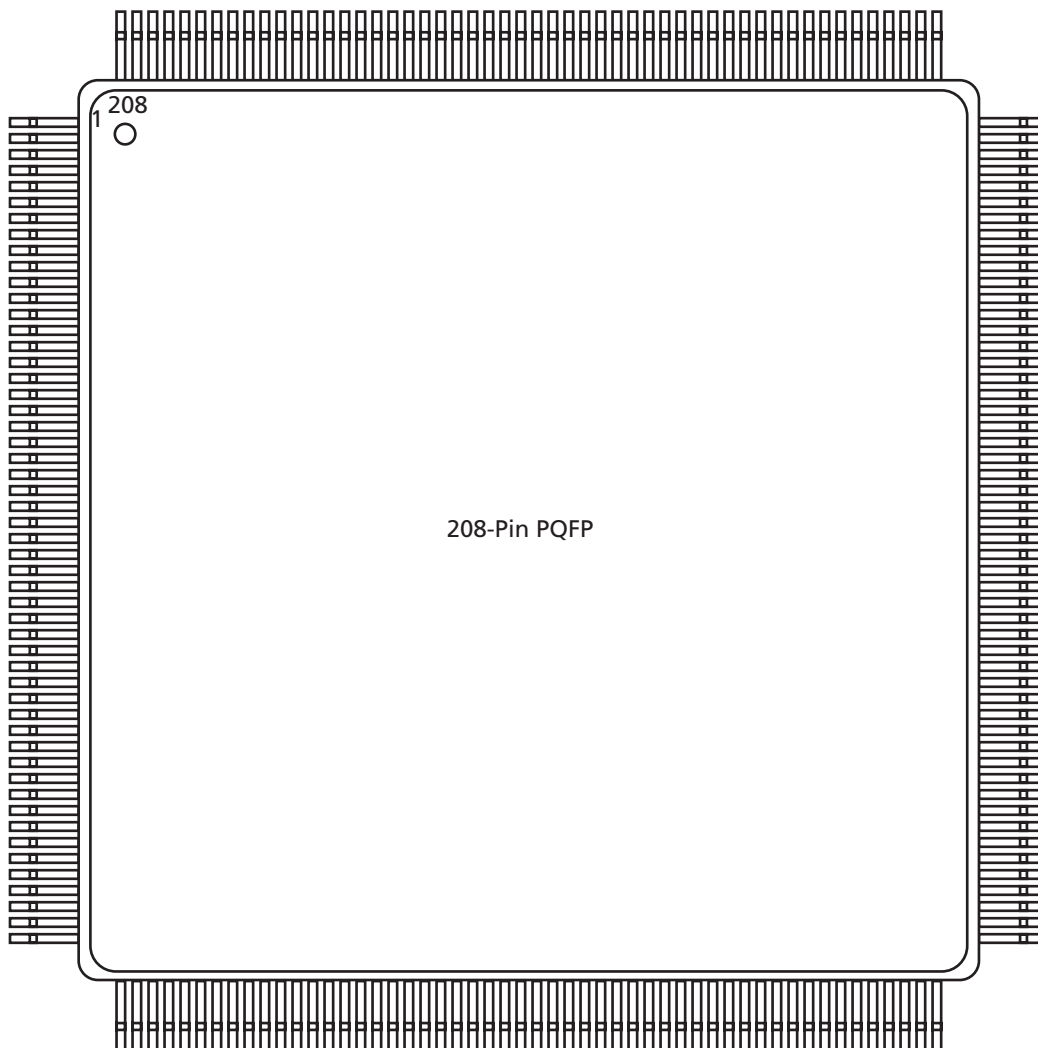
Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.actel.com/products/solutions/package/docs.aspx.

208-Pin PQFP	
Pin Number	A3PE600 Function
1	GND
2	GNDQ
3	VMV7
4	GAB2/IO133PSB7V1
5	GAA2/IO134PDB7V1
6	IO134NDB7V1
7	GAC2/IO132PDB7V1
8	IO132NDB7V1
9	IO130PDB7V1
10	IO130NDB7V1
11	IO127PDB7V1
12	IO127NDB7V1
13	IO126PDB7V0
14	IO126NDB7V0
15	IO124PSB7V0
16	V_{CC}
17	GND
18	$V_{CCI}B7$
19	IO122PPB7V0
20	IO121PSB7V0
21	IO122NPB7V0
22	GFC1/IO120PSB7V0
23	GFB1/IO119PDB7V0
24	GFB0/IO119NDB7V0
25	V_{COMPLF}
26	GFA0/IO118NPB6V1
27	V_{CCPLF}
28	GFA1/IO118PPB6V1
29	GND
30	GFA2/IO117PDB6V1
31	IO117NDB6V1
32	GFB2/IO116PPB6V1
33	GFC2/IO115PPB6V1
34	IO116NPB6V1
35	IO115NPB6V1
36	V_{CC}

208-Pin PQFP	
Pin Number	A3PE600 Function
37	IO112PDB6V1
38	IO112NDB6V1
39	IO108PSB6V0
40	$V_{CCI}B6$
41	GND
42	IO106PDB6V0
43	IO106NDB6V0
44	GEC1/IO104PDB6V0
45	GEC0/IO104NDB6V0
46	GEB1/IO103PPB6V0
47	GEA1/IO102PPB6V0
48	GEB0/IO103NPB6V0
49	GEA0/IO102NPB6V0
50	VMV6
51	GNDQ
52	GND
53	VMV5
54	GNDQ
55	IO101NDB5V2
56	GEA2/IO101PDB5V2
57	IO100NDB5V2
58	GEB2/IO100PDB5V2
59	IO99NDB5V2
60	GEC2/IO99PDB5V2
61	IO98PSB5V2
62	$V_{CCI}B5$
63	IO96PSB5V2
64	IO94NDB5V1
65	GND
66	IO94PDB5V1
67	IO92NDB5V1
68	IO92PDB5V1
69	IO88NDB5V0
70	IO88PDB5V0
71	V_{CC}
72	$V_{CCI}B5$

208-Pin PQFP	
Pin Number	A3PE600 Function
73	IO85NPB5V0
74	IO84NPB5V0
75	IO85PPB5V0
76	IO84PPB5V0
77	IO83NPB5V0
78	IO82NPB5V0
79	IO83PPB5V0
80	IO82PPB5V0
81	GND
82	IO80NDB4V1
83	IO80PDB4V1
84	IO79NPB4V1
85	IO78NPB4V1
86	IO79PPB4V1
87	IO78PPB4V1
88	V_{CC}
89	$V_{CCI}B4$
90	IO76NDB4V1
91	IO76PDB4V1
92	IO72NDB4V0
93	IO72PDB4V0
94	IO70NDB4V0
95	GDC2/IO70PDB4V0
96	IO68NDB4V0
97	GND
98	GDA2/IO68PDB4V0
99	GDB2/IO69PSB4V0
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV4
105	GND
106	V_{PUMP}
107	GNDQ
108	TDO

208-Pin PQFP		208-Pin PQFP		208-Pin PQFP	
Pin Number	A3PE600 Function	Pin Number	A3PE600 Function	Pin Number	A3PE600 Function
109	TRST	145	IO44NDB2V1	181	IO18NPB0V2
110	V$_{JTAG}$	146	IO44PDB2V1	182	IO17PPB0V2
111	VMV3	147	IO43NDB2V0	183	IO16PPB0V2
112	GDA0/IO67NPB3V1	148	IO43PDB2V0	184	IO17NPB0V2
113	GDB0/IO66NPB3V1	149	IO40NDB2V0	185	IO16NPB0V2
114	GDA1/IO67PPB3V1	150	IO40PDB2V0	186	V$_{CCI}$B0
115	GDB1/IO66PPB3V1	151	GBC2/IO38PSB2V0	187	V$_{CC}$
116	GDC0/IO65NDB3V1	152	GBA2/IO36PSB2V0	188	IO15PDB0V2
117	GDC1/IO65PDB3V1	153	GBB2/IO37PSB2V0	189	IO15NDB0V2
118	IO62NDB3V1	154	VMV2	190	IO13PDB0V2
119	IO62PDB3V1	155	GNDQ	191	IO13NDB0V2
120	IO58NDB3V0	156	GND	192	IO11PSB0V1
121	IO58PDB3V0	157	VMV1	193	IO09PDB0V1
122	GND	158	GNDQ	194	IO09NDB0V1
123	V$_{CCI}$B3	159	GBA1/IO35PDB1V1	195	GND
124	GCC2/IO55PSB3V0	160	GBA0/IO35NDB1V1	196	IO07PDB0V1
125	GCB2/IO54PSB3V0	161	GBB1/IO34PDB1V1	197	IO07NDB0V1
126	NC	162	GND	198	IO05PDB0V0
127	IO53NDB3V0	163	GBB0/IO34NDB1V1	199	IO05NDB0V0
128	GCA2/IO53PDB3V0	164	GBC1/IO33PDB1V1	200	V$_{CCI}$B0
129	GCA1/IO52PPB3V0	165	GBC0/IO33NDB1V1	201	GAC1/IO02PDB0V0
130	GND	166	IO31PDB1V1	202	GAC0/IO02NDB0V0
131	V$_{CCPLC}$	167	IO31NDB1V1	203	GAB1/IO01PDB0V0
132	GCA0/IO52NPB3V0	168	IO27PDB1V0	204	GAB0/IO01NDB0V0
133	V$_{COMPLC}$	169	IO27NDB1V0	205	GAA1/IO00PDB0V0
134	GCB0/IO51NDB2V1	170	V$_{CCI}$B1	206	GAA0/IO00NDB0V0
135	GCB1/IO51PDB2V1	171	V$_{CC}$	207	GNDQ
136	GCC1/IO50PSB2V1	172	IO23PPB1V0	208	VMV0
137	IO49NDB2V1	173	IO22PSB1V0		
138	IO49PDB2V1	174	IO23NPB1V0		
139	IO48PSB2V1	175	IO21PDB1V0		
140	V$_{CCI}$B2	176	IO21NDB1V0		
141	GND	177	IO19PPB0V2		
142	V$_{CC}$	178	GND		
143	IO47NDB2V1	179	IO18PPB0V2		
144	IO47PDB2V1	180	IO19NPB0V2		

208-Pin PQFP		208-Pin PQFP		208-Pin PQFP	
Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function
1	GND	37	IO184PDB6V2	73	IO145NDB5V1
2	GNDQ	38	IO184NDB6V2	74	IO145PDB5V1
3	VMV7	39	IO180PSB6V1	75	IO143NDB5V1
4	GAB2/IO220PSB7V3	40	$V_{CCI}B6$	76	IO143PDB5V1
5	GAA2/IO221PDB7V3	41	GND	77	IO137NDB5V0
6	IO221NDB7V3	42	IO176PDB6V1	78	IO137PDB5V0
7	GAC2/IO219PDB7V3	43	IO176NDB6V1	79	IO135NDB5V0
8	IO219NDB7V3	44	GEC1/IO169PDB6V0	80	IO135PDB5V0
9	IO215PDB7V3	45	GEC0/IO169NDB6V0	81	GND
10	IO215NDB7V3	46	GEB1/IO168PPB6V0	82	IO131NDB4V2
11	IO212PDB7V2	47	GEA1/IO167PPB6V0	83	IO131PDB4V2
12	IO212NDB7V2	48	GEB0/IO168NPB6V0	84	IO129NDB4V2
13	IO208PDB7V2	49	GEA0/IO167NPB6V0	85	IO129PDB4V2
14	IO208NDB7V2	50	VMV6	86	IO127NDB4V2
15	IO204PSB7V1	51	GNDQ	87	IO127PDB4V2
16	V_{CC}	52	GND	88	V_{CC}
17	GND	53	VMV5	89	$V_{CCI}B4$
18	$V_{CCI}B7$	54	GNDQ	90	IO121NDB4V1
19	IO200PDB7V1	55	IO166NDB5V3	91	IO121PDB4V1
20	IO200NDB7V1	56	GEA2/IO166PDB5V3	92	IO119NDB4V1
21	IO196PSB7V0	57	IO165NDB5V3	93	IO119PDB4V1
22	GFC1/IO192PSB7V0	58	GEB2/IO165PDB5V3	94	IO113NDB4V0
23	GFB1/IO191PDB7V0	59	IO164NDB5V3	95	GDC2/IO113PDB4V0
24	GFB0/IO191NDB7V0	60	GEC2/IO164PDB5V3	96	IO112NDB4V0
25	V_{COMPLF}	61	IO163PSB5V3	97	GND
26	GFA0/IO190NPB6V2	62	$V_{CCI}B5$	98	GDB2/IO112PDB4V0
27	V_{CCPLF}	63	IO161PSB5V3	99	GDA2/IO111PSB4V0
28	GFA1/IO190PPB6V2	64	IO157NDB5V2	100	GNDQ
29	GND	65	GND	101	TCK
30	GFA2/IO189PDB6V2	66	IO157PDB5V2	102	TDI
31	IO189NDB6V2	67	IO153NDB5V2	103	TMS
32	GFB2/IO188PPB6V2	68	IO153PDB5V2	104	VMV4
33	GFC2/IO187PPB6V2	69	IO149NDB5V1	105	GND
34	IO188NPB6V2	70	IO149PDB5V1	106	V_{PUMP}
35	IO187NPB6V2	71	V_{CC}	107	GNDQ
36	V_{CC}	72	$V_{CCI}B5$	108	TDO

208-Pin PQFP	
Pin Number	A3PE1500 Function
109	TRST
110	V$_{JTAG}$
111	VMV3
112	GDA0/IO110NPB3V2
113	GDB0/IO109NPB3V2
114	GDA1/IO110PPB3V2
115	GDB1/IO109PPB3V2
116	GDC0/IO108NDB3V2
117	GDC1/IO108PDB3V2
118	IO105NDB3V2
119	IO105PDB3V2
120	IO101NDB3V1
121	IO101PDB3V1
122	GND
123	V$_{CCI}$B3
124	GCC2/IO90PSB3V0
125	GCB2/IO89PSB3V0
126	NC
127	IO88NDB3V0
128	GCA2/IO88PDB3V0
129	GCA1/IO87PPB3V0
130	GND
131	V$_{CCPLC}$
132	GCA0/IO87NPB3V0
133	V$_{COMPLC}$
134	GCB0/IO86NDB2V3
135	GCB1/IO86PDB2V3
136	GCC1/IO85PSB2V3
137	IO83NDB2V3
138	IO83PDB2V3
139	IO81PSB2V3
140	V$_{CCI}$B2
141	GND
142	V$_{CC}$
143	IO73NDB2V2
144	IO73PDB2V2

208-Pin PQFP	
Pin Number	A3PE1500 Function
145	IO71NDB2V2
146	IO71PDB2V2
147	IO67NDB2V1
148	IO67PDB2V1
149	IO65NDB2V1
150	IO65PDB2V1
151	GBC2/IO60PSB2V0
152	GBA2/IO58PSB2V0
153	GBB2/IO59PSB2V0
154	VMV2
155	GNDQ
156	GND
157	VMV1
158	GNDQ
159	GBA1/IO57PDB1V3
160	GBA0/IO57NDB1V3
161	GBB1/IO56PDB1V3
162	GND
163	GBB0/IO56NDB1V3
164	GBC1/IO55PDB1V3
165	GBC0/IO55NDB1V3
166	IO51PDB1V2
167	IO51NDB1V2
168	IO47PDB1V1
169	IO47NDB1V1
170	V$_{CCI}$B1
171	V$_{CC}$
172	IO43PSB1V1
173	IO41PDB1V1
174	IO41NDB1V1
175	IO35PDB1V0
176	IO35NDB1V0
177	IO31PDB0V3
178	GND
179	IO31NDB0V3
180	IO29PDB0V3

208-Pin PQFP	
Pin Number	A3PE1500 Function
181	IO29NDB0V3
182	IO27PDB0V3
183	IO27NDB0V3
184	IO23PDB0V2
185	IO23NDB0V2
186	V$_{CCI}$B0
187	V$_{CC}$
188	IO18PDB0V2
189	IO18NDB0V2
190	IO15PDB0V1
191	IO15NDB0V1
192	IO12PSB0V1
193	IO11PDB0V1
194	IO11NDB0V1
195	GND
196	IO08PDB0V1
197	IO08NDB0V1
198	IO05PDB0V0
199	IO05NDB0V0
200	V$_{CCI}$B0
201	GAC1/IO02PDB0V0
202	GAC0/IO02NDB0V0
203	GAB1/IO01PDB0V0
204	GAB0/IO01NDB0V0
205	GAA1/IO00PDB0V0
206	GAA0/IO00NDB0V0
207	GNDQ
208	VMV0

208-Pin PQFP		208-Pin PQFP		208-Pin PQFP	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
1	GND	40	$V_{CCI}B6$	79	IO194NDB5V0
2	GNDQ	41	GND	80	IO194PDB5V0
3	VMV7	42	IO244PDB6V1	81	GND
4	GAB2/IO308PSB7V4	43	IO244NDB6V1	82	IO184NDB4V3
5	GAA2/IO309PDB7V4	44	GEC1/IO236PDB6V0	83	IO184PDB4V3
6	IO309NDB7V4	45	GEC0/IO236NDB6V0	84	IO180NDB4V3
7	GAC2/IO307PDB7V4	46	GEB1/IO235PPB6V0	85	IO180PDB4V3
8	IO307NDB7V4	47	GEA1/IO234PPB6V0	86	IO176NDB4V2
9	IO303PDB7V3	48	GEB0/IO235NPB6V0	87	IO176PDB4V2
10	IO303NDB7V3	49	GEA0/IO234NPB6V0	88	V_{CC}
11	IO299PDB7V3	50	VMV6	89	$V_{CCI}B4$
12	IO299NDB7V3	51	GNDQ	90	IO170NDB4V2
13	IO295PDB7V2	52	GND	91	IO170PDB4V2
14	IO295NDB7V2	53	VMV5	92	IO166NDB4V1
15	IO291PSB7V2	54	GNDQ	93	IO166PDB4V1
16	V_{CC}	55	IO233NDB5V4	94	IO156NDB4V0
17	GND	56	GEA2/IO233PDB5V4	95	GDC2/IO156PDB4V0
18	$V_{CCI}B7$	57	IO232NDB5V4	96	IO154NPB4V0
19	IO285PDB7V1	58	GEB2/IO232PDB5V4	97	GND
20	IO285NDB7V1	59	IO231NDB5V4	98	GDB2/IO155PSB4V0
21	IO279PSB7V0	60	GEC2/IO231PDB5V4	99	GDA2/IO154PPB4V0
22	GFC1/IO275PSB7V0	61	IO230PSB5V4	100	GNDQ
23	GFB1/IO274PDB7V0	62	$V_{CCI}B5$	101	TCK
24	GFB0/IO274NDB7V0	63	IO218NDB5V3	102	TDI
25	V_{COMPLF}	64	IO218PDB5V3	103	TMS
26	GFA0/IO273NPB6V4	65	GND	104	VMV4
27	V_{CCPLF}	66	IO214PSB5V2	105	GND
28	GFA1/IO273PPB6V4	67	IO212NDB5V2	106	V_{PUMP}
29	GND	68	IO212PDB5V2	107	GNDQ
30	GFA2/IO272PDB6V4	69	IO208NDB5V1	108	TDO
31	IO272NDB6V4	70	IO208PDB5V1	109	TRST
32	GFB2/IO271PPB6V4	71	V_{CC}	110	V_{JTAG}
33	GFC2/IO270PPB6V4	72	$V_{CCI}B5$	111	VMV3
34	IO271NPB6V4	73	IO202NDB5V1	112	GDA0/IO153NPB3V4
35	IO270NPB6V4	74	IO202PDB5V1	113	GDB0/IO152NPB3V4
36	V_{CC}	75	IO198NDB5V0	114	GDA1/IO153PPB3V4
37	IO252PDB6V2	76	IO198PDB5V0	115	GDB1/IO152PPB3V4
38	IO252NDB6V2	77	IO197NDB5V0	116	GDC0/IO151NDB3V4
39	IO248PSB6V1	78	IO197PDB5V0		

208-Pin PQFP	
Pin Number	A3PE3000 Function
117	GDC1/IO151PDB3V4
118	IO134NDB3V2
119	IO134PDB3V2
120	IO132NDB3V2
121	IO132PDB3V2
122	GND
123	V$_{CCI}$B3
124	GCC2/IO117PSB3V0
125	GCB2/IO116PSB3V0
126	NC
127	IO115NDB3V0
128	GCA2/IO115PDB3V0
129	GCA1/IO114PPB3V0
130	GND
131	V$_{CCPLC}$
132	GCA0/IO114NPB3V0
133	V$_{COMPLC}$
134	GCB0/IO113NDB2V3
135	GCB1/IO113PDB2V3
136	GCC1/IO112PSB2V3
137	IO110NDB2V3
138	IO110PDB2V3
139	IO106PSB2V3
140	V$_{CCI}$B2
141	GND
142	V$_{CC}$
143	IO99NDB2V2
144	IO99PDB2V2
145	IO96NDB2V1
146	IO96PDB2V1
147	IO91NDB2V1
148	IO91PDB2V1
149	IO88NDB2V0
150	IO88PDB2V0
151	GBC2/IO84PSB2V0
152	GBA2/IO82PSB2V0
153	GBB2/IO83PSB2V0
154	VMV2
155	GNDQ

208-Pin PQFP	
Pin Number	A3PE3000 Function
156	GND
157	VMV1
158	GNDQ
159	GBA1/IO81PDB1V4
160	GBA0/IO81NDB1V4
161	GBB1/IO80PDB1V4
162	GND
163	GBB0/IO80NDB1V4
164	GBC1/IO79PDB1V4
165	GBC0/IO79NDB1V4
166	IO74PDB1V4
167	IO74NDB1V4
168	IO70PDB1V3
169	IO70NDB1V3
170	V$_{CCI}$B1
171	V$_{CC}$
172	IO56PSB1V1
173	IO55PDB1V1
174	IO55NDB1V1
175	IO54PDB1V1
176	IO54NDB1V1
177	IO40PDB0V4
178	GND
179	IO40NDB0V4
180	IO37PDB0V4
181	IO37NDB0V4
182	IO35PDB0V4
183	IO35NDB0V4
184	IO32PDB0V3
185	IO32NDB0V3
186	V$_{CCI}$B0
187	V$_{CC}$
188	IO28PDB0V3
189	IO28NDB0V3
190	IO24PDB0V2
191	IO24NDB0V2
192	IO21PSB0V2
193	IO16PDB0V1
194	IO16NDB0V1

208-Pin PQFP	
Pin Number	A3PE3000 Function
195	GND
196	IO11PDB0V1
197	IO11NDB0V1
198	IO08PDB0V0
199	IO08NDB0V0
200	V$_{CCI}$B0
201	GAC1/IO02PDB0V0
202	GAC0/IO02NDB0V0
203	GAB1/IO01PDB0V0
204	GAB0/IO01NDB0V0
205	GAA1/IO00PDB0V0
206	GAA0/IO00NDB0V0
207	GNDQ
208	VMV0

256-Pin FBGA
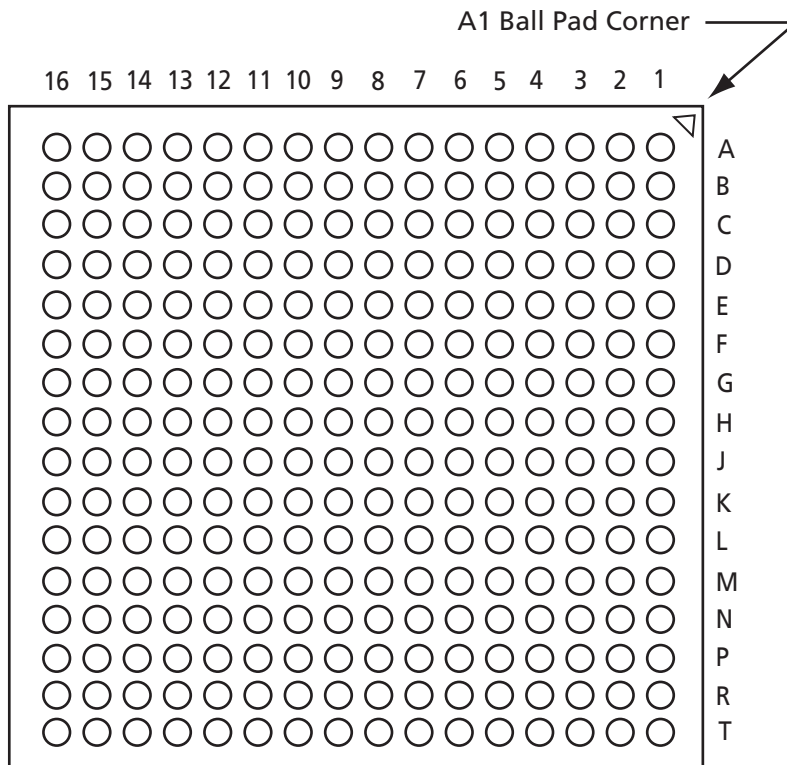
A1 Ball Pad Corner

16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

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Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.actel.com/products/solutions/package/docs.aspx.

256-Pin FBGA	
Pin Number	A3PE600 Function
A1	GND
A2	GAA0/IO00NDB0V0
A3	GAA1/IO00PDB0V0
A4	GAB0/IO01NDB0V0
A5	IO05PDB0V0
A6	IO10PDB0V1
A7	IO12PDB0V2
A8	IO16NDB0V2
A9	IO23NDB1V0
A10	IO23PDB1V0
A11	IO28NDB1V1
A12	IO28PDB1V1
A13	GBB1/IO34PDB1V1
A14	GBA0/IO35NDB1V1
A15	GBA1/IO35PDB1V1
A16	GND
B1	GAB2/IO133PDB7V1
B2	GAA2/IO134PDB7V1
B3	GNDQ
B4	GAB1/IO01PDB0V0
B5	IO05NDB0V0
B6	IO10NDB0V1
B7	IO12NDB0V2
B8	IO16PDB0V2
B9	IO20NDB1V0
B10	IO24NDB1V0
B11	IO24PDB1V0
B12	GBC1/IO33PDB1V1
B13	GBB0/IO34NDB1V1
B14	GNDQ
B15	GBA2/IO36PDB2V0
B16	IO42NDB2V0
C1	IO133NDB7V1
C2	IO134NDB7V1
C3	VMV7
C4	V_{CCPLA}

256-Pin FBGA	
Pin Number	A3PE600 Function
C5	GAC0/IO02NDB0V0
C6	GAC1/IO02PDB0V0
C7	IO15NDB0V2
C8	IO15PDB0V2
C9	IO20PDB1V0
C10	IO25NDB1V0
C11	IO27PDB1V0
C12	GBC0/IO33NDB1V1
C13	V_{CCPLB}
C14	VMV2
C15	IO36NDB2V0
C16	IO42PDB2V0
D1	IO128PDB7V1
D2	IO129PDB7V1
D3	GAC2/IO132PDB7V1
D4	V_{COMPLA}
D5	GNDQ
D6	IO09NDB0V1
D7	IO09PDB0V1
D8	IO13PDB0V2
D9	IO21PDB1V0
D10	IO25PDB1V0
D11	IO27NDB1V0
D12	GNDQ
D13	V_{COMPLB}
D14	GBB2/IO37PDB2V0
D15	IO39PDB2V0
D16	IO39NDB2V0
E1	IO128NDB7V1
E2	IO129NDB7V1
E3	IO132NDB7V1
E4	IO130PDB7V1
E5	VMV0
E6	VvB0
E7	$V_{CCI}B0$
E8	IO13NDB0V2

256-Pin FBGA	
Pin Number	A3PE600 Function
E9	IO21NDB1V0
E10	$V_{CCI}B1$
E11	$V_{CCI}B1$
E12	VMV1
E13	GBC2/IO38PDB2V0
E14	IO37NDB2V0
E15	IO41NDB2V0
E16	IO41PDB2V0
F1	IO124PDB7V0
F2	IO125PDB7V0
F3	IO126PDB7V0
F4	IO130NDB7V1
F5	$V_{CCI}B7$
F6	GND
F7	V_{CC}
F8	V_{CC}
F9	V_{CC}
F10	V_{CC}
F11	GND
F12	$V_{CCI}B2$
F13	IO38NDB2V0
F14	IO40NDB2V0
F15	IO40PDB2V0
F16	IO45PSB2V1
G1	IO124NDB7V0
G2	IO125NDB7V0
G3	IO126NDB7V0
G4	GFC1/IO120PPB7V0
G5	$V_{CCI}B7$
G6	V_{CC}
G7	GND
G8	GND
G9	GND
G10	GND
G11	V_{CC}
G12	$V_{CCI}B2$

256-Pin FBGA	
Pin Number	A3PE600 Function
G13	GCC1/IO50PPB2V1
G14	IO44NDB2V1
G15	IO44PDB2V1
G16	IO49NSB2V1
H1	GFB0/IO119NPB7V0
H2	GFA0/IO118NDB6V1
H3	GFB1/IO119PPB7V0
H4	V_{COMPLF}
H5	GFC0/IO120NPB7V0
H6	V_{CC}
H7	GND
H8	GND
H9	GND
H10	GND
H11	V_{CC}
H12	GCC0/IO50NPB2V1
H13	GCB1/IO51PPB2V1
H14	GCA0/IO52NPB3V0
H15	V_{COMPLC}
H16	GCB0/IO51NPB2V1
J1	GFA2/IO117PSB6V1
J2	GFA1/IO118PDB6V1
J3	V_{CCPLF}
J4	IO116NDB6V1
J5	GFB2/IO116PDB6V1
J6	V_{CC}
J7	GND
J8	GND
J9	GND
J10	GND
J11	V_{CC}
J12	GCB2/IO54PPB3V0
J13	GCA1/IO52PPB3V0
J14	GCC2/IO55PPB3V0
J15	V_{CCPLC}
J16	GCA2/IO53PSB3V0

256-Pin FBGA	
Pin Number	A3PE600 Function
K1	GFC2/IO115PSB6V1
K2	IO113PPB6V1
K3	IO112PDB6V1
K4	IO112NDB6V1
K5	$V_{CCI}B6$
K6	V_{CC}
K7	GND
K8	GND
K9	GND
K10	GND
K11	V_{CC}
K12	$V_{CCI}B3$
K13	IO54NPB3V0
K14	IO57NPB3V0
K15	IO55NPB3V0
K16	IO57PPB3V0
L1	IO113NPB6V1
L2	IO109PPB6V0
L3	IO108PDB6V0
L4	IO108NDB6V0
L5	$V_{CCI}B6$
L6	GND
L7	V_{CC}
L8	V_{CC}
L9	V_{CC}
L10	V_{CC}
L11	GND
L12	$V_{CCI}B3$
L13	GDB0/IO66NPB3V1
L14	IO60NDB3V1
L15	IO60PDB3V1
L16	IO61PDB3V1
M1	IO109NPB6V0
M2	IO106NDB6V0
M3	IO106PDB6V0
M4	GEC0/IO104NPB6V0

256-Pin FBGA	
Pin Number	A3PE600 Function
M5	VMV5
M6	$V_{CCI}B5$
M7	$V_{CCI}B5$
M8	IO84NDB5V0
M9	IO84PDB5V0
M10	$V_{CCI}B4$
M11	$V_{CCI}B4$
M12	VMV3
M13	V_{CCPLD}
M14	GDB1/IO66PPB3V1
M15	GDC1/IO65PDB3V1
M16	IO61NDB3V1
N1	IO105PDB6V0
N2	IO105NDB6V0
N3	GEC1/IO104PPB6V0
N4	V_{COMPLE}
N5	GNDQ
N6	GEA2/IO101PPB5V2
N7	IO92NDB5V1
N8	IO90NDB5V1
N9	IO82NDB5V0
N10	IO74NDB4V1
N11	IO74PDB4V1
N12	GNDQ
N13	V_{COMPLD}
N14	V_{JTAG}
N15	GDC0/IO65NDB3V1
N16	GDA1/IO67PDB3V1
P1	GEB1/IO103PDB6V0
P2	GEB0/IO103NDB6V0
P3	VMV6
P4	V_{CCPLE}
P5	IO101NPB5V2
P6	IO95PPB5V1
P7	IO92PDB5V1
P8	IO90PDB5V1

256-Pin FBGA	
Pin Number	A3PE600 Function
P9	IO82PDB5V0
P10	IO76NDB4V1
P11	IO76PDB4V1
P12	VMV4
P13	TCK
P14	V$_{PUMP}$
P15	TRST
P16	GDA0/IO67NDB3V1
R1	GEA1/IO102PDB6V0
R2	GEA0/IO102NDB6V0
R3	GNDQ
R4	GEC2/IO99PDB5V2
R5	IO95NPB5V1
R6	IO91NDB5V1
R7	IO91PDB5V1
R8	IO83NDB5V0
R9	IO83PDB5V0
R10	IO77NDB4V1
R11	IO77PDB4V1
R12	IO69NDB4V0
R13	GDB2/IO69PDB4V0
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO100NDB5V2
T3	GEB2/IO100PDB5V2
T4	IO99NDB5V2
T5	IO88NDB5V0
T6	IO88PDB5V0
T7	IO89NSB5V0
T8	IO80NSB4V1
T9	IO81NDB4V1
T10	IO81PDB4V1
T11	IO70NDB4V0
T12	GDC2/IO70PDB4V0

256-Pin FBGA	
Pin Number	A3PE600 Function
T13	IO68NDB4V0
T14	GDA2/IO68PDB4V0
T15	TMS
T16	GND

324-Pin FBGA
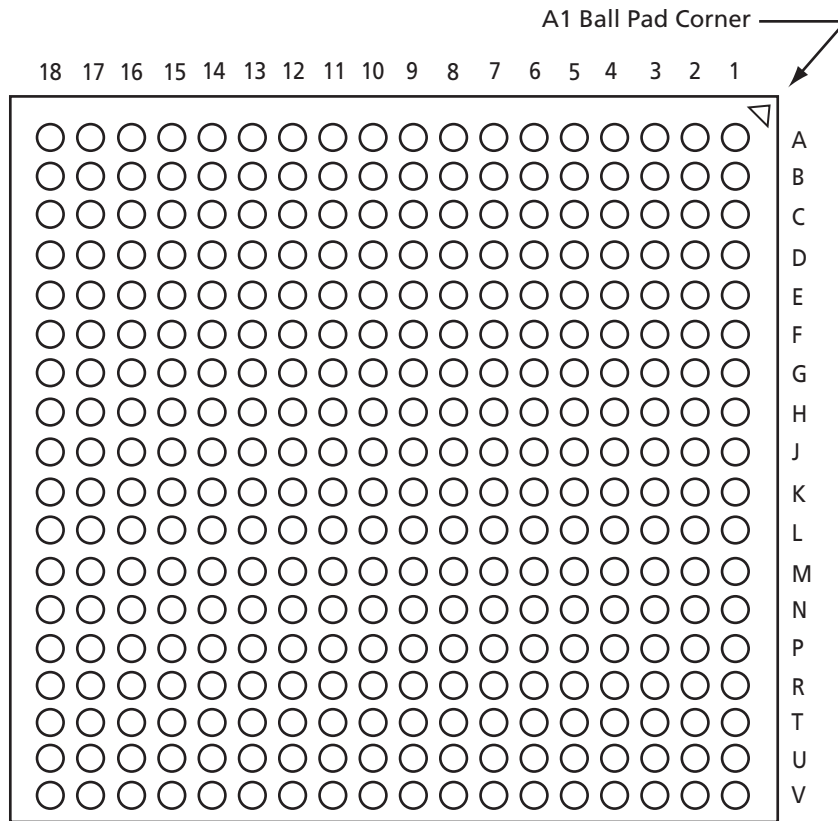
A1 Ball Pad Corner ⎯⎯⎯

Note: *This is the bottom view of the package.*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.actel.com/products/solutions/package/docs.aspx.

324-Pin FBGA	
Pin Number	A3PE3000 FBGA
A1	GND
A2	IO08NDB0V0
A3	IO08PDB0V0
A4	IO10NDB0V1
A5	IO10PDB0V1
A6	IO12PDB0V1
A7	GND
A8	IO32NDB0V3
A9	IO32PDB0V3
A10	IO42PPB1V0
A11	IO52NPB1V1
A12	GND
A13	IO66NDB1V3
A14	IO72NDB1V3
A15	IO72PDB1V3
A16	IO74NDB1V4
A17	IO74PDB1V4
A18	GND
B1	IO305PDB7V3
B2	GAB2/IO308PDB7V4
B3	GAA0/IO00NPB0V0
B4	$V_{CCI}B0$
B5	GNDQ
B6	IO12NDB0V1
B7	IO18NDB0V2
B8	$V_{CCI}B0$
B9	IO42NPB1V0
B10	IO44NDB1V0
B11	$V_{CCI}B1$
B12	IO52PPB1V1
B13	IO66PDB1V3
B14	GNDQ
B15	$V_{CCI}B1$
B16	GBA0/IO81NDB1V4
B17	GBA1/IO81PDB1V4
B18	IO88PDB2V0

324-Pin FBGA	
Pin Number	A3PE3000 FBGA
C1	IO305NDB7V3
C2	IO308NDB7V4
C3	GAA2/IO309PPB7V4
C4	GAA1/IO00PPB0V0
C5	VMV0
C6	IO14NDB0V1
C7	IO18PDB0V2
C8	IO40NDB0V4
C9	IO40PDB0V4
C10	IO44PDB1V0
C11	IO56NDB1V1
C12	IO64NDB1V2
C13	IO64PDB1V2
C14	VMV1
C15	GBC0/IO79NDB1V4
C16	GBC1/IO79PDB1V4
C17	GBB2/IO83PPB2V0
C18	IO88NDB2V0
D1	IO303PDB7V3
D2	$V_{CCI}B7$
D3	GAC2/IO307PPB7V4
D4	IO309NPB7V4
D5	GAB1/IO01PPB0V0
D6	IO14PDB0V1
D7	IO24NDB0V2
D8	IO24PDB0V2
D9	IO28PDB0V3
D10	IO48NDB1V0
D11	IO56PDB1V1
D12	IO60PPB1V2
D13	GBB0/IO80NDB1V4
D14	GBB1/IO80PDB1V4
D15	GBA2/IO82PDB2V0
D16	IO83NPB2V0
D17	$V_{CCI}B2$
D18	IO90PDB2V1

324-Pin FBGA	
Pin Number	A3PE3000 FBGA
E1	IO303NDB7V3
E2	GNDQ
E3	VMV7
E4	IO307NPB7V4
E5	V_{CCPLA}
E6	GAB0/IO01NPB0V0
E7	$V_{CCI}B0$
E8	GND
E9	IO28NDB0V3
E10	IO48PDB1V0
E11	GND
E12	$V_{CCI}B1$
E13	IO60NPB1V2
E14	V_{CCPLB}
E15	IO82NDB2V0
E16	VMV2
E17	GNDQ
E18	IO90NDB2V1
F1	IO299NDB7V3
F2	IO299PDB7V3
F3	IO295PDB7V2
F4	IO295NDB7V2
F5	V_{COMPLA}
F6	IO291PPB7V2
F7	GAC0/IO02NDB0V0
F8	GAC1/IO02PDB0V0
F9	IO26PDB0V3
F10	IO34PDB0V4
F11	IO58NDB1V2
F12	IO58PDB1V2
F13	IO94PPB2V1
F14	V_{COMPLB}
F15	GBC2/IO84PDB2V0
F16	IO84NDB2V0
F17	IO92NDB2V1
F18	IO92PDB2V1

324-Pin FBGA	
Pin Number	A3PE3000 FBGA
G1	GND
G2	IO287PDB7V1
G3	IO287NDB7V1
G4	IO283PPB7V1
G5	$V_{CCI}B7$
G6	IO279PDB7V0
G7	IO291NPB7V2
G8	V_{CC}
G9	IO26NDB0V3
G10	IO34NDB0V4
G11	V_{CC}
G12	IO94NPB2V1
G13	IO98PDB2V2
G14	$V_{CCI}B2$
G15	GCC0/IO112NPB2V3
G16	IO104PDB2V2
G17	IO104NDB2V2
G18	GND
H1	IO267PDB6V4
H2	$V_{CCI}B7$
H3	IO283NPB7V1
H4	GFB1/IO274PPB7V0
H5	GND
H6	IO279NDB7V0
H7	V_{CC}
H8	V_{CC}
H9	GND
H10	GND
H11	V_{CC}
H12	V_{CC}
H13	IO98NDB2V2
H14	GND
H15	GCB1/IO113PDB2V3
H16	GCC1/IO112PPB2V3
H17	$V_{CCI}B2$
H18	IO108PDB2V3

324-Pin FBGA	
Pin Number	A3PE3000 FBGA
J1	IO267NDB6V4
J2	GFA0/IO273NDB6V4
J3	V_{COMPLF}
J4	GFA2/IO272PDB6V4
J5	GFB0/IO274NPB7V0
J6	GFC0/IO275NDB7V0
J7	GFC1/IO275PDB7V0
J8	GND
J9	GND
J10	GND
J11	GND
J12	GCA2/IO115PDB3V0
J13	GCA1/IO114PDB3V0
J14	GCA0/IO114NDB3V0
J15	GCB0/IO113NDB2V3
J16	V_{COMPLC}
J17	IO120NPB3V0
J18	IO108NDB2V3
K1	IO263PDB6V3
K2	GFA1/IO273PDB6V4
K3	V_{CCPLF}
K4	IO272NDB6V4
K5	GFC2/IO270PPB6V4
K6	GFB2/IO271PDB6V4
K7	IO271NDB6V4
K8	GND
K9	GND
K10	GND
K11	GND
K12	IO115NDB3V0
K13	GCB2/IO116PDB3V0
K14	IO116NDB3V0
K15	GCC2/IO117PDB3V0
K16	V_{CCPLC}
K17	IO124NPB3V1
K18	IO120PPB3V0

324-Pin FBGA	
Pin Number	A3PE3000 FBGA
L1	IO263NDB6V3
L2	$V_{CCI}B6$
L3	IO259PDB6V3
L4	IO259NDB6V3
L5	GND
L6	IO270NPB6V4
L7	V_{CC}
L8	V_{CC}
L9	GND
L10	GND
L11	V_{CC}
L12	V_{CC}
L13	IO132PDB3V2
L14	GND
L15	IO117NDB3V0
L16	IO128NPB3V1
L17	$V_{CCI}B3$
L18	IO124PPB3V1
M1	GND
M2	IO255PDB6V2
M3	IO255NDB6V2
M4	IO251PPB6V2
M5	$V_{CCI}B6$
M6	GEB0/IO235NDB6V0
M7	GEB1/IO235PDB6V0
M8	V_{CC}
M9	IO192PPB4V4
M10	IO154NPB4V0
M11	V_{CC}
M12	GDA0/IO153NPB3V4
M13	IO132NDB3V2
M14	$V_{CCI}B3$
M15	IO134NDB3V2
M16	IO134PDB3V2
M17	IO128PPB3V1
M18	GND

324-Pin FBGA		324-Pin FBGA		324-Pin FBGA	
Pin Number	A3PE3000 FBGA	Pin Number	A3PE3000 FBGA	Pin Number	A3PE3000 FBGA
N1	IO247NDB6V1	R1	IO245NDB6V1	U1	IO241NDB6V0
N2	IO247PDB6V1	R2	V$_{CCI}$B6	U2	GEA2/IO233PPB5V4
N3	IO251NPB6V2	R3	GEA1/IO234PPB6V0	U3	GEC2/IO231PPB5V4
N4	GEC0/IO236NDB6V0	R4	IO232NDB5V4	U4	V$_{CCI}$B5
N5	V$_{COMPLE}$	R5	GEB2/IO232PDB5V4	U5	GNDQ
N6	IO212NDB5V2	R6	IO214NDB5V2	U6	IO208PDB5V1
N7	IO212PDB5V2	R7	IO202PDB5V1	U7	IO198PPB5V0
N8	IO192NPB4V4	R8	IO194PDB5V0	U8	V$_{CCI}$B5
N9	IO174PDB4V2	R9	IO186PDB4V4	U9	IO182NPB4V3
N10	IO170PDB4V2	R10	IO178PDB4V3	U10	IO180NPB4V3
N11	GDA2/IO154PPB4V0	R11	IO168NSB4V1	U11	V$_{CCI}$B4
N12	GDB2/IO155PPB4V0	R12	IO164PDB4V1	U12	IO166PPB4V1
N13	GDA1/IO153PPB3V4	R13	GDC2/IO156PDB4V0	U13	IO162PDB4V1
N14	V$_{COMPLD}$	R14	TCK	U14	GNDQ
N15	GDB0/IO152NDB3V4	R15	V$_{PUMP}$	U15	V$_{CCI}$B4
N16	GDB1/IO152PDB3V4	R16	TRST	U16	TMS
N17	IO138NDB3V3	R17	V$_{CCI}$B3	U17	VMV3
N18	IO138PDB3V3	R18	IO142NDB3V3	U18	IO146NDB3V4
P1	IO245PDB6V1	T1	IO241PDB6V0	V1	GND
P2	GNDQ	T2	GEA0/IO234NPB6V0	V2	IO218NDB5V3
P3	VMV6	T3	IO233NPB5V4	V3	IO218PDB5V3
P4	GEC1/IO236PDB6V0	T4	IO231NPB5V4	V4	IO206NDB5V1
P5	V$_{CCPLE}$	T5	VMV5	V5	IO206PDB5V1
P6	IO214PDB5V2	T6	IO208NDB5V1	V6	IO198NPB5V0
P7	V$_{CCI}$B5	T7	IO202NDB5V1	V7	GND
P8	GND	T8	IO194NDB5V0	V8	IO190NDB4V4
P9	IO174NDB4V2	T9	IO186NDB4V4	V9	IO190PDB4V4
P10	IO170NDB4V2	T10	IO178NDB4V3	V10	IO182PPB4V3
P11	GND	T11	IO166NPB4V1	V11	IO180PPB4V3
P12	V$_{CCI}$B4	T12	IO164NDB4V1	V12	GND
P13	IO155NPB4V0	T13	IO156NDB4V0	V13	IO162NDB4V1
P14	V$_{CCPLD}$	T14	VMV4	V14	IO160NDB4V0
P15	V$_{JTAG}$	T15	TDI	V15	IO160PDB4V0
P16	GDC0/IO151NDB3V4	T16	GNDQ	V16	IO158NDB4V0
P17	GDC1/IO151PDB3V4	T17	TDO	V17	IO158PDB4V0
P18	IO142PDB3V3	T18	IO146PDB3V4	V18	GND

484-Pin FBGA

A1 Ball Pad Corner

Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.actel.com/products/solutions/package/docs.aspx.

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	A3PE600 Function	Pin Number	A3PE600 Function	Pin Number	A3PE600 Function
A1	GND	AA15	NC	B7	IO07PDB0V1
A2	GND	AA16	IO71NDB4V0	B8	IO11NDB0V1
A3	$V_{CCI}B0$	AA17	IO71PDB4V0	B9	IO17NDB0V2
A4	IO06NDB0V1	AA18	NC	B10	IO14PDB0V2
A5	IO06PDB0V1	AA19	NC	B11	IO19PDB0V2
A6	IO08NDB0V1	AA20	NC	B12	IO22NDB1V0
A7	IO08PDB0V1	AA21	$V_{CCI}B3$	B13	IO26NDB1V0
A8	IO11PDB0V1	AA22	GND	B14	NC
A9	IO17PDB0V2	AB1	GND	B15	NC
A10	IO18NDB0V2	AB2	GND	B16	IO30NDB1V1
A11	IO18PDB0V2	AB3	$V_{CCI}B5$	B17	IO30PDB1V1
A12	IO22PDB1V0	AB4	IO97NDB5V2	B18	IO32PDB1V1
A13	IO26PDB1V0	AB5	IO97PDB5V2	B19	NC
A14	IO29NDB1V1	AB6	IO93NDB5V1	B20	NC
A15	IO29PDB1V1	AB7	IO93PDB5V1	B21	$V_{CCI}B2$
A16	IO31NDB1V1	AB8	IO87NDB5V0	B22	GND
A17	IO31PDB1V1	AB9	IO87PDB5V0	C1	$V_{CCI}B7$
A18	IO32NDB1V1	AB10	NC	C2	NC
A19	NC	AB11	NC	C3	NC
A20	$V_{CCI}B1$	AB12	IO75NDB4V1	C4	NC
A21	GND	AB13	IO75PDB4V1	C5	GND
A22	GND	AB14	IO72NDB4V0	C6	IO04NDB0V0
AA1	GND	AB15	IO72PDB4V0	C7	IO04PDB0V0
AA2	$V_{CCI}B6$	AB16	IO73NDB4V0	C8	V_{CC}
AA3	NC	AB17	IO73PDB4V0	C9	V_{CC}
AA4	IO98PDB5V2	AB18	NC	C10	IO14NDB0V2
AA5	IO96NDB5V2	AB19	NC	C11	IO19NDB0V2
AA6	IO96PDB5V2	AB20	$V_{CCI}B4$	C12	NC
AA7	IO86NDB5V0	AB21	GND	C13	NC
AA8	IO86PDB5V0	AB22	GND	C14	V_{CC}
AA9	IO85PDB5V0	B1	GND	C15	V_{CC}
AA10	IO85NDB5V0	B2	$V_{CCI}B7$	C16	NC
AA11	IO78PPB4V1	B3	NC	C17	NC
AA12	IO79NDB4V1	B4	IO03NDB0V0	C18	GND
AA13	IO79PDB4V1	B5	IO03PDB0V0	C19	NC
AA14	NC	B6	IO07NDB0V1	C20	NC

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	**A3PE600 Function**	**Pin Number**	**A3PE600 Function**	**Pin Number**	**A3PE600 Function**
C21	NC	E11	IO16PDB0V2	G3	NC
C22	$V_{CCI}B2$	E12	IO20NDB1V0	G4	IO128PDB7V1
D1	NC	E13	IO24NDB1V0	G5	IO129PDB7V1
D2	NC	E14	IO24PDB1V0	G6	GAC2/IO132PDB7V1
D3	NC	E15	GBC1/IO33PDB1V1	G7	V_{COMPLA}
D4	GND	E16	GBB0/IO34NDB1V1	G8	GNDQ
D5	GAA0/IO00NDB0V0	E17	GNDQ	G9	IO09NDB0V1
D6	GAA1/IO00PDB0V0	E18	GBA2/IO36PDB2V0	G10	IO09PDB0V1
D7	GAB0/IO01NDB0V0	E19	IO42NDB2V0	G11	IO13PDB0V2
D8	IO05PDB0V0	E20	GND	G12	IO21PDB1V0
D9	IO10PDB0V1	E21	NC	G13	IO25PDB1V0
D10	IO12PDB0V2	E22	NC	G14	IO27NDB1V0
D11	IO16NDB0V2	F1	NC	G15	GNDQ
D12	IO23NDB1V0	F2	IO131NDB7V1	G16	V_{COMPLB}
D13	IO23PDB1V0	F3	IO131PDB7V1	G17	GBB2/IO37PDB2V0
D14	IO28NDB1V1	F4	IO133NDB7V1	G18	IO39PDB2V0
D15	IO28PDB1V1	F5	IO134NDB7V1	G19	IO39NDB2V0
D16	GBB1/IO34PDB1V1	F6	VMV7	G20	IO43PDB2V0
D17	GBA0/IO35NDB1V1	F7	V_{CCPLA}	G21	IO43NDB2V0
D18	GBA1/IO35PDB1V1	F8	GAC0/IO02NDB0V0	G22	NC
D19	GND	F9	GAC1/IO02PDB0V0	H1	NC
D20	NC	F10	IO15NDB0V2	H2	NC
D21	NC	F11	IO15PDB0V2	H3	V_{CC}
D22	NC	F12	IO20PDB1V0	H4	IO128NDB7V1
E1	NC	F13	IO25NDB1V0	H5	IO129NDB7V1
E2	NC	F14	IO27PDB1V0	H6	IO132NDB7V1
E3	GND	F15	GBC0/IO33NDB1V1	H7	IO130PDB7V1
E4	GAB2/IO133PDB7V1	F16	V_{CCPLB}	H8	VMV0
E5	GAA2/IO134PDB7V1	F17	VMV2	H9	VCCIB0
E6	GNDQ	F18	IO36NDB2V0	H10	$V_{CCI}B0$
E7	GAB1/IO01PDB0V0	F19	IO42PDB2V0	H11	IO13NDB0V2
E8	IO05NDB0V0	F20	NC	H12	IO21NDB1V0
E9	IO10NDB0V1	F21	NC	H13	$V_{CCI}B1$
E10	IO12NDB0V2	F22	NC	H14	$V_{CCI}B1$
		G1	IO127NDB7V1	H15	VMV1
		G2	IO127PDB7V1		

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	A3PE600 Function	Pin Number	A3PE600 Function	Pin Number	A3PE600 Function
H16	GBC2/IO38PDB2V0	K8	$V_{CCI}B7$	L21	IO47NDB2V1
H17	IO37NDB2V0	K9	V_{CC}	L22	IO47PDB2V1
H18	IO41NDB2V0	K10	GND	M1	NC
H19	IO41PDB2V0	K11	GND	M2	IO114NPB6V1
H20	V_{CC}	K12	GND	M3	IO117NDB6V1
H21	NC	K13	GND	M4	GFA2/IO117PDB6V1
H22	NC	K14	V_{CC}	M5	GFA1/IO118PDB6V1
J1	IO123NDB7V0	K15	$V_{CCI}B2$	M6	V_{CCPLF}
J2	IO123PDB7V0	K16	GCC1/IO50PPB2V1	M7	IO116NDB6V1
J3	NC	K17	IO44NDB2V1	M8	GFB2/IO116PDB6V1
J4	IO124PDB7V0	K18	IO44PDB2V1	M9	V_{CC}
J5	IO125PDB7V0	K19	IO49NPB2V1	M10	GND
J6	IO126PDB7V0	K20	IO45NPB2V1	M11	GND
J7	IO130NDB7V1	K21	IO48NDB2V1	M12	GND
J8	$V_{CCI}B7$	K22	IO46NDB2V1	M13	GND
J9	GND	L1	NC	M14	V_{CC}
J10	V_{CC}	L2	IO122PDB7V0	M15	GCB2/IO54PPB3V0
J11	V_{CC}	L3	IO122NDB7V0	M16	GCA1/IO52PPB3V0
J12	V_{CC}	L4	GFB0/IO119NPB7V0	M17	GCC2/IO55PPB3V0
J13	V_{CC}	L5	GFA0/IO118NDB6V1	M18	V_{CCPLC}
J14	GND	L6	GFB1/IO119PPB7V0	M19	GCA2/IO53PDB3V0
J15	$V_{CCI}B2$	L7	V_{COMPLF}	M20	IO53NDB3V0
J16	IO38NDB2V0	L8	GFC0/IO120NPB7V0	M21	IO56PDB3V0
J17	IO40NDB2V0	L9	V_{CC}	M22	NC
J18	IO40PDB2V0	L10	GND	N1	IO114PPB6V1
J19	IO45PPB2V1	L11	GND	N2	IO111NDB6V1
J20	NC	L12	GND	N3	NC
J21	IO48PDB2V1	L13	GND	N4	GFC2/IO115PPB6V1
J22	IO46PDB2V1	L14	V_{CC}	N5	IO113PPB6V1
K1	IO121NDB7V0	L15	GCC0/IO50NPB2V1	N6	IO112PDB6V1
K2	IO121PDB7V0	L16	GCB1/IO51PPB2V1	N7	IO112NDB6V1
K3	NC	L17	GCA0/IO52NPB3V0	N8	$V_{CCI}B6$
K4	IO124NDB7V0	L18	V_{COMPLC}	N9	V_{CC}
K5	IO125NDB7V0	L19	GCB0/IO51NPB2V1	N10	GND
K6	IO126NDB7V0	L20	IO49PPB2V1	N11	GND
K7	GFC1/IO120PPB7V0			N12	GND

484-Pin FBGA	
Pin Number	A3PE600 Function
N13	GND
N14	V$_{CC}$
N15	V$_{CCI}$B3
N16	IO54NPB3V0
N17	IO57NPB3V0
N18	IO55NPB3V0
N19	IO57PPB3V0
N20	NC
N21	IO56NDB3V0
N22	IO58PDB3V0
P1	NC
P2	IO111PDB6V1
P3	IO115NPB6V1
P4	IO113NPB6V1
P5	IO109PPB6V0
P6	IO108PDB6V0
P7	IO108NDB6V0
P8	V$_{CCI}$B6
P9	GND
P10	V$_{CC}$
P11	V$_{CC}$
P12	V$_{CC}$
P13	V$_{CC}$
P14	GND
P15	V$_{CCI}$B3
P16	GDB0/IO66NPB3V1
P17	IO60NDB3V1
P18	IO60PDB3V1
P19	IO61PDB3V1
P20	NC
P21	IO59PDB3V0
P22	IO58NDB3V0
R1	NC
R2	IO110PDB6V0
R3	V$_{CC}$
R4	IO109NPB6V0

484-Pin FBGA	
Pin Number	A3PE600 Function
R5	IO106NDB6V0
R6	IO106PDB6V0
R7	GEC0/IO104NPB6V0
R8	VMV5
R9	V$_{CCI}$B5
R10	V$_{CCI}$B5
R11	IO84NDB5V0
R12	IO84PDB5V0
R13	V$_{CCI}$B4
R14	V$_{CCI}$B4
R15	VMV3
R16	V$_{CCPLD}$
R17	GDB1/IO66PPB3V1
R18	GDC1/IO65PDB3V1
R19	IO61NDB3V1
R20	V$_{CC}$
R21	IO59NDB3V0
R22	IO62PDB3V1
T1	NC
T2	IO110NDB6V0
T3	NC
T4	IO105PDB6V0
T5	IO105NDB6V0
T6	GEC1/IO104PPB6V0
T7	V$_{COMPLE}$
T8	GNDQ
T9	GEA2/IO101PPB5V2
T10	IO92NDB5V1
T11	IO90NDB5V1
T12	IO82NDB5V0
T13	IO74NDB4V1
T14	IO74PDB4V1
T15	GNDQ
T16	V$_{COMPLD}$
T17	V$_{JTAG}$
T18	GDC0/IO65NDB3V1

484-Pin FBGA	
Pin Number	A3PE600 Function
T19	GDA1/IO67PDB3V1
T20	NC
T21	IO64PDB3V1
T22	IO62NDB3V1
U1	NC
U2	IO107PDB6V0
U3	IO107NDB6V0
U4	GEB1/IO103PDB6V0
U5	GEB0/IO103NDB6V0
U6	VMV6
U7	V$_{CCPLE}$
U8	IO101NPB5V2
U9	IO95PPB5V1
U10	IO92PDB5V1
U11	IO90PDB5V1
U12	IO82PDB5V0
U13	IO76NDB4V1
U14	IO76PDB4V1
U15	VMV4
U16	TCK
U17	V$_{PUMP}$
U18	TRST
U19	GDA0/IO67NDB3V1
U20	NC
U21	IO64NDB3V1
U22	IO63PDB3V1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO102PDB6V0
V5	GEA0/IO102NDB6V0
V6	GNDQ
V7	GEC2/IO99PDB5V2
V8	IO95NPB5V1

484-Pin FBGA	
Pin Number	A3PE600 Function
V9	IO91NDB5V1
V10	IO91PDB5V1
V11	IO83NDB5V0
V12	IO83PDB5V0
V13	IO77NDB4V1
V14	IO77PDB4V1
V15	IO69NDB4V0
V16	GDB2/IO69PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO63NDB3V1
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO100NDB5V2
W6	GEB2/IO100PDB5V2
W7	IO99NDB5V2
W8	IO88NDB5V0
W9	IO88PDB5V0
W10	IO89NDB5V0
W11	IO80NDB4V1
W12	IO81NDB4V1
W13	IO81PDB4V1
W14	IO70NDB4V0
W15	GDC2/IO70PDB4V0
W16	IO68NDB4V0
W17	GDA2/IO68PDB4V0
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC

484-Pin FBGA	
Pin Number	A3PE600 Function
Y1	$V_{CCI}B6$
Y2	NC
Y3	NC
Y4	IO98NDB5V2
Y5	GND
Y6	IO94NDB5V1
Y7	IO94PDB5V1
Y8	V_{CC}
Y9	V_{CC}
Y10	IO89PDB5V0
Y11	IO80PDB4V1
Y12	IO78NPB4V1
Y13	NC
Y14	V_{CC}
Y15	V_{CC}
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	$V_{CCI}B3$

484-Pin FBGA	
Pin Number	A3PE1500 Function
A1	GND
A2	GND
A3	$V_{CCI}B0$
A4	IO05NDB0V0
A5	IO05PDB0V0
A6	IO11NDB0V1
A7	IO11PDB0V1
A8	IO15PDB0V1
A9	IO17PDB0V2
A10	IO27NDB0V3
A11	IO27PDB0V3
A12	IO32PDB1V0
A13	IO43PDB1V1
A14	IO47NDB1V1
A15	IO47PDB1V1
A16	IO51NDB1V2
A17	IO51PDB1V2
A18	IO54NDB1V3
A19	NC
A20	$V_{CCI}B1$
A21	GND
A22	GND
AA1	GND
AA2	$V_{CCI}B6$
AA3	NC
AA4	IO161PDB5V3
AA5	IO155NDB5V2
AA6	IO155PDB5V2
AA7	IO154NDB5V2
AA8	IO154PDB5V2
AA9	IO143PDB5V1
AA10	IO143NDB5V1
AA11	IO131PPB4V2
AA12	IO129NDB4V2
AA13	IO129PDB4V2
AA14	NC

484-Pin FBGA	
Pin Number	A3PE1500 Function
AA15	NC
AA16	IO117NDB4V0
AA17	IO117PDB4V0
AA18	IO115NDB4V0
AA19	IO115PDB4V0
AA20	NC
AA21	$V_{CCI}B3$
AA22	GND
AB1	GND
AB2	GND
AB3	$V_{CCI}B5$
AB4	IO159NDB5V3
AB5	IO159PDB5V3
AB6	IO149NDB5V1
AB7	IO149PDB5V1
AB8	IO138NDB5V0
AB9	IO138PDB5V0
AB10	NC
AB11	NC
AB12	IO127NDB4V2
AB13	IO127PDB4V2
AB14	IO125NDB4V1
AB15	IO125PDB4V1
AB16	IO122NDB4V1
AB17	IO122PDB4V1
AB18	NC
AB19	NC
AB20	$V_{CCI}B4$
AB21	GND
AB22	GND
B1	GND
B2	$V_{CCI}B7$
B3	NC
B4	IO03NDB0V0
B5	IO03PDB0V0
B6	IO10NDB0V1

484-Pin FBGA	
Pin Number	A3PE1500 Function
B7	IO10PDB0V1
B8	IO15NDB0V1
B9	IO17NDB0V2
B10	IO20PDB0V2
B11	IO29PDB0V3
B12	IO32NDB1V0
B13	IO43NDB1V1
B14	NC
B15	NC
B16	IO53NDB1V2
B17	IO53PDB1V2
B18	IO54PDB1V3
B19	NC
B20	NC
B21	$V_{CCI}B2$
B22	GND
C1	$V_{CCI}B7$
C2	NC
C3	NC
C4	NC
C5	GND
C6	IO07NDB0V0
C7	IO07PDB0V0
C8	V_{CC}
C9	V_{CC}
C10	IO20NDB0V2
C11	IO29NDB0V3
C12	NC
C13	NC
C14	V_{CC}
C15	V_{CC}
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

484-Pin FBGA	
Pin Number	A3PE1500 Function
C21	NC
C22	V$_{CCI}$B2
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO09PDB0V1
D9	IO13PDB0V1
D10	IO21PDB0V2
D11	IO31NDB0V3
D12	IO37NDB1V0
D13	IO37PDB1V0
D14	IO49NDB1V2
D15	IO49PDB1V2
D16	GBB1/IO56PDB1V3
D17	GBA0/IO57NDB1V3
D18	GBA1/IO57PDB1V3
D19	GND
D20	NC
D21	IO69PDB2V1
D22	NC
E1	NC
E2	IO218PPB7V3
E3	GND
E4	GAB2/IO220PDB7V3
E5	GAA2/IO221PDB7V3
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO09NDB0V1
E9	IO13NDB0V1
E10	IO21NDB0V2
E11	IO31PDB0V3
E12	IO35NDB1V0

484-Pin FBGA	
Pin Number	A3PE1500 Function
E13	IO41NDB1V1
E14	IO41PDB1V1
E15	GBC1/IO55PDB1V3
E16	GBB0/IO56NDB1V3
E17	GNDQ
E18	GBA2/IO58PDB2V0
E19	IO63NDB2V0
E20	GND
E21	IO69NDB2V1
E22	NC
F1	IO218NPB7V3
F2	IO216NDB7V3
F3	IO216PDB7V3
F4	IO220NDB7V3
F5	IO221NDB7V3
F6	VMV7
F7	V$_{CCPLA}$
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO23NDB0V2
F11	IO23PDB0V2
F12	IO35PDB1V0
F13	IO39NDB1V0
F14	IO45PDB1V1
F15	GBC0/IO55NDB1V3
F16	V$_{CCPLB}$
F17	VMV2
F18	IO58NDB2V0
F19	IO63PDB2V0
F20	NC
F21	NC
F22	NC
G1	IO211NDB7V2
G2	IO211PDB7V2
G3	NC
G4	IO214PDB7V3

484-Pin FBGA	
Pin Number	A3PE1500 Function
G5	IO217PDB7V3
G6	GAC2/IO219PDB7V3
G7	V$_{COMPLA}$
G8	GNDQ
G9	IO19NDB0V2
G10	IO19PDB0V2
G11	IO25PDB0V3
G12	IO33PDB1V0
G13	IO39PDB1V0
G14	IO45NDB1V1
G15	GNDQ
G16	V$_{COMPLB}$
G17	GBB2/IO59PDB2V0
G18	IO62PDB2V0
G19	IO62NDB2V0
G20	IO71PDB2V2
G21	IO71NDB2V2
G22	NC
H1	IO209PSB7V2
H2	NC
H3	V$_{CC}$
H4	IO214NDB7V3
H5	IO217NDB7V3
H6	IO219NDB7V3
H7	IO215PDB7V3
H8	VMV0
H9	V$_{CCI}$B0
H10	V$_{CCI}$B0
H11	IO25NDB0V3
H12	IO33NDB1V0
H13	V$_{CCI}$B1
H14	V$_{CCI}$B1
H15	VMV1
H16	GBC2/IO60PDB2V0
H17	IO59NDB2V0
H18	IO67NDB2V1

484-Pin FBGA	
Pin Number	A3PE1500 Function
H19	IO67PDB2V1
H20	V_{CC}
H21	VMV2
H22	IO74PSB2V2
J1	IO212NDB7V2
J2	IO212PDB7V2
J3	VMV7
J4	IO206PDB7V1
J5	IO204PDB7V1
J6	IO210PDB7V2
J7	IO215NDB7V3
J8	V_{CCI}B7
J9	GND
J10	V_{CC}
J11	V_{CC}
J12	V_{CC}
J13	V_{CC}
J14	GND
J15	V_{CCI}B2
J16	IO60NDB2V0
J17	IO65NDB2V1
J18	IO65PDB2V1
J19	IO75PPB2V2
J20	GNDQ
J21	IO77PDB2V2
J22	IO79PDB2V3
K1	IO200NDB7V1
K2	IO200PDB7V1
K3	GNDQ
K4	IO206NDB7V1
K5	IO204NDB7V1
K6	IO210NDB7V2
K7	GFC1/IO192PPB7V0
K8	V_{CCI}B7
K9	V_{CC}
K10	GND

484-Pin FBGA	
Pin Number	A3PE1500 Function
K11	GND
K12	GND
K13	GND
K14	V_{CC}
K15	V_{CCI}B2
K16	GCC1/IO85PPB2V3
K17	IO73NDB2V2
K18	IO73PDB2V2
K19	IO81NPB2V3
K20	IO75NPB2V2
K21	IO77NDB2V2
K22	IO79NDB2V3
L1	NC
L2	IO196PDB7V0
L3	IO196NDB7V0
L4	GFB0/IO191NPB7V0
L5	GFA0/IO190NDB6V2
L6	GFB1/IO191PPB7V0
L7	V_{COMPLF}
L8	GFC0/IO192NPB7V0
L9	V_{CC}
L10	GND
L11	GND
L12	GND
L13	GND
L14	V_{CC}
L15	GCC0/IO85NPB2V3
L16	GCB1/IO86PPB2V3
L17	GCA0/IO87NPB3V0
L18	V_{COMPLC}
L19	GCB0/IO86NPB2V3
L20	IO81PPB2V3
L21	IO83NDB2V3
L22	IO83PDB2V3
M1	GNDQ
M2	IO185NPB6V2

484-Pin FBGA	
Pin Number	A3PE1500 Function
M3	IO189NDB6V2
M4	GFA2/IO189PDB6V2
M5	GFA1/IO190PDB6V2
M6	V_{CCPLF}
M7	IO188NDB6V2
M8	GFB2/IO188PDB6V2
M9	V_{CC}
M10	GND
M11	GND
M12	GND
M13	GND
M14	V_{CC}
M15	GCB2/IO89PPB3V0
M16	GCA1/IO87PPB3V0
M17	GCC2/IO90PPB3V0
M18	V_{CCPLC}
M19	GCA2/IO88PDB3V0
M20	IO88NDB3V0
M21	IO93PDB3V0
M22	NC
N1	IO185PPB6V2
N2	IO183NDB6V2
N3	VMV6
N4	GFC2/IO187PPB6V2
N5	IO184PPB6V2
N6	IO186PDB6V2
N7	IO186NDB6V2
N8	V_{CCI}B6
N9	V_{CC}
N10	GND
N11	GND
N12	GND
N13	GND
N14	V_{CC}
N15	V_{CCI}B3
N16	IO89NPB3V0

484-Pin FBGA	
Pin Number	A3PE1500 Function
N17	IO91NPB3V0
N18	IO90NPB3V0
N19	IO91PPB3V0
N20	GNDQ
N21	IO93NDB3V0
N22	IO95PDB3V1
P1	NC
P2	IO183PDB6V2
P3	IO187NPB6V2
P4	IO184NPB6V2
P5	IO176PPB6V1
P6	IO182PDB6V1
P7	IO182NDB6V1
P8	$V_{CCI}B6$
P9	GND
P10	V_{CC}
P11	V_{CC}
P12	V_{CC}
P13	V_{CC}
P14	GND
P15	$V_{CCI}B3$
P16	GDB0/IO109NPB3V2
P17	IO97NDB3V1
P18	IO97PDB3V1
P19	IO99PDB3V1
P20	VMV3
P21	IO98PDB3V1
P22	IO95NDB3V1
R1	NC
R2	IO177PDB6V1
R3	V_{CC}
R4	IO176NPB6V1
R5	IO174NDB6V0
R6	IO174PDB6V0
R7	GEC0/IO169NPB6V0
R8	VMV5

484-Pin FBGA	
Pin Number	A3PE1500 Function
R9	$V_{CCI}B5$
R10	$V_{CCI}B5$
R11	IO135NDB5V0
R12	IO135PDB5V0
R13	$V_{CCI}B4$
R14	$V_{CCI}B4$
R15	VMV3
R16	V_{CCPLD}
R17	GDB1/IO109PPB3V2
R18	GDC1/IO108PDB3V2
R19	IO99NDB3V1
R20	V_{CC}
R21	IO98NDB3V1
R22	IO101PDB3V1
T1	NC
T2	IO177NDB6V1
T3	NC
T4	IO171PDB6V0
T5	IO171NDB6V0
T6	GEC1/IO169PPB6V0
T7	V_{COMPLE}
T8	GNDQ
T9	GEA2/IO166PPB5V3
T10	IO145NDB5V1
T11	IO141NDB5V0
T12	IO139NDB5V0
T13	IO119NDB4V1
T14	IO119PDB4V1
T15	GNDQ
T16	V_{COMPLD}
T17	V_{JTAG}
T18	GDC0/IO108NDB3V2
T19	GDA1/IO110PDB3V2
T20	NC
T21	IO103PDB3V2
T22	IO101NDB3V1

484-Pin FBGA	
Pin Number	A3PE1500 Function
U1	IO175PPB6V1
U2	IO173PDB6V0
U3	IO173NDB6V0
U4	GEB1/IO168PDB6V0
U5	GEB0/IO168NDB6V0
U6	VMV6
U7	V_{CCPLE}
U8	IO166NPB5V3
U9	IO157PPB5V2
U10	IO145PDB5V1
U11	IO141PDB5V0
U12	IO139PDB5V0
U13	IO121NDB4V1
U14	IO121PDB4V1
U15	VMV4
U16	TCK
U17	V_{PUMP}
U18	TRST
U19	GDA0/IO110NDB3V2
U20	NC
U21	IO103NDB3V2
U22	IO105PDB3V2
V1	NC
V2	IO175NPB6V1
V3	GND
V4	GEA1/IO167PDB6V0
V5	GEA0/IO167NDB6V0
V6	GNDQ
V7	GEC2/IO164PDB5V3
V8	IO157NPB5V2
V9	IO151NDB5V2
V10	IO151PDB5V2
V11	IO137NDB5V0
V12	IO137PDB5V0
V13	IO123NDB4V1

484-Pin FBGA	
Pin Number	**A3PE1500 Function**
V14	IO123PDB4V1
V15	IO112NDB4V0
V16	GDB2/IO112PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO105NDB3V2
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO165NDB5V3
W6	GEB2/IO165PDB5V3
W7	IO164NDB5V3
W8	IO153NDB5V2
W9	IO153PDB5V2
W10	IO147NDB5V1
W11	IO133NDB4V2
W12	IO130NDB4V2
W13	IO130PDB4V2
W14	IO113NDB4V0
W15	GDC2/IO113PDB4V0
W16	IO111NDB4V0
W17	GDA2/IO111PDB4V0
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	$V_{CCI}B6$
Y2	NC
Y3	NC
Y4	IO161NDB5V3
Y5	GND

484-Pin FBGA	
Pin Number	**A3PE1500 Function**
Y6	IO163NDB5V3
Y7	IO163PDB5V3
Y8	V_{CC}
Y9	V_{CC}
Y10	IO147PDB5V1
Y11	IO133PDB4V2
Y12	IO131NPB4V2
Y13	NC
Y14	V_{CC}
Y15	V_{CC}
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	$V_{CCI}B3$

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
A1	GND	AA15	IO170PDB4V2	B7	IO14PDB0V1
A2	GND	AA16	IO166NDB4V1	B8	IO18NDB0V2
A3	$V_{CCI}B0$	AA17	IO166PDB4V1	B9	IO24NDB0V2
A4	IO10NDB0V1	AA18	IO160NDB4V0	B10	IO34PDB0V4
A5	IO10PDB0V1	AA19	IO160PDB4V0	B11	IO40PDB0V4
A6	IO16NDB0V1	AA20	IO158NPB4V0	B12	IO46NDB1V0
A7	IO16PDB0V1	AA21	$V_{CCI}B3$	B13	IO54NDB1V1
A8	IO18PDB0V2	AA22	GND	B14	IO62NDB1V2
A9	IO24PDB0V2	AB1	GND	B15	IO62PDB1V2
A10	IO28NDB0V3	AB2	GND	B16	IO68NDB1V3
A11	IO28PDB0V3	AB3	$V_{CCI}B5$	B17	IO68PDB1V3
A12	IO46PDB1V0	AB4	IO216NDB5V2	B18	IO72PDB1V3
A13	IO54PDB1V1	AB5	IO216PDB5V2	B19	IO74PDB1V4
A14	IO56NDB1V1	AB6	IO210NDB5V2	B20	IO76NPB1V4
A15	IO56PDB1V1	AB7	IO210PDB5V2	B21	$V_{CCI}B2$
A16	IO64NDB1V2	AB8	IO208NDB5V1	B22	GND
A17	IO64PDB1V2	AB9	IO208PDB5V1	C1	$V_{CCI}B7$
A18	IO72NDB1V3	AB10	IO197NDB5V0	C2	IO303PDB7V3
A19	IO74NDB1V4	AB11	IO197PDB5V0	C3	IO305PDB7V3
A20	$V_{CCI}B1$	AB12	IO174NDB4V2	C4	IO06NPB0V0
A21	GND	AB13	IO174PDB4V2	C5	GND
A22	GND	AB14	IO172NDB4V2	C6	IO12NDB0V1
AA1	GND	AB15	IO172PDB4V2	C7	IO12PDB0V1
AA2	$V_{CCI}B6$	AB16	IO168NDB4V1	C8	V_{CC}
AA3	IO228PDB5V4	AB17	IO168PDB4V1	C9	V_{CC}
AA4	IO224PDB5V3	AB18	IO162NDB4V1	C10	IO34NDB0V4
AA5	IO218NDB5V3	AB19	IO162PDB4V1	C11	IO40NDB0V4
AA6	IO218PDB5V3	AB20	$V_{CCI}B4$	C12	IO48NDB1V0
AA7	IO212NDB5V2	AB21	GND	C13	IO48PDB1V0
AA8	IO212PDB5V2	AB22	GND	C14	V_{CC}
AA9	IO198PDB5V0	B1	GND	C15	V_{CC}
AA10	IO198NDB5V0	B2	$V_{CCI}B7$	C16	IO70NDB1V3
AA11	IO188PPB4V4	B3	IO06PPB0V0	C17	IO70PDB1V3
AA12	IO180NDB4V3	B4	IO08NDB0V0	C18	GND
AA13	IO180PDB4V3	B5	IO08PDB0V0	C19	IO76PPB1V4
AA14	IO170NDB4V2	B6	IO14NDB0V1	C20	IO88NDB2V0

484-Pin FBGA	
Pin Number	**A3PE3000 Function**
C21	IO94PPB2V1
C22	V$_{CCI}$B2
D1	IO293PDB7V2
D2	IO303NDB7V3
D3	IO305NDB7V3
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO20PDB0V2
D9	IO22PDB0V2
D10	IO30PDB0V3
D11	IO38NDB0V4
D12	IO52NDB1V1
D13	IO52PDB1V1
D14	IO66NDB1V3
D15	IO66PDB1V3
D16	GBB1/IO80PDB1V4
D17	GBA0/IO81NDB1V4
D18	GBA1/IO81PDB1V4
D19	GND
D20	IO88PDB2V0
D21	IO90PDB2V1
D22	IO94NPB2V1
E1	IO293NDB7V2
E2	IO299PPB7V3
E3	GND
E4	GAB2/IO308PDB7V4
E5	GAA2/IO309PDB7V4
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO20NDB0V2
E9	IO22NDB0V2
E10	IO30NDB0V3
E11	IO38PDB0V4
E12	IO44NDB1V0

484-Pin FBGA	
Pin Number	**A3PE3000 Function**
E13	IO58NDB1V2
E14	IO58PDB1V2
E15	GBC1/IO79PDB1V4
E16	GBB0/IO80NDB1V4
E17	GNDQ
E18	GBA2/IO82PDB2V0
E19	IO86NDB2V0
E20	GND
E21	IO90NDB2V1
E22	IO98PDB2V2
F1	IO299NPB7V3
F2	IO301NDB7V3
F3	IO301PDB7V3
F4	IO308NDB7V4
F5	IO309NDB7V4
F6	VMV7
F7	V$_{CCPLA}$
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO32NDB0V3
F11	IO32PDB0V3
F12	IO44PDB1V0
F13	IO50NDB1V1
F14	IO60PDB1V2
F15	GBC0/IO79NDB1V4
F16	V$_{CCPLB}$
F17	VMV2
F18	IO82NDB2V0
F19	IO86PDB2V0
F20	IO96PDB2V1
F21	IO96NDB2V1
F22	IO98NDB2V2
G1	IO289NDB7V1
G2	IO289PDB7V1
G3	IO291PPB7V2
G4	IO295PDB7V2

484-Pin FBGA	
Pin Number	**A3PE3000 Function**
G5	IO297PDB7V2
G6	GAC2/IO307PDB7V4
G7	V$_{COMPLA}$
G8	GNDQ
G9	IO26NDB0V3
G10	IO26PDB0V3
G11	IO36PDB0V4
G12	IO42PDB1V0
G13	IO50PDB1V1
G14	IO60NDB1V2
G15	GNDQ
G16	V$_{COMPLB}$
G17	GBB2/IO83PDB2V0
G18	IO92PDB2V1
G19	IO92NDB2V1
G20	IO102PDB2V2
G21	IO102NDB2V2
G22	IO105NDB2V2
H1	IO286PSB7V1
H2	IO291NPB7V2
H3	V$_{CC}$
H4	IO295NDB7V2
H5	IO297NDB7V2
H6	IO307NDB7V4
H7	IO287PDB7V1
H8	VMV0
H9	V$_{CCI}$B0
H10	V$_{CCI}$B0
H11	IO36NDB0V4
H12	IO42NDB1V0
H13	V$_{CCI}$B1
H14	V$_{CCI}$B1
H15	VMV1
H16	GBC2/IO84PDB2V0
H17	IO83NDB2V0
H18	IO100NDB2V2

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
H19	IO100PDB2V2	K11	GND	M3	IO272NDB6V4
H20	V_{CC}	K12	GND	M4	GFA2/IO272PDB6V4
H21	VMV2	K13	GND	M5	GFA1/IO273PDB6V4
H22	IO105PDB2V2	K14	V_{CC}	M6	V_{CCPLF}
J1	IO285NDB7V1	K15	$V_{CCI}B2$	M7	IO271NDB6V4
J2	IO285PDB7V1	K16	GCC1/IO112PPB2V3	M8	GFB2/IO271PDB6V4
J3	VMV7	K17	IO108NDB2V3	M9	V_{CC}
J4	IO279PDB7V0	K18	IO108PDB2V3	M10	GND
J5	IO283PDB7V1	K19	IO110NPB2V3	M11	GND
J6	IO281PDB7V0	K20	IO106NPB2V3	M12	GND
J7	IO287NDB7V1	K21	IO109NDB2V3	M13	GND
J8	$V_{CCI}B7$	K22	IO107NDB2V3	M14	V_{CC}
J9	GND	L1	IO257PSB6V2	M15	GCB2/IO116PPB3V0
J10	V_{CC}	L2	IO276PDB7V0	M16	GCA1/IO114PPB3V0
J11	V_{CC}	L3	IO276NDB7V0	M17	GCC2/IO117PPB3V0
J12	V_{CC}	L4	GFB0/IO274NPB7V0	M18	V_{CCPLC}
J13	V_{CC}	L5	GFA0/IO273NDB6V4	M19	GCA2/IO115PDB3V0
J14	GND	L6	GFB1/IO274PPB7V0	M20	IO115NDB3V0
J15	$V_{CCI}B2$	L7	V_{COMPLF}	M21	IO126PDB3V1
J16	IO84NDB2V0	L8	GFC0/IO275NPB7V0	M22	IO124PSB3V1
J17	IO104NDB2V2	L9	V_{CC}	N1	IO255PPB6V2
J18	IO104PDB2V2	L10	GND	N2	IO253NDB6V2
J19	IO106PPB2V3	L11	GND	N3	VMV6
J20	GNDQ	L12	GND	N4	GFC2/IO270PPB6V4
J21	IO109PDB2V3	L13	GND	N5	IO261PPB6V3
J22	IO107PDB2V3	L14	V_{CC}	N6	IO263PDB6V3
K1	IO277NDB7V0	L15	GCC0/IO112NPB2V3	N7	IO263NDB6V3
K2	IO277PDB7V0	L16	GCB1/IO113PPB2V3	N8	$V_{CCI}B6$
K3	GNDQ	L17	GCA0/IO114NPB3V0	N9	V_{CC}
K4	IO279NDB7V0	L18	V_{COMPLC}	N10	GND
K5	IO283NDB7V1	L19	GCB0/IO113NPB2V3	N11	GND
K6	IO281NDB7V0	L20	IO110PPB2V3	N12	GND
K7	GFC1/IO275PPB7V0	L21	IO111NDB2V3	N13	GND
K8	$V_{CCI}B7$	L22	IO111PDB2V3	N14	V_{CC}
K9	V_{CC}	M1	GNDQ	N15	$V_{CCI}B3$
K10	GND	M2	IO255NPB6V2	N16	IO116NPB3V0

484-Pin FBGA	
Pin Number	**A3PE3000 Function**
N17	IO132NPB3V2
N18	IO117NPB3V0
N19	IO132PPB3V2
N20	GNDQ
N21	IO126NDB3V1
N22	IO128PDB3V1
P1	IO247PDB6V1
P2	IO253PDB6V2
P3	IO270NPB6V4
P4	IO261NPB6V3
P5	IO249PPB6V1
P6	IO259PDB6V3
P7	IO259NDB6V3
P8	$V_{CCI}B6$
P9	GND
P10	V_{CC}
P11	V_{CC}
P12	V_{CC}
P13	V_{CC}
P14	GND
P15	$V_{CCI}B3$
P16	GDB0/IO152NPB3V4
P17	IO136NDB3V2
P18	IO136PDB3V2
P19	IO138PDB3V3
P20	VMV3
P21	IO130PDB3V2
P22	IO128NDB3V1
R1	IO247NDB6V1
R2	IO245PDB6V1
R3	V_{CC}
R4	IO249NPB6V1
R5	IO251NDB6V2
R6	IO251PDB6V2
R7	GEC0/IO236NPB6V0
R8	VMV5

484-Pin FBGA	
Pin Number	**A3PE3000 Function**
R9	$V_{CCI}B5$
R10	$V_{CCI}B5$
R11	IO196NDB5V0
R12	IO196PDB5V0
R13	$V_{CCI}B4$
R14	$V_{CCI}B4$
R15	VMV3
R16	V_{CCPLD}
R17	GDB1/IO152PPB3V4
R18	GDC1/IO151PDB3V4
R19	IO138NDB3V3
R20	V_{CC}
R21	IO130NDB3V2
R22	IO134PDB3V2
T1	IO243PPB6V1
T2	IO245NDB6V1
T3	IO243NPB6V1
T4	IO241PDB6V0
T5	IO241NDB6V0
T6	GEC1/IO236PPB6V0
T7	V_{COMPLE}
T8	GNDQ
T9	GEA2/IO233PPB5V4
T10	IO206NDB5V1
T11	IO202NDB5V1
T12	IO194NDB5V0
T13	IO186NDB4V4
T14	IO186PDB4V4
T15	GNDQ
T16	V_{COMPLD}
T17	V_{JTAG}
T18	GDC0/IO151NDB3V4
T19	GDA1/IO153PDB3V4
T20	IO144PDB3V3
T21	IO140PDB3V3
T22	IO134NDB3V2

484-Pin FBGA	
Pin Number	**A3PE3000 Function**
U1	IO240PPB6V0
U2	IO238PDB6V0
U3	IO238NDB6V0
U4	GEB1/IO235PDB6V0
U5	GEB0/IO235NDB6V0
U6	VMV6
U7	V_{CCPLE}
U8	IO233NPB5V4
U9	IO222PPB5V3
U10	IO206PDB5V1
U11	IO202PDB5V1
U12	IO194PDB5V0
U13	IO176NDB4V2
U14	IO176PDB4V2
U15	VMV4
U16	TCK
U17	V_{PUMP}
U18	TRST
U19	GDA0/IO153NDB3V4
U20	IO144NDB3V3
U21	IO140NDB3V3
U22	IO142PDB3V3
V1	IO239PDB6V0
V2	IO240NPB6V0
V3	GND
V4	GEA1/IO234PDB6V0
V5	GEA0/IO234NDB6V0
V6	GNDQ
V7	GEC2/IO231PDB5V4
V8	IO222NPB5V3
V9	IO204NDB5V1
V10	IO204PDB5V1
V11	IO195NDB5V0
V12	IO195PDB5V0
V13	IO178NDB4V3
V14	IO178PDB4V3

484-Pin FBGA	
Pin Number	A3PE3000 Function
V15	IO155NDB4V0
V16	GDB2/IO155PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	IO146PDB3V4
V22	IO142NDB3V3
W1	IO239NDB6V0
W2	IO237PDB6V0
W3	IO230PSB5V4
W4	GND
W5	IO232NDB5V4
W6	GEB2/IO232PDB5V4
W7	IO231NDB5V4
W8	IO214NDB5V2
W9	IO214PDB5V2
W10	IO200NDB5V0
W11	IO192NDB4V4
W12	IO184NDB4V3
W13	IO184PDB4V3
W14	IO156NDB4V0
W15	GDC2/IO156PDB4V0
W16	IO154NDB4V0
W17	GDA2/IO154PDB4V0
W18	TMS
W19	GND
W20	IO150NDB3V4
W21	IO146NDB3V4
W22	IO148PPB3V4
Y1	$V_{CCI}B6$
Y2	IO237NDB6V0
Y3	IO228NDB5V4
Y4	IO224NDB5V3
Y5	GND
Y6	IO220NDB5V3

484-Pin FBGA	
Pin Number	A3PE3000 Function
Y7	IO220PDB5V3
Y8	V_{CC}
Y9	V_{CC}
Y10	IO200PDB5V0
Y11	IO192PDB4V4
Y12	IO188NPB4V4
Y13	IO187PSB4V4
Y14	V_{CC}
Y15	V_{CC}
Y16	IO164NDB4V1
Y17	IO164PDB4V1
Y18	GND
Y19	IO158PPB4V0
Y20	IO150PDB3V4
Y21	IO148NPB3V4
Y22	$V_{CCI}B3$

676-Pin FBGA

A1 Ball Pad Corner

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        26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1
      O O O O O O O O O O O O O O O O O O O O O O O O O O   A
      O O O O O O O O O O O O O O O O O O O O O O O O O O   B
      O O O O O O O O O O O O O O O O O O O O O O O O O O   C
      O O O O O O O O O O O O O O O O O O O O O O O O O O   D
      O O O O O O O O O O O O O O O O O O O O O O O O O O   E
      O O O O O O O O O O O O O O O O O O O O O O O O O O   F
      O O O O O O O O O O O O O O O O O O O O O O O O O O   G
      O O O O O O O O O O O O O O O O O O O O O O O O O O   H
      O O O O O O O O O O O O O O O O O O O O O O O O O O   J
      O O O O O O O O O O O O O O O O O O O O O O O O O O   K
      O O O O O O O O O O O O O O O O O O O O O O O O O O   L
      O O O O O O O O O O O O O O O O O O O O O O O O O O   M
      O O O O O O O O O O O O O O O O O O O O O O O O O O   N
      O O O O O O O O O O O O O O O O O O O O O O O O O O   P
      O O O O O O O O O O O O O O O O O O O O O O O O O O   R
      O O O O O O O O O O O O O O O O O O O O O O O O O O   T
      O O O O O O O O O O O O O O O O O O O O O O O O O O   U
      O O O O O O O O O O O O O O O O O O O O O O O O O O   V
      O O O O O O O O O O O O O O O O O O O O O O O O O O   W
      O O O O O O O O O O O O O O O O O O O O O O O O O O   Y
      O O O O O O O O O O O O O O O O O O O O O O O O O O   AA
      O O O O O O O O O O O O O O O O O O O O O O O O O O   AB
      O O O O O O O O O O O O O O O O O O O O O O O O O O   AC
      O O O O O O O O O O O O O O O O O O O O O O O O O O   AD
      O O O O O O O O O O O O O O O O O O O O O O O O O O   AE
      O O O O O O O O O O O O O O O O O O O O O O O O O O   AF
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Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at
http://www.actel.com/products/solutions/package/docs.aspx.

676-Pin FBGA	
Pin Number	A3PE1500 Function
A1	GND
A2	GND
A3	GAA0/IO00NDB0V0
A4	GAA1/IO00PDB0V0
A5	IO06NDB0V0
A6	IO09NDB0V1
A7	IO09PDB0V1
A8	IO14NDB0V1
A9	IO14PDB0V1
A10	IO22NDB0V2
A11	IO22PDB0V2
A12	IO26NDB0V3
A13	IO26PDB0V3
A14	IO30NDB0V3
A15	IO30PDB0V3
A16	IO34NDB1V0
A17	IO34PDB1V0
A18	IO38NDB1V0
A19	IO38PDB1V0
A20	IO41PDB1V1
A21	IO44PDB1V1
A22	IO49PDB1V2
A23	IO50PDB1V2
A24	GBC1/IO55PDB1V3
A25	GND
A26	GND
AA1	IO174PDB6V0
AA2	IO171PDB6V0
AA3	GEA1/IO167PPB6V0
AA4	GEC0/IO169NPB6V0
AA5	V_{COMPLE}
AA6	GND
AA7	IO165NDB5V3
AA8	GEB2/IO165PDB5V3
AA9	IO163PDB5V3
AA10	IO159NDB5V3

676-Pin FBGA	
Pin Number	A3PE1500 Function
AA11	IO153NDB5V2
AA12	IO147NDB5V1
AA13	IO139NDB5V0
AA14	IO137NDB5V0
AA15	IO123NDB4V1
AA16	IO123PDB4V1
AA17	IO117NDB4V0
AA18	IO117PDB4V0
AA19	GDB2/IO112PDB4V0
AA20	GNDQ
AA21	TDO
AA22	GND
AA23	GND
AA24	IO102NDB3V1
AA25	IO102PDB3V1
AA26	IO98NDB3V1
AB1	IO174NDB6V0
AB2	IO171NDB6V0
AB3	GEB1/IO168PPB6V0
AB4	GEA0/IO167NPB6V0
AB5	V_{CCPLE}
AB6	GND
AB7	GND
AB8	IO156NDB5V2
AB9	IO156PDB5V2
AB10	IO150PDB5V1
AB11	IO155PDB5V2
AB12	IO142PDB5V0
AB13	IO135NDB5V0
AB14	IO135PDB5V0
AB15	IO132PDB4V2
AB16	IO129PDB4V2
AB17	IO121PDB4V1
AB18	IO119NDB4V1
AB19	IO112NDB4V0
AB20	VMV4

676-Pin FBGA	
Pin Number	A3PE1500 Function
AB21	TCK
AB22	TRST
AB23	GDC0/IO108NDB3V2
AB24	GDC1/IO108PDB3V2
AB25	IO104NDB3V2
AB26	IO104PDB3V2
AC1	IO170PDB6V0
AC2	GEB0/IO168NPB6V0
AC3	IO166NPB5V3
AC4	GNDQ
AC5	GND
AC6	IO160PDB5V3
AC7	IO161PDB5V3
AC8	IO154PDB5V2
AC9	GND
AC10	IO150NDB5V1
AC11	IO155NDB5V2
AC12	IO142NDB5V0
AC13	IO138NDB5V0
AC14	IO138PDB5V0
AC15	IO132NDB4V2
AC16	IO129NDB4V2
AC17	IO121NDB4V1
AC18	IO119PDB4V1
AC19	IO118NDB4V0
AC20	IO118PDB4V0
AC21	IO114PPB4V0
AC22	TMS
AC23	V_{JTAG}
AC24	VMV3
AC25	IO106NDB3V2
AC26	IO106PDB3V2
AD1	IO170NDB6V0
AD2	GEA2/IO166PPB5V3
AD3	VMV5
AD4	GEC2/IO164PDB5V3

676-Pin FBGA	
Pin Number	A3PE1500 Function
AD5	IO162PDB5V3
AD6	IO160NDB5V3
AD7	IO161NDB5V3
AD8	IO154NDB5V2
AD9	IO148PDB5V1
AD10	IO151PDB5V2
AD11	IO144PDB5V1
AD12	IO140PDB5V0
AD13	IO143PDB5V1
AD14	IO141PDB5V0
AD15	IO134PDB4V2
AD16	IO133PDB4V2
AD17	IO127PDB4V2
AD18	IO130PDB4V2
AD19	IO126PDB4V1
AD20	IO124PDB4V1
AD21	IO120PDB4V1
AD22	IO114NPB4V0
AD23	TDI
AD24	GNDQ
AD25	GDA0/IO110NDB3V2
AD26	GDA1/IO110PDB3V2
AE1	GND
AE2	GND
AE3	GND
AE4	IO164NDB5V3
AE5	IO162NDB5V3
AE6	IO158PPB5V2
AE7	IO157PPB5V2
AE8	IO152PPB5V2
AE9	IO148NDB5V1
AE10	IO151NDB5V2
AE11	IO144NDB5V1
AE12	IO140NDB5V0
AE13	IO143NDB5V1
AE14	IO141NDB5V0

676-Pin FBGA	
Pin Number	A3PE1500 Function
AE15	IO134NDB4V2
AE16	IO133NDB4V2
AE17	IO127NDB4V2
AE18	IO130NDB4V2
AE19	IO126NDB4V1
AE20	IO124NDB4V1
AE21	IO120NDB4V1
AE22	IO116PDB4V0
AE23	GDC2/IO113PDB4V0
AE24	GDA2/IO111PDB4V0
AE25	GND
AE26	GND
AF1	GND
AF2	GND
AF3	GND
AF4	GND
AF5	IO158NPB5V2
AF6	IO157NPB5V2
AF7	IO152NPB5V2
AF8	IO146NDB5V1
AF9	IO146PDB5V1
AF10	IO149NDB5V1
AF11	IO149PDB5V1
AF12	IO145NDB5V1
AF13	IO145PDB5V1
AF14	IO136NDB5V0
AF15	IO136PDB5V0
AF16	IO131NDB4V2
AF17	IO131PDB4V2
AF18	IO128NDB4V2
AF19	IO128PDB4V2
AF20	IO122NDB4V1
AF21	IO122PDB4V1
AF22	IO116NDB4V0
AF23	IO113NDB4V0
AF24	IO111NDB4V0

676-Pin FBGA	
Pin Number	A3PE1500 Function
AF25	GND
AF26	GND
B1	GND
B2	GND
B3	GND
B4	GND
B5	IO06PDB0V0
B6	IO04NDB0V0
B7	IO07NDB0V0
B8	IO11NDB0V1
B9	IO10NDB0V1
B10	IO16NDB0V2
B11	IO20NDB0V2
B12	IO24NDB0V3
B13	IO23NDB0V2
B14	IO28NDB0V3
B15	IO31NDB0V3
B16	IO32PDB1V0
B17	IO36PDB1V0
B18	IO37PDB1V0
B19	IO42NPB1V1
B20	IO41NDB1V1
B21	IO44NDB1V1
B22	IO49NDB1V2
B23	IO50NDB1V2
B24	GBC0/IO55NDB1V3
B25	GND
B26	GND
C1	GND
C2	GND
C3	GND
C4	GND
C5	GAA2/IO221PDB7V3
C6	IO04PDB0V0
C7	IO07PDB0V0
C8	IO11PDB0V1

676-Pin FBGA	
Pin Number	A3PE1500 Function
C9	IO10PDB0V1
C10	IO16PDB0V2
C11	IO20PDB0V2
C12	IO24PDB0V3
C13	IO23PDB0V2
C14	IO28PDB0V3
C15	IO31PDB0V3
C16	IO32NDB1V0
C17	IO36NDB1V0
C18	IO37NDB1V0
C19	IO45NDB1V1
C20	IO42PPB1V1
C21	IO46NPB1V1
C22	IO48NPB1V2
C23	GBB0/IO56NPB1V3
C24	VMV1
C25	GBC2/IO60PDB2V0
C26	IO60NDB2V0
D1	IO218NDB7V3
D2	IO218PDB7V3
D3	GND
D4	VMV7
D5	IO221NDB7V3
D6	GAC0/IO02NDB0V0
D7	GAC1/IO02PDB0V0
D8	IO05NDB0V0
D9	IO08PDB0V1
D10	IO12NDB0V1
D11	IO18NDB0V2
D12	IO17NDB0V2
D13	IO25NDB0V3
D14	IO29NDB0V3
D15	IO33NDB1V0
D16	IO40PDB1V1
D17	IO43NDB1V1
D18	IO47PDB1V1

676-Pin FBGA	
Pin Number	A3PE1500 Function
D19	IO45PDB1V1
D20	IO46PPB1V1
D21	IO48PPB1V2
D22	GBA0/IO57NPB1V3
D23	GNDQ
D24	GBB1/IO56PPB1V3
D25	GBB2/IO59PDB2V0
D26	IO59NDB2V0
E1	IO212PDB7V2
E2	IO211NDB7V2
E3	IO211PDB7V2
E4	IO220NPB7V3
E5	GNDQ
E6	GAB2/IO220PPB7V3
E7	GAB1/IO01PDB0V0
E8	IO05PDB0V0
E9	IO08NDB0V1
E10	IO12PDB0V1
E11	IO18PDB0V2
E12	IO17PDB0V2
E13	IO25PDB0V3
E14	IO29PDB0V3
E15	IO33PDB1V0
E16	IO40NDB1V1
E17	IO43PDB1V1
E18	IO47NDB1V1
E19	IO54NDB1V3
E20	IO52NDB1V2
E21	IO52PDB1V2
E22	V_{CCPLB}
E23	GBA1/IO57PPB1V3
E24	IO63PDB2V0
E25	IO63NDB2V0
E26	IO68PDB2V1
F1	IO212NDB7V2
F2	IO203PPB7V1

676-Pin FBGA	
Pin Number	A3PE1500 Function
F3	IO213NDB7V2
F4	IO213PDB7V2
F5	GND
F6	V_{CCPLA}
F7	GAB0/IO01NDB0V0
F8	GNDQ
F9	IO03PDB0V0
F10	IO13PDB0V1
F11	IO15PDB0V1
F12	IO19PDB0V2
F13	IO21PDB0V2
F14	IO27NDB0V3
F15	IO35PDB1V0
F16	IO39NDB1V0
F17	IO51PDB1V2
F18	IO53PDB1V2
F19	IO54PDB1V3
F20	VMV2
F21	V_{COMPLB}
F22	IO61PDB2V0
F23	IO61NDB2V0
F24	IO66PDB2V1
F25	IO66NDB2V1
F26	IO68NDB2V1
G1	IO203NPB7V1
G2	IO207NDB7V2
G3	IO207PDB7V2
G4	IO216NDB7V3
G5	IO216PDB7V3
G6	V_{COMPLA}
G7	VMV0
G8	V_{CC}
G9	IO03NDB0V0
G10	IO13NDB0V1
G11	IO15NDB0V1
G12	IO19NDB0V2

676-Pin FBGA	
Pin Number	A3PE1500 Function
G13	IO21NDB0V2
G14	IO27PDB0V3
G15	IO35NDB1V0
G16	IO39PDB1V0
G17	IO51NDB1V2
G18	IO53NDB1V2
G19	$V_{CCI}B1$
G20	GBA2/IO58PPB2V0
G21	GNDQ
G22	IO64NDB2V1
G23	IO64PDB2V1
G24	IO72PDB2V2
G25	IO72NDB2V2
G26	IO78PDB2V2
H1	IO208NDB7V2
H2	IO208PDB7V2
H3	IO209NDB7V2
H4	IO209PDB7V2
H5	IO219NDB7V3
H6	GAC2/IO219PDB7V3
H7	$V_{CCI}B7$
H8	V_{CC}
H9	$V_{CCI}B0$
H10	$V_{CCI}B0$
H11	$V_{CCI}B0$
H12	$V_{CCI}B0$
H13	$V_{CCI}B0$
H14	$V_{CCI}B1$
H15	$V_{CCI}B1$
H16	$V_{CCI}B1$
H17	$V_{CCI}B1$
H18	$V_{CCI}B1$
H19	V_{CC}
H20	V_{CC}
H21	IO58NPB2V0
H22	IO70PDB2V1

676-Pin FBGA	
Pin Number	A3PE1500 Function
H23	IO69PDB2V1
H24	IO76PDB2V2
H25	IO76NDB2V2
H26	IO78NDB2V2
J1	IO197NDB7V0
J2	IO197PDB7V0
J3	VMV7
J4	IO215NDB7V3
J5	IO215PDB7V3
J6	IO214PDB7V3
J7	IO214NDB7V3
J8	$V_{CCI}B7$
J9	V_{CC}
J10	V_{CC}
J11	V_{CC}
J12	V_{CC}
J13	V_{CC}
J14	V_{CC}
J15	V_{CC}
J16	V_{CC}
J17	V_{CC}
J18	V_{CC}
J19	$V_{CCI}B2$
J20	IO62PDB2V0
J21	IO62NDB2V0
J22	IO70NDB2V1
J23	IO69NDB2V1
J24	VMV2
J25	IO80PDB2V3
J26	IO80NDB2V3
K1	IO195PDB7V0
K2	IO199NDB7V1
K3	IO199PDB7V1
K4	IO205NDB7V1
K5	IO205PDB7V1
K6	IO217PDB7V3

676-Pin FBGA	
Pin Number	A3PE1500 Function
K7	IO217NDB7V3
K8	$V_{CCI}B7$
K9	V_{CC}
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K15	GND
K16	GND
K17	GND
K18	V_{CC}
K19	$V_{CCI}B2$
K20	IO65PDB2V1
K21	IO65NDB2V1
K22	IO74PDB2V2
K23	IO74NDB2V2
K24	IO75PDB2V2
K25	IO75NDB2V2
K26	IO84PDB2V3
L1	IO195NDB7V0
L2	IO198PPB7V0
L3	GNDQ
L4	IO201PDB7V1
L5	IO201NDB7V1
L6	IO210NDB7V2
L7	IO210PDB7V2
L8	$V_{CCI}B7$
L9	V_{CC}
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L15	GND
L16	GND

676-Pin FBGA		676-Pin FBGA		676-Pin FBGA	
Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function
L17	GND	N1	GFB0/IO191NPB7V0	P11	GND
L18	V$_{CC}$	N2	V$_{COMPLF}$	P12	GND
L19	V$_{CCI}$B2	N3	GFB1/IO191PPB7V0	P13	GND
L20	IO67PDB2V1	N4	IO196PDB7V0	P14	GND
L21	IO67NDB2V1	N5	GFA0/IO190NDB6V2	P15	GND
L22	IO71PDB2V2	N6	IO200PDB7V1	P16	GND
L23	IO71NDB2V2	N7	IO200NDB7V1	P17	GND
L24	GNDQ	N8	V$_{CCI}$B7	P18	V$_{CC}$
L25	IO82PDB2V3	N9	V$_{CC}$	P19	V$_{CCI}$B3
L26	IO84NDB2V3	N10	GND	P20	GCC0/IO85NDB2V3
M1	IO198NPB7V0	N11	GND	P21	GCC1/IO85PDB2V3
M2	IO202PDB7V1	N12	GND	P22	GCB1/IO86PPB2V3
M3	IO202NDB7V1	N13	GND	P23	IO88NPB3V0
M4	IO206NDB7V1	N14	GND	P24	GCA1/IO87PDB3V0
M5	IO206PDB7V1	N15	GND	P25	V$_{CCPLC}$
M6	IO204NDB7V1	N16	GND	P26	V$_{COMPLC}$
M7	IO204PDB7V1	N17	GND	R1	IO189NDB6V2
M8	V$_{CCI}$B7	N18	V$_{CC}$	R2	IO185PDB6V2
M9	V$_{CC}$	N19	V$_{CCI}$B2	R3	IO187NPB6V2
M10	GND	N20	IO79PDB2V3	R4	IO193NPB7V0
M11	GND	N21	IO79NDB2V3	R5	GFC2/IO187PPB6V2
M12	GND	N22	GCA2/IO88PPB3V0	R6	GFC1/IO192PDB7V0
M13	GND	N23	IO81NPB2V3	R7	GFC0/IO192NDB7V0
M14	GND	N24	GCA0/IO87NDB3V0	R8	V$_{CCI}$B6
M15	GND	N25	GCB0/IO86NPB2V3	R9	V$_{CC}$
M16	GND	N26	IO83NDB2V3	R10	GND
M17	GND	P1	GFA2/IO189PDB6V2	R11	GND
M18	V$_{CC}$	P2	V$_{CCPLF}$	R12	GND
M19	V$_{CCI}$B2	P3	IO193PPB7V0	R13	GND
M20	IO73NDB2V2	P4	IO196NDB7V0	R14	GND
M21	IO73PDB2V2	P5	GFA1/IO190PDB6V2	R15	GND
M22	IO81PPB2V3	P6	IO194PDB7V0	R16	GND
M23	IO77PDB2V2	P7	IO194NDB7V0	R17	GND
M24	IO77NDB2V2	P8	V$_{CCI}$B6	R18	V$_{CC}$
M25	IO82NDB2V3	P9	V$_{CC}$	R19	V$_{CCI}$B3
M26	IO83PDB2V3	P10	GND	R20	NC

676-Pin FBGA		676-Pin FBGA		676-Pin FBGA	
Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function	Pin Number	A3PE1500 Function
R21	IO89NDB3V0	U5	IO182PDB6V1	V15	V_{CC}
R22	GCB2/IO89PDB3V0	U6	IO178PDB6V1	V16	V_{CC}
R23	IO90NDB3V0	U7	IO178NDB6V1	V17	V_{CC}
R24	GCC2/IO90PDB3V0	U8	$V_{CCI}B6$	V18	V_{CC}
R25	IO91PDB3V0	U9	V_{CC}	V19	$V_{CCI}B3$
R26	IO91NDB3V0	U10	GND	V20	IO107PDB3V2
T1	IO186PDB6V2	U11	GND	V21	IO107NDB3V2
T2	IO185NDB6V2	U12	GND	V22	IO103NDB3V2
T3	GNDQ	U13	GND	V23	IO103PDB3V2
T4	IO180PDB6V1	U14	GND	V24	VMV3
T5	IO180NDB6V1	U15	GND	V25	IO95NDB3V1
T6	IO188NDB6V2	U16	GND	V26	IO94PDB3V0
T7	GFB2/IO188PDB6V2	U17	GND	W1	IO179NDB6V1
T8	$V_{CCI}B6$	U18	V_{CC}	W2	IO179PDB6V1
T9	V_{CC}	U19	$V_{CCI}B3$	W3	IO177NDB6V1
T10	GND	U20	NC	W4	IO177PDB6V1
T11	GND	U21	IO101NDB3V1	W5	IO172PDB6V0
T12	GND	U22	IO101PDB3V1	W6	IO172NDB6V0
T13	GND	U23	IO92NDB3V0	W7	V_{CC}
T14	GND	U24	IO92PDB3V0	W8	V_{CC}
T15	GND	U25	IO95PDB3V1	W9	$V_{CCI}B5$
T16	GND	U26	IO93NPB3V0	W10	$V_{CCI}B5$
T17	GND	V1	IO183PDB6V2	W11	$V_{CCI}B5$
T18	V_{CC}	V2	IO183NDB6V2	W12	$V_{CCI}B5$
T19	$V_{CCI}B3$	V3	VMV6	W13	$V_{CCI}B5$
T20	IO99PDB3V1	V4	IO181PDB6V1	W14	$V_{CCI}B4$
T21	IO99NDB3V1	V5	IO181NDB6V1	W15	$V_{CCI}B4$
T22	IO97PDB3V1	V6	IO176PDB6V1	W16	$V_{CCI}B4$
T23	IO97NDB3V1	V7	IO176NDB6V1	W17	$V_{CCI}B4$
T24	GNDQ	V8	$V_{CCI}B6$	W18	$V_{CCI}B4$
T25	IO93PPB3V0	V9	V_{CC}	W19	V_{CC}
T26	NC	V10	V_{CC}	W20	$V_{CCI}B3$
U1	IO186NDB6V2	V11	V_{CC}	W21	GDB0/IO109NDB3V2
U2	IO184NDB6V2	V12	V_{CC}	W22	GDB1/IO109PDB3V2
U3	IO184PDB6V2	V13	V_{CC}	W23	IO105NDB3V2
U4	IO182NDB6V1	V14	V_{CC}	W24	IO105PDB3V2

676-Pin FBGA	
Pin Number	A3PE1500 Function
W25	IO96PDB3V1
W26	IO94NDB3V0
Y1	IO175NDB6V1
Y2	IO175PDB6V1
Y3	IO173NDB6V0
Y4	IO173PDB6V0
Y5	GEC1/IO169PPB6V0
Y6	GNDQ
Y7	VMV6
Y8	$V_{CCI}B5$
Y9	IO163NDB5V3
Y10	IO159PDB5V3
Y11	IO153PDB5V2
Y12	IO147PDB5V1
Y13	IO139PDB5V0
Y14	IO137PDB5V0
Y15	IO125NDB4V1
Y16	IO125PDB4V1
Y17	IO115NDB4V0
Y18	IO115PDB4V0
Y19	V_{CC}
Y20	V_{PUMP}
Y21	V_{COMPLD}
Y22	V_{CCPLD}
Y23	IO100NDB3V1
Y24	IO100PDB3V1
Y25	IO96NDB3V1
Y26	IO98PDB3V1

896-Pin FBGA
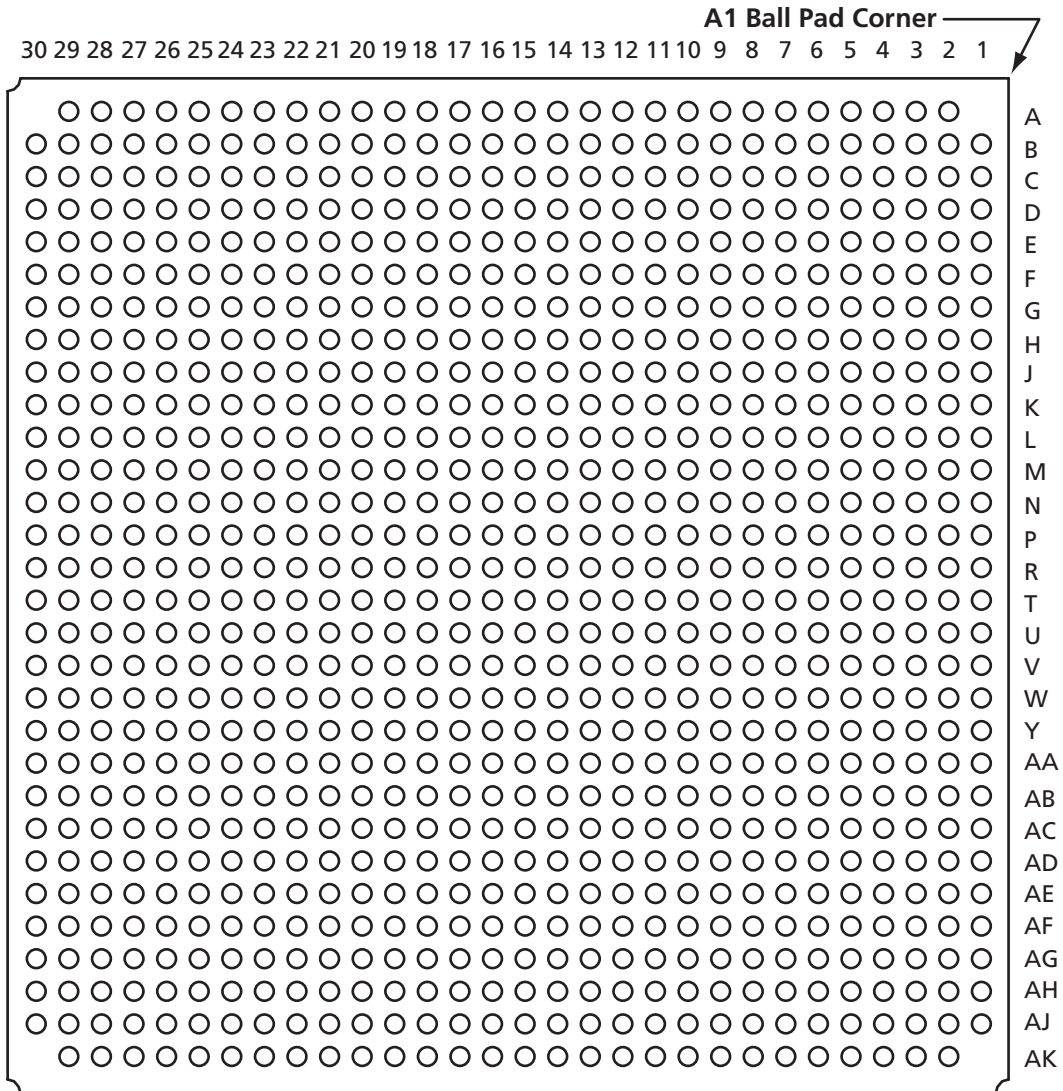
A1 Ball Pad Corner

30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

896-Pin FBGA		896-Pin FBGA		896-Pin FBGA	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
A2	GND	AA9	GEB1/IO235PPB6V0	AB15	IO198PDB5V0
A3	GND	AA10	V$_{CC}$	AB16	IO192NDB4V4
A4	IO14NPB0V1	AA11	IO226PPB5V4	AB17	IO192PDB4V4
A5	GND	AA12	V$_{CCI}$B5	AB18	IO178NDB4V3
A6	IO07NPB0V0	AA13	V$_{CCI}$B5	AB19	IO178PDB4V3
A7	GND	AA14	V$_{CCI}$B5	AB20	IO174NDB4V2
A8	IO09NDB0V1	AA15	V$_{CCI}$B5	AB21	IO162NPB4V1
A9	IO17NDB0V2	AA16	V$_{CCI}$B4	AB22	V$_{CC}$
A10	IO17PDB0V2	AA17	V$_{CCI}$B4	AB23	V$_{CCPLD}$
A11	IO21NDB0V2	AA18	V$_{CCI}$B4	AB24	V$_{CCI}$B3
A12	IO21PDB0V2	AA19	V$_{CCI}$B4	AB25	IO150PDB3V4
A13	IO33NDB0V4	AA20	IO174PDB4V2	AB26	IO148PDB3V4
A14	IO33PDB0V4	AA21	V$_{CC}$	AB27	IO147NDB3V4
A15	IO35NDB0V4	AA22	IO142NPB3V3	AB28	IO145PDB3V3
A16	IO35PDB0V4	AA23	IO144NDB3V3	AB29	IO143PDB3V3
A17	IO41NDB1V0	AA24	IO144PDB3V3	AB30	IO137PDB3V2
A18	IO43NDB1V0	AA25	IO146NDB3V4	AC1	IO254PDB6V2
A19	IO43PDB1V0	AA26	IO146PDB3V4	AC2	IO254NDB6V2
A20	IO45NDB1V0	AA27	IO147PDB3V4	AC3	IO240PDB6V0
A21	IO45PDB1V0	AA28	IO139NDB3V3	AC4	GEC1/IO236PDB6V0
A22	IO57NDB1V2	AA29	IO139PDB3V3	AC5	IO237PDB6V0
A23	IO57PDB1V2	AA30	IO133NDB3V2	AC6	IO237NDB6V0
A24	GND	AB1	IO256NDB6V2	AC7	V$_{COMPLE}$
A25	IO69PPB1V3	AB2	IO244PDB6V1	AC8	GND
A26	GND	AB3	IO244NDB6V1	AC9	IO226NPB5V4
A27	GBC1/IO79PPB1V4	AB4	IO241PDB6V0	AC10	IO222NDB5V3
A28	GND	AB5	IO241NDB6V0	AC11	IO216NPB5V2
A29	GND	AB6	IO243NPB6V1	AC12	IO210NPB5V2
AA1	IO256PDB6V2	AB7	V$_{CCI}$B6	AC13	IO204NDB5V1
AA2	IO248PDB6V1	AB8	V$_{CCPLE}$	AC14	IO204PDB5V1
AA3	IO248NDB6V1	AB9	V$_{CC}$	AC15	IO194NDB5V0
AA4	IO246NDB6V1	AB10	IO222PDB5V3	AC16	IO188NDB4V4
AA5	GEA1/IO234PDB6V0	AB11	IO218PPB5V3	AC17	IO188PDB4V4
AA6	GEA0/IO234NDB6V0	AB12	IO206NDB5V1	AC18	IO182PPB4V3
AA7	IO243PPB6V1	AB13	IO206PDB5V1	AC19	IO170NPB4V2
AA8	IO245NDB6V1	AB14	IO198NDB5V0	AC20	IO164NDB4V1

896-Pin FBGA		896-Pin FBGA		896-Pin FBGA	
Pin Number	**A3PE3000 Function**	**Pin Number**	**A3PE3000 Function**	**Pin Number**	**A3PE3000 Function**
AC21	IO164PDB4V1	AD27	GDA0/IO153NDB3V4	AF3	V$_{CCI}$B6
AC22	IO162PPB4V1	AD28	GDC0/IO151NDB3V4	AF4	IO220NPB5V3
AC23	GND	AD29	GDC1/IO151PDB3V4	AF5	V$_{CC}$
AC24	V$_{COMPLD}$	AD30	GND	AF6	IO228NDB5V4
AC25	IO150NDB3V4	AE1	IO242PPB6V1	AF7	V$_{CCI}$B5
AC26	IO148NDB3V4	AE2	V$_{CC}$	AF8	IO230PDB5V4
AC27	GDA1/IO153PDB3V4	AE3	IO239PDB6V0	AF9	IO229NDB5V4
AC28	IO145NDB3V3	AE4	IO239NDB6V0	AF10	IO229PDB5V4
AC29	IO143NDB3V3	AE5	VMV6	AF11	IO214PPB5V2
AC30	IO137NDB3V2	AE6	GND	AF12	IO208NDB5V1
AD1	GND	AE7	GNDQ	AF13	IO208PDB5V1
AD2	IO242NPB6V1	AE8	IO230NDB5V4	AF14	IO200PDB5V0
AD3	IO240NDB6V0	AE9	IO224NPB5V3	AF15	IO196NDB5V0
AD4	GEC0/IO236NDB6V0	AE10	IO214NPB5V2	AF16	IO186NDB4V4
AD5	V$_{CCI}$B6	AE11	IO212NDB5V2	AF17	IO186PDB4V4
AD6	GNDQ	AE12	IO212PDB5V2	AF18	IO180NDB4V3
AD7	V$_{CC}$	AE13	IO202NPB5V1	AF19	IO180PDB4V3
AD8	VMV5	AE14	IO200NDB5V0	AF20	IO168NDB4V1
AD9	V$_{CCI}$B5	AE15	IO196PDB5V0	AF21	IO168PDB4V1
AD10	IO224PPB5V3	AE16	IO190NDB4V4	AF22	IO160NDB4V0
AD11	IO218NPB5V3	AE17	IO184PDB4V3	AF23	IO158NPB4V0
AD12	IO216PPB5V2	AE18	IO184NDB4V3	AF24	V$_{CCI}$B4
AD13	IO210PPB5V2	AE19	IO172PDB4V2	AF25	IO154NPB4V0
AD14	IO202PPB5V1	AE20	IO172NDB4V2	AF26	V$_{CC}$
AD15	IO194PDB5V0	AE21	IO166NDB4V1	AF27	TDO
AD16	IO190PDB4V4	AE22	IO160PDB4V0	AF28	V$_{CCI}$B3
AD17	IO182NPB4V3	AE23	GNDQ	AF29	GNDQ
AD18	IO176NDB4V2	AE24	VMV4	AF30	GND
AD19	IO176PDB4V2	AE25	GND	AG1	IO238NPB6V0
AD20	IO170PPB4V2	AE26	GDB0/IO152NDB3V4	AG2	V$_{CC}$
AD21	IO166PDB4V1	AE27	GDB1/IO152PDB3V4	AG3	IO232NPB5V4
AD22	V$_{CCI}$B4	AE28	VMV3	AG4	GND
AD23	TCK	AE29	V$_{CC}$	AG5	IO220PPB5V3
AD24	V$_{CC}$	AE30	IO149PDB3V4	AG6	IO228PDB5V4
AD25	TRST	AF1	GND	AG7	IO231NDB5V4
AD26	V$_{CCI}$B3	AF2	IO238PPB6V0	AG8	GEC2/IO231PDB5V4

896-Pin FBGA		896-Pin FBGA		896-Pin FBGA	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
AG9	IO225NPB5V3	AH15	IO195NDB5V0	AJ21	IO173PDB4V2
AG10	IO223NPB5V3	AH16	IO185NDB4V3	AJ22	IO163NDB4V1
AG11	IO221PDB5V3	AH17	IO185PDB4V3	AJ23	IO163PDB4V1
AG12	IO221NDB5V3	AH18	IO181PDB4V3	AJ24	IO167NPB4V1
AG13	IO205NPB5V1	AH19	IO177NDB4V2	AJ25	V_{CC}
AG14	IO199NDB5V0	AH20	IO171NPB4V2	AJ26	IO156NPB4V0
AG15	IO199PDB5V0	AH21	IO165PPB4V1	AJ27	V_{CC}
AG16	IO187NDB4V4	AH22	IO161PPB4V0	AJ28	TMS
AG17	IO187PDB4V4	AH23	IO157NDB4V0	AJ29	GND
AG18	IO181NDB4V3	AH24	IO157PDB4V0	AJ30	GND
AG19	IO171PPB4V2	AH25	IO155NDB4V0	AK2	GND
AG20	IO165NPB4V1	AH26	$V_{CCI}B4$	AK3	GND
AG21	IO161NPB4V0	AH27	TDI	AK4	IO217PPB5V2
AG22	IO159NDB4V0	AH28	V_{CC}	AK5	GND
AG23	IO159PDB4V0	AH29	V_{PUMP}	AK6	IO215PPB5V2
AG24	IO158PPB4V0	AH30	GND	AK7	GND
AG25	GDB2/IO155PDB4V0	AJ1	GND	AK8	IO207NDB5V1
AG26	GDA2/IO154PPB4V0	AJ2	GND	AK9	IO207PDB5V1
AG27	GND	AJ3	GEA2/IO233PPB5V4	AK10	IO201NDB5V0
AG28	V_{JTAG}	AJ4	V_{CC}	AK11	IO201PDB5V0
AG29	V_{CC}	AJ5	IO217NPB5V2	AK12	IO193NDB4V4
AG30	IO149NDB3V4	AJ6	V_{CC}	AK13	IO193PDB4V4
AH1	GND	AJ7	IO215NPB5V2	AK14	IO197PDB5V0
AH2	IO233NPB5V4	AJ8	IO213NDB5V2	AK15	IO191NDB4V4
AH3	V_{CC}	AJ9	IO213PDB5V2	AK16	IO191PDB4V4
AH4	GEB2/IO232PPB5V4	AJ10	IO209NDB5V1	AK17	IO189NDB4V4
AH5	$V_{CCI}B5$	AJ11	IO209PDB5V1	AK18	IO189PDB4V4
AH6	IO219NDB5V3	AJ12	IO203NDB5V1	AK19	IO179PPB4V3
AH7	IO219PDB5V3	AJ13	IO203PDB5V1	AK20	IO175NDB4V2
AH8	IO227NDB5V4	AJ14	IO197NDB5V0	AK21	IO175PDB4V2
AH9	IO227PDB5V4	AJ15	IO195PDB5V0	AK22	IO169NDB4V1
AH10	IO225PPB5V3	AJ16	IO183NDB4V3	AK23	IO169PDB4V1
AH11	IO223PPB5V3	AJ17	IO183PDB4V3	AK24	GND
AH12	IO211NDB5V2	AJ18	IO179NPB4V3	AK25	IO167PPB4V1
AH13	IO211PDB5V2	AJ19	IO177PDB4V2	AK26	GND
AH14	IO205PPB5V1	AJ20	IO173NDB4V2	AK27	GDC2/IO156PPB4V0

896-Pin FBGA	
Pin Number	A3PE3000 Function
AK28	GND
AK29	GND
B1	GND
B2	GND
B3	GAA2/IO309PPB7V4
B4	V_{CC}
B5	IO14PPB0V1
B6	V_{CC}
B7	IO07PPB0V0
B8	IO09PDB0V1
B9	IO15PPB0V1
B10	IO19NDB0V2
B11	IO19PDB0V2
B12	IO29NDB0V3
B13	IO29PDB0V3
B14	IO31PPB0V3
B15	IO37NDB0V4
B16	IO37PDB0V4
B17	IO41PDB1V0
B18	IO51NDB1V1
B19	IO59PDB1V2
B20	IO53PDB1V1
B21	IO53NDB1V1
B22	IO61NDB1V2
B23	IO61PDB1V2
B24	IO69NPB1V3
B25	V_{CC}
B26	GBC0/IO79NPB1V4
B27	V_{CC}
B28	IO64NPB1V2
B29	GND
B30	GND
C1	GND
C2	IO309NPB7V4
C3	V_{CC}
C4	GAA0/IO00NPB0V0

896-Pin FBGA	
Pin Number	A3PE3000 Function
C5	V_{CCI}B0
C6	IO03PDB0V0
C7	IO03NDB0V0
C8	GAB1/IO01PDB0V0
C9	IO05PDB0V0
C10	IO15NPB0V1
C11	IO25NDB0V3
C12	IO25PDB0V3
C13	IO31NPB0V3
C14	IO27NDB0V3
C15	IO39NDB0V4
C16	IO39PDB0V4
C17	IO55PPB1V1
C18	IO51PDB1V1
C19	IO59NDB1V2
C20	IO63NDB1V2
C21	IO63PDB1V2
C22	IO67NDB1V3
C23	IO67PDB1V3
C24	IO75NDB1V4
C25	IO75PDB1V4
C26	V_{CCI}B1
C27	IO64PPB1V2
C28	V_{CC}
C29	GBA1/IO81PPB1V4
C30	GND
D1	IO303PPB7V3
D2	V_{CC}
D3	IO305NPB7V3
D4	GND
D5	GAA1/IO00PPB0V0
D6	GAC1/IO02PDB0V0
D7	IO06NPB0V0
D8	GAB0/IO01NDB0V0
D9	IO05NDB0V0
D10	IO11NDB0V1

896-Pin FBGA	
Pin Number	A3PE3000 Function
D11	IO11PDB0V1
D12	IO23NDB0V2
D13	IO23PDB0V2
D14	IO27PDB0V3
D15	IO40PDB0V4
D16	IO47NDB1V0
D17	IO47PDB1V0
D18	IO55NPB1V1
D19	IO65NDB1V3
D20	IO65PDB1V3
D21	IO71NDB1V3
D22	IO71PDB1V3
D23	IO73NDB1V4
D24	IO73PDB1V4
D25	IO74NDB1V4
D26	GBB0/IO80NPB1V4
D27	GND
D28	GBA0/IO81NPB1V4
D29	V_{CC}
D30	GBA2/IO82PPB2V0
E1	GND
E2	IO303NPB7V3
E3	V_{CCI}B7
E4	IO305PPB7V3
E5	V_{CC}
E6	GAC0/IO02NDB0V0
E7	V_{CCI}B0
E8	IO06PPB0V0
E9	IO24NDB0V2
E10	IO24PDB0V2
E11	IO13NDB0V1
E12	IO13PDB0V1
E13	IO34NDB0V4
E14	IO34PDB0V4
E15	IO40NDB0V4
E16	IO49NDB1V1

896-Pin FBGA		896-Pin FBGA		896-Pin FBGA	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
E17	IO49PDB1V1	F23	IO72PDB1V3	G29	IO100PPB2V2
E18	IO50PDB1V1	F24	GNDQ	G30	GND
E19	IO58PDB1V2	F25	GND	H1	IO294PDB7V2
E20	IO60NDB1V2	F26	VMV2	H2	IO294NDB7V2
E21	IO77PDB1V4	F27	IO86PDB2V0	H3	IO300NDB7V3
E22	IO68NDB1V3	F28	IO92PDB2V1	H4	IO300PDB7V3
E23	IO68PDB1V3	F29	V_{CC}	H5	IO295PDB7V2
E24	$V_{CCI}B1$	F30	IO100NPB2V2	H6	IO299PDB7V3
E25	IO74PDB1V4	G1	GND	H7	V_{COMPLA}
E26	V_{CC}	G2	IO296NPB7V2	H8	GND
E27	GBB1/IO80PPB1V4	G3	IO306NDB7V4	H9	IO08NDB0V0
E28	$V_{CCI}B2$	G4	IO297NDB7V2	H10	IO08PDB0V0
E29	IO82NPB2V0	G5	$V_{CCI}B7$	H11	IO18PDB0V2
E30	GND	G6	GNDQ	H12	IO26NPB0V3
F1	IO296PPB7V2	G7	V_{CC}	H13	IO28NDB0V3
F2	V_{CC}	G8	VMV0	H14	IO28PDB0V3
F3	IO306PDB7V4	G9	$V_{CCI}B0$	H15	IO38PPB0V4
F4	IO297PDB7V2	G10	IO10NDB0V1	H16	IO42NDB1V0
F5	VMV7	G11	IO16NDB0V1	H17	IO52NDB1V1
F6	GND	G12	IO22PDB0V2	H18	IO52PDB1V1
F7	GNDQ	G13	IO26PPB0V3	H19	IO62NDB1V2
F8	IO12NDB0V1	G14	IO38NPB0V4	H20	IO62PDB1V2
F9	IO12PDB0V1	G15	IO36NDB0V4	H21	IO70NDB1V3
F10	IO10PDB0V1	G16	IO46NDB1V0	H22	IO70PDB1V3
F11	IO16PDB0V1	G17	IO46PDB1V0	H23	GND
F12	IO22NDB0V2	G18	IO56NDB1V1	H24	V_{COMPLB}
F13	IO30NDB0V3	G19	IO56PDB1V1	H25	GBC2/IO84PDB2V0
F14	IO30PDB0V3	G20	IO66NDB1V3	H26	IO84NDB2V0
F15	IO36PDB0V4	G21	IO66PDB1V3	H27	IO96PDB2V1
F16	IO48NDB1V0	G22	$V_{CCI}B1$	H28	IO96NDB2V1
F17	IO48PDB1V0	G23	VMV1	H29	IO89PDB2V0
F18	IO50NDB1V1	G24	V_{CC}	H30	IO89NDB2V0
F19	IO58NDB1V2	G25	GNDQ	J1	IO290NDB7V2
F20	IO60PDB1V2	G26	$V_{CCI}B2$	J2	IO290PDB7V2
F21	IO77NDB1V4	G27	IO86NDB2V0	J3	IO302NDB7V3
F22	IO72NDB1V3	G28	IO92NDB2V1	J4	IO302PDB7V3

896-Pin FBGA		896-Pin FBGA		896-Pin FBGA	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
J5	IO295NDB7V2	K11	IO04PPB0V0	L17	V_{CC}
J6	IO299NDB7V3	K12	$V_{CCI}B0$	L18	V_{CC}
J7	$V_{CCI}B7$	K13	$V_{CCI}B0$	L19	V_{CC}
J8	V_{CCPLA}	K14	$V_{CCI}B0$	L20	V_{CC}
J9	V_{CC}	K15	$V_{CCI}B0$	L21	IO78NPB1V4
J10	IO04NPB0V0	K16	$V_{CCI}B1$	L22	IO104NPB2V2
J11	IO18NDB0V2	K17	$V_{CCI}B1$	L23	IO98NDB2V2
J12	IO20NDB0V2	K18	$V_{CCI}B1$	L24	IO98PDB2V2
J13	IO20PDB0V2	K19	$V_{CCI}B1$	L25	IO87PDB2V0
J14	IO32NDB0V3	K20	IO76PPB1V4	L26	IO87NDB2V0
J15	IO32PDB0V3	K21	V_{CC}	L27	IO97PDB2V1
J16	IO42PDB1V0	K22	IO78PPB1V4	L28	IO101PDB2V2
J17	IO44NDB1V0	K23	IO88NDB2V0	L29	IO103PDB2V2
J18	IO44PDB1V0	K24	IO88PDB2V0	L30	IO119NDB3V0
J19	IO54NDB1V1	K25	IO94PDB2V1	M1	IO282NDB7V1
J20	IO54PDB1V1	K26	IO94NDB2V1	M2	IO282PDB7V1
J21	IO76NPB1V4	K27	IO85PDB2V0	M3	IO292NDB7V2
J22	V_{CC}	K28	IO85NDB2V0	M4	IO292PDB7V2
J23	V_{CCPLB}	K29	IO93PDB2V1	M5	IO283NDB7V1
J24	$V_{CCI}B2$	K30	IO93NDB2V1	M6	IO285PDB7V1
J25	IO90PDB2V1	L1	IO286NDB7V1	M7	IO287PDB7V1
J26	IO90NDB2V1	L2	IO286PDB7V1	M8	IO289PDB7V1
J27	GBB2/IO83PDB2V0	L3	IO298NDB7V3	M9	IO289NDB7V1
J28	IO83NDB2V0	L4	IO298PDB7V3	M10	$V_{CCI}B7$
J29	IO91PDB2V1	L5	IO283PDB7V1	M11	V_{CC}
J30	IO91NDB2V1	L6	IO291NDB7V2	M12	GND
K1	IO288NDB7V1	L7	IO291PDB7V2	M13	GND
K2	IO288PDB7V1	L8	IO293PDB7V2	M14	GND
K3	IO304NDB7V3	L9	IO293NDB7V2	M15	GND
K4	IO304PDB7V3	L10	IO307NPB7V4	M16	GND
K5	GAB2/IO308PDB7V4	L11	V_{CC}	M17	GND
K6	IO308NDB7V4	L12	V_{CC}	M18	GND
K7	IO301PDB7V3	L13	V_{CC}	M19	GND
K8	IO301NDB7V3	L14	V_{CC}	M20	V_{CC}
K9	GAC2/IO307PPB7V4	L15	V_{CC}	M21	$V_{CCI}B2$
K10	V_{CC}	L16	V_{CC}	M22	NC

896-Pin FBGA	
Pin Number	A3PE3000 Function
M23	IO104PPB2V2
M24	IO102PDB2V2
M25	IO102NDB2V2
M26	IO95PDB2V1
M27	IO97NDB2V1
M28	IO101NDB2V2
M29	IO103NDB2V2
M30	IO119PDB3V0
N1	IO276PDB7V0
N2	IO278PDB7V0
N3	IO280PDB7V0
N4	IO284PDB7V1
N5	IO279PDB7V0
N6	IO285NDB7V1
N7	IO287NDB7V1
N8	IO281NDB7V0
N9	IO281PDB7V0
N10	$V_{CCI}B7$
N11	V_{CC}
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
N18	GND
N19	GND
N20	V_{CC}
N21	$V_{CCI}B2$
N22	IO106NDB2V3
N23	IO106PDB2V3
N24	IO108PDB2V3
N25	IO108NDB2V3
N26	IO95NDB2V1
N27	IO99NDB2V2
N28	IO99PDB2V2

896-Pin FBGA	
Pin Number	A3PE3000 Function
N29	IO107PDB2V3
N30	IO107NDB2V3
P1	IO276NDB7V0
P2	IO278NDB7V0
P3	IO280NDB7V0
P4	IO284NDB7V1
P5	IO279NDB7V0
P6	GFC1/IO275PDB7V0
P7	GFC0/IO275NDB7V0
P8	IO277PDB7V0
P9	IO277NDB7V0
P10	$V_{CCI}B7$
P11	V_{CC}
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P18	GND
P19	GND
P20	V_{CC}
P21	$V_{CCI}B2$
P22	GCC1/IO112PDB2V3
P23	IO110PDB2V3
P24	IO110NDB2V3
P25	IO109PPB2V3
P26	IO111NPB2V3
P27	IO105PDB2V2
P28	IO105NDB2V2
P29	GCC2/IO117PDB3V0
P30	IO117NDB3V0
R1	GFC2/IO270PDB6V4
R2	GFB1/IO274PPB7V0
R3	V_{COMPLF}
R4	GFA0/IO273NDB6V4

896-Pin FBGA	
Pin Number	A3PE3000 Function
R5	GFB0/IO274NPB7V0
R6	IO271NDB6V4
R7	GFB2/IO271PDB6V4
R8	IO269PDB6V4
R9	IO269NDB6V4
R10	$V_{CCI}B7$
R11	V_{CC}
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R17	GND
R18	GND
R19	GND
R20	V_{CC}
R21	$V_{CCI}B2$
R22	GCC0/IO112NDB2V3
R23	GCB2/IO116PDB3V0
R24	IO118PDB3V0
R25	IO111PPB2V3
R26	IO122PPB3V1
R27	GCA0/IO114NPB3V0
R28	V_{COMPLC}
R29	GCB1/IO113PPB2V3
R30	IO115NPB3V0
T1	IO270NDB6V4
T2	V_{CCPLF}
T3	GFA2/IO272PPB6V4
T4	GFA1/IO273PDB6V4
T5	IO272NPB6V4
T6	IO267NDB6V4
T7	IO267PDB6V4
T8	IO265PDB6V3
T9	IO263PDB6V3
T10	$V_{CCI}B6$

896-Pin FBGA		896-Pin FBGA		896-Pin FBGA	
Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function	Pin Number	A3PE3000 Function
T11	V_{CC}	U17	GND	V23	IO128NDB3V1
T12	GND	U18	GND	V24	IO132PDB3V2
T13	GND	U19	GND	V25	IO130PPB3V2
T14	GND	U20	V_{CC}	V26	IO126NDB3V1
T15	GND	U21	$V_{CCI}B3$	V27	IO129NDB3V1
T16	GND	U22	IO120PDB3V0	V28	IO127NDB3V1
T17	GND	U23	IO128PDB3V1	V29	IO125NDB3V1
T18	GND	U24	IO124PDB3V1	V30	IO123PDB3V1
T19	GND	U25	IO124NDB3V1	W1	IO266NDB6V4
T20	V_{CC}	U26	IO126PDB3V1	W2	IO262NDB6V3
T21	$V_{CCI}B3$	U27	IO129PDB3V1	W3	IO260NDB6V3
T22	IO109NPB2V3	U28	IO127PDB3V1	W4	IO252NDB6V2
T23	IO116NDB3V0	U29	IO125PDB3V1	W5	IO251NDB6V2
T24	IO118NDB3V0	U30	IO121NDB3V0	W6	IO251PDB6V2
T25	IO122NPB3V1	V1	IO268NDB6V4	W7	IO255NDB6V2
T26	GCA1/IO114PPB3V0	V2	IO262PDB6V3	W8	IO249PPB6V1
T27	GCB0/IO113NPB2V3	V3	IO260PDB6V3	W9	IO253PDB6V2
T28	GCA2/IO115PPB3V0	V4	IO252PDB6V2	W10	$V_{CCI}B6$
T29	V_{CCPLC}	V5	IO257NPB6V2	W11	V_{CC}
T30	IO121PDB3V0	V6	IO261NPB6V3	W12	GND
U1	IO268PDB6V4	V7	IO255PDB6V2	W13	GND
U2	IO264NDB6V3	V8	IO259PDB6V3	W14	GND
U3	IO264PDB6V3	V9	IO259NDB6V3	W15	GND
U4	IO258PDB6V3	V10	$V_{CCI}B6$	W16	GND
U5	IO258NDB6V3	V11	V_{CC}	W17	GND
U6	IO257PPB6V2	V12	GND	W18	GND
U7	IO261PPB6V3	V13	GND	W19	GND
U8	IO265NDB6V3	V14	GND	W20	V_{CC}
U9	IO263NDB6V3	V15	GND	W21	$V_{CCI}B3$
U10	$V_{CCI}B6$	V16	GND	W22	IO134PDB3V2
U11	V_{CC}	V17	GND	W23	IO138PDB3V3
U12	GND	V18	GND	W24	IO132NDB3V2
U13	GND	V19	GND	W25	IO136NPB3V2
U14	GND	V20	V_{CC}	W26	IO130NPB3V2
U15	GND	V21	$V_{CCI}B3$	W27	IO141PDB3V3
U16	GND	V22	IO120NDB3V0	W28	IO135PDB3V2

896-Pin FBGA	
Pin Number	**A3PE3000 Function**
W29	IO131PDB3V2
W30	IO123NDB3V1
Y1	IO266PDB6V4
Y2	IO250PDB6V2
Y3	IO250NDB6V2
Y4	IO246PDB6V1
Y5	IO247NDB6V1
Y6	IO247PDB6V1
Y7	IO249NPB6V1
Y8	IO245PDB6V1
Y9	IO253NDB6V2
Y10	GEB0/IO235NPB6V0
Y11	V_{CC}
Y12	V_{CC}
Y13	V_{CC}
Y14	V_{CC}
Y15	V_{CC}
Y16	V_{CC}
Y17	V_{CC}
Y18	V_{CC}
Y19	V_{CC}
Y20	V_{CC}
Y21	IO142PPB3V3
Y22	IO134NDB3V2
Y23	IO138NDB3V3
Y24	IO140NDB3V3
Y25	IO140PDB3V3
Y26	IO136PPB3V2
Y27	IO141NDB3V3
Y28	IO135NDB3V2
Y29	IO131NDB3V2
Y30	IO133PDB3V2

Part Number and Revision Date

Part Number 51700098-003-5
Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.5)	Page
v1.4 (June 2008)	The A3PE600 "484-Pin FBGA" table was missing G22. The pin and its function were added to the table.	3-17
v1.3 (April 2008)	The naming conventions changed for the following pins in the "484-Pin FBGA" for the A3PE600: **Pin Number** **New Function Name** J19 IO45PPB2V1 K20 IO45NPB2V1 M2 IO114NPB6V1 N1 IO114PPB6V1 N4 GFC2/IO115PPB6V1 P3 IO115NPB6V1	3-17
v1.2 (April 2008)	The "324-Pin FBGA" package diagram was replaced.	3-12
v1.1	The following pins had duplicates and the extra pins were deleted from the "208-Pin PQFP" A3PE3000 table: 36, 62, 171 Note: There were no pin function changes in this update.	3-6
	The following pins had duplicates and the extra pins were deleted from the "324-Pin FBGA" table: E2, E3, E16, E17, P2, P3, T16, U17 Note: There were no pin function changes in this update.	3-13
	The "256-Pin FBGA" was updated for the A3PE600 device because the old PAT where based on the IFX die, and this is the final UMC die version.	3-17
	The "484-Pin FBGA" was updated for the A3PE600 device because the old PAT where based on the IFX die, and this is the final UMC die version.	3-17
	The following pins had duplicates and the extra pins were deleted from the "896-Pin FBGA" table: AD6, AE5, AE28, AF29, F5, F26, G6, G25 Note: There were no pin function changes in this update.	3-41
v1.0 (January 2008)	The "208-Pin PQFP" pin table for A3PE3000 was updated.	3-6
	The "324-Pin FBGA" pin table for A3PE3000 is new.	3-13
	The "484-Pin FBGA" pin table for A3PE3000 is new.	3-27
	The "896-Pin FBGA" pin table for A3PE3000 is new.	3-41
v2.1 (July 2007)	This document was previously in datasheet v2.1. As a result of moving to the handbook format, Actel has restarted the version numbers so the new version number is v1.0.	N/A

Previous Version	Changes in Current Version (v1.5)	Page
Advance v0.6 (January 2007)	Notes were added to the package diagrams identifying if they were top or bottom view.	N/A
	The A3PE1500 "208-Pin PQFP" table is new.	4-4
	The A3PE1500 "484-Pin FBGA" table is new.	4-18
	The A3PE1500 "A3PE1500 Function" table is new.	4-24
Advance v0.2	The A3PE3000 "208-Pin PQFP" pin table was updated.	4-6

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Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," "Preliminary," and "Production." The definition of these categories are as follows:

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The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

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