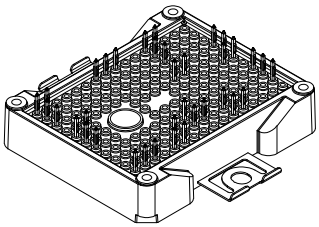
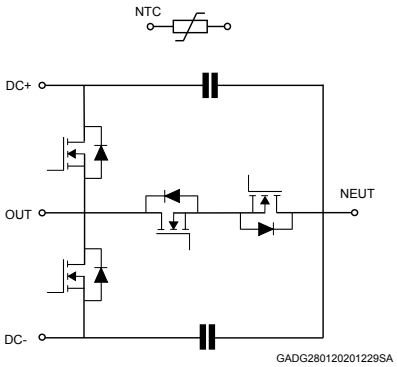
A2U12M12W2-F1C

Datasheet

ACEPACK 2 power module, 3-level topology, 1200 V, 100 A based on SiC Power MOSFET



ACEPACK 2



Features

- ACEPACK 2 power module
  - 13 mΩ of typical $R_{DS(on)}$ each switch (2 dice in parallel per switch)
  - 2.5 kVrms insulation voltage
  - Integrated NTC temperature sensor
  - DC link capacitors between DC BUS and neutral
  - AIN DBC improved thermal performance
  - Press fit contact pins

Applications

- High frequency converters

Description

This ACEPACK 2 power module represents a leg of a T-type 3-level inverter topology that integrates the advanced silicon carbide power MOSFET technology from STMicroelectronics. This module is manufactured using both the innovative properties of the wide bandgap materials and the high thermal performance substrate, which results in exceptional low on-resistance per unit area and excellent switching performance almost independent of temperature. A negative temperature sensor and three DC link capacitors are also included to optimize switching behavior.

Product status link
A2U12M12W2-F1C

Product summary	
Order code	A2U12M12W2-F1C
Marking	A2U12M12W2-F1C
Package	ACEPACK 2
Leads type	Press fit
Packing	Tray

1 Electrical ratings

1.1 Inverter switch

(Every switch is made by two SiC MOSFET in parallel and their gates are shorted during every single test, T_J = 25 °C unless otherwise specified).

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain source voltage	1200	V
V_{GS}	Gate-source voltage	-10 to 22	V
V_{GSop}	Gate-source voltage (recommended operating values)	-5 to 18	V
I_D	Drain current (continuous) at T_C = 25 °C	100	A
I_{DM} (1)	Drain current (pulsed)	200	A
P_{TOT}	Total power dissipation at T_C = 25 °C	326	W
T_J	Maximum junction temperature	175	°C
T_{Jop}	Operating junction temperature range under switching conditions	-40 to 150	°C

1. *Pulse width is limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case, each switch	0.46	°C/W

Table 3. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 18 V, I_D = 90 A		13	17	mΩ
		V_{GS} = 18 V, I_D = 90 A, T_C = 150 °C		20		
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	1.85	3.1	4.9	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 1200 V			200	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = -10 to 22 V			±1	µA
C_{iss}	Input capacitance	V_{DS} = 400 V, f = 1 MHz, V_{GS} = 0 V		7000		pF
C_{oss}	Output capacitance			360		
C_{rss}	Reverse transfer capacitance			60		
R_G	Intrinsic gate resistance	f = 1 MHz, open drain		1		Ω
Q_g	Total gate charge	V_{DS} = 400 V, I_D = 100 A, V_{GS} = -5 V to 18 V		312		nC
Q_{gs}	Gate-source charge			89		
Q_{gd}	Gate-drain charge			108.4		

Table 4. Switching energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}(1)	Turn-on switching energy	V_{DS} = 800 V, I_D = 50 A,	-	1019	-	µJ
E_{off}(1)	Turn-off switching energy	R_G = 3.4 Ω, V_{GS} = -5 to 18 V	-	378	-	

1. *Values are referred to the discrete device SCTW70N120G2V.*

Table 5. Source-drain antiparallel diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage drop	I_{SD} = 50 A, V_{GS} = 0 V	-	2.7	-	V
t_{rr}(1)	Reverse recovery time	I_{SD} = 50 A, V_{DD} = 800 V, V_{GS} = -5 to 18 V	-	11.16	-	ns
Q_{rr}(1)	Reverse recovery charge		-	276	-	nC
I_{RRM}(1)	Reverse recovery current		-	40	-	A

1. *Values are referred to the discrete device SCTW70N120G2V.*

1.2 DC link capacitor (CGA9Q1C0G2J104J280KC)

Table 6. Absolute maximum rating for capacitor

Symbol	Parameter	Value	Unit
V_{MAX}	Maximum DC voltage	630	V
T_{Jop}	Operative temperature range	-40 to 125	°C

Table 7. Electrical characteristics – capacitor

Symbol	Parameter	Value	Unit
C1, C2	Capacitance value	100	nF
	Tolerance	±5	%

1.3 NTC (B57451V5103G362)

Table 8. Absolute maximum ratings for NTC temperature sensor, considered as stand-alone

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{25}	Resistance rating	T = 25 °C		10		kΩ
$\Delta R_{25}/R$	Resistance tolerance		-2		+2	%
R_{100}	Resistance rating	T = 100 °C		674.8		Ω
$\Delta R_{100}/R$	Resistance tolerance		-4.75		4.75	%
$R_{25/50}$	B-value	T=25 °C to 50 °C		3940		K
$R_{25/85}$		T=25 °C to 85 °C		3980		
$R_{25/100}$		T=25 °C to 100 °C (±1%)		4000		
T	Operating temperature range		-40		150	°C

Figure 1. **NTC typical resistance vs temperature**

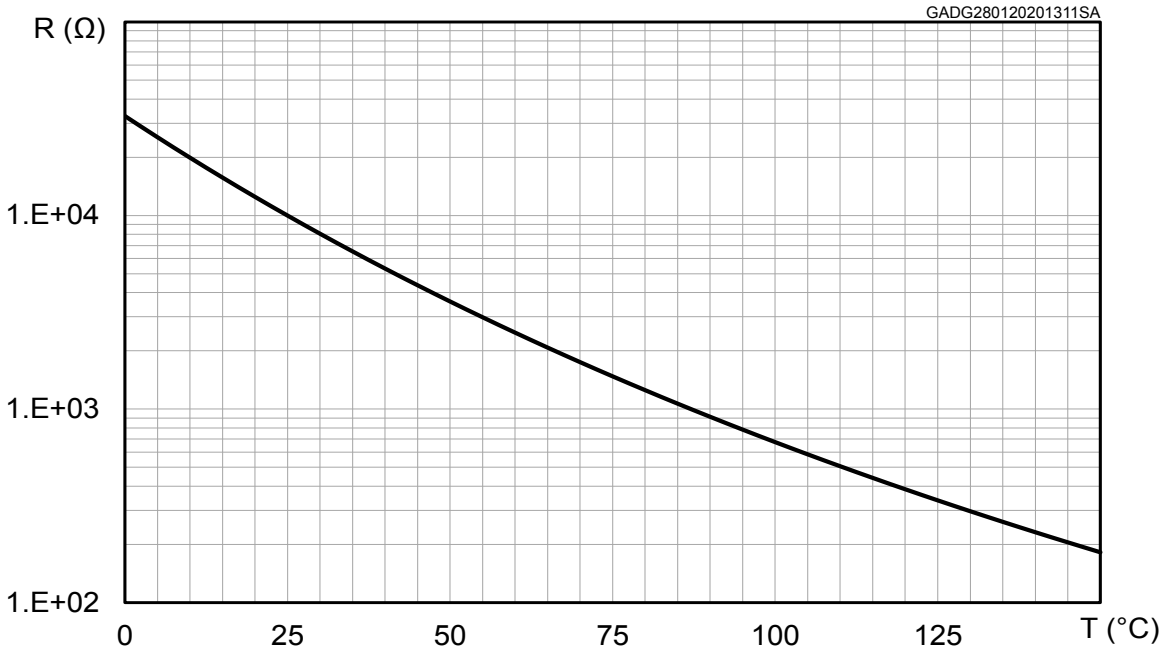
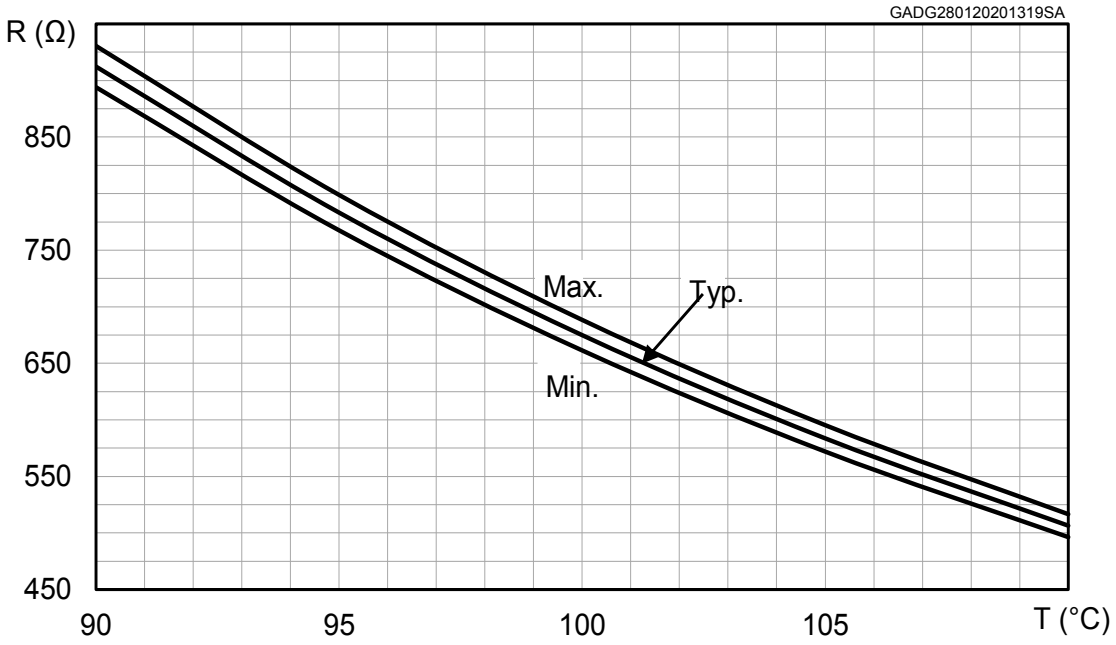


Figure 2. **NTC resistance vs temperature, zoom**



1.4 Package

Table 9. Absolute maximum ratings for ACEPACK 2 package

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{isol}	Isolation voltage			2.5	kV
M_d	Screw mounting torque	40		80	Nm
CTI	Comparative tracking index	200			
L_s	Stray inductance module loop		10		nH
R_s	Module lead resistance, terminals to chip		1		mΩ
T_{stg}	Storage temperature range	-40		125	°C

2 Electrical characteristics (curves)

Every switch is made by two SiC MOSFET in parallel and their gates are shorted during every single test.

Figure 3. Typical output characteristics (T_J = -40 °C)

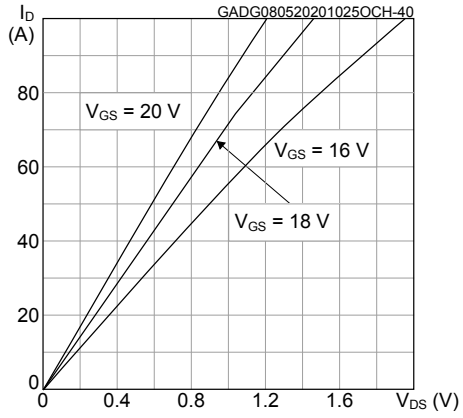


Figure 4. Typical output characteristics (T_J = 25 °C)

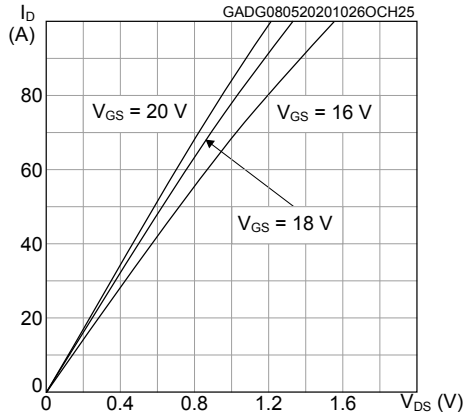


Figure 5. Typical output characteristics (T_J = 150 °C)

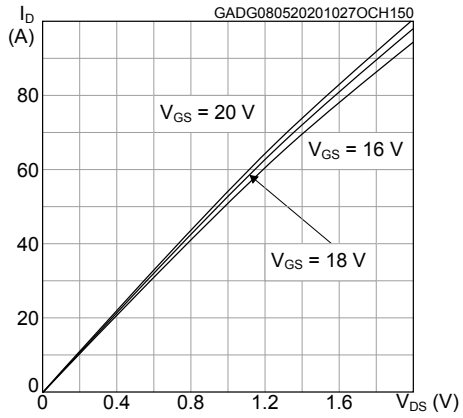


Figure 6. Typical transfer characteristics

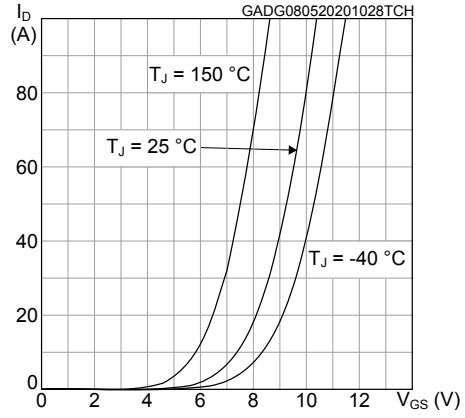


Figure 7. Typical diode foward charcteristics (terminal)

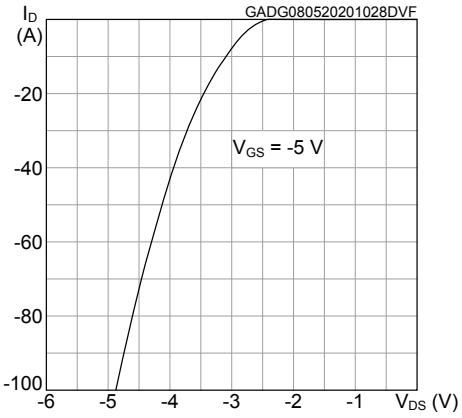
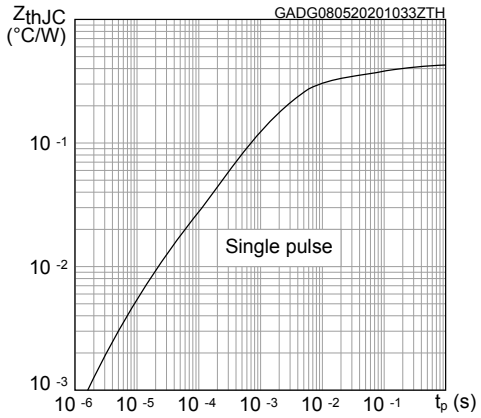


Figure 8. Maximum transient thermal impedance



3 Topology and pin description

Figure 9. **Electrical topology and pin description**

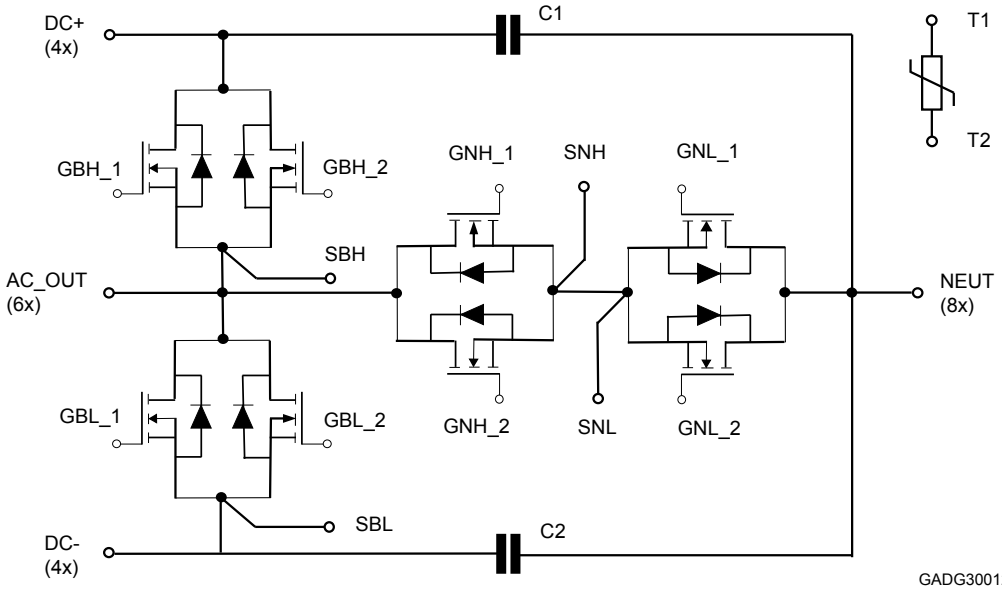
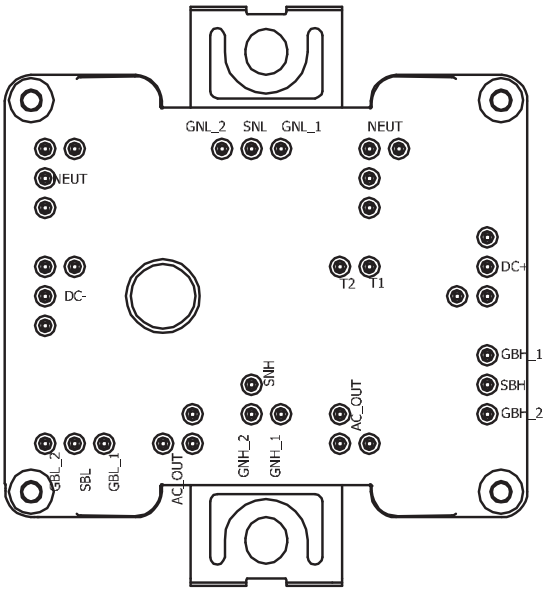


Figure 10. **Package top view with pinout**

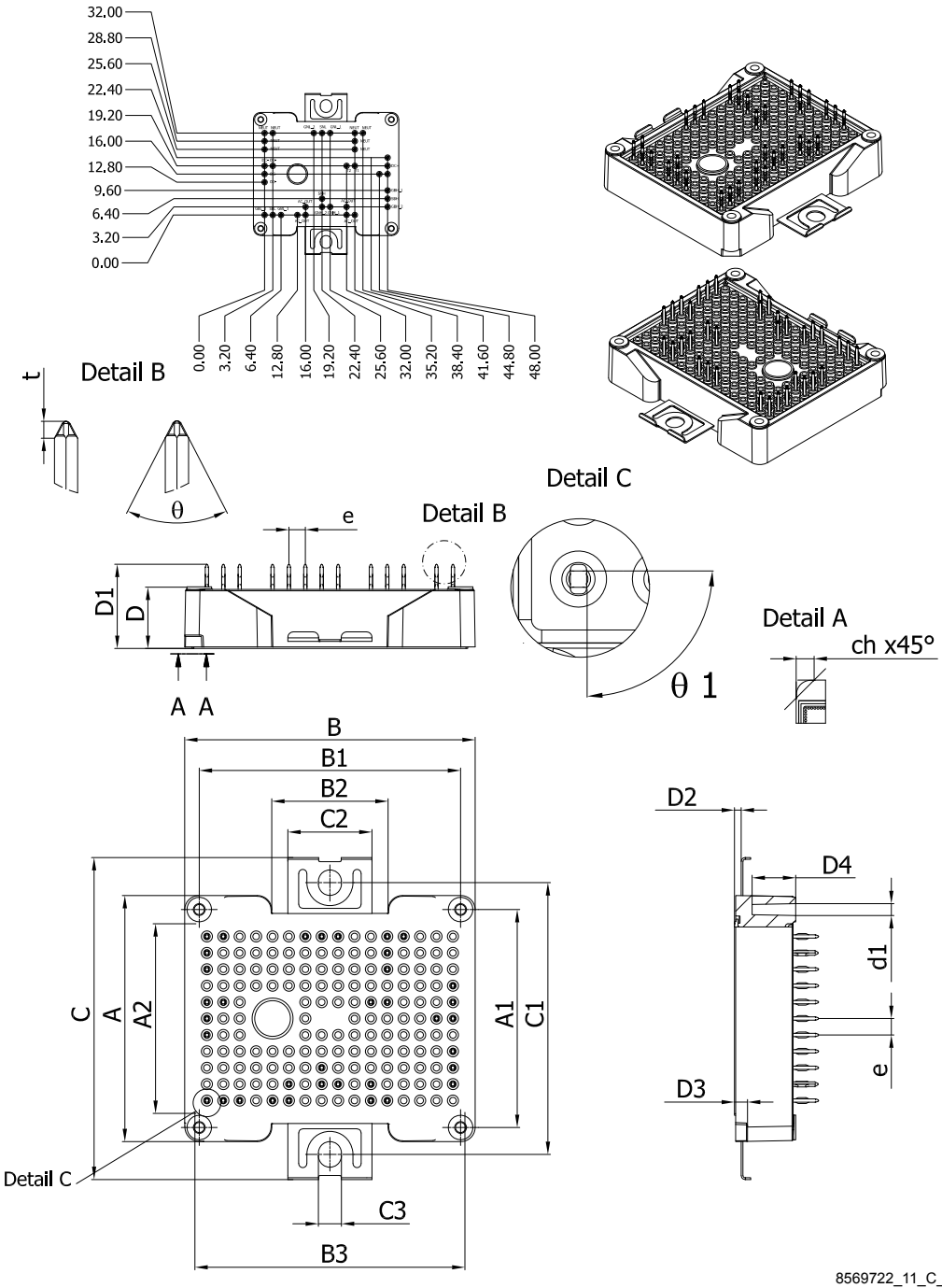


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 ACEPACK 2, 3-level press fit package information

Figure 11. ACEPACK 2, 3-level press fit package outline (dimensions are in mm)

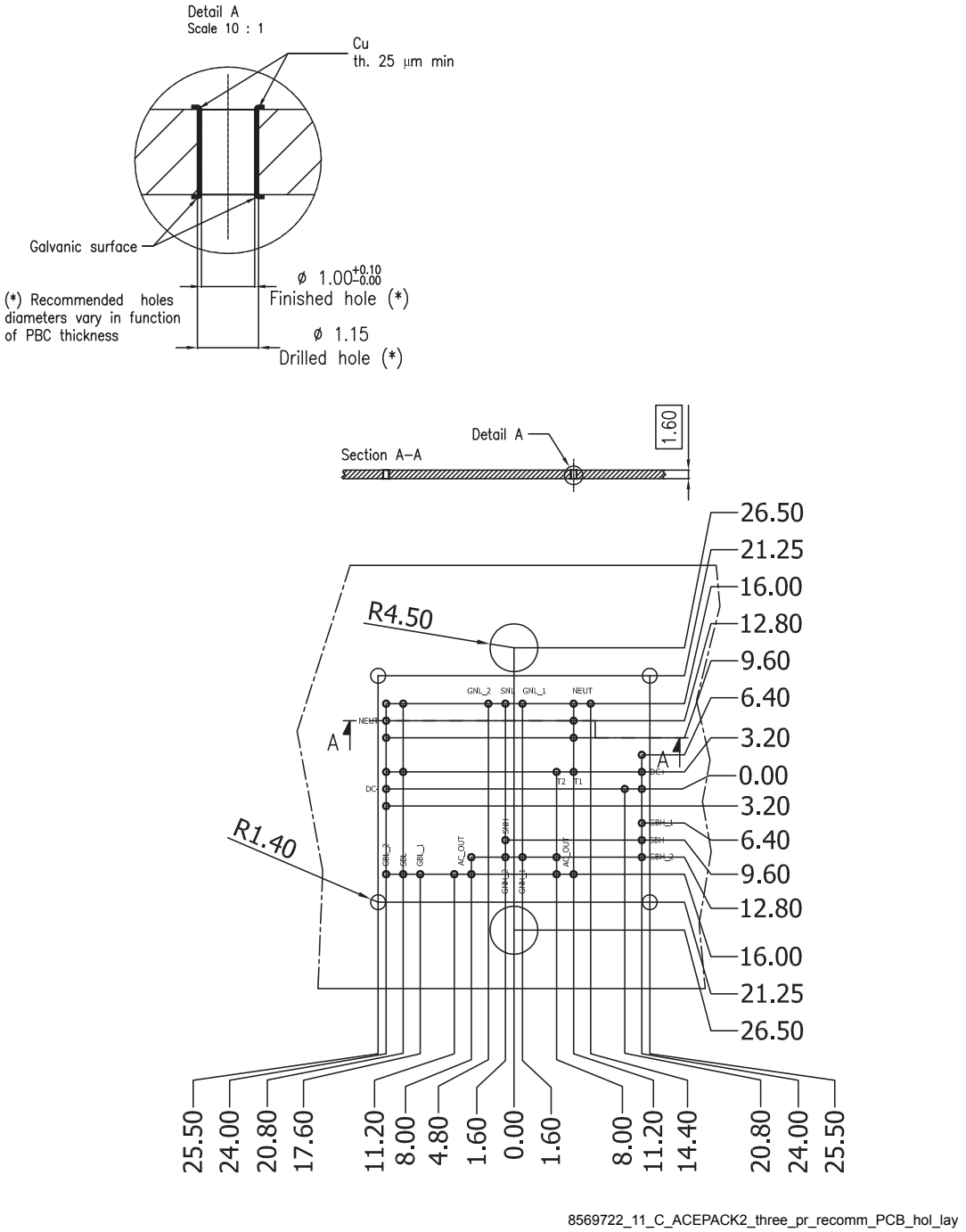


8569722_11_C_Three_PFP

Table 10. ACEPACK 2, 3-level press fit mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	47.70	48.00	48.30
A1	42.30	42.50	42.70
A2		37.00 REF	
B	56.40	56.70	57.00
B1	50.85	51.00	51.15
B2	22.40	22.70	23.00
B3		52.70 REF	
C	62.30	62.80	63.30
C1	52.90	53.00	53.10
C2	16.20	16.40	16.60
C3	4.40	4.50	4.60
D	11.90	12.25	12.60
D1	16.45	16.70	17.10
D2	1.35	1.55	1.75
D3	2.55	2.75	2.95
D4			8.50
t	0.30	0.40	0.50
θ	52°	60°	68°
θ1		90°	
e		3.20 BSC	
d1		2.30 REF	
ch		3.50 REF	

Figure 12. ACEPACK 2, 3-level press fit recommended PCB holes layout (dimensions are in mm)



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Revision history

Table 11. **Document revision history**

Date	Revision	Changes
06-Sep-2021	1	First release.

Contents