SONY

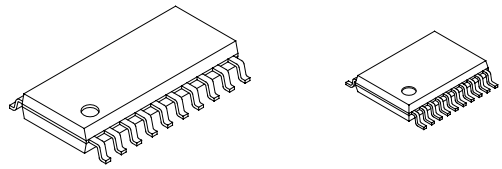
CXA2550M/N

RF Amplifier for CD Players

Description

The CXA2550M/N is an IC developed for compact disc players. This IC incorporates an RF amplifier, focus error amplifier, tracking error amplifier, APC circuit and RF level control circuit. (The voltage-converted optical pickup output is supported.)

CXA2550M	CXA2550N
20 pin SOP (Plastic)	20 pin SSOP (Plastic)



Features

- Low power consumption (35mW at 3.5V)
- APC circuit
- RF level control circuit
- Both single power supply and dual power supply operations possible.

Structure

Bipolar silicon monolithic IC

Applications

Compact disc players

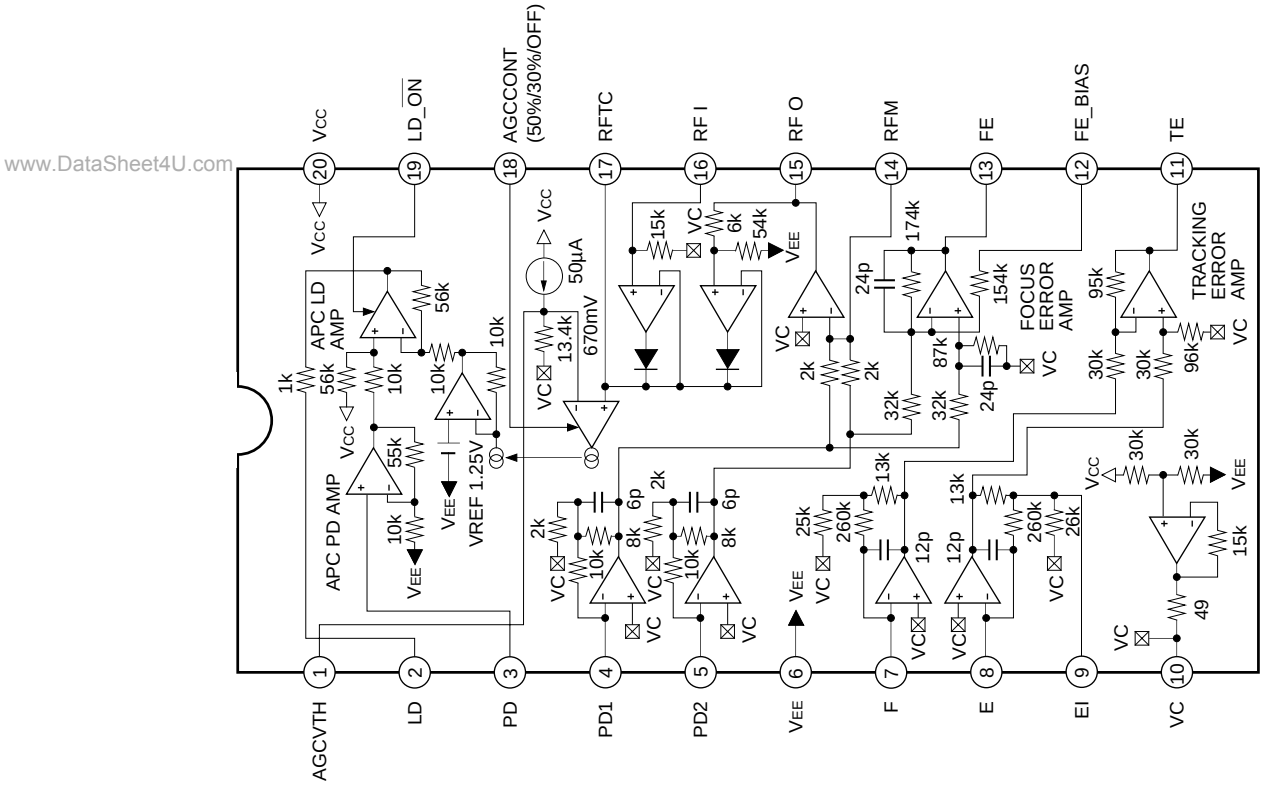
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation			
	P_D (SOP)	620	mW
	(SSOP)	370	mW

Operating Conditions

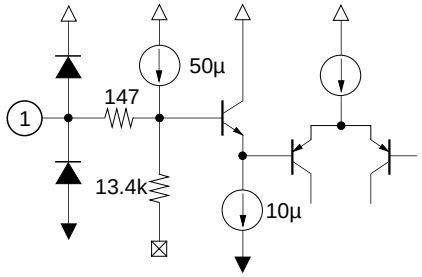
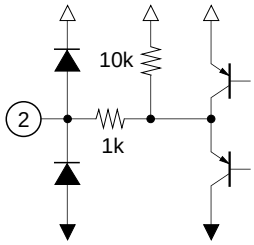
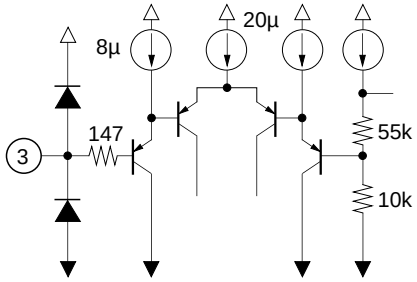
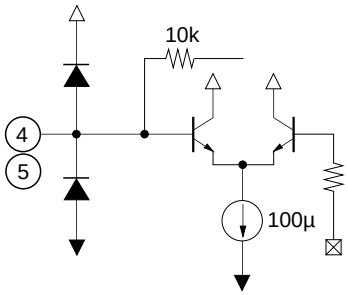
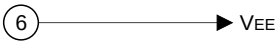
Supply voltage	$V_{CC} – V_{EE}$	3.0 to 4.0	V

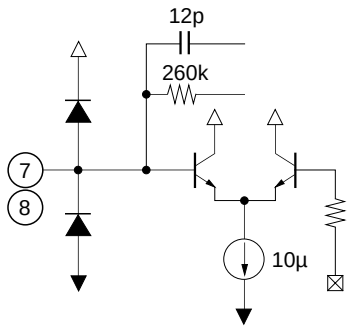
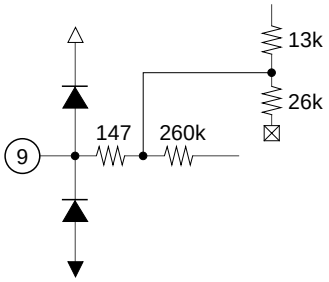
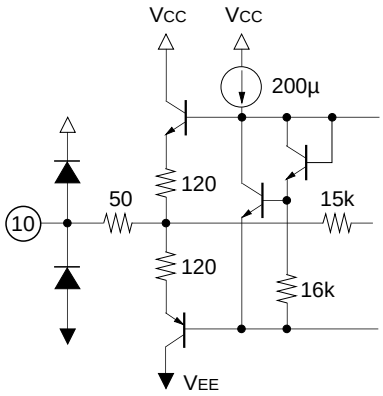
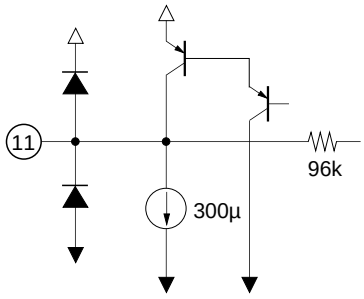
Block Diagram and Pin Configuration (Top View)

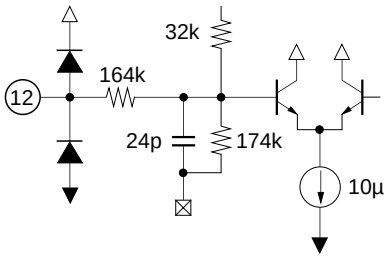
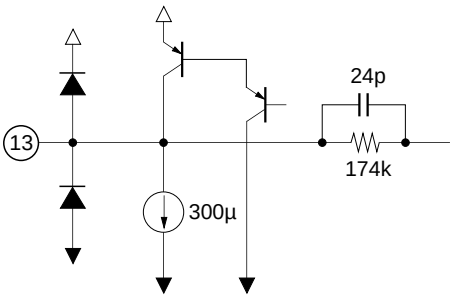
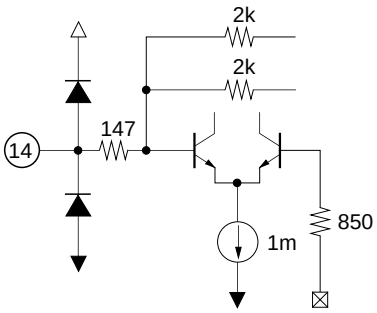
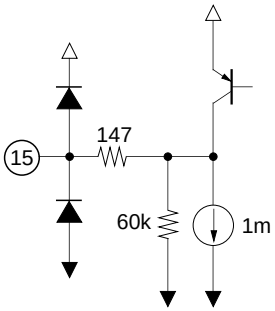


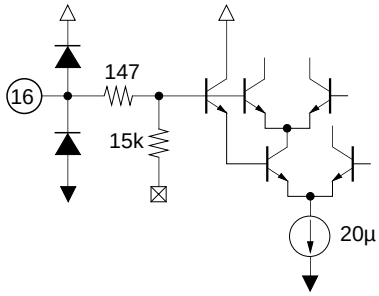
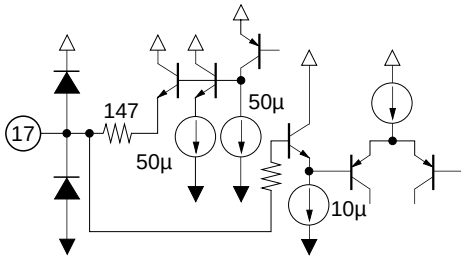
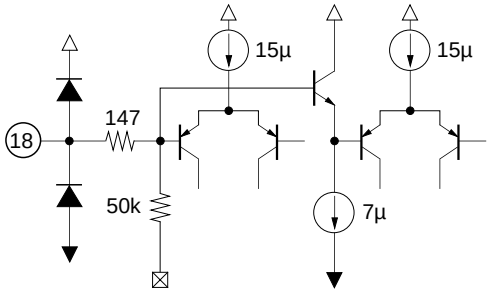
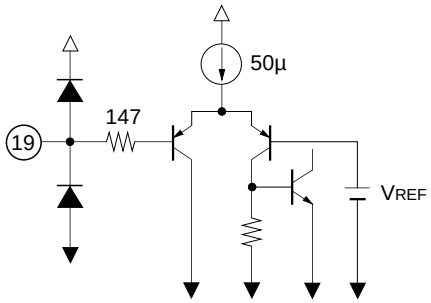
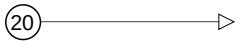
E97514B25

Pin Description

Pin No.	Symbol	I/O	Equivalent circuit	Description
1	AGCVTH	—		Reference level variable pin for RF level control. The reference level can be varied by the external resistor.
2	LD	O		APC amplifier output pin.
3	PD	I		APC amplifier input pin.
4 5	PD1 PD2	I I		Inversion input pin for RF I-V amplifiers. Connect these pins to the photodiodes A + C and B + D respectively. The current is supplied.
6	V_{EE}	—		V_{EE} pin.

Pin No.	Symbol	I/O	Equivalent circuit	Description
7 8	F E	I I		Inversion input pin for F and E I-V amplifiers. Connect these pins to the photodiodes F and E respectively. The current is supplied.
9	EI	—		Gain adjustment pin for I-V amplifier.
10	VC	O		DC voltage output pin of (Vcc + V_{EE})/2. Connect to GND for ±1.75 power supply; connect a smoothing capacitor for single +3.5V power supply.
11	TE	O		Tracking error amplifier output pin. E-F signal is output.

Pin No.	Symbol	I/O	Equivalent circuit	Description
12	FE_BIAS	I		Bias adjustment pin for inverted side of focus error amplifier.
13	FE	O		Focus error amplifier output pin.
14	RFM	I		RF amplifier inverted side input pin. RF amplifier gain is determined by the resistor connected between this pin and RFO pin.
15	RF O	O		RF amplifier output pin.

Pin No.	Symbol	I/O	Equivalent circuit	Description
16	RF I	I		The RF amplifier output RFO is input with its capacitance coupled.
17	RFTC	—		External time-constant pin for RF level control.
18	AGCCONT	I		RF level control ON (limit level of 50%/30%)/OFF switching pin. OFF for Vcc, 30% for open or Vc and 50% for V_{EE}.
19	LD_$\overline{ON}$	I		APC amplifier ON/OFF switching pin. OFF for Vcc and ON for V_{EE}.
20	V_{CC}			Vcc pin.

Electrical Characteristics

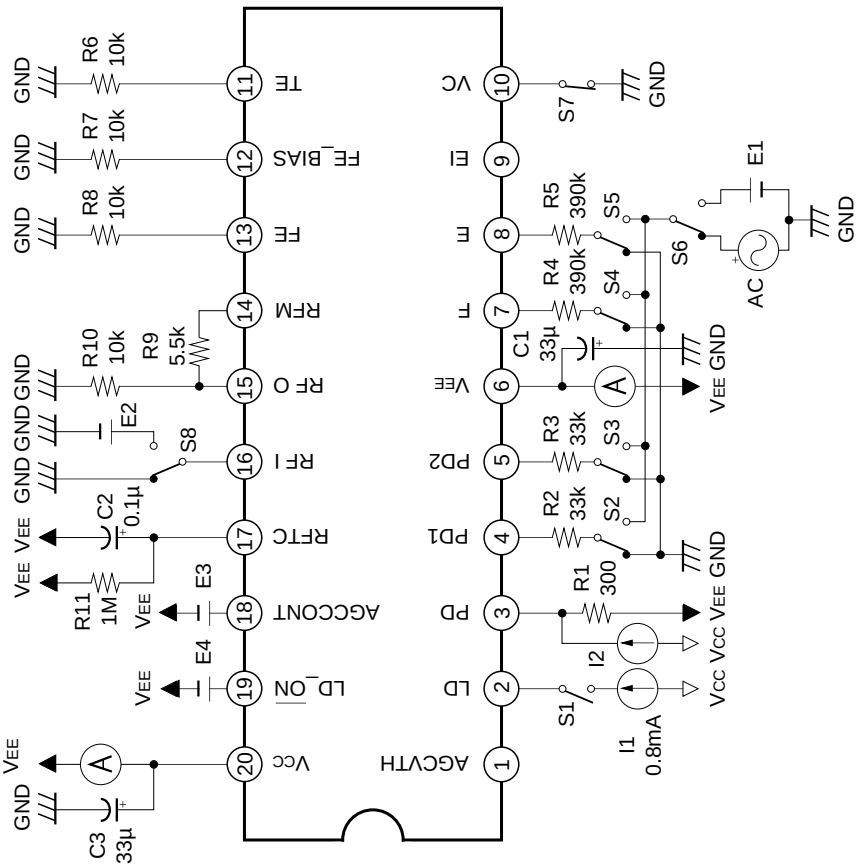
(Ta = 25°C, V_{CC} = 1.75V, V_{EE} = –1.75V, VC = GND)

No.	Measurement item		Symbol	SW conditions								Bias conditions						Measurement pin	Description of I/O waveform and measurement method		Min.	Typ.	Max.	Unit
				1	2	3	4	5	6	7	8	I1	I2	E1	E2	E3	E4							
1	Current consumption		I_{CC}							O								20	Input GND		6.37	9.8	13.23	mA
2			I_{EE}							O								6	Input GND		–13.23	–9.8	–6.37	mA
3	RF amplifier	Offset voltage 1	V15-1															15	Input resistance 33kΩ	Output DC measurement	–50.0	–10	60.0	mV
4		Voltage gain	V15-2		O	O												15	Input 1kHz 120mVp-p	Output AC measurement	16.7	19.7	22.7	dB
5		Frequency response	V15-3															15	Input 3MHz 120mVpp	Output AC measurement	–3	—	—	dB
6		Maximum output amplitude H	V15-4		O	O			O					300mV				15		Output DC measurement	1.45	—	—	V
7		Maximum output amplitude L	V15-5		O	O			O					–300mV				15		Output DC measurement	—	—	–1.25	V
8	FE amplifier	Offset voltage	V13-1															13	Input resistance 33kΩ	Output DC measurement	–120.0	0	120.0	mV
9		Voltage gain 1	V13-2		O													13	Input 1kHz 120mVp-p	Output AC measurement	16.4	19.4	22.4	dB
10		Voltage gain 2	V13-3			O												13	Input 1kHz 120mVp-p	Output AC measurement	16.4	19.4	22.4	dB
11		Voltage gain difference	V13-4															13	V13-4 = V13-2 – V13-3		–3.0	0	3.0	dB
12		Maximum output amplitude L	V13-5			O			O					300mV				13		Output DC measurement	—	—	–1.25	V
13		Maximum output amplitude H	V13-6		O				O					300mV				13		Output DC measurement	1.25	—	—	V
14	TE amplifier	Offset voltage 1	V11-1															11	Input resistance 390kΩ	Output DC measurement	–50	0	50	mV
15		Voltage gain 1	V11-2				O											11	Input 1kHz 240mVp-p	Output AC measurement	7.3	10.3	13.3	dB
16		Voltage gain 2	V11-3					O										11	Input 1kHz 240mVp-p	Output AC measurement	7.3	10.3	13.3	dB
17		Voltage gain difference	V11-4															11	V11-4 = V11-2 – V11-3		–3.0	0	3.0	dB
18		Maximum output amplitude H	V11-5				O		O					1V				11		Output DC measurement	1.25	—	—	V
19		Maximum output amplitude L	V11-6					O	O					1V				11		Output DC measurement	—	—	–1.25	V
20	APC	Output voltage 1	V2-1										450µA			2.7V	2.0V	2		Output DC measurement	–830	–330	170	mV
21		Output voltage 2	V2-2										570µA			2.7V	2.0V	2		Output DC measurement	470	970	1470	mV
22		Output voltage 3	V2-3										0µA			2.7V	0.5V	2	LD OFF	Output DC measurement	1400	1590	—	mV
23		Maximum output amplitude	V2-5	O								0.8mA	0µA			2.7V	2.0V	2		Output DC measurement	–600	—	100	mV

No.	Measurement item		Symbol	SW conditions								Bias conditions						Measure-ment pin	Description of I/O waveform and measurement method		Min.	Typ.	Max.	Unit
				1	2	3	4	5	6	7	8	I1	I2	E1	E2	E3	E4							
24	RF level control	50% limit	V2-7		O	O							800µA	50mV		0.5V/ 2.7V	2.0V	2	Level control: 50% – Level control OFF		–1900	–1322	–100	mV
25		30% limit	V2-8		O	O							700µA	50mV		1.3V/ 2.7V	2.0V	2	Level control: 30% – Level control OFF		–1700	–1163	–200	mV
26		–50% limit	V2-9						O		O		230µA		800mV	0.5V/ 2.7V	2.0V	2	Level control: –50% – Level control OFF		700	1471	1900	mV
27		–30% limit	V2-10						O		O		320µA		800mV	2.2V/ 2.7V	2.0V	2	Level control: –30% – Level control OFF		700	1204	1700	mV
28	AGCCONT	High Level	V18-1															18			2.7	—	—	V
29		Middle Level	V18-2															18			1.3	—	2.2	V
30		Low Level	V18-3															18			—	—	0.5	V
31	Center output voltage		V10-1							O								10		Output DC measurement	–100	—	100	mV

Note) O in the SW conditions 7 represents the OFF state.

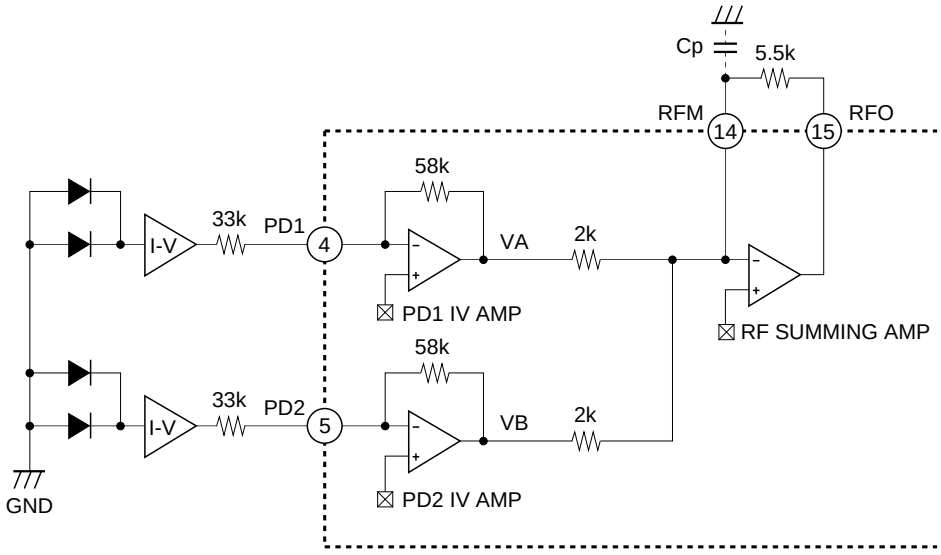
Electrical Characteristics Measurement Circuit



Description of Functions

RF Amplifier

The photodiode current input to the input pins (PD1, PD2) are current-to-voltage (I-V) converted by the equivalent resistance of 58kΩ at PD I-V amplifiers, respectively. The signal is added by the RF summing amplifier and then the I-V converted output voltage of the photodiode (A + B + C + D) is output to RFO pin. This pin is used check the eye pattern.

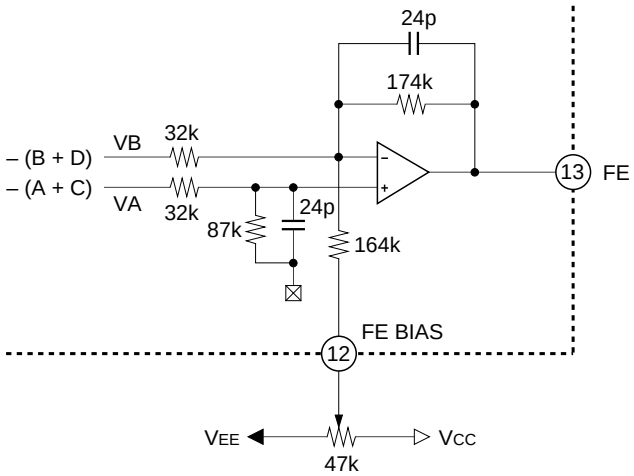


The frequency response of the RF output signal can be equalized by adding the capacitance (Cp) to RFI pin. The low frequency component of the RFO output voltage is as follows;

$$V_{RFO} = -2.75 \times (V_A + V_B)$$
$$= 159.5k\Omega \times (iPD1 + iPD2)$$

Focus Error Amplifier

The difference between the RF I-V amplifier output VA and VB is obtained and the I-V converted voltage of the photodiode (A + C – B – D) is output.

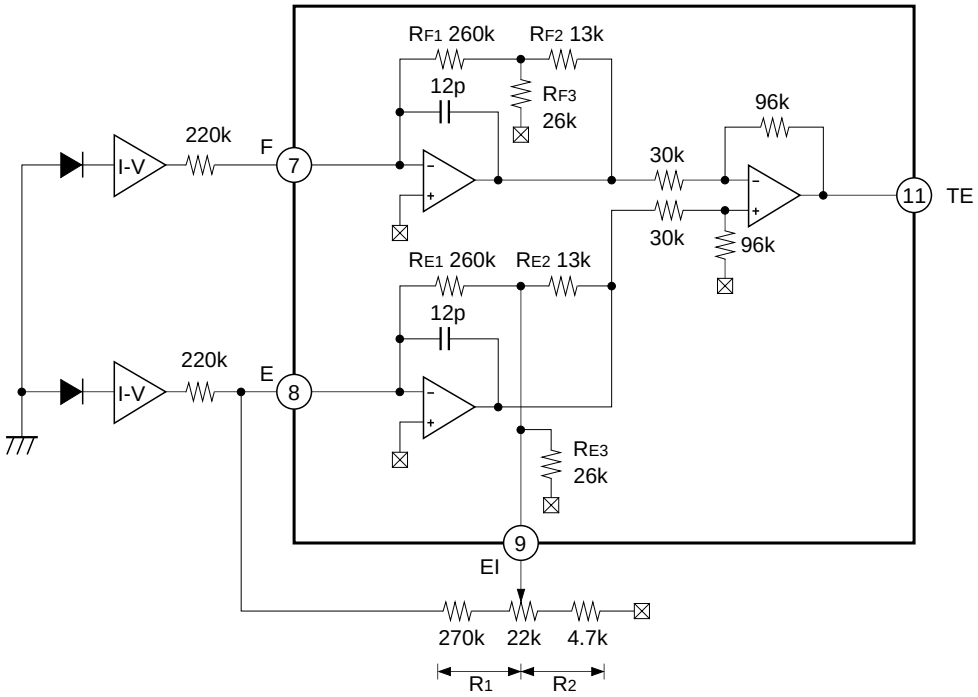


The FE output voltage (low frequency) is as follows;

$$V_{FE} = 5.4 \times (V_A - V_B)$$
$$= (iPD2 - iPD1) \times 315k\Omega$$

Tracking Error Amplifier

Each signal current from the photodiodes E and F is I-V converted and input to Pins 7 and 8 via a resistor which determines the gain. The signal is amplified by the gain amplifier, operated by the tracking error amplifier and then the (F-E) signal is output to Pin 11.



The balance adjustment is performed by varying the combined resistance value of the feedback resistors, which are T type-configured at the E I-V amplifier, by using the external resistance value of EI pin.

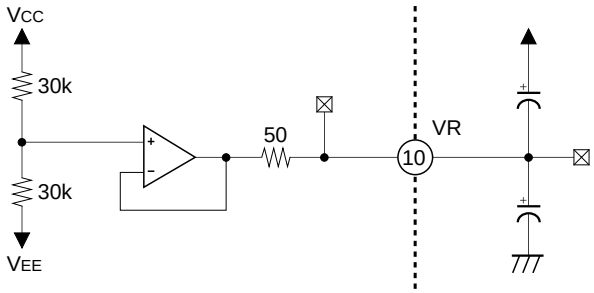
$$\text{F I-V amplifier feedback resistance value} = R_{F1} + R_{F2} + \frac{R_{F1} \times R_{F2}}{R_{F3}} = 403k\Omega$$

$$\text{E I-V amplifier feedback resistance value} = (R_{E1} \,//\, R_1) + R_{E2} + \frac{(R_{E1} \,//\, R_1) \times R_{E2}}{(R_{E3} \,//\, R_2)}$$

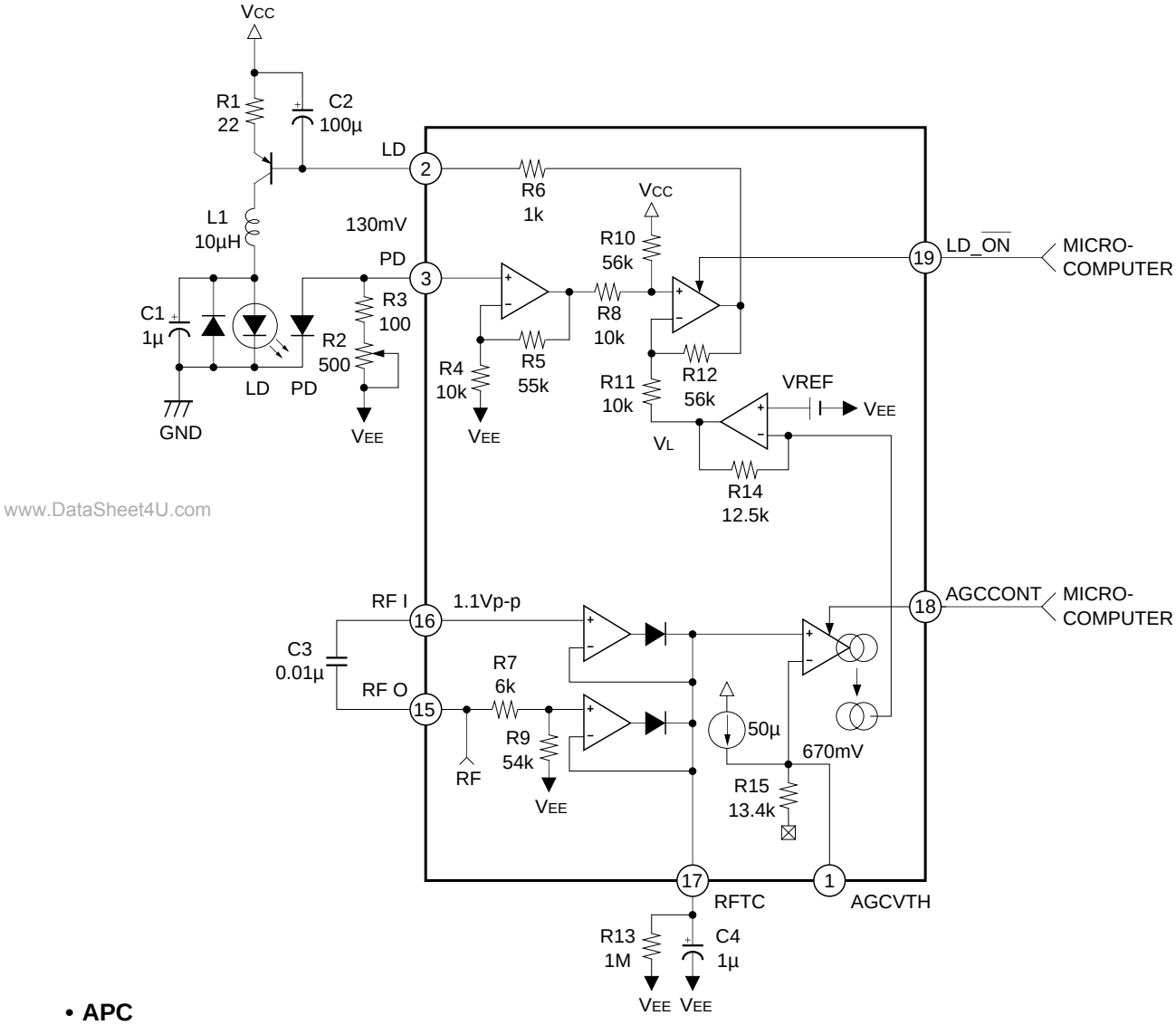
Leave EI pin open when the balance adjustment is not executed in this IC.
The gain for F I-V and E I-V amplifiers becomes the same when EI pin is left open.

Center Voltage Generation Circuit

This circuit provides the center potential when this IC is used at single power supply. The maximum current is approximately ±3mA. The output impedance is approximately 50Ω.



APC & Laser Power Control



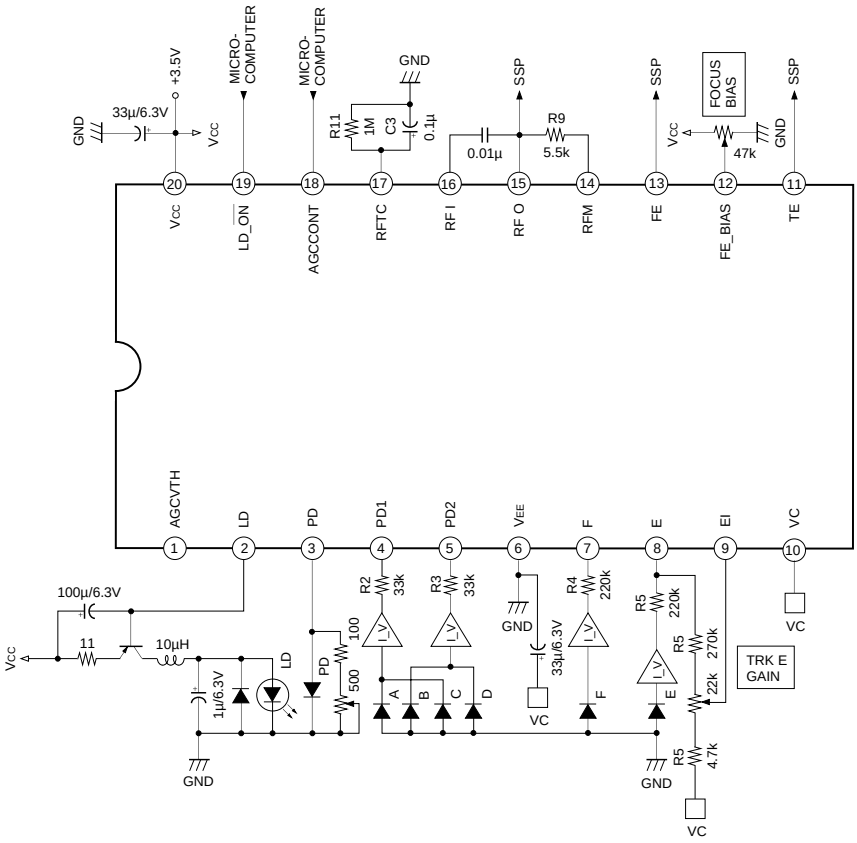
• APC

When the laser diode is driven by a constant current, the optical power output has extremely large negative temperature characteristics. The APC circuit is used to maintain the optical power output at a constant level. The laser diode current is controlled according to the monitor photo diode output.

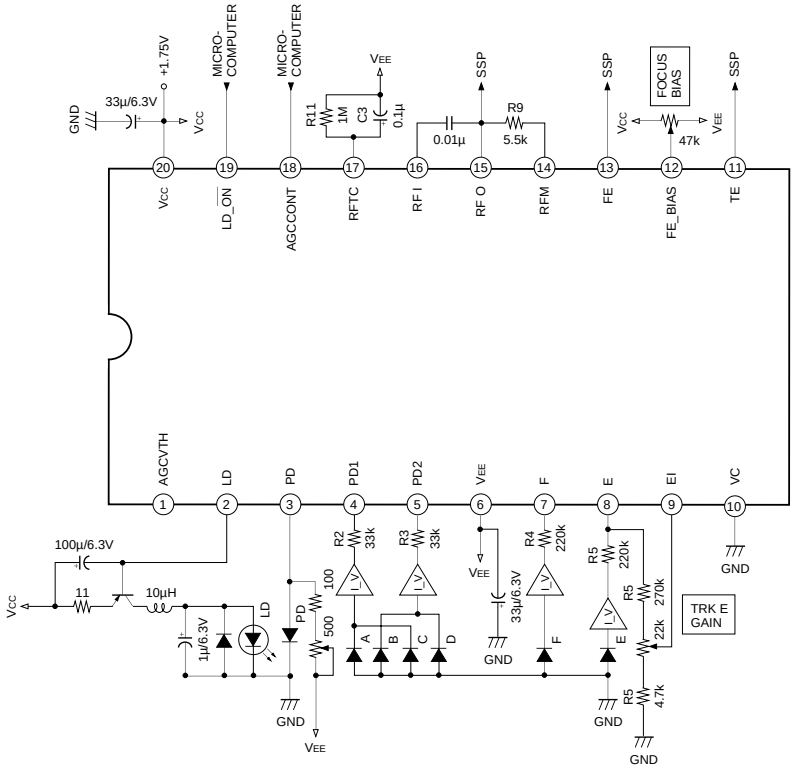
APC is set to ON by connecting the LD_$\overline{ON}$ pin to VCC; OFF by connecting it to VCC.

Application Circuit

• For single power supply +3.5V



• For dual power supply ±1.75V



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

• LASER POWER CONTROL (LPC)

The RF level is stabilized by attaching an offset to the APC V_L and controlling the laser power in sync with the RF level fluctuations.

The RF O and RF I levels are compared and the larger of the two is smoothed by the RFTC's external CR.

This signal is then compared with the reference level.

The laser power is controlled by attaching an offset to V_L according to the results of comparison with the reference level.

Set the reference level to 670mV. (center voltage reference)

When the reference level is changed, connect the external resistor to the AGCVTH pin (Pin 1). The reference level can be lowered by connecting the resistor between Pin 1 and the center output voltage or between Pin 20 and V_{CC}.

The AGCCONT pin (pin 18) is used to switch the level of the laser power control circuit; OFF, ON (laser power limit of 30%) and ON (laser power limit of 50%)

Note) For the laser power limit, 50% is recommended for PD IC; 30% for LC.

AGCCONT	LPC	LPC limit	V_L variable range
H (V_{CC})	OFF	—	Approximately 1.27V
M (VC or OPEN)	ON	30%	Approximately 1.27V ± 350mV
L (V_{EE})	ON	50%	Approximately 1.27V ± 570mV

Notes on Operation

1. Power supply

The CXA2550M/N can be used either at dual power supply or single power supply. The table below shows the connection of power supply for each case.

	V_{CC}	V_{EE}	VC
Dual power supply	+power supply	–power supply	GND
Single power supply	Power supply	GND	OPEN

2. RF amplifier

In this circuit, the IC internal phase compensation value is set so as to support the voltage output-type pickup. Therefore, when the current output-type pickup is used, the capacitance of optical pickup and leads etc. are attached to PD1 and PD2 pins and oscillation may occur.

3. laser power control

The RF level is stabilized by attaching an offset to the APC V_L and controlling the laser power in sync with the RF level fluctuations. Therefore, use this circuit in the state where the focus servo is applied.

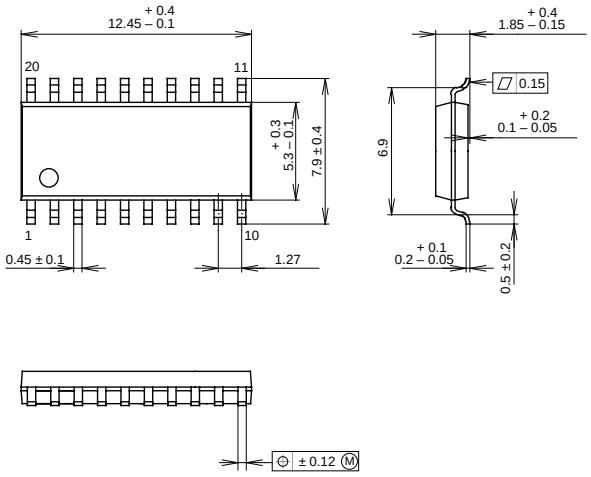
The laser life is shortened by increasing the laser power when the less light is reflected from the disc. It is recommended that the typical laser power value is set lower to maintain the laser life.

Take care of the laser maximum ratings when using the laser power control circuit.

Package Outline Unit: mm

CXA2550M

20PIN SOP (PLASTIC) 300mil



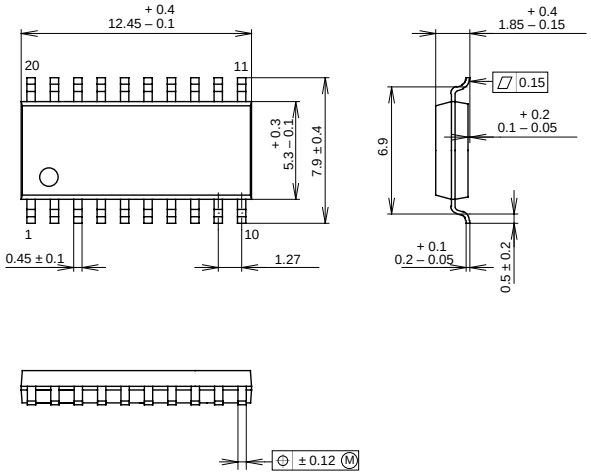
PACKAGE STRUCTURE

SONY CODE	SOP-20P-L01
EIAJ CODE	*SOP020-P-0300-A
JEDEC CODE	

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.3g

SCT Ass'y

20PIN SOP (PLASTIC) 300mil



PACKAGE STRUCTURE

SONY CODE	SOP-20P-L01
EIAJ CODE	*SOP020-P-0300-A
JEDEC CODE	

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.3g

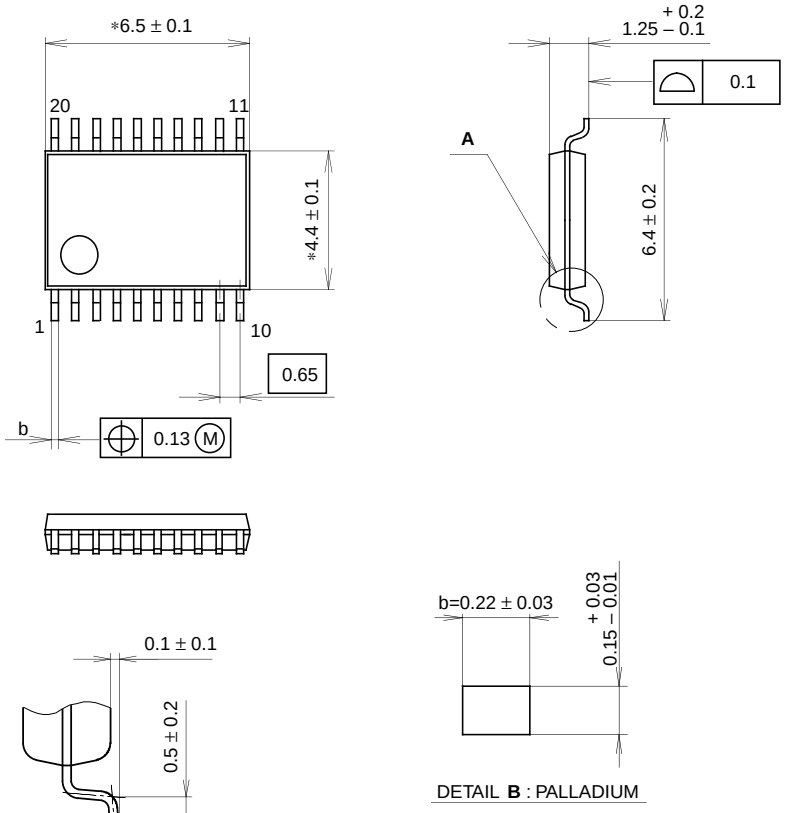
LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm

Package Outline Unit: mm

CXA2550N

20PIN SSOP (PLASTIC)



DETAIL **B** : PALLADIUM

DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-20P-L01
EIAJ CODE	SSOP020-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g