

Low-Voltage Full-Bridge Brushless DC Motor Driver with Hall Commutation, Externally Controlled Speed Regulation, Soft Switching, and Reverse Battery, Short Circuit, and Thermal Shutdown Protection

Features and Benefits

- Low voltage operation: 1.8 to 4.2 V
- Externally controlled motor speed regulation
- Fast motor startup and braking function allows faster start-stop cycles
- Reverse voltage protection on the VDD and SLEEP pins
- Output short circuit and thermal shutdown protection
- Soft switching algorithm for reduced audible switching noise and EMI interference
- Unidirectional operating mode results in motor rotation in only one direction
- Chopper stabilization reduces Hall signal offset drifts and results in increased signal accuracy over full operating temperature range
- Sleep mode pin allows device enable/disable for reducing average power consumption
- Antistall feature guarantees continuous rotation
- Single-chip solution for high reliability
- Miniature MLP/DFN package

Package:

6-contact MLP/DFN 1.5 mm × 2 mm. 0.40 mm maximum overall height (EW package)



Description

The A1444 and A1445 are full-bridge motor drivers designed to drive low-voltage brushless DC (BLDC) motors in applications that require rotor speed control and fast rotor start-stop cycles. A high density CMOS semiconductor process allows the integration of a Hall element, a full-bridge output driver, and PWM speed control logic into one monolithic IC. Commutation of the motor is achieved by use of a single Hall element to detect the rotational position of an alternating-pole ring magnet. Low-voltage design techniques have been employed to achieve full device functionality down to a V_{DD} of 1.8 V. The voltage applied to the PDC pin is used to externally control the maximum speed of the motor by adjusting the PWM duty cycle of the output driver.

The A1444 and A1445 employ a soft switching algorithm to reduce audible switching noise and EMI interference. The externally controlled speed regulation and braking functions can be used to create motor designs requiring faster start-stop cycles. The A1444 and A1445 have different selectable internal PWM duty cycle options to accommodate a wide range of motor designs. Each device has a braking function enable pin that also includes a micropower sleep mode for battery management in portable electronic devices. This feature eliminates the requirement for a FET transistor to switch the device on and off.

The devices are optimized for vibration motor applications that require fast start-stop cycles, such as in cellular phones,

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Functional Block Diagram

Description (continued)

pagers, and hand-held video game controllers. The devices can also be used for low-power fan motors rated at 5 V. This fully integrated single-chip solution provides enhanced reliability, including reverse battery protection and output short circuit protection.

The small package outline and low profile make this device ideally suited for use in applications where printed circuit board

area and component headroom are at a premium. It is available in a lead (Pb) free (leadframe plating nickel palladium) 6-contact MLP/DFN microleadframe package for surface mount assembly. The underside of the package also features an exposed pad for enhanced thermal dissipation.

Selection Guide

| A1444FFWLT_P ² 1.5 mm × 2 mm 0.38 mm nominal overall package b | Part Number | Packing ¹ | Package |
|---|---------------------------|----------------------------|---|
| | A1444EEWLT-P ² | 2000 pieces per 7 in real | 1.5 mm × 2 mm , 0.38 mm nominal overall package height, |
| A1445EEWLT-P2 6-contact MLP/DFN with exposed thermal pad | A1445EEWLT-P2 | Suco pieces per 7-in. reel | 6-contact MLP/DFN with exposed thermal pad |



¹Contact Allegro for additional packing options

²Variant is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: May 4, 2009.

Absolute Maximum Ratings

| Characteristic | Symbol | Notes | Rating | Units |
|-------------------------------|----------------------|---|-------------------------------|-------|
| Forward Supply Voltage | V _{DD} | | 5.0 | V |
| Reverse Supply Voltage | V _{RDD} | | -5.0 | V |
| Forward Output Voltage | V _{OUT} | V _{DD} > 0 V | 0 to V _{DD} + 0.3 | V |
| Reverse Output Voltage | V _{ROUT} | V _{DD} > 0 V | -0.3 | V |
| SLEEP Input Voltage | V _{IN} | | 0 to V _{DD} + 0.3 | V |
| SLEEP Reverse Input Voltage | V _{RIN} | | -5.0 | V |
| PDC Input Voltage | V _{PDC} | | -0.3 to V _{DD} + 0.3 | V |
| Continuous Output Current | I _{OUT} | Positive I_{LOAD} flow is from VOUT1 to VOUT2, $T_J < T_J(max)$ | ±250 | mA |
| Peak Output Current | I _{OUT(pk)} | <1 ms | ±500 | mA |
| Operating Ambient Temperature | T _A | Range E | -40 to 85 | °C |
| Maximum Junction Temperature | T _J (max) | | 165 | °C |
| Storage Temperature | T _{stg} | | -65 to 170 | °C |

Thermal Characteristics may require derating at maximum conditions, see Power Derating section

| Characteristic | Symbol | Test Conditions* | Value | Units |
|----------------------------|--------|--|-------|-------|
| Package Thermal Resistance | B | On 2-layer PCB, with 0.23 in. ² copper area each side | 125 | °C/W |
| | Reja | On 4-layer PCB based on JEDEC standard | 64 | °C/W |

*Additional thermal information available on the Allegro website

| Pin | -οι | ıt Di | iag | ram | |
|---------------------|-------------------|-------|-------------------|-----------------------|--|
| VDD SLEEP PCD | (1) (2) (3) | PAD | (6) (5) (4) | VOUT2 VOUT1 GND | |

Terminal List

| Number | Name | Function |
|--------|-------|---|
| 1 | VDD | Supply voltage |
| 2 | SLEEP | Toggles sleep and enable modes, low sleep mode voltage initiates motor braking and low power mode |
| 3 | PDC | Voltage on this pin selects among discrete internal PWM duty cycle values to control motor speed |
| 4 | GND | Ground |
| 5 | VOUT1 | First output |
| 6 | VOUT2 | Second output |



ELECTRICAL CHARACTERISTICS Valid over supply voltage and ambient temperature ranges, unless otherwise noted

| Characteristics | Symbol | Test Conditions | | Min. | Typ. ¹ | Max. | Unit |
|--|------------------------|--|--|----------------------|-------------------|---------------------|------|
| Supply Voltage | V _{DD} | T _J < T _J (I | max) | 2.0 | _ | 4.2 | V |
| Extended Supply Voltage ² | V _{DDE} | T _J < T _J (I | max) | 1.8 | _ | 4.2 | V |
| Supply Current | | V _{IN} >V _{IN} | $_{\rm H}$, T _A = 25°C, no load | - | 4 | 6 | mA |
| | DD(ON) | $V_{IN} < V_{IN}$ | $V_{IN} < V_{INLO}, T_A = 25^{\circ}C$ | | _ | 10 | μA |
| | | I _{OUT} = 50 | _{OUT} = 50 mA, V _{DD} = 2 V, T _A = 25°C | | 3.9 | - | Ω |
| Total Output On-Resistance ³ | R _{DS(on)} | I _{OUT} = 50 |) mA, V _{DD} = 3 V, T _A = 25°C | - | 2.6 | - | Ω |
| | | I _{OUT} = 50 | 0 mA, V _{DD} = 4 V, T _A = 25°C | - | 2.2 | - | Ω |
| Reverse Battery Current | I _{RDD} | V_{RDD} = -4.2 V, current flowing out of VDD pin, T _A = 25°C | | - | - | -10 | mA |
| | V _{INHI} | | | | _ | - | V |
| | V _{INLO} | | | - | _ | $0.2 \times V_{DD}$ | V |
| SLEEP Input Current | I _{IN} | V _{DD} = 3. | 6 V | - | 1.0 | 5 | μA |
| SLEEP Reverse Input Current | I _{RIN} | V_{RIN} = -4.2 V, current flowing out of SLEEP pin, T _A = 25°C | | _ | - | -10 | mA |
| Restart Delay ⁴ | t _{RS} | V _{DD} = 3.6 V | | _ | 100 | - | ms |
| Hall Chopping Settling Time ⁵ | t _{S(CHOP)} | | | _ | 160 | - | μs |
| Thermal Shutdown Limit | T _{JTSD} | Device is active | | - | 165 | - | °C |
| Thermal Shutdown Hysteresis | T _{JTSD(HYS)} | Device is active | | - | 20 | - | °C |
| Internal PWM Frequency | f _{PWM} | | | - | 40 | - | kHz |
| PDC High Level Threshold | V _{PDCH} | PDC input going from low to high state | | V _{DD} -0.5 | _ | V _{DD} | V |
| PDC Low Level Threshold | V _{PDCL} | PDC input going from high to low state | | 0 | _ | 0.5 | V |
| PDC Input Current ⁶ | I _{PDCH} | Steady state condition, PDC pin high | | - | _ | 30 | μΑ |
| | I _{PDCL} | Steady s | tate condition, PDC pin low state | -30 | _ | - | μA |
| | | | $V_{PDC} < V_{PDCL}, V_{DD} = V_{DDN}, S_{ROT} > S_{ROT(th)}$ | - | 56 | - | % |
| | | A1444 | PDC Pin Floating, $V_{DD} = V_{DDN}$, S _{ROT} > S _{ROT(th)} | - | 62 | - | % |
| Internal DWM Duty Cuale | | | $V_{PDC} > V_{PDCH}, V_{DD} = V_{DDN},$ $S_{ROT} > S_{ROT(th)}$ | _ | 68 | - | % |
| | DCPWM | | $V_{PDC} < V_{PDCL}, V_{DD} = V_{DDN},$ $S_{ROT} > S_{ROT(th)}$ | - | 71 | - | % |
| | | A1445 | PDC Pin Floating, $V_{DD} = V_{DDN}$, S _{ROT} > S _{ROT(th)} | - | 80 | - | % |
| | | | $\label{eq:pdc} \begin{array}{ c c } V_{PDC} > V_{PDCH}, \ V_{DD} = V_{DDN}, \\ S_{ROT} > S_{ROT(th)} \end{array}$ | _ | 89 | - | % |

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ELECTRICAL CHARACTERISTICS (continued) valid over supply voltage and ambient temperature ranges, unless otherwise noted

| Characteristics | Symbol | Test Conditions | Min. | Typ. ¹ | Max. | Unit |
|-----------------------|------------------|--|------|-------------------|------|------|
| | B _{OP} | $2 \text{ V} \leq \text{V}_{\text{DD}} \leq 4 \text{ V}$ | _ | 35 | 75 | G |
| Magnetic Switchpoints | B _{RP} | $2 \text{ V} \leq \text{V}_{\text{DD}} \leq 4 \text{ V}$ | -75 | -35 | _ | G |
| | B _{HYS} | $2 \text{ V} \leq \text{V}_{\text{DD}} \leq 4 \text{ V}$ | _ | 70 | _ | G |
| Output Polarity | VOUT1 | B < B _{RP} | _ | LOW | - | V |
| | | B > B _{OP} | _ | HIGH | - | V |
| | VOUT2 | B < B _{RP} | _ | HIGH | _ | V |
| | | B > B _{OP} | _ | LOW | - | V |

¹Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions, such as $T_A = 25^{\circ}$ C. Performance may vary for individual units, within the specified maximum and minimum limits.

²Device operates with lower supply voltages, down to 1.8 V, with slight variation in specification of magnetic switchpoints and Total Output On-Resistance. ³Total Output On-Resistance = $R_{DS(on)Q1} + R_{DS(on)Q4}$, or $R_{DS(on)Q2} + R_{DS(on)Q3}$, where Qx refers to the internal full-bridge transistors.

⁴Restart Delay is the duration required from power-up of the device to valid device output.

⁵Hall Chopping Settling Time is the delay from power-on of the device to the initial valid device output.

⁶Positive current is defined as flowing into the device.



Functional Description

Soft Switching

The A1444 and A1445 devices include a soft switching algorithm that controls the output switching slew rate for both output pins. As a result, the devices are ideal for use in applications requiring low audible switching noise and low EMI interference.

Braking and Sleep Mode

The SLEEP pin accepts an external signal that enables braking and a sleep mode. During braking, the device reverses the polarity of the output bridge for a fixed time period, then the device enters sleep mode. In sleep mode, the device current consumption gets reduced to an extremely low level, conserving battery power.

Antistall Algorithm

If a stall condition occurs, the device will execute an antistall algorithm to restart the motor.

Device Start-up

The start-up behavior of the device output is determined by the applied magnetic field, as specified in the Electrical Characteristics table.

Speed Control

When the rate of rotation exceeds the specified threshold, $S_{ROT(th)}$, the A1444/A1445 output bridge becomes controlled by an internally generated PWM signal. The duty cycle of the internal PWM signal regulates the maximum motor rpm. The PWM duty cycle, however, is user-selectable through the state of the PDC pin. The PWM duty cycle options are given in the Electrical Characteristics table.



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Application Information

Two typical application circuits are shown in figures 1 and 2. The application circuit in figure 1 shows the device $\overline{\text{SLEEP}}$ pin controlled by the user. In this case, the device is powered continuously and the average supply current would switch between low and high values depending on the state of the $\overline{\text{SLEEP}}$ pin.

Figure 2 illustrates an applications circuit where the device supply pin and $\overline{\text{SLEEP}}$ pin are connected together. When power is applied to the device, it enters enable mode and operates with high average supply current.

Note that:

- No external diode is required for reverse battery protection because the protection is fully integrated into the IC.
- Thermal shutdown also is integrated to protect the device against inadvertent output shorts during manufacturing or testing.
- In these figures, the PDC pin is tied to GND. Alternatively, the PDC pin could be tied to any of the voltage rails or left floating, which will determine the internal PWM duty cycle as specified in the Electrical Characteristics table.



Figure 1. Application circuit showing user-controlled sleep/enable mode, while the A144x remains powered at all times



Figure 2. Application circuit showing simultaneous user control of power supply and sleep mode.



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Power Derating

The device must be operated below the maximum junction temperature of the device, T_J (max). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J . (Thermal data is also available on the Allegro MicroSystems website.)

The package thermal resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the effective thermal conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A , and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J , at various P_D levels.

$$P_{\rm D} = V_{\rm IN} \times I_{\rm IN} \tag{1}$$

$$\Delta T = P_D \times R_{\theta JA} \tag{2}$$

$$T_J = T_A + \Delta T \tag{3}$$

For a load of 30 Ω , and given common conditions such as: T_A= 25°C, V_{DD} = 3 V, I_{DD} = 85 mA, V_{LOAD} = 2.43 V, I_{LOAD} = 83 mA, and R_{θ JA} = 250 °C/W,

then:

$$\begin{split} P_D &= V_{DD} \times I_{DD} - V_{LOAD} \times I_{LOAD} \\ &= 3 \ V \times 83 \ mA - 2.43 \ V \times 81 \ mA \\ &= 52.17 \ mW \\ \Delta T &= P_D \times R_{\theta JA} \\ &= 52.17 \ mW \times 250 \ ^{\circ}C/W \\ &= 13 \ ^{\circ}C \\ T_J &= T_A + \Delta T \\ &= 25 \ ^{\circ}C + 13 \ ^{\circ}C \\ &= 38 \ ^{\circ}C \end{split}$$

A worst-case estimate, $P_D(max)$, represents the maximum allowable power level, without exceeding $T_J(max)$, at a selected $R_{\theta JA}$ and T_A .





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Package:

6-contact MLP/DFN 1.5 mm × 2 mm. 0.40 mm maximum overall height (EW package)



Description

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The devices are optimized for vibration motor applications that require fast start-stop cycles, such as in cellular phones,

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Functional Block Diagram

Description (continued)

pagers, and hand-held video game controllers. The devices can also be used for low-power fan motors rated at 5 V. This fully integrated single-chip solution provides enhanced reliability, including reverse battery protection and output short circuit protection.

The small package outline and low profile make this device ideally suited for use in applications where printed circuit board

area and component headroom are at a premium. It is available in a lead (Pb) free (leadframe plating nickel palladium) 6-contact MLP/DFN microleadframe package for surface mount assembly. The underside of the package also features an exposed pad for enhanced thermal dissipation.

Selection Guide

| A1444FFWLT_P ² 1.5 mm × 2 mm 0.38 mm nominal overall package b | Part Number | Packing ¹ | Package |
|---|---------------------------|----------------------------|---|
| | A1444EEWLT-P ² | 2000 pieces per 7 in real | 1.5 mm × 2 mm , 0.38 mm nominal overall package height, |
| A1445EEWLT-P2 6-contact MLP/DFN with exposed thermal pad | A1445EEWLT-P2 | Suco pieces per 7-in. reel | 6-contact MLP/DFN with exposed thermal pad |



¹Contact Allegro for additional packing options

²Variant is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: May 4, 2009.

Absolute Maximum Ratings

| Characteristic | Symbol | Notes | Rating | Units |
|-------------------------------|----------------------|---|-------------------------------|-------|
| Forward Supply Voltage | V _{DD} | | 5.0 | V |
| Reverse Supply Voltage | V _{RDD} | | -5.0 | V |
| Forward Output Voltage | V _{OUT} | V _{DD} > 0 V | 0 to V _{DD} + 0.3 | V |
| Reverse Output Voltage | V _{ROUT} | V _{DD} > 0 V | -0.3 | V |
| SLEEP Input Voltage | V _{IN} | | 0 to V _{DD} + 0.3 | V |
| SLEEP Reverse Input Voltage | V _{RIN} | | -5.0 | V |
| PDC Input Voltage | V _{PDC} | | -0.3 to V _{DD} + 0.3 | V |
| Continuous Output Current | I _{OUT} | Positive I_{LOAD} flow is from VOUT1 to VOUT2, $T_J < T_J(max)$ | ±250 | mA |
| Peak Output Current | I _{OUT(pk)} | <1 ms | ±500 | mA |
| Operating Ambient Temperature | T _A | Range E | -40 to 85 | °C |
| Maximum Junction Temperature | T _J (max) | | 165 | °C |
| Storage Temperature | T _{stg} | | -65 to 170 | °C |

Thermal Characteristics may require derating at maximum conditions, see Power Derating section

| Characteristic | Symbol | Test Conditions* | Value | Units |
|----------------------------|--------|--|-------|-------|
| Package Thermal Resistance | B | On 2-layer PCB, with 0.23 in. ² copper area each side | 125 | °C/W |
| | Reja | On 4-layer PCB based on JEDEC standard | 64 | °C/W |

*Additional thermal information available on the Allegro website

| Pin | -οι | ıt Di | iag | ram | |
|---------------------|-------------------|-------|-------------------|-----------------------|--|
| VDD SLEEP PCD | (1) (2) (3) | PAD | (6) (5) (4) | VOUT2 VOUT1 GND | |

Terminal List

| Number | Name | Function |
|--------|-------|---|
| 1 | VDD | Supply voltage |
| 2 | SLEEP | Toggles sleep and enable modes, low sleep mode voltage initiates motor braking and low power mode |
| 3 | PDC | Voltage on this pin selects among discrete internal PWM duty cycle values to control motor speed |
| 4 | GND | Ground |
| 5 | VOUT1 | First output |
| 6 | VOUT2 | Second output |



ELECTRICAL CHARACTERISTICS Valid over supply voltage and ambient temperature ranges, unless otherwise noted

| Characteristics | Symbol | | Test Conditions | Min. | Typ. ¹ | Max. | Unit |
|--|------------------------|--|--|----------------------|-------------------|---------------------|------|
| Supply Voltage | V _{DD} | T _J < T _J (max) | | 2.0 | _ | 4.2 | V |
| Extended Supply Voltage ² | V _{DDE} | T _J < T _J (I | $T_J < T_J(max)$ | | _ | 4.2 | V |
| Supply Current | I _{DD(ON)} | $V_{IN} > V_{INHI}$, $T_A = 25^{\circ}C$, no load | | - | 4 | 6 | mA |
| | | $V_{IN} < V_{INLO}, T_A = 25^{\circ}C$ | | - | _ | 10 | μA |
| Total Output On-Resistance ³ | R _{DS(on)} | I _{OUT} = 50 mA, V _{DD} = 2 V, T _A = 25°C | | - | 3.9 | - | Ω |
| | | I_{OUT} = 50 mA, V_{DD} = 3 V, T_{A} = 25°C | | - | 2.6 | - | Ω |
| | | I_{OUT} = 50 mA, V_{DD} = 4 V, T_A = 25°C | | - | 2.2 | - | Ω |
| Reverse Battery Current | I _{RDD} | V_{RDD} = –4.2 V, current flowing out of VDD pin, T_{A} = 25°C | | - | - | -10 | mA |
| SLEEP Input Threshold | V _{INHI} | | | $0.7 \times V_{DD}$ | _ | - | V |
| | V _{INLO} | | | - | _ | $0.2 \times V_{DD}$ | V |
| SLEEP Input Current | I _{IN} | V _{DD} = 3. | V _{DD} = 3.6 V | | 1.0 | 5 | μA |
| SLEEP Reverse Input Current | I _{RIN} | V_{RIN} = -4.2 V, current flowing out of SLEEP pin, T _A = 25°C | | _ | - | -10 | mA |
| Restart Delay ⁴ | t _{RS} | V _{DD} = 3.6 V | | _ | 100 | - | ms |
| Hall Chopping Settling Time ⁵ | t _{S(CHOP)} | | | _ | 160 | - | μs |
| Thermal Shutdown Limit | T _{JTSD} | Device is active | | - | 165 | - | °C |
| Thermal Shutdown Hysteresis | T _{JTSD(HYS)} | Device is active | | - | 20 | - | °C |
| Internal PWM Frequency | f _{PWM} | | | - | 40 | - | kHz |
| PDC High Level Threshold | V _{PDCH} | PDC input going from low to high state | | V _{DD} -0.5 | _ | V _{DD} | V |
| PDC Low Level Threshold | V _{PDCL} | PDC input going from high to low state | | 0 | _ | 0.5 | V |
| PDC Input Current ⁶ | I _{PDCH} | Steady state condition, PDC pin high | | - | _ | 30 | μΑ |
| | I _{PDCL} | Steady state condition, PDC pin low state | | -30 | _ | - | μA |
| Internal PWM Duty Cycle | DC _{PWM} | A1444 | $V_{PDC} < V_{PDCL}, V_{DD} = V_{DDN}, S_{ROT} > S_{ROT(th)}$ | - | 56 | - | % |
| | | | PDC Pin Floating, $V_{DD} = V_{DDN}$, S _{ROT} > S _{ROT(th)} | - | 62 | - | % |
| | | | $V_{PDC} > V_{PDCH}, V_{DD} = V_{DDN},$ $S_{ROT} > S_{ROT(th)}$ | _ | 68 | - | % |
| | | A1445 | $V_{PDC} < V_{PDCL}, V_{DD} = V_{DDN},$ $S_{ROT} > S_{ROT(th)}$ | - | 71 | - | % |
| | | | PDC Pin Floating, $V_{DD} = V_{DDN}$, S _{ROT} > S _{ROT(th)} | - | 80 | - | % |
| | | | $\label{eq:pdc} \begin{array}{ c c } V_{PDC} > V_{PDCH}, \ V_{DD} = V_{DDN}, \\ S_{ROT} > S_{ROT(th)} \end{array}$ | - | 89 | - | % |

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ELECTRICAL CHARACTERISTICS (continued) valid over supply voltage and ambient temperature ranges, unless otherwise noted

| Characteristics | Symbol | Test Conditions | Min. | Typ. ¹ | Max. | Unit |
|-----------------------|------------------|--|------|-------------------|------|------|
| Magnetic Switchpoints | B _{OP} | $2 \text{ V} \leq \text{V}_{\text{DD}} \leq 4 \text{ V}$ | _ | 35 | 75 | G |
| | B _{RP} | $2 \text{ V} \leq \text{V}_{\text{DD}} \leq 4 \text{ V}$ | -75 | -35 | _ | G |
| | B _{HYS} | $2 \text{ V} \leq \text{V}_{\text{DD}} \leq 4 \text{ V}$ | _ | 70 | _ | G |
| Output Polarity | VOUT1 | B < B _{RP} | _ | LOW | - | V |
| | | B > B _{OP} | _ | HIGH | - | V |
| | VOUT2 | B < B _{RP} | _ | HIGH | _ | V |
| | | B > B _{OP} | _ | LOW | - | V |

¹Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions, such as $T_A = 25^{\circ}$ C. Performance may vary for individual units, within the specified maximum and minimum limits.

²Device operates with lower supply voltages, down to 1.8 V, with slight variation in specification of magnetic switchpoints and Total Output On-Resistance. ³Total Output On-Resistance = $R_{DS(on)Q1} + R_{DS(on)Q4}$, or $R_{DS(on)Q2} + R_{DS(on)Q3}$, where Qx refers to the internal full-bridge transistors.

⁴Restart Delay is the duration required from power-up of the device to valid device output.

⁵Hall Chopping Settling Time is the delay from power-on of the device to the initial valid device output.

⁶Positive current is defined as flowing into the device.



Functional Description

Soft Switching

The A1444 and A1445 devices include a soft switching algorithm that controls the output switching slew rate for both output pins. As a result, the devices are ideal for use in applications requiring low audible switching noise and low EMI interference.

Braking and Sleep Mode

The SLEEP pin accepts an external signal that enables braking and a sleep mode. During braking, the device reverses the polarity of the output bridge for a fixed time period, then the device enters sleep mode. In sleep mode, the device current consumption gets reduced to an extremely low level, conserving battery power.

Antistall Algorithm

If a stall condition occurs, the device will execute an antistall algorithm to restart the motor.

Device Start-up

The start-up behavior of the device output is determined by the applied magnetic field, as specified in the Electrical Characteristics table.

Speed Control

When the rate of rotation exceeds the specified threshold, $S_{ROT(th)}$, the A1444/A1445 output bridge becomes controlled by an internally generated PWM signal. The duty cycle of the internal PWM signal regulates the maximum motor rpm. The PWM duty cycle, however, is user-selectable through the state of the PDC pin. The PWM duty cycle options are given in the Electrical Characteristics table.



Low-Voltage Full-Bridge Brushless DC Motor Driver with Hall Commutation, Externally Controlled Speed Regulation, Soft Switching, and Reverse Battery, Short Circuit, and Thermal Shutdown Protection

Application Information

Two typical application circuits are shown in figures 1 and 2. The application circuit in figure 1 shows the device $\overline{\text{SLEEP}}$ pin controlled by the user. In this case, the device is powered continuously and the average supply current would switch between low and high values depending on the state of the $\overline{\text{SLEEP}}$ pin.

Figure 2 illustrates an applications circuit where the device supply pin and $\overline{\text{SLEEP}}$ pin are connected together. When power is applied to the device, it enters enable mode and operates with high average supply current.

Note that:

- No external diode is required for reverse battery protection because the protection is fully integrated into the IC.
- Thermal shutdown also is integrated to protect the device against inadvertent output shorts during manufacturing or testing.
- In these figures, the PDC pin is tied to GND. Alternatively, the PDC pin could be tied to any of the voltage rails or left floating, which will determine the internal PWM duty cycle as specified in the Electrical Characteristics table.



Figure 1. Application circuit showing user-controlled sleep/enable mode, while the A144x remains powered at all times



Figure 2. Application circuit showing simultaneous user control of power supply and sleep mode.



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Power Derating

The device must be operated below the maximum junction temperature of the device, T_J (max). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J . (Thermal data is also available on the Allegro MicroSystems website.)

The package thermal resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the effective thermal conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A , and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J , at various P_D levels.

$$P_{\rm D} = V_{\rm IN} \times I_{\rm IN} \tag{1}$$

$$\Delta T = P_D \times R_{\theta JA} \tag{2}$$

$$T_J = T_A + \Delta T \tag{3}$$

For a load of 30 Ω , and given common conditions such as: T_A= 25°C, V_{DD} = 3 V, I_{DD} = 85 mA, V_{LOAD} = 2.43 V, I_{LOAD} = 83 mA, and R_{θ JA} = 250 °C/W,

then:

$$\begin{split} P_D &= V_{DD} \times I_{DD} - V_{LOAD} \times I_{LOAD} \\ &= 3 \ V \times 83 \ mA - 2.43 \ V \times 81 \ mA \\ &= 52.17 \ mW \\ \Delta T &= P_D \times R_{\theta JA} \\ &= 52.17 \ mW \times 250 \ ^{\circ}C/W \\ &= 13 \ ^{\circ}C \\ T_J &= T_A + \Delta T \\ &= 25 \ ^{\circ}C + 13 \ ^{\circ}C \\ &= 38 \ ^{\circ}C \end{split}$$

A worst-case estimate, $P_D(max)$, represents the maximum allowable power level, without exceeding $T_J(max)$, at a selected $R_{\theta JA}$ and T_A .





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