CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**A104SN03 V1**
CUSTOMER APPROVED	Title : Name :

☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.____)**

☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.____)**

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☐ **CUSTOMER REMARK :**

AUO PM :

P/N : _____

Comment :

Doc. version :	0.4
Total pages :	33
Date :	2009/02/04

Product Specification

10.4" COLOR TFT-LCD MODULE

Model Name : **A104SN03 V1**

Planned Lifetime:	From 2008/Dec To 2010/Dec
Phase-out Control:	From 2010/Jul To 2010/Dec
EOL Schedule:	2010/Dec

< ◆ >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2008/10/29	All	First Draft
0.1	2008/11/12	24	Update Response time
		29	Update drawing
0.2	2009/01/07	4	Update drawing
		17	Update Register Table
		18	Delete R1 setting
0.3	2009/1/16	4	Update drawing
		10	Delete extra Electrical DC Characteristics
		32	Add Application Circuit
0.4	2009/02/04	8	Delete extra note

Contents

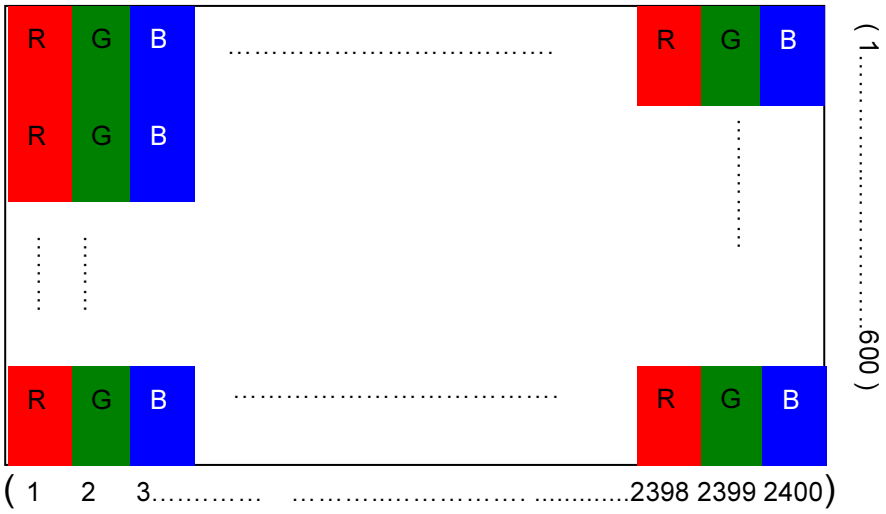
A. General Information

This product is for portable DVD and digital photo frame application.

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	10.4(Diagonal)	
2	Display Resolution	dot	800RGB(W)x600(H)	
3	Overall Dimension	mm	228.4(W)x175.4(H)x6.2(D)	Note 1
4	Active Area	mm	211.2(W)x158.4(H)	
5	Pixel Pitch	mm	0.264(W)x0.264(H)	
6	Color Configuration	--	R. G. B. Stripe	Note 2
7	Color Depth	--	16.7M Colors	Note 3
8	NTSC Ratio	%	50	
9	Display Mode	--	Normally White	
10	Panel surface Treatment	--	Anti-Glare, 3H	
11	Weight	g	400±20	
12	Panel Power Consumption	W	0.43	Note 4
13	Backlight Power Consumption	W	2.97	
14	Viewing direction		6 o'clock (gray inversion)	

Note 1: Not include blacklight cable and FPC. Refer next page to get further information.

Note 2: Below figure shows dot stripe arrangement.

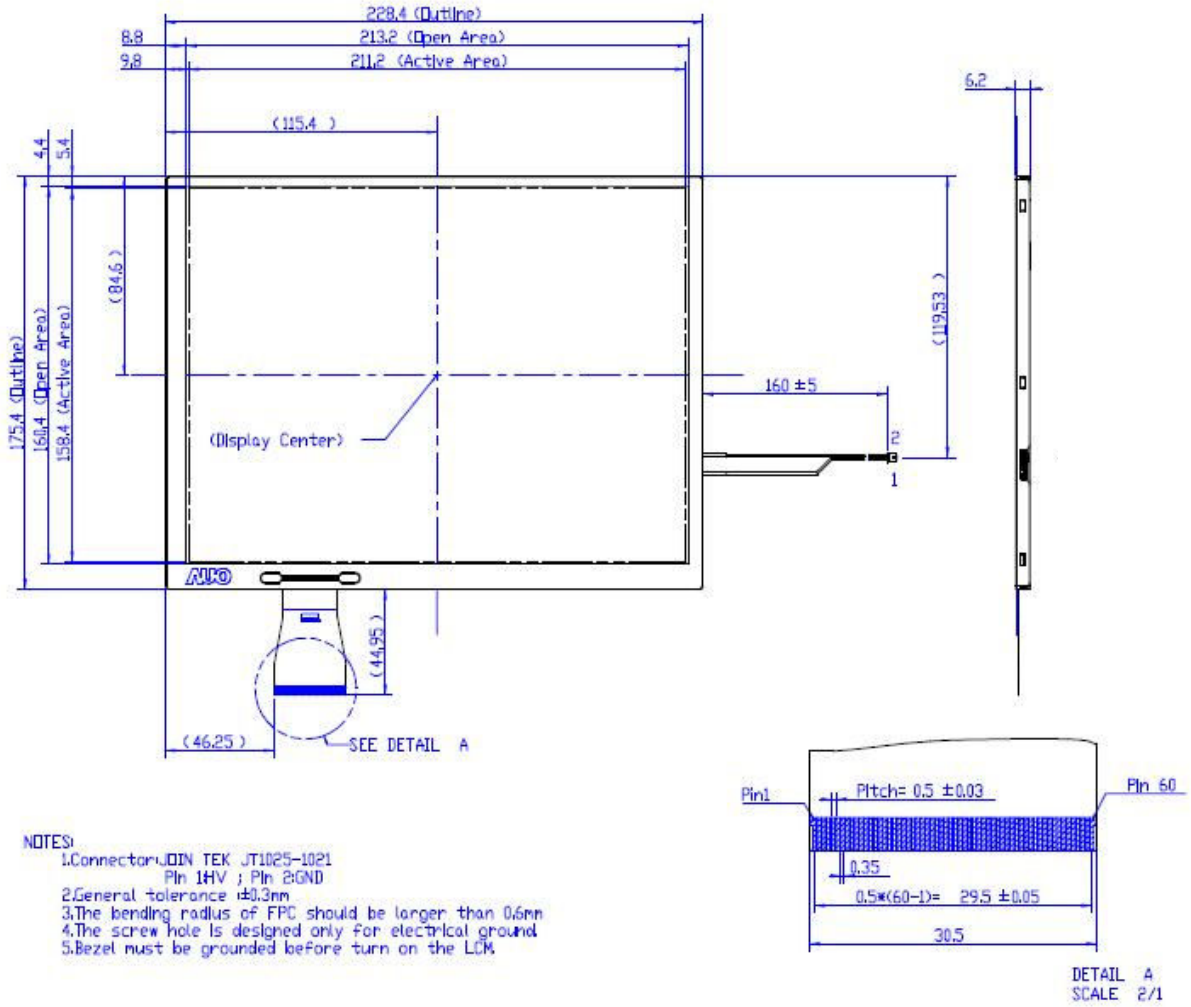


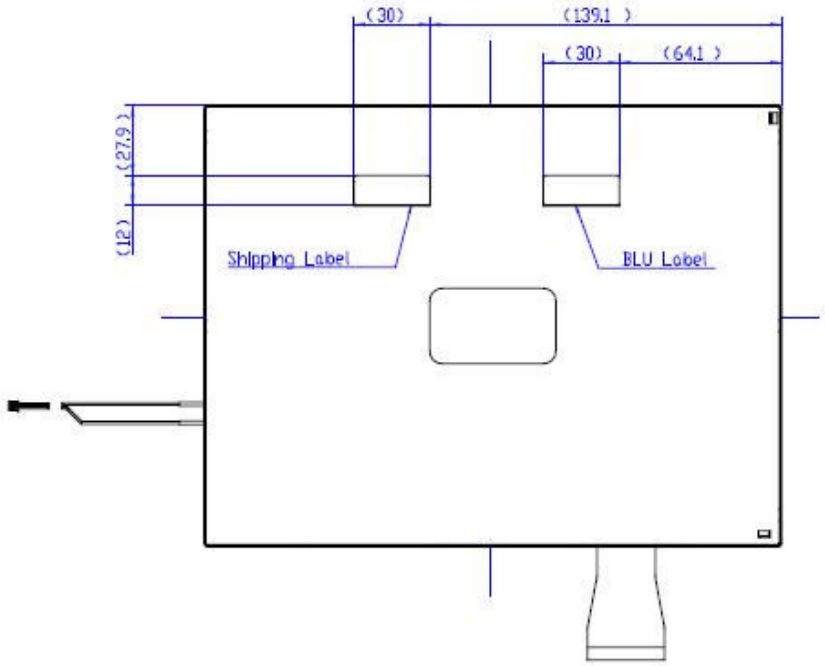
Note 3: The full color display depends on 24-bit data signal (pin 4~27).

Note 4: Please refer to Electrical Characteristics chapter.

B. Outline Dimension

1. TFT-LCD Module





C. Electrical Specifications

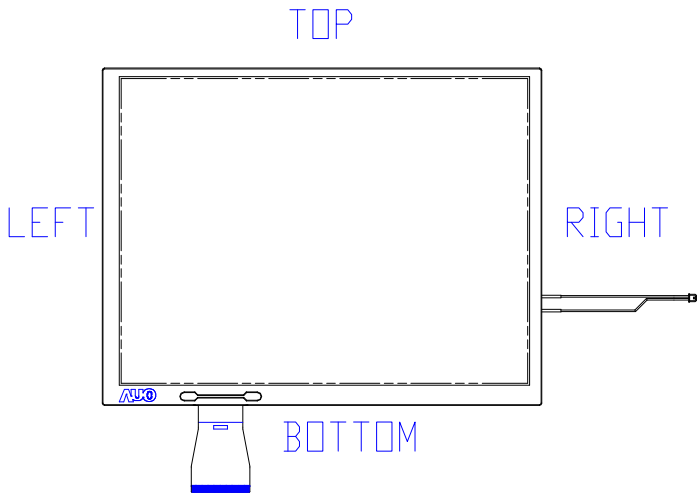
1. TFT LCD Panel Pin Assignment

Recommended connector : HRS FH28-60S-0.5SH

Pin no	Symbol	I/O	Description	Remark
1	AGND	P	Ground for analog circuit	
2	AVDD	P	Analog power supply voltage	
3	VDDIO	P	Digital interface supply voltage	
4	R0	I	Red data input (LSB)	
5	R1	I	Red data input	
6	R2	I	Red data input	
7	R3	I	Red data input	
8	R4	I	Red data input	
9	R5	I	Red data input	
10	R6	I	Red data input	
11	R7	I	Red data input (MSB)	
12	G0	I	Green data input (LSB)	
13	G1	I	Green data input	
14	G2	I	Green data input	
15	G3	I	Green data input	
16	G4	I	Green data input	
17	G5	I	Green data input	
18	G6	I	Green data input	
19	G7	I	Green data input (MSB)	
20	B0	I	Blue data input (LSB)	
21	B1	I	Blue data input	
22	B2	I	Blue data input	
23	B3	I	Blue data input	
24	B4	I	Blue data input	
25	B5	I	Blue data input	
26	B6	I	Blue data input	
27	B7	I	Blue data input (MSB)	
28	DCLK	I	Data clock input	
29	DE	I	Data enable signal	
30	HSYNC	I	Horizontal sync input. (Negative polarity)	
31	VSYNC	I	Vertical sync input. (Negative polarity)	
32	SCL	I	Serial communication clock input	
33	SDA	I	Serial communication data input	
34	CSB	I	Serial communication chip select	

35	NC	-	For test, do not connect (Please leave it open)	
36	VDDIO	P	Digital interface supply voltage	
37	NC	-	For test, do not connect (Please leave it open)	
38	GND	P	Ground for digital circuit	
39	AGND	P	Ground for analog circuit	
40	AVDD	P	Analog power supply voltage	
41	VCOMin	I	For external VCOM DC input	
42	DITH	I	Dithering setting DITH = "L" 6bit resolution(LSB last 2 bits of input data turncated) DITH = "H" 8bit resolution(Default setting)	
43	NC	-	For test, do not connect (Please leave it open)	
44	VCOM	O	connect a capacitor	
45	V10	I	Gamma correction voltage reference	
46	V9	I	Gamma correction voltage reference	
47	V8	I	Gamma correction voltage reference	
48	V7	I	Gamma correction voltage reference	
49	V6	I	Gamma correction voltage reference	
50	V5	I	Gamma correction voltage reference	
51	V4	I	Gamma correction voltage reference	
52	V3	I	Gamma correction voltage reference	
53	V2	I	Gamma correction voltage reference	
54	V1	I	Gamma correction voltage reference	
55	NC	-	For test, do not connect (Please leave it open)	
56	VGH	P	Positive power for TFT	
57	VDDIO	P	Digital interface supply voltage	
58	VGL	P	Negative power supply for Gate driver.	
59	GND	P	Ground for digital circuit	
60	NC	-	For test, do not connect (Please leave it open)	

I: Input; P: Power



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2. Backlight Pin Assignment

Recommended connector : JOIN TEK JT1025-1021

Pin no	Symbol	I/O	Description	Remark
1	VLED+	P	Backlight LED anode	
2	VLED-	P	Backlight LED cathode	

3. Absolute Maximum Ratings

Item	Symbol	Conditio	Min.	Max.	Unit	Remark
Power voltage	VDDIO	GND=0	-0.5	5	V	Digital Power Supply
	AVDD	AGND=0	-0.5	15	V	Analog power supply
	VGH	GND=0	-0.3	42	V	Gate driver supply voltage
	VGL		-20	0.3	V	Gate driver supply voltage
	VGH－VGL		-	40	V	Gate driver supply voltage
Input signal voltage	V_I		-0.3	VDDIO+0.3	V	Note 1
	VCOMin		0	5	V	VCOM DC Voltage
Operating	Topa		-10	60	℃	
Storage	Tstg		-20	70	℃	

Note 1: Functional operation should be restricted under ambient temperature (25℃).

Note 2: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

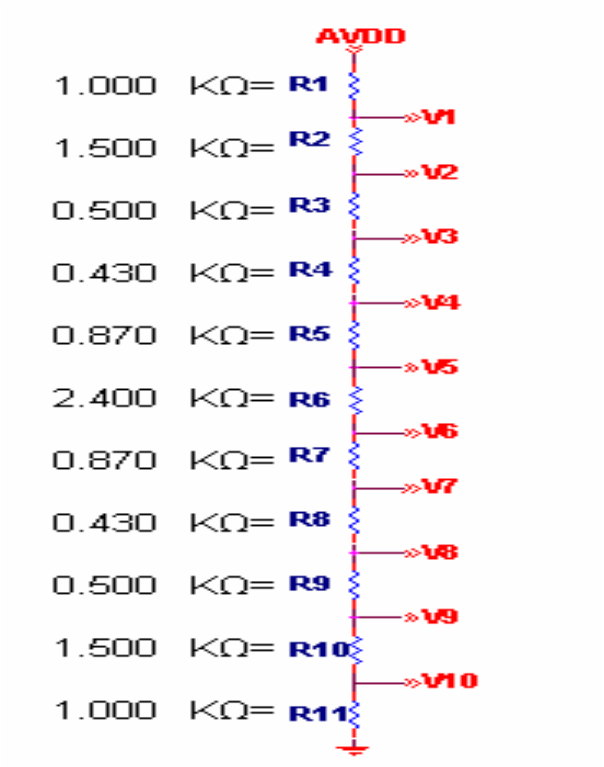
3. Electrical DC Characteristics

a. Typical Operation Condition (AGND =GND = 0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Voltage		VDDIO	3.0	3.3	3.6	V	Digital Power Supply
		AVDD	10.5	11	11.5	V	Analog Power Supply
		VGH	14	15	16	V	Positive power supply for gate driver
		VGL	-7.5	-7	-6.5	V	Negative power supply for gate driver
Input Signal Voltage	H Level	VIH	0.7xVDDIO	--	VDDIO	V	
	L Level	VIL	GND	--	0.3xVDDIO	V	
Gamma reference voltage		V1 ~ V5	AVDD/2	-	AVDD – 1	V	Note 1
		V6 ~ V10	1	-	AVDD/2	V	
VCOMin		V_{CDC}	3.75	3.95	4.15	V	Note 2

Note 1: Gamma suggested circuit is as follows

Pin	Voltage(V)
AVDD	11
V1	10
V2	8.5
V3	8
V4	7.57
V5	6.7
V6	4.3
V7	3.43
V8	3
V9	2.5
V10	1



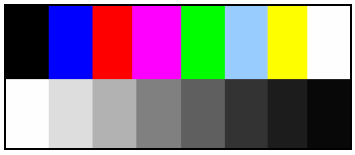
Note2: Based on recommended Gamma 2.2 voltage.

b. Current Consumption (AGND=GND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input current for VDDIO	IVDDIO	VDDIO = 3.3V		10	20	mA	Note 1, 2
Input current for AVDD	IAVDD	AVDD = 11V		24	30	mA	Note 1, 2
Input current for VGH	IVGH	VGH = 15V	--	0.4	0.6	mA	Note 1, 2
Input current for VGL	IVGL	VGL = -7V	-0.6	-0.4	--	mA	Note 1, 2

Note 1:Test Condition is under typical Eletrical DC and AC characteristics.

Note 2: Test pattern is the following picture.

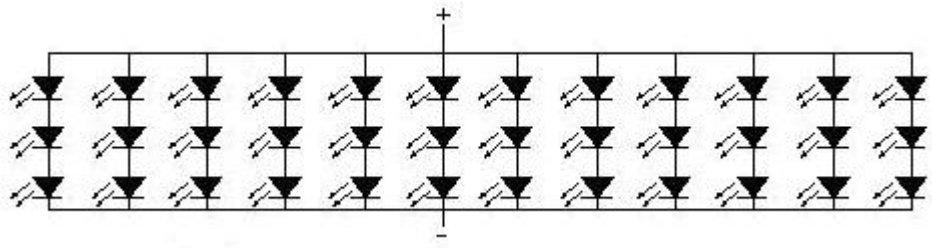


c. Backlight Driving Conditions

The backlight (LED module, Note 1) is suggested to drive by constant current with typical value.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED light bar Current	I_L	--	300	--	mA	
Power Consumption	P	--	3	3.21	W	Note 1
LED Life Time	L_L	10,000	--	--	Hr	Note 2, 3

Note 1: The LED driving condition is defined for LED module (36 LED). The Voltage range will be 8.8V to 10.7V based on suggested driving current set as 300mA.



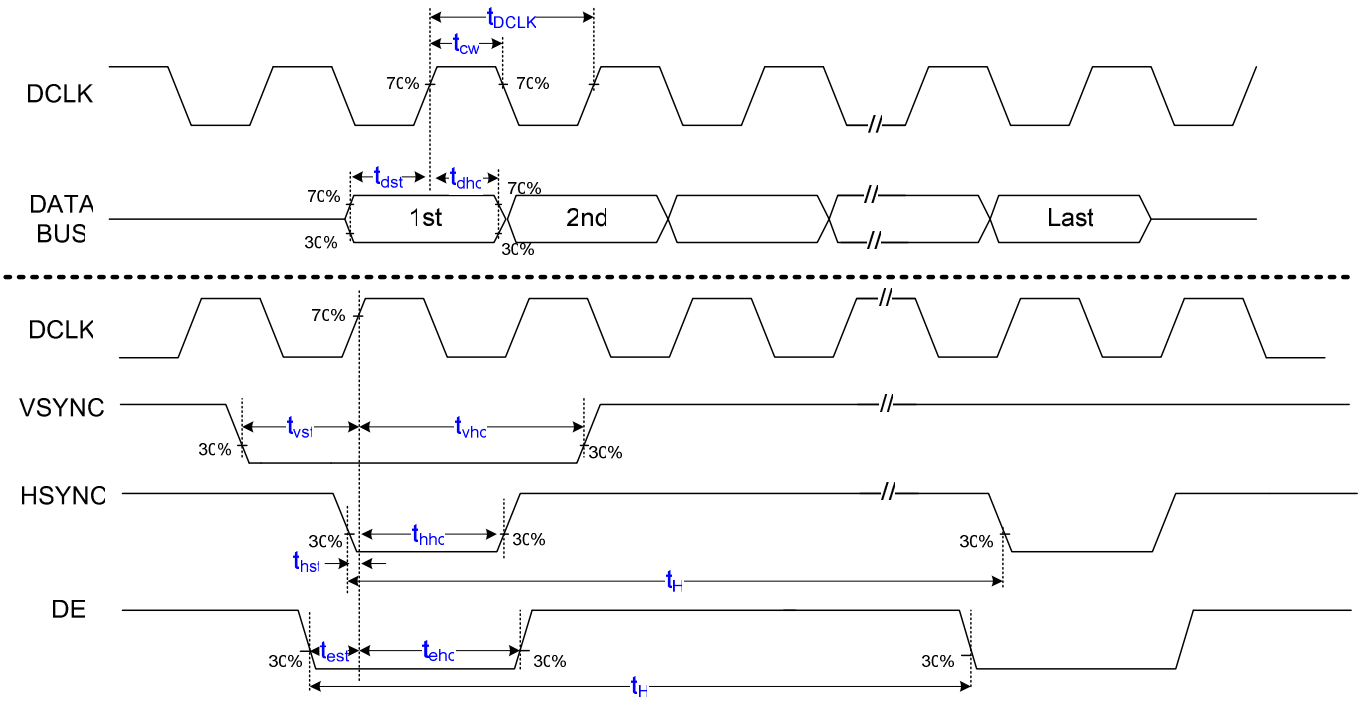
Note 2: Define “LED Lifetime”: brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25℃ and LED lightbar current = 300mA.

Note 3: If it uses larger LED lightbar current more than 300mA, it maybe decreases the LED lifetime.

4. Electrical AC Characteristics

a. Signal AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK duty cycle	--	40	50	60	%	t_{cw} / t_{DCLK} x100%
VSYNC setup time	t_{vst}	0	--	--	ns	
VSYNC hold time	t_{vhd}	2	--	--	ns	
HSYNC setup time	t_{hst}	5	--	--	ns	
HSYNC hold time	t_{hhd}	10	--	--	ns	
Data setup time	t_{dst}	5	--	--	ns	
Data hold time	t_{dhd}	10	--	--	ns	
Data enable set-up time	t_{est}	4	--	--	ns	
Data enable hold time	t_{ehd}	2	--	--	ns	

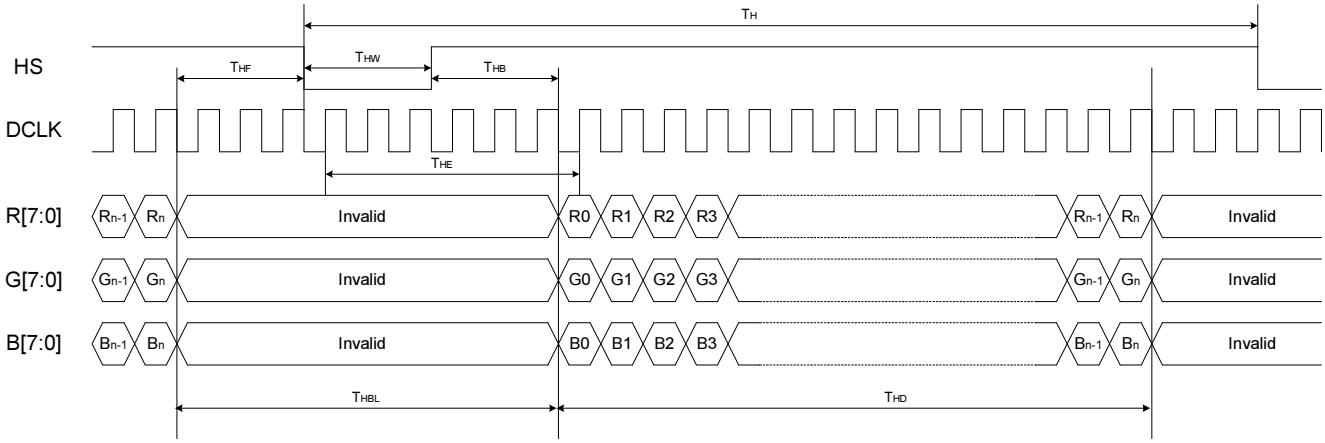


t_H: HSYNC period

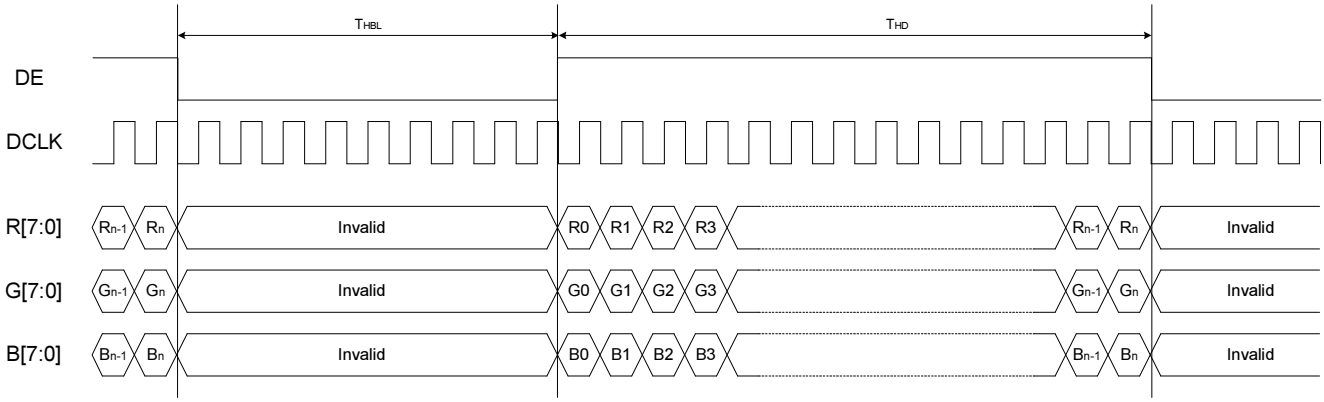
t_{DCLK}: DCLK period

t_{cw}: the width of DCLK high

b. Input Timing



Horizontal input timing. (HV mode)

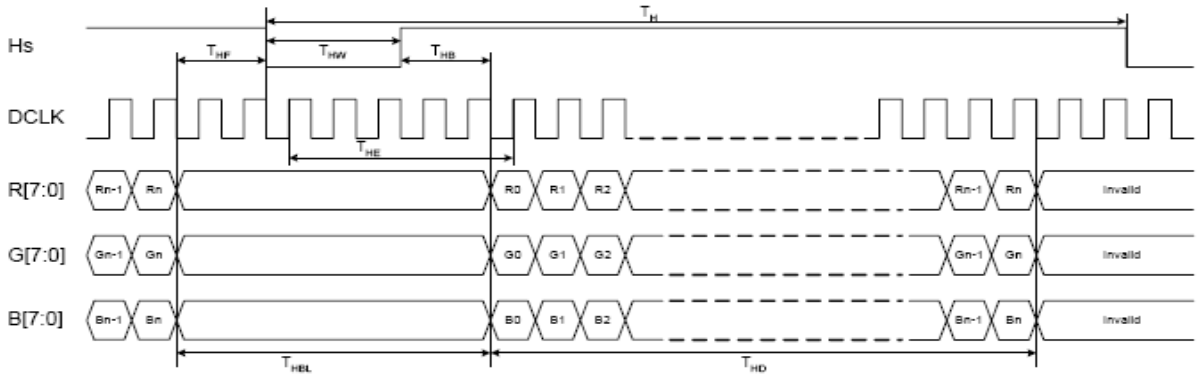


Horizontal input timing. (DE mode)

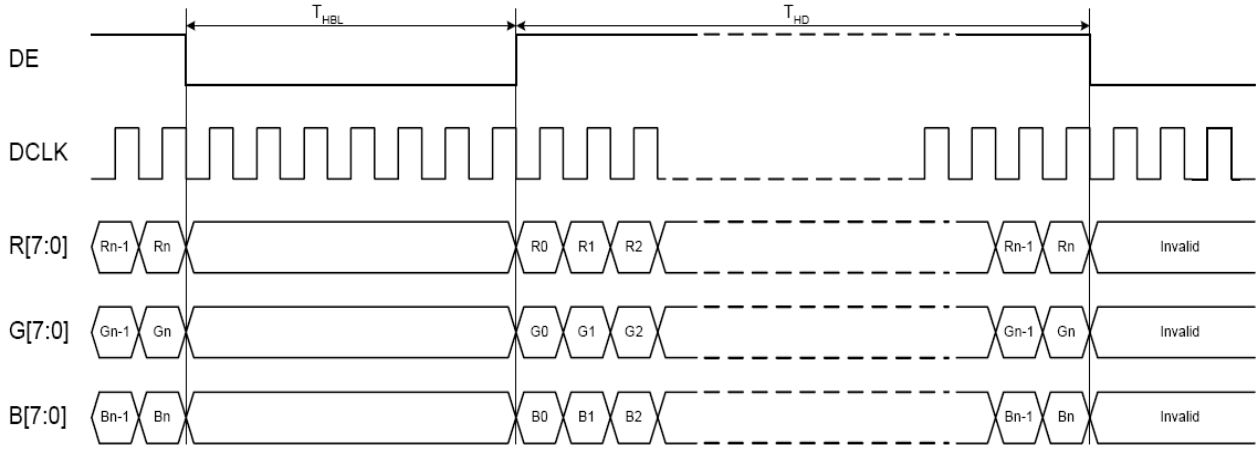
Horizontal Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency	F_{DCLK}	25	40	45	MHz	
DCLK period	T_{DCLK}	22	25	40	ns	
Hsync period (= T_{HD} + T_{HBL})	T_H	1026	1056	1183	DCLK	
Active Area	T_{HD}	-	800	-	DCLK	
Horizontal blanking (= T_{HF} + T_{HE})	T_{HBL}	226	256	383	DCLK	
Hsync front porch	T_{HF}	10	40	167	DCLK	
Delay from Hsync to 1st data input (= T_{HW} + T_{HB})	T_{HE}		216		DCLK	

Hsync pulse width	T_{HW}	1	128	136	DCLK	
Hsync back porch	T_{HB}	80	88	215	DCLK	



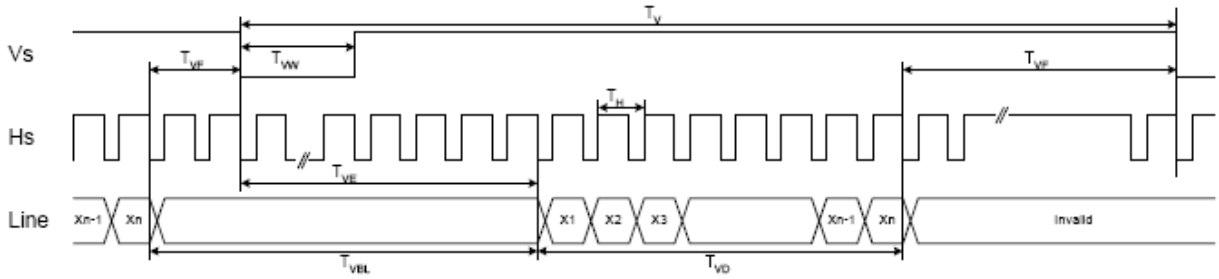
Horizontal input timing (HV mode)



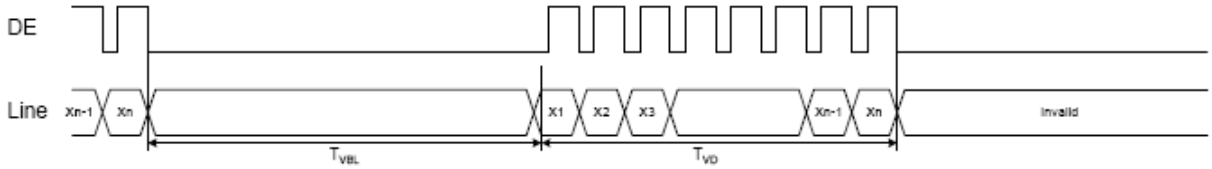
Horizontal input timing (DE mode)

Vertical Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Vsync period (= T_{VD} + T_{VBL})	T_V	-	628	635	Th	
Active lines	T_{VD}	-	600	-	Th	
Vertical blanking (= T_{VF} + T_{VE})	T_{VBL}	-	28	35	Th	
Vsync front porch	T_{VF}	-	1	8	Th	
GD start pulse delay	T_{VE}	-	27	-	Th	
Vsync pulse width	T_{VW}	1	3	16	Th	
Hsync/Vsync phase shift	T_{VPD}	2	320	-	DCLK	



Vertical timing (HV mode)

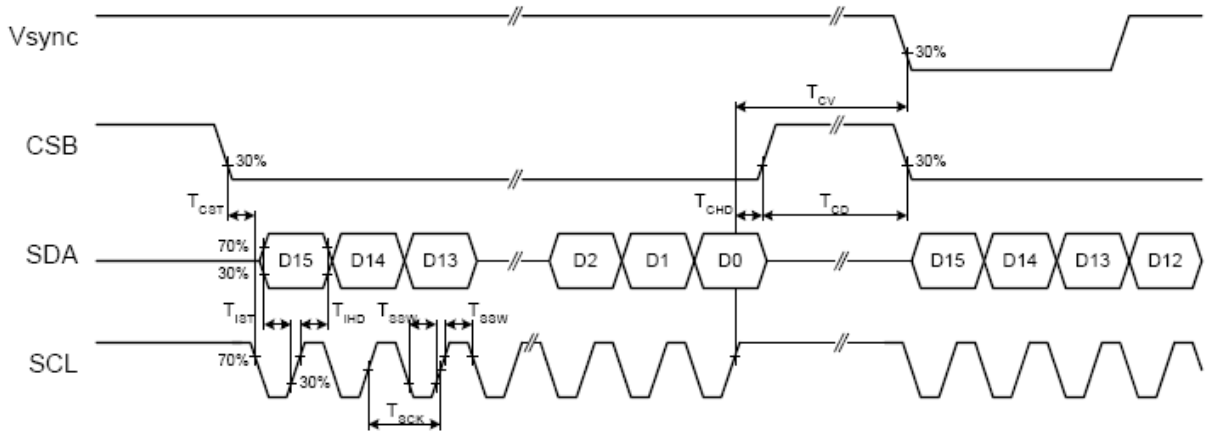


Vertical timing (DE mode)

5. Serial Interface Characteristics

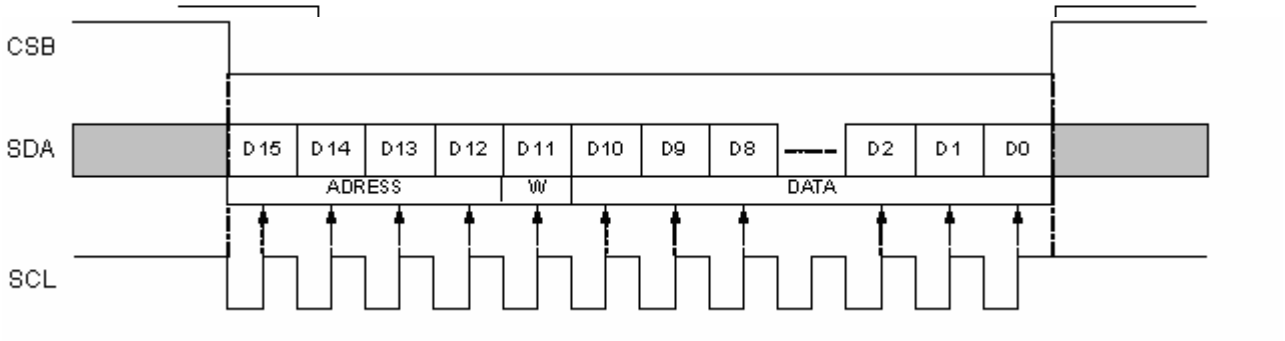
a. Serial Control Interface AC Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Serial data setup time	T_{IST}	120	-	-	ns	
Serial data hold time	T_{IHD}	120	-	-	ns	
CSB setup time	T_{CST}	120	-	-	ns	
CSB hold time	T_{CHD}	120	-	-	ns	
Serial clock high/low	T_{SSW}	120	-	-	ns	
Serial clock	T_{SCK}	320	-	-	ns	
Delay from CSB to VSYNC	T_{CV}	1	-	-	us	
Chip select distinguish	T_{CD}	1	-	-	us	
Serial data output delay	T_{ID}	-	-	60	ns	CL=20pF



b Serial Interface Timing

There is a total of 6 registers each containing several parameters. For a detailed description of the parameters refer to register table. The serial register has read/write function. D[15:12] are the register address, D[11] defines the read or write mode and D[10:0] are the data.



Serial Interface Write sequence

1. At power-on, the default values specified for each parameter are taken.
2. If less than 16-bit data are read during the CS low time period, the data is cancelled.
   a. The write operation is cancelled.
3. All items are set at the falling edge of the vertical sync, except R0[1:0].
4. When GRB is activated through the serial interface, all registers are cleared, except the GRB value.
5. The register setting values are valid when VCC already goes to high and after VSYNC starts.
6. It is suggested that VSYNC, HSYNC, DCLK always exists in the same time. But if HSYNC, DCLK stops, only VSYNC operating, the register setting is still valid.
7. If the chip goes to standby mode, the register value will still keep. MCU can wake up the chip only by changing standby mode value from low to high.
8. The register setting values are rewritten by the influence of static electricity, a noise, etc. to unsuitable value, incorrect operating may occur. It is suggested that the SPI interface will setup as frequently as possible.

c. Register Table (Default Value)

Reg	ADDRESS					R/W	DATA									
No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	(01)		(01)		(1)	U/D (0)	SHL (1)	(1)	(0)	GRB (1)	STB (1)
R2	0	0	1	0	0	×	×	×	HDL (80h)							
R3	0	0	1	1	0	×	×	(0)	(0)	(0)	(0)	(0)	VDL (1000)			
R4	0	1	0	0	0	×	×	(1)	(0)	(0)	(0)	(1)	(1111)			
R6	0	1	1	0	0	×	(0)	EnGB12 (1)	EnGB11 (1)	EnGB10 (1)	(0)	(0)	EnGB5 (1)	EnGB4 (1)	EnGB3 (1)	(0)

X: Reserved. Please set to “0”.

<Note>：Sending serial commands periodically is recommended to improve ESD protection ability.

d. Register Description

a. R0 setting

Address	**Bit**	**Description**		**Default**
0000	[10..0]	Bits 10-9	AUO Internal Use	01
		Bits7-8	AUO Internal Use	01
		Bit6 (DITH)	Dithering function.	1
		Bit5 (U/D)	Vertical shift direction selection.	0
		Bit4 (SHL)	Horizontal shift direction selection.	1
		Bit3	AUO Internal Use.	1
		Bit2	AUO Internal Use	0
		Bit1 (GRB)	Global reset.	1
		Bit0 (STB)	Standby mode setting.	1

Bit6	DITH function
0	DITH off.
1	DITH on. **(default)**

Bit5	U/D function
0	Scan down; First line= Gn -> Gn-1 -> … -> G2 -> Last line=G0. **(default)**
1	Scan up; First line= G0 -> G2 -> … -> Gn-1 -> Last line=Gn

Bit4	SHL function
0	Shift left; First data= Y600 -> Y599 -> … -> Y2 -> Last data=Y1.
1	Shift right; First data= Y1 -> Y2 -> … -> Y599 -> Last data=Y600. **(default)**

Bit1	GRB function
0	The controller is reset. Reset all registers to default value.
1	Normal operation. **(default)**

Bit0	STB function
0	T-CON, source driver and DC-DCs converters are off. All outputs are set to GND.
1	Normal operation. **(default)**

b. R2 setting

Address	**Bit**	**Description**		**Default**
0010	[7..0]	Bit7-0(HDL)	Horizontal start pulse adjustment function	80H

Bit7-0	HDL function
00h	$T_{HE} = T_{HEtyp}$ - 128 CLK period.
80h	$T_{HE} = T_{HEtyp}$. **(default)**
FFh	$T_{HE} = T_{HEtyp}$ + 127 CLK period.

c. R3 setting

Address	**Bit**	**Description**		**Default**
0011	[8..0]	Bit8	AUO Internal Use	0
		Bit7	AUO Internal Use	0
		Bit6	AUO Internal Use	0
		Bit5	AUO Internal Use	0
		Bit4	AUO Internal Use	0
		Bit3-0(VDL)	Vertical start pulse adjustment function	1000

Bit3-0	VDL function
0000	$T_{VE} = T_{VEtyp}$ – 8 Hs period.
0001	$T_{VE} = T_{VEtyp}$ – 7 Hs period.
0010	$T_{VE} = T_{VEtyp}$ – 6 Hs period.
0011	$T_{VE} = T_{VEtyp}$ – 5 Hs period.
0100	$T_{VE} = T_{VEtyp}$ – 4 Hs period.
0101	$T_{VE} = T_{VEtyp}$ – 3 Hs period.
0110	$T_{VE} = T_{VEtyp}$ – 2 Hs period.
0111	$T_{VE} = T_{VEtyp}$ – 1 Hs period.
1000	$T_{VE} = T_{VEtyp}$. (default)
1001	$T_{VE} = T_{VEtyp}$ – 1 Hs period.
1010	$T_{VE} = T_{VEtyp}$ – 2 Hs period.
1011	$T_{VE} = T_{VEtyp}$ – 3 Hs period.
1100	$T_{VE} = T_{VEtyp}$ – 4 Hs period.

1101	$T_{VE} = T_{VEtyp} – 5$ Hs period.
1110	$T_{VE} = T_{VEtyp} – 6$ Hs period.
1111	$T_{VE} = T_{VEtyp} – 7$ Hs period.

d. R6 setting

Address	**Bit**	**Description**		**Default**
0110	[9..0]	Bits9	AUO Internal Use	0
		Bits8(EnGB12)	Gamma buffer Enable for V9	1
		Bits7(EnGB11)	Gamma buffer Enable for V8	1
		Bits6(EnGB10)	Gamma buffer Enable for V7	1
		Bits5	AUO Internal Use	0
		Bits4	AUO Internal Use	0
		Bits3(EnGB5)	Gamma buffer Enable for V4	1
		Bits2(EnGB4)	Gamma buffer Enable for V3	1
		Bits1(EnGB3)	Gamma buffer Enable for V2	1
		Bits0	AUO Internal Use	0

Bitx	EnGBx function
0	Gamma buffer for VX is disabled (High Z).
1	Gamma buffer is enabled. VX must be connected externally.

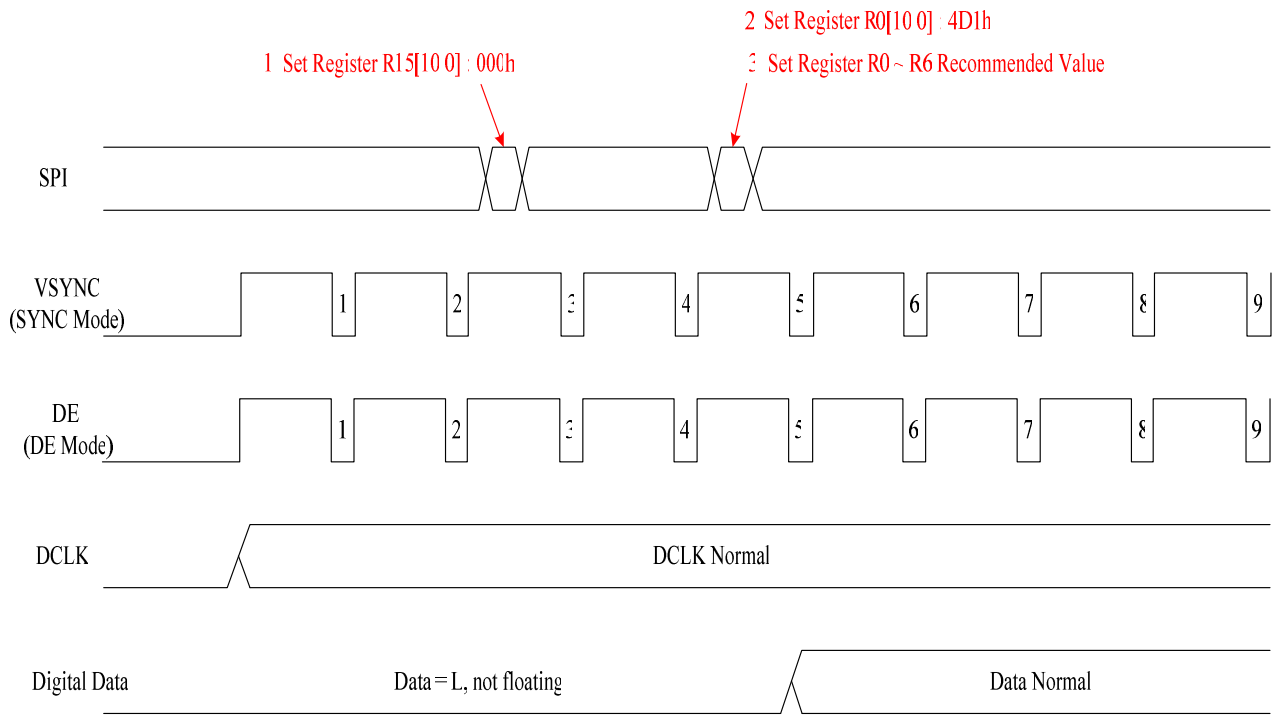
6. Power On/Off Characteristics

a. Recommended Power On Register Setting

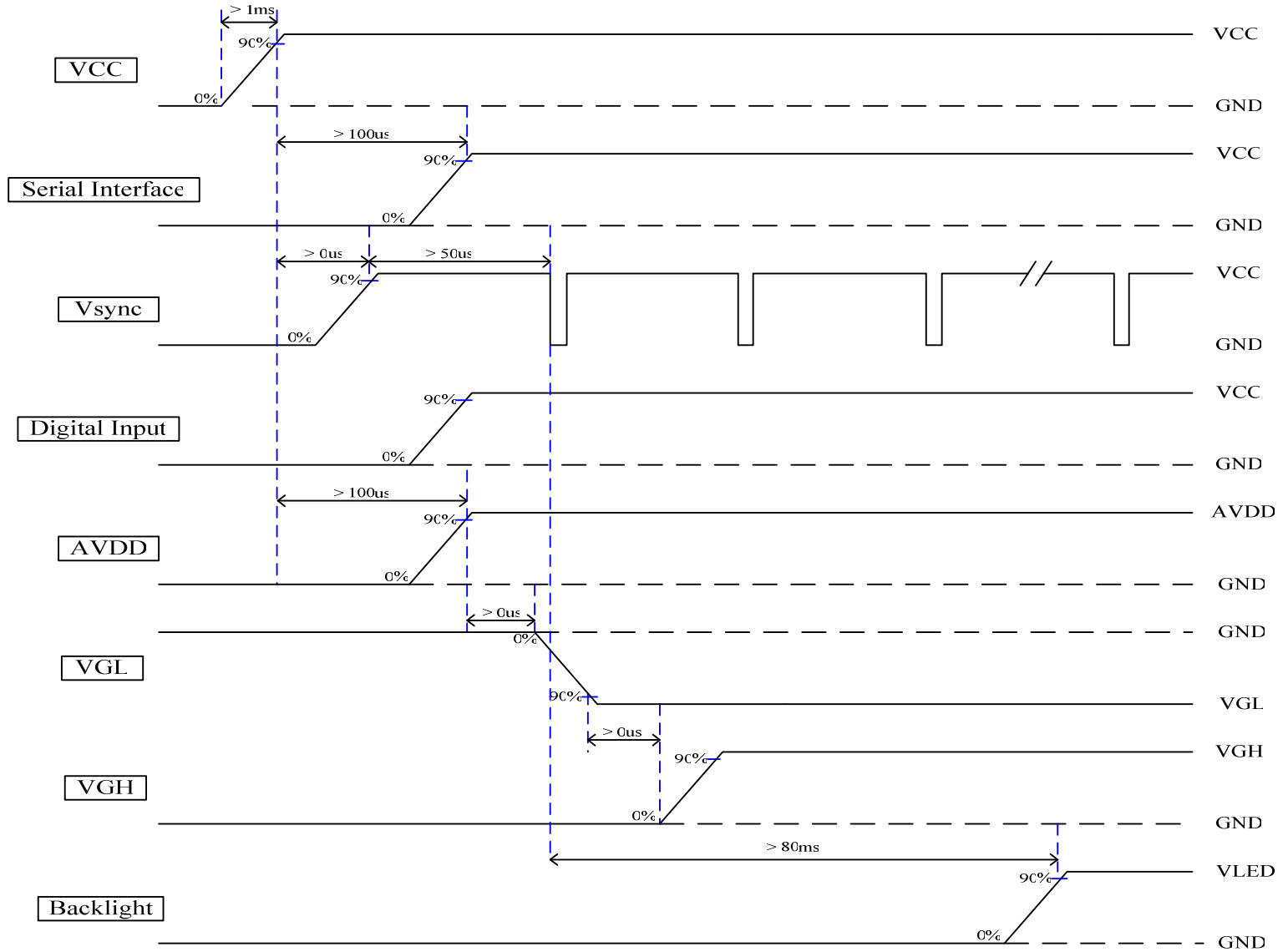
Reg	ADDRESS				R/W	DATA										
No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	10		01		1	0	1	0	0	1	1
R1	0	0	0	1	0	0	01		01		2Fh					
R2	0	0	1	0	0	0	0	0	80h							
R3	0	0	1	1	0	0	0	0	0	0	0	0	1000			
R4	0	1	0	0	0	0	0	1	1	00		1	1111			
R6	0	1	1	0	0	0	0	1	1	1	0	0	1	1	1	0

Note : Start to provide SPI commend at least after 2 frame.

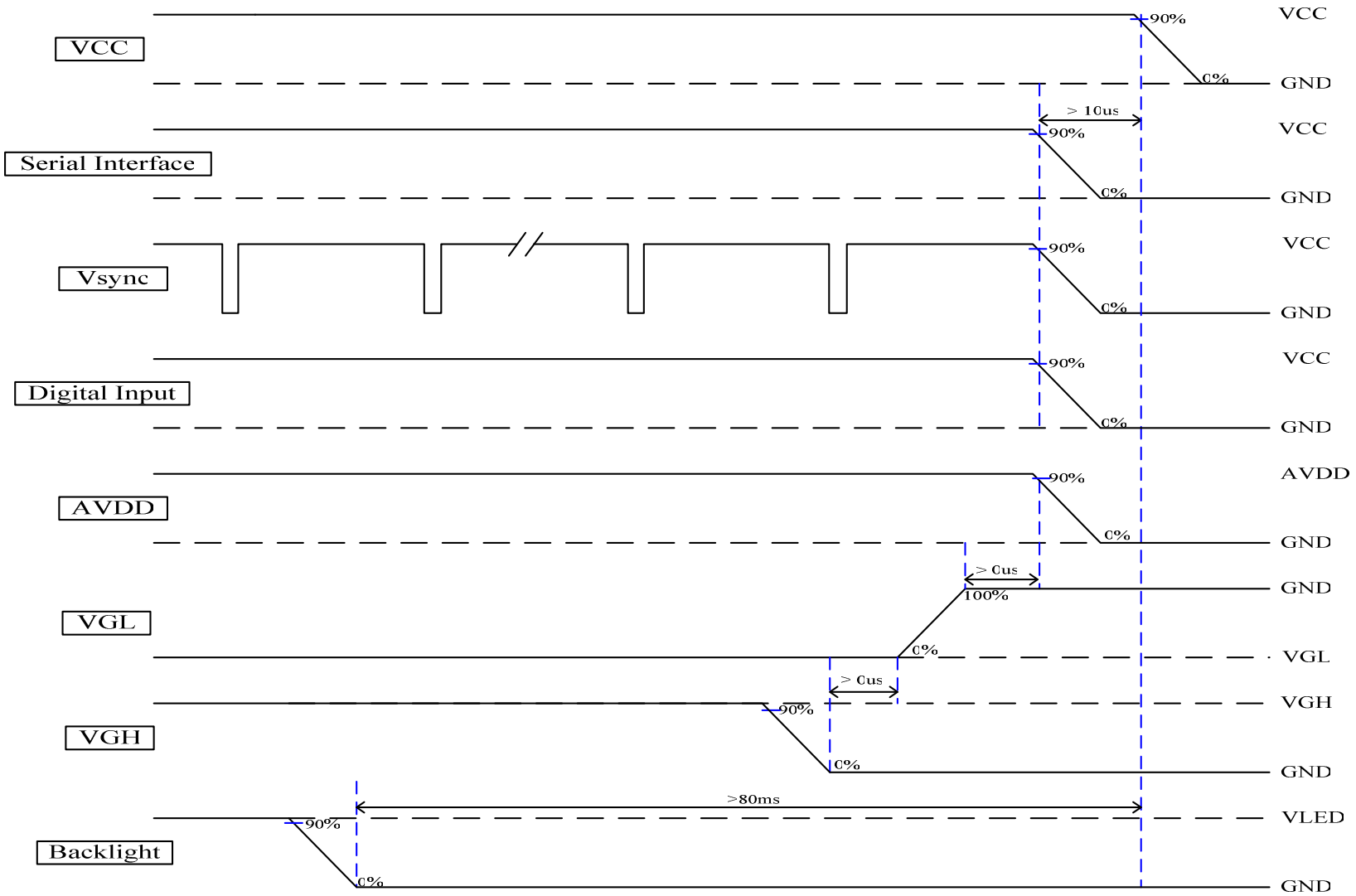
1. Send R15 : 000h(Normal register bank) at first.
2. Wait at least after more than one frame, send R0 : 4D1h(Global Reset)
3. After send Global Reset, start to send R0 to R6 recommend register value.



b. Recommended Power On Sequence



c. Power Off Sequence



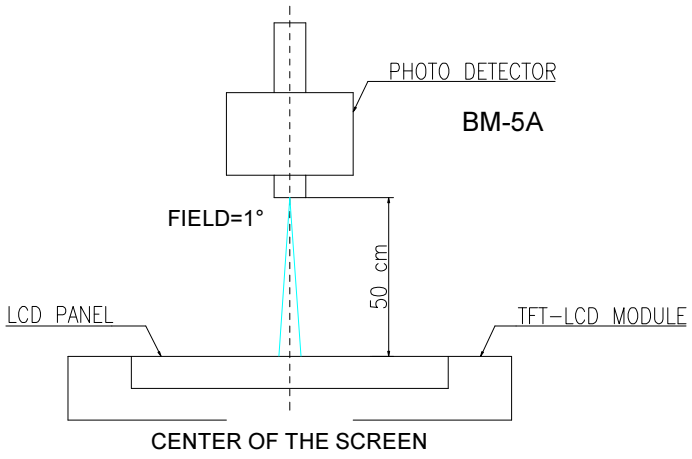
D. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall		 Tr Tf	 θ=0°	 -- --	 30	 7 33	 ms ms	Note 3
Contrast ratio		CR	At optimized viewing angle	300	500	--		Note 4
Viewing Angle	Top Bottom Left Right		CR≧10	40 50 65 65	50 60 75 75	-- -- -- --	deg.	Note 5
Brightness		Y_L	θ=0°	250	300	--	cd/m^2	Note 6
Chromaticity	White	X	θ=0°	0.28	0.33	0.38		
		Y	θ=0°	0.30	0.35	0.40		
	Red	X	θ=0°	0.550	0.600	0.650		
		Y	θ=0°	0.324	0.374	0.424		
	Green	X	θ=0°	0.306	0.356	0.406		
		Y	θ=0°	0.531	0.581	0.631		
	Blue	X	θ=0°	0.094	0.144	0.194		
		Y	θ=0°	0.043	0.093	0.143		
Uniformity		ΔY_L	%	75	80		--	Note 7

Note 1: Ambient temperature =25℃, and LED lightbar current I_L = 300mA. To be measured in the dark room.

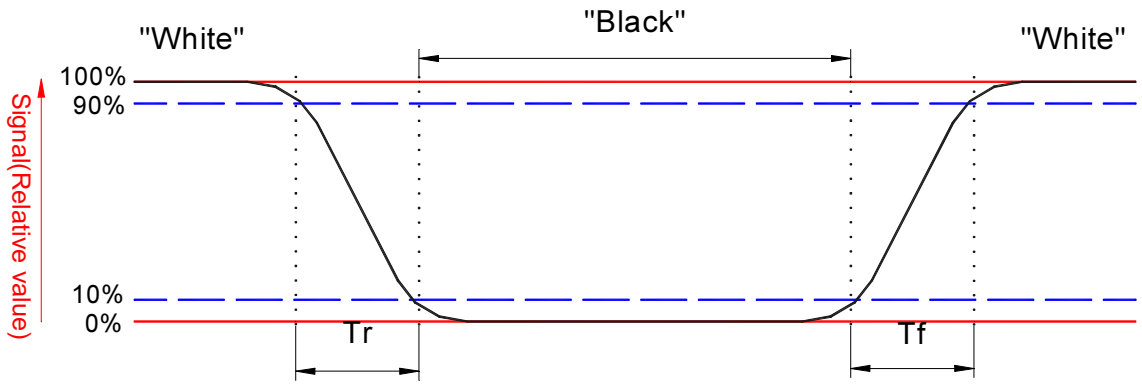
Note 2: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 15 minutes operation.



Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

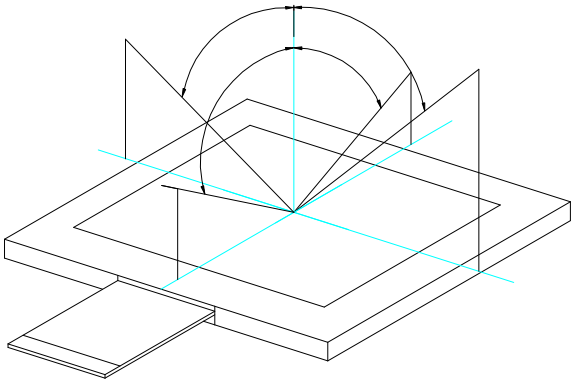


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

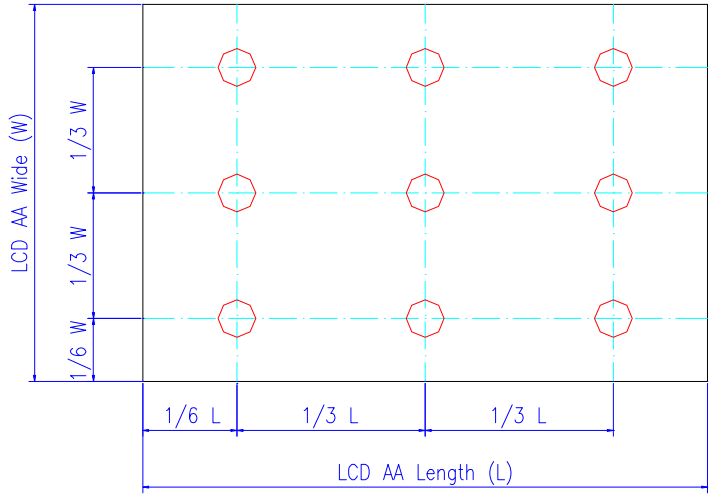
$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.



Note 6. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 7: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

E. Reliability Test Items

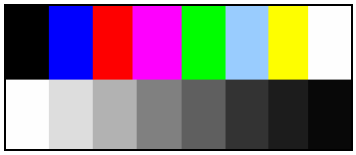
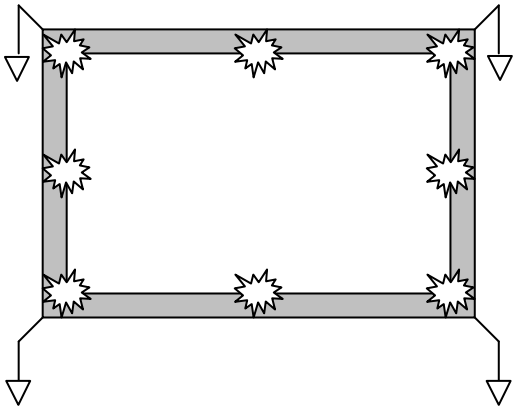
No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 70℃ 240Hrs	
2	Low Temperature Storage	Ta= -20℃ 240Hrs	
3	High Ttemperature Operation	Tp= 60℃ 240Hrs	
4	Low Temperature Operation	Ta=-10℃ 240Hrs	
5	High Temperature & High Humidity	Tp= 50℃. 80% RH 240Hrs	Operation
6	Heat Shock	-10℃~60℃/ 100 cycles 1Hrs/cycle	Non-operation
7	Electrostatic Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B	Note 5
8	Image Sticking	25℃, 4hrs	Note 6
9	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10 ~ 55 ~ 10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A : 15 minutes
10	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
11	Vibration (With Carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
12	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	
13	Pressure	5kg, 5sec	Note 7

Note 1: Ta: Ambient Temperature. Tp: Panel Surface Temperature

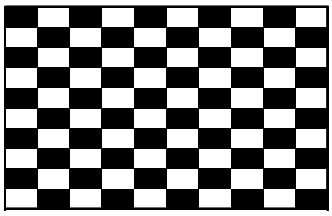
Note 2: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 3: All the cosmetic specification is judged before the reliability stress.

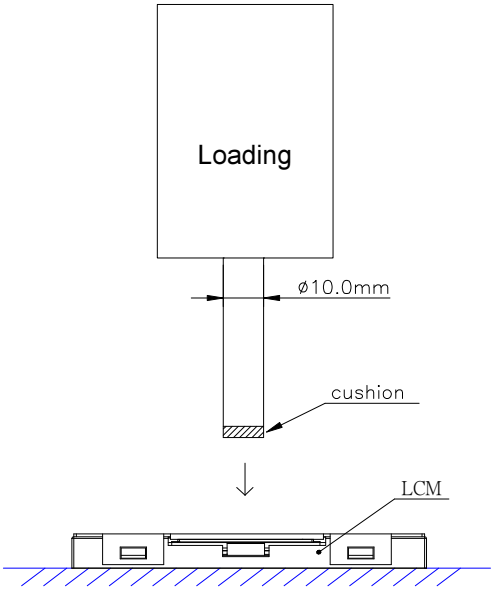
Note5 : All test techniques follow IEC6100-4-2 standard.

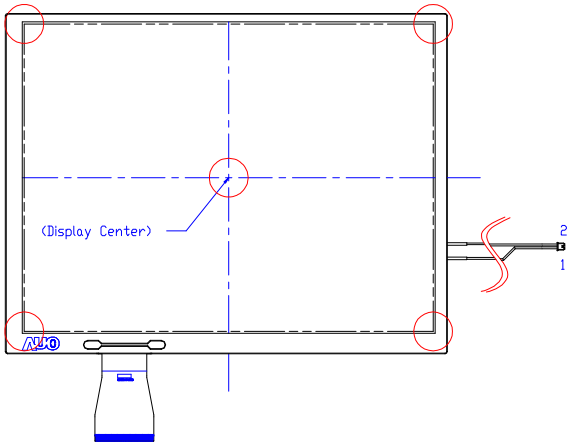
Test Condition		Note
Pattern		
Procedure And Set-up	Contact Discharge：330Ω, 150pF, 1sec, 8 point, 10times/point Air Discharge：330Ω, 150pF, 1sec, 8 point, 10times/point 	
Criteria	B – Some performance degradation allowed. No data lost. Self-recoverable hardware failure.	

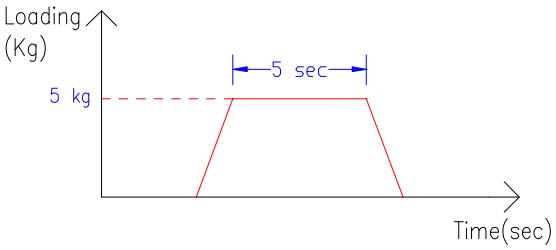
Note 6: Operate with chess board pattern as figure and lasting time and temperature as the conditions. Then judge with 50% gray level, the mura is less than JND 2.5



Note 7: The panel is tested as figure. The jig isψ10 mm made by Cu with rubber and the loading speed is 3mm/min on position A~E. After the condition, no glass crack will be found and panel function check is OK.(no guarantee LC mura、LC bubble)

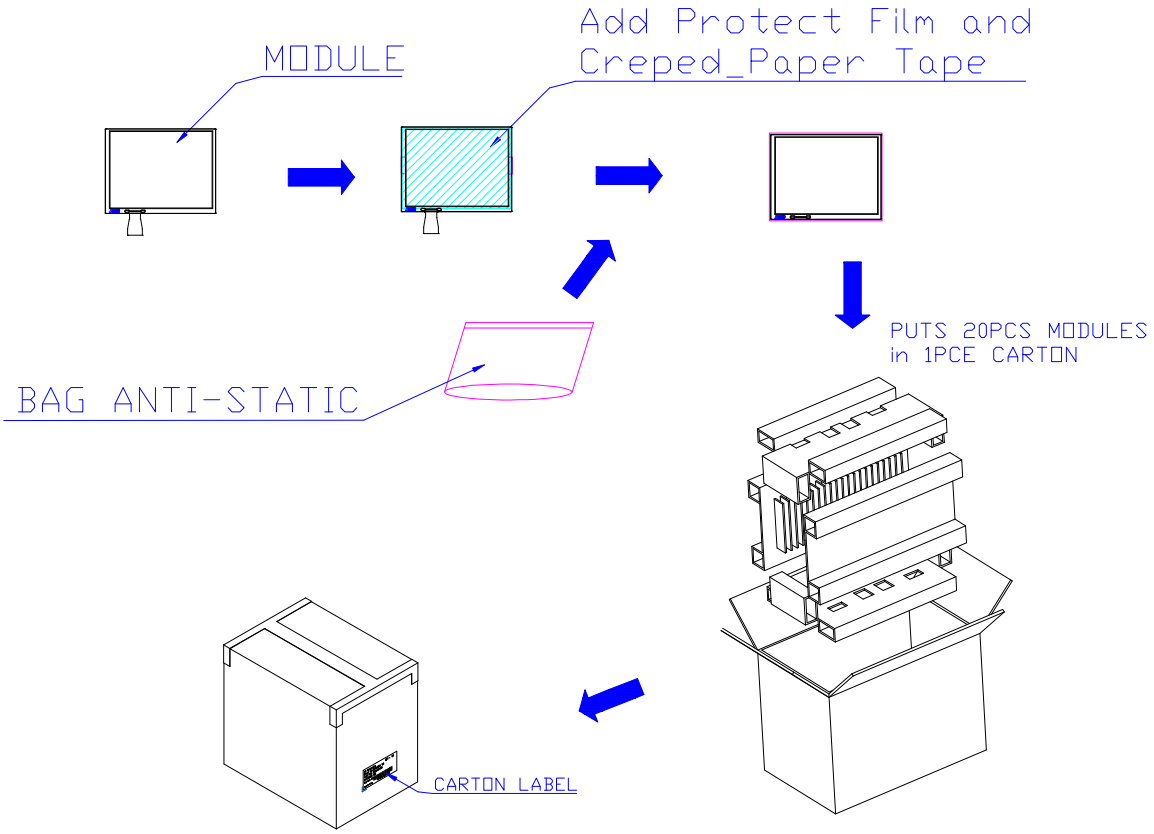






F. Packing and Marking

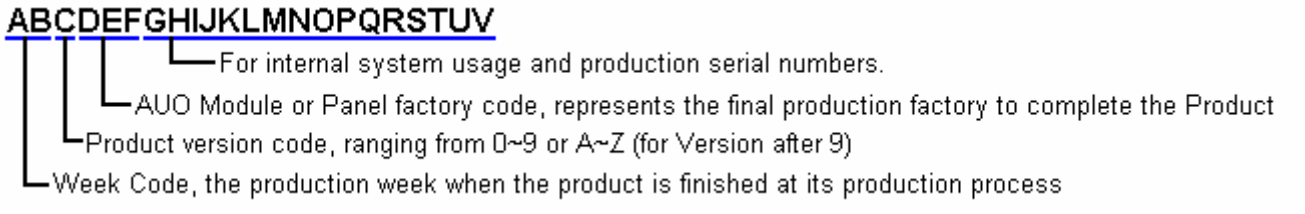
1. Packing Form



MAX. CAPACITY: 20MODULES
MAX. WEIGHT: 11 kg
CARTON Dim.:483(L)mm*296(W)mm*355(H)mm

2. Module/Panel Label Information

The module/panel (collectively called as the “Product”) will be attached with a label of Shipping Number which represents the identification of the Product at a specific location. Refer to the Product outline drawing for detailed location and size of the label. The label is composed of a 22-digit serial number and printed with code 39/128 with the following definition:



Example:

501M06ZL06123456781Z05:

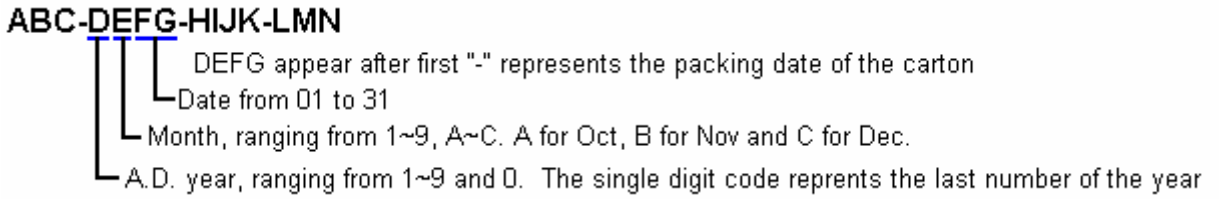
Product Manufacturing Week Code: WK50

Product Version: Version 1

Product Manufactuing Factory: M06

3. Carton Label Information

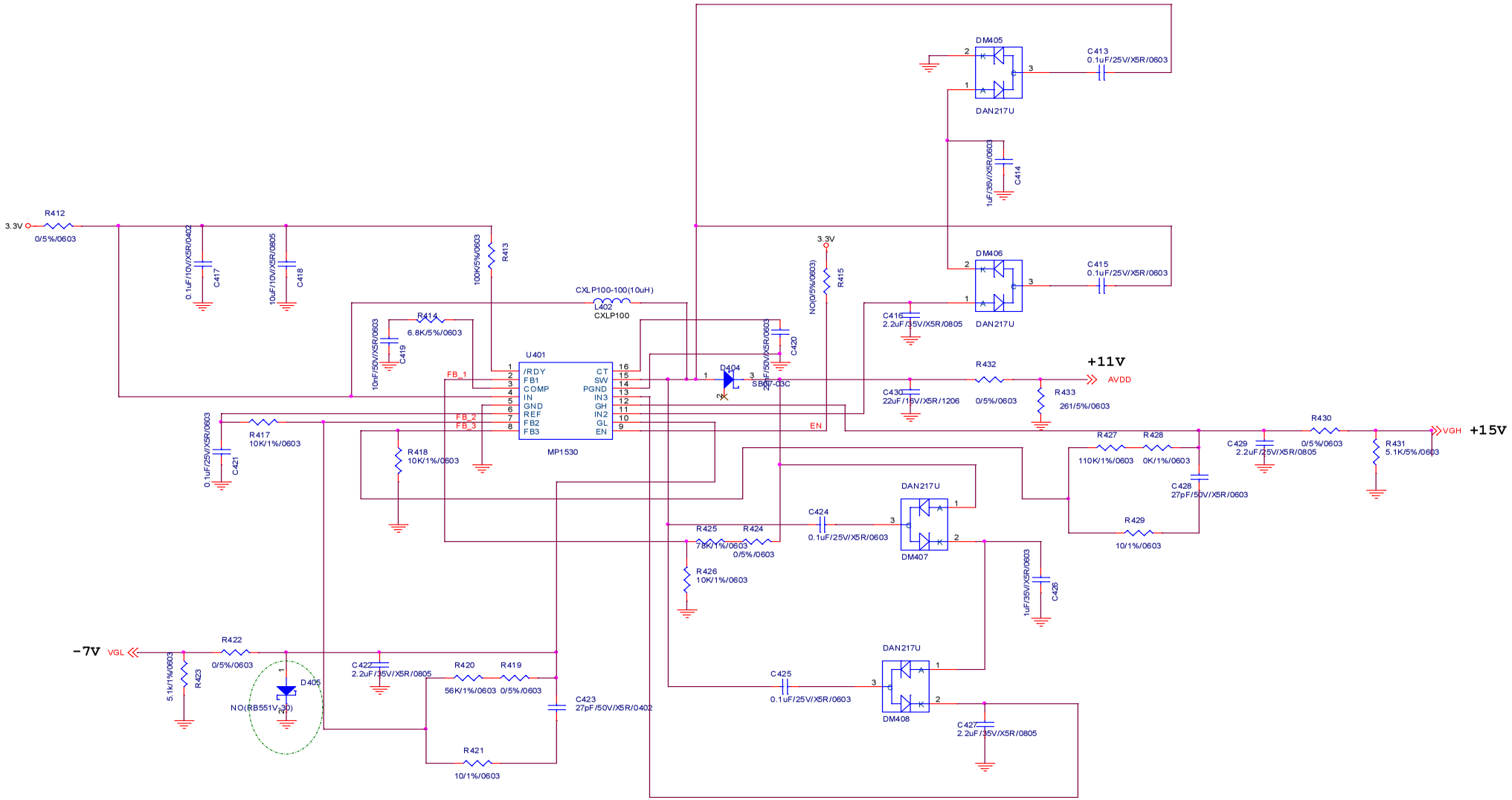
The packing carton will be attached with a carton label where packing Q’ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed. The Carton Number is apparing in the following format:



Refer to the drawing of packing format for the location and size of the carton label.

G. Application Note

Application Circuit



H. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.
22. Please use SSCG(Spread Spectrum Clock Generator) at system for EMI reduction.