Version	1.0
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Product Specification

Color TFT-LCD module

MODEL NAME: A104SN03 V0

(◆) Preliminary Specification

(.....) Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	19/Mar/2008	All	First draft.
0.1	31/Mar/2008	16	Update Outline dimension drawing
0.2	14/April/2008	6	Update Backlight driving conditions
		11	Update Optical specification
		16	Update Outline dimension drawing
0.3	15/April/2008	17	Add Suggestion- System block
0.4	17/April/2008	3	Update Pin1 I/O
		4	Update Pin38,Pin39,P59 I/O
		4	Delete Note1
		5	Update Absolute maximum ratings- Input signal voltage
		5	Update Typical operating conditions -Item
0.5	28/April/2008	5	Update Absolute maximum ratings
		5	Update TFT-LCD Typical operating conditions
		11	Update Optical specification
		14	Update Packing form
		15	Update Suggested Gamma Voltage
0.6	5/May/2008	2	Add Total Power Consumption
		5	Update Typical operating conditions
		6	Update Lamp starting voltage
		11	Update Optical specification
0.7	16/June/2008	2	Update Weight
		3	Modify Pin Assignment(Add SPI pins)
		6	Update Backlight driving conditions/ Add note
		9~14	Add SPI timing
		15~16	Modify Power On Off Sequence
		17	Update Optical specification
		22	Modify outline drawing
0.8	14/July/2008	6	Update Backlight driving conditions

		14	Add note on Recommended Power On Register Setting
		20	Update Packing
0.9	29/July/2008	14	Update note on Recommended Power On Register
1.0	12/August/20	20	Update Packing form

A. PHYSICAL SPECIFICATIONS **2**

B. ELECTRICAL SPECIFICATIONS **3**

1.PIN ASSIGNMENT 3

a. TFT-LCD panel driving section *3*

b. Backlight driving section (Refer to Figure 1) *4*

2. ABSOLUTE MAXIMUM RATINGS 5

3. ELECTRICAL CHARACTERISTICS 5

a. TFT-LCD Typical operating conditions (AGND=GND=0V) *5*

b. Backlight driving conditions *5*

4. AC TIMING 6

5. RGB PARALLEL INPUT TIMING 7

a. Horizontal timing *7*

b. Vertical timing *8*

6. SERIAL CONTROL INTERFACE 9

7. REGISTER BANK 10

8. SERIAL REGISTER TABLE(DEFAULT VALUE) 11

9. REGISTER DESCRIPTION 11

a. Power on sequence *15*

b. Power off sequence *16*

C. OPTICAL SPECIFICATION (NOTE 1, NOTE 2) **17**

D. RELIABILITY TEST CONDITIONS (NOTE 2): **19**

E. PACKING FORM **20**

F. SUGGESTED GAMMA VOLTAGE **21**

APPENDIX: **22**

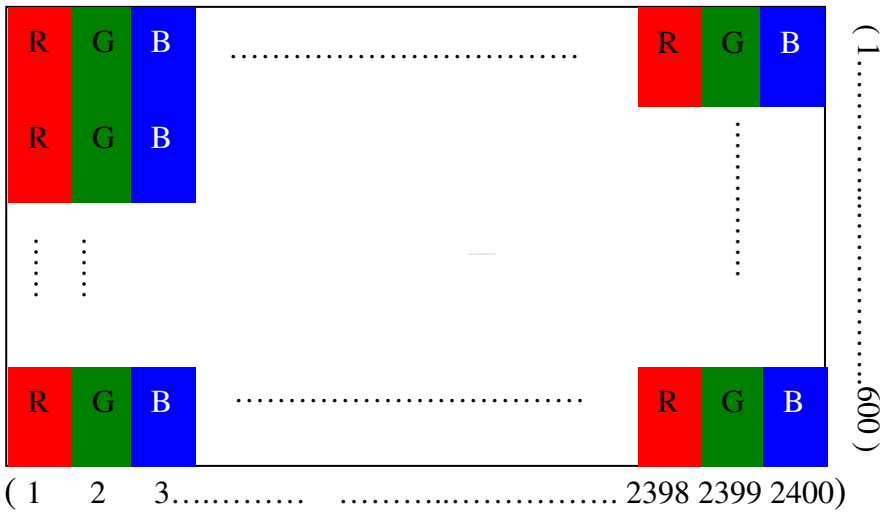
FIG.1-(A) OUTLINE DIMENSION OF TFT-LCD MODULE (FRONT SIDE) 22

G. SUGGESTION- SYSTEM BLOCK **23**

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution (dot)	800RGB(W)x600(H)	
2	Active area (mm)	211.2(W)x158.4(H)	
3	Screen size(inch)	10.4(Diagonal)	
4	Dot pitch (mm)	0.264(W)x0.264(H)	
5	Color configuration	R. G. B. stripe	Note 1
6	Overall dimension (mm)	228.4(W)x175.4(H)x6.2(D)	Note 2
7	Weight (g)	400±20	
8	Surface treatment	Anti-Glare	
9	Backlight unit	CCFL	
10	Total Power Consumption (Watt)	5.7 W Typ. (Include Logic and BLU power)	

Note 1: Below figure shows the dot stripe arrangement.



Note 2: Refer to Fig. 1

B. Electrical specifications

1.Pin assignment

a. TFT-LCD panel driving section

Pin no	Symbol	I/O	Description	Remark
1	AGND	G	Analog Ground	
2	AVDD	P	Analog Power	
3	VCC	P	Digital Power	
4	R0	I	Data input (LSB)	
5	R1	I	Data input	
6	R2	I	Data input	
7	R3	I	Data input	
8	R4	I	Data input	
9	R5	I	Data input	
10	R6	I	Data input	
11	R7	I	Data input (MSB)	
12	G0	I	Data input (LSB)	
13	G1	I	Data input	
14	G2	I	Data input	
15	G3	I	Data input	
16	G4	I	Data input	
17	G5	I	Data input	
18	G6	I	Data input	
19	G7	I	Data input (MSB)	
20	B0	I	Data input (LSB)	
21	B1	I	Data input	
22	B2	I	Data input	
23	B3	I	Data input	
24	B4	I	Data input	
25	B5	I	Data input	
26	B6	I	Data input	
27	B7	I	Data input (MSB)	
28	DCLK	I	Clock input	
29	DE	I	Data enable signal	
30	HSYNC	I	Horizontal sync input. (Negative polarity)	
31	VSYNC	I	Vertical sync input. (Negative polarity)	
32	SCL	I	Serial communication clock input	
33	SDA	I	Serial communication data input	
34	CSB	I	Serial communication chip select	
35	NC	-	For test, do not connect (Please leave it open)	

36	VCC	P	Digital Power	
37	NC	-	For test, do not connect (Please leave it open)	
38	GND	G	Digital ground	
39	AGND	G	Analog ground	
40	AVDD	P	Analog Power	
41	VCOMin	I	For external VCOM DC input	
42	DITH	I	Dithering setting DITH = "L" 6bit resolution(last 2 bits of input data turncated) DITH = "H" 8bit resolution(Default setting)	
43	NC	-	For test, do not connect (Please leave it open)	
44	VCOM	O	connect a capacitor	
45	V10	P	Gamma correction voltage reference	
46	V9	P	Gamma correction voltage reference	
47	V8	P	Gamma correction voltage reference	
48	V7	P	Gamma correction voltage reference	
49	V6	P	Gamma correction voltage reference	
50	V5	P	Gamma correction voltage reference	
51	V4	P	Gamma correction voltage reference	
52	V3	P	Gamma correction voltage reference	
53	V2	P	Gamma correction voltage reference	
54	V1	P	Gamma correction voltage reference	
55	NC	-	For test, do not connect (Please leave it open)	
56	VGH	P	Positive power for TFT	
57	VCC	P	Digital Power	
58	VGL	P	Negative power for TFT	
59	GND	G	Digital Ground	
60	NC	-	For test, do not connect (Please leave it open)	

I: Input; P: Power; G: Ground; C: Capacitor

b. Backlight driving section (Refer to Figure 1)

No.	Symbol	I/O	Description	Remark
1	HI	I	Power supply for backlight unit (High voltage)	--
2	GND	-	Ground for backlight unit	--

2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VCC	GND=0	-0.5	5	V	
	AVDD	AGND=0	-0.5	15	V	
	VGH	GND=0	-0.3	42	V	
	VGL		-20	0.3	V	
	$V_{GH}-V_{GL}$		-	40	V	
Input signal voltage	V_I		-0.3	V_{CC}+0.3	V	Note 1
	VCOMin		0	5	V	
Operating temperature	Topa		-10	60	□	
Storage temperature	Tstg		-20	70	□	

Note 1: HS , VS , DE , Digital Data

3. Electrical characteristics

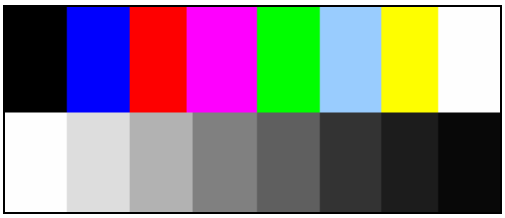
a. TFT-LCD Typical operating conditions (AGND=GND=0V)

ITEM		Symbol	MIN.	TYP.	MAX.	UNIT	Remark
Power supply		VCC	3.0	3.3	3.6	V	Note3
		I_{VCC}	--	10	20	mA	Pin3 + Pin36+Pin57
		AVDD	10.5	11	11.5	V	Note3
		I_{AVDD}	--	24	30	mA	Pin2 + Pin40
		VGH	14	15	16	V	Note3
		I_{VGH}	--	0.4	0.6	mA	Pin56
		VGL	-7.5	-7	-6.5	V	Note3
		I_{VGL}	-0.6	-0.4	--	mA	Pin58
Input Signal voltage	H Level	V_{IH}	$0.7V_{CC}$	-	V_{CC}	V	
	L Level	V_{IL}	GND	-	$0.3V_{CC}$	V	
Input Reference Voltage		V1 ~ V5	AVDD/2	-	AVDD – 1	V	
		V6 ~ V10	1	-	AVDD/2	V	
VCOMin		V_{CDC}	3.75	3.95	4.15	V	Note 1

Note1: Above every operation range is based on stable operation from suggested application circuit.

Note2: Based on recommended Gamma 2.2 voltage.

Note3: Typical current test pattern



b. Backlight driving conditions

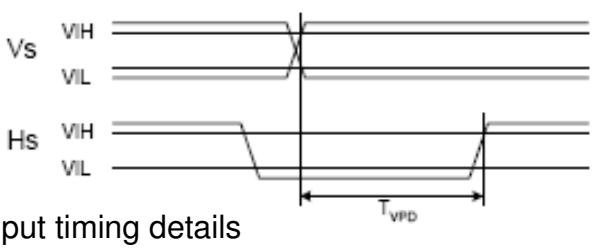
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	--	--	--	Vrms	-

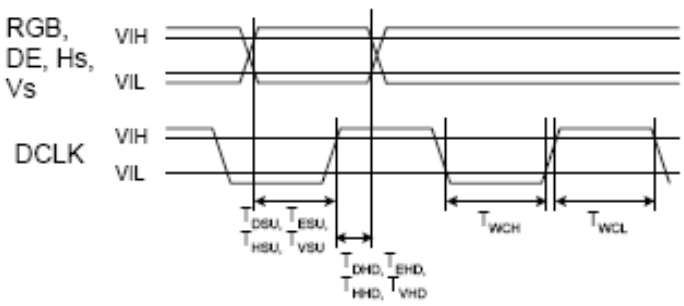
	V_L	709	788	867	Vrms	At 6.5 mA, Note 7
	V_L	--	--	--	Vrms	-
Lamp current	I_L	5.5	6.5	7.5	mArms	Note 8
Frequency	F_L	45	--	80	kHz	Note 3
Lamp starting voltage	V_S	1200	--	--	Vrms	Note 1,4,6
		1630	--	--	Vrms	Note 2,4,6
Lamp life time		10,000	--	--	Hr	Note 5

Note 1: Ta = 25℃.
Note 2: Ta = 0℃.
Note 3: The lamp frequency should be selected as different as possible from display horizontal synchronous signal to avoid interference.
Note 4: The "MIN" of "Starting voltage" means the minimum voltage to light normally in the LCD module, and the start up voltage should be kept at least 1 second.
Note 5: The" Lamp life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃, I_L=6.5mA.
Note 6: Lamp starting voltage means you must provide voltage exceeds the value list on the table!
Note 7: Measure Machine：NF[As-114B]. Measure Mode：C.C. Measure Condition： Frequency：46KHz, Capacity：15pF
Note 8: Inverter type：KODA，Capacity：15pF，Frequency：46KHz
Note 9: In order to prevent the noise or electrical static to disturb display signal, please make sure system ground to touch metal frame well.

4. AC Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Clock High time	T_{WCL}	8	-	-	ns	
Clock Low time	T_{WCH}	8	-	-	ns	
Hsync setup time	T_{HSU}	5	-	-	ns	
Hsync hold time	T_{HHD}	10	-	-	ns	
Vsync setup time	T_{VSU}	0	-	-	ns	
Vsync hold time	T_{VHD}	2	-	-	ns	
Data setup time	T_{DSU}	5	-	-	ns	
Data hold time	T_{DHD}	10	-	-	ns	
Data enable set-up time	T_{ESU}	4	-	-	ns	
Data enable hold time	T_{EHD}	2	-	-	ns	



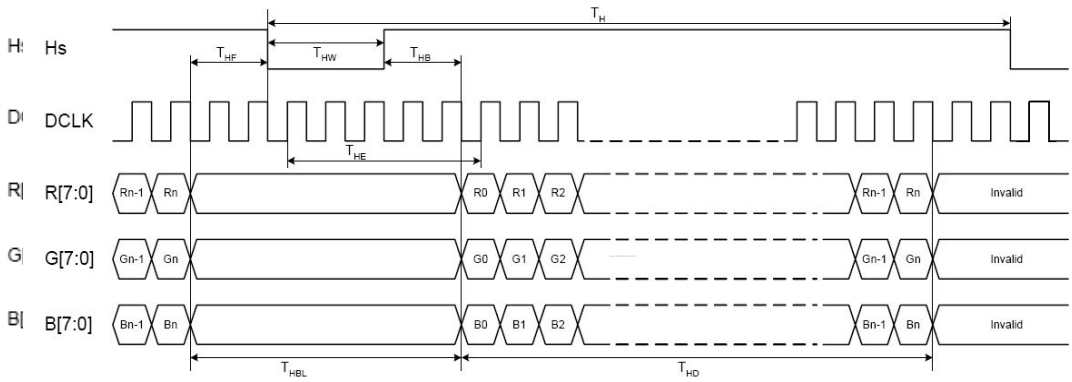


Input timing details

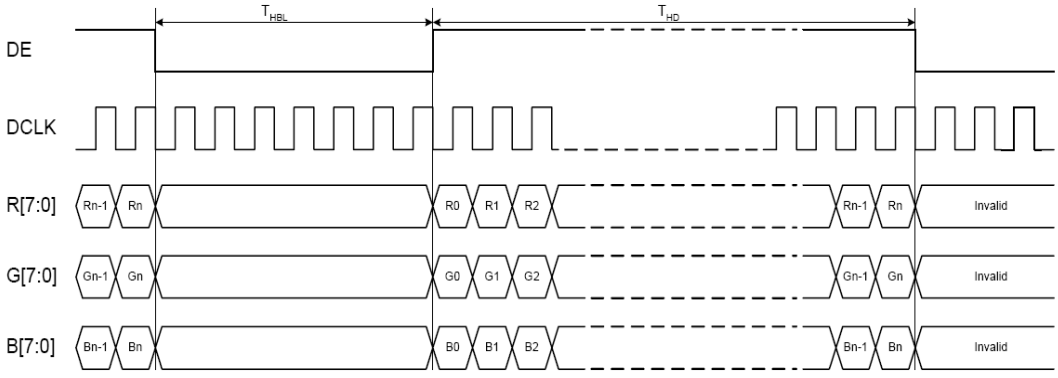
5. RGB Parallel Input Timing

a. Horizontal timing

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency	F_{DCLK}	25	40	45	MHz	
DCLK period	T_{DCLK}	22	25	40	ns	
Hsync period (= T_{HD} + T_{HBL})	T_H	1026	1056	1183	DCLK	
Active Area	T_{HD}	-	800	-	DCLK	
Horizontal blanking (= T_{HF} + T_{HE})	T_{HBL}	226	256	383	DCLK	
Hsync front porch	T_{HF}	10	40	167	DCLK	
Delay from Hsync to 1st data input (= T_{HW} + T_{HB})	T_{HE}		216		DCLK	
Hsync pulse width	T_{HW}	1	128	136	DCLK	
Hsync back porch	T_{HB}	80	88	215	DCLK	



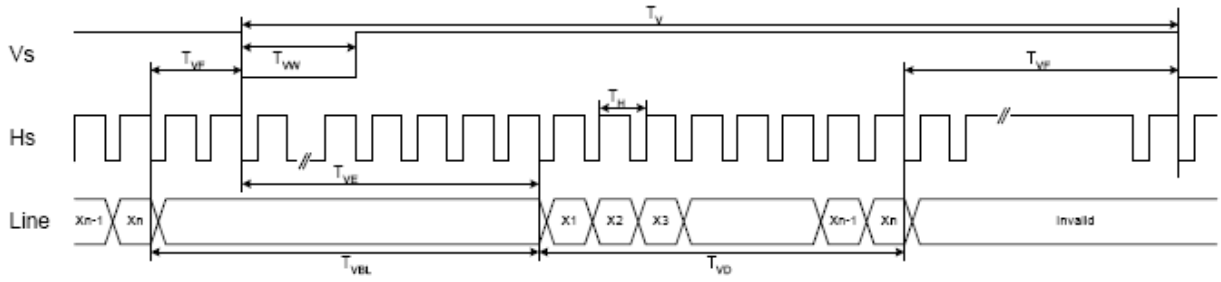
Horizontal input timing (HV mode)



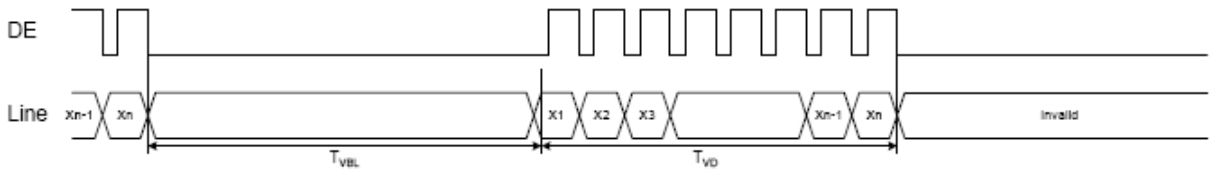
Horizontal input timing (DE mode)

b. Vertical timing

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Vsync period (= T_{VD} + T_{VBL})	T_V	-	628	635	Th	
Active lines	T_{VD}	-	600	-	Th	
Vertical blanking (= T_{VF} + T_{VE})	T_{VBL}	-	28	35	Th	
Vsync front porch	T_{VF}	-	1	8	Th	
GD start pulse delay	T_{VE}	-	27	-	Th	
Vsync pulse width	T_{VW}	1	3	16	Th	
Hsync/Vsync phase shift	T_{VPD}	2	320	-	DCLK	



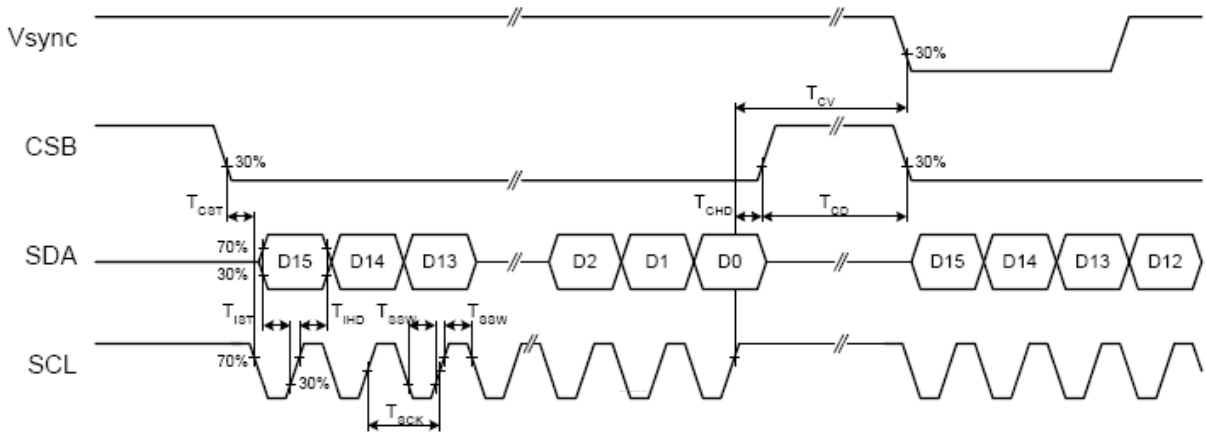
Vertical timing (HV mode)



Vertical timing (DE mode)

6. Serial Control Interface

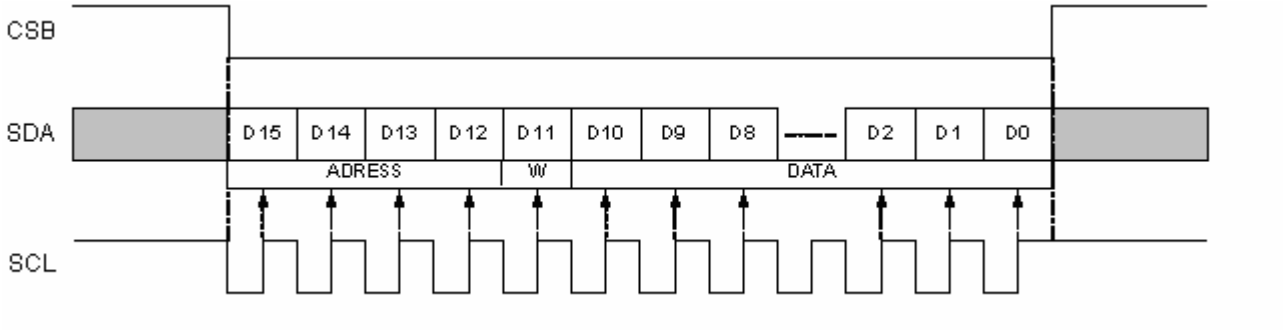
Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Serial data setup time	T_{IST}	120	-	-	ns	
Serial data hold time	T_{IHD}	120	-	-	ns	
CSB setup time	T_{CST}	120	-	-	ns	
CSB hold time	T_{CHD}	120	-	-	ns	
Serial clock high/low	T_{SSW}	120	-	-	ns	
Serial clock	T_{SCK}	320	-	-	ns	
Delay from CSB to VSYNC	T_{CV}	1	-	-	us	
Chip select distinguish	T_{CD}	1	-	-	us	
Serial data output delay	T_{ID}	-	-	60	ns	CL=20pF



AC serial interface write mode timings

7. Register Bank

There is a total of 6 registers each containing several parameters. For a detailed description of the parameters refer to register table. The serial register has read/write function. D[15:12] are the register address, D[11] defines the read or write mode and D[10:0] are the data.



Serial Interface Write sequence

1. At power-on, the default values specified for each parameter are taken.
2. If less than 16-bit data are read during the CS low time period, the data is cancelled.
   a. The write operation is cancelled.
3. All items are set at the falling edge of the vertical sync, except R0[1:0].
4. When GRB is activated through the serial interface, all registers are cleared, except the GRB value.
5. The register setting values are valid when VCC already goes to high and after VSYNC starts.
6. It is suggested that VSYNC, HSYNC, DCLK always exists in the same time. But if HSYNC, DCLK stops, only VSYNC operating, the register setting is still valid.
7. If the chip goes to standby mode, the register value will still keep. MCU can wake up the chip only by changing standby mode value from low to high.
8. The register setting values are rewritten by the influence of static electricity, a noise, etc. to unsuitable value, incorrect operating may occur. It is suggested that the SPI interface will setup as frequently as possible.

8. Serial Register table(Default Value)

Reg	ADDRESS				R/W	DATA										
No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	(01)		(01)		(1)	U/D (0)	SHL (1)	(1)	(0)	GRB (1)	STB (1)
R1	0	0	0	1	0	×	(0)	(1)	VCOM_M (01)		VCOM_LVL (2Fh)					
R2	0	0	1	0	0	×	×	×	HDL (80h)							
R3	0	0	1	1	0	×	×	(0)	(0)	(0)	(0)	(0)	VDL (1000)			
R4	0	1	0	0	0	×	×	(1)	(0)	(0)	(0)	(1)	(1111)			
R6	0	1	1	0	0	×	(0)	EnGB12 (1)	EnGB11 (1)	EnGB10 (1)	(0)	(0)	EnGB5 (1)	EnGB4 (1)	EnGB3 (1)	(0)

X: Reserved. Please set to “0”.

9. Register Description

a. R0 setting

Address	**Bit**	**Description**		**Default**
0000	[10..0]	Bits 10-9	AUO Internal Use	01
		Bits7-8	AUO Internal Use	01
		Bit6 (DITH)	Dithering function.	1
		Bit5 (U/D)	Vertical shift direction selection.	0
		Bit4 (SHL)	Horizontal shift direction selection.	1
		Bit3	AUO Internal Use.	1
		Bit2	AUO Internal Use	0
		Bit1 (GRB)	Global reset.	1
		Bit0 (STB)	Standby mode setting.	1

Bit6	DITH function
0	DITH off.
1	DITH on. **(default)**

Bit5	U/D function
0	Scan down; First line= Gn -> Gn-1 -> … -> G2 -> Last line=G0. **(default)**
1	Scan up; First line= G0 -> G2 -> … -> Gn-1 -> Last line=Gn

Bit4	SHL function
0	Shift left; First data= Y600 -> Y599 -> … -> Y2 -> Last data=Y1.
1	Shift right; First data= Y1 -> Y2 -> … -> Y599 -> Last data=Y600. **(default)**

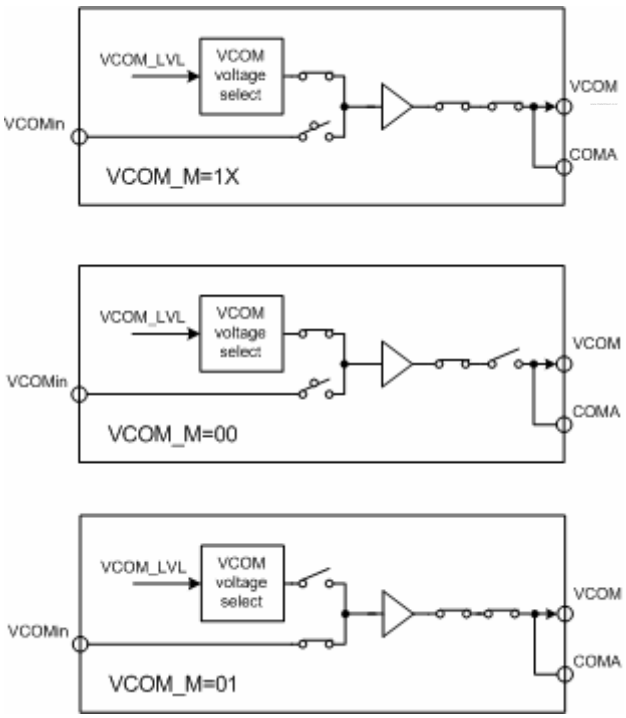
Bit1	GRB function
0	The controller is reset. Reset all registers to default value.
1	Normal operation. **(default)**

Bit0	STB function
0	T-CON, source driver and DC-DCs converters are off. All outputs are set to GND.
1	Normal operation. **(default)**

b. R1 setting

Address	**Bit**	**Description**		**Default**
0001	[8..0]	Bit9-8	AUO Internal Use	01
		Bit7-6 (VCOM_M)	VCOM mode signal.	01
		Bit5-0 (VCOM_LVL)	VCOM level adjustment. Step 31.25mV/LSB @AVDD=12.5V (AVDD/400)	2FH

Bit7-6	VCOM_M function
00	VCOM generator disabled. VCOM is generated externally.
01	VOM internal reference disabled. DC voltage of VCOM follows VCOMin signal. **(default)**
1x	VCOM generator enabled. DC voltage of VCOM follows VCOM_LVL settings.



Bit5-0	VCOM_LVL function @V1=12.5V
00h	VCOM_LVL = V1/2-47*31/25mV = 4.78125V
01h	VCOM_LVL = V1/2-46*31/25mV = 4.8125V
2Fh	VCOM_LVL = V1/2 = 6.25 **(default)**
3Eh	VCOM_LVL = V1/2+15*31.25mV = 6.71875V
3Fh	VCOM_LVL = V1/2+16*31.25mV = 6.75V

c. R2 setting

Address	Bit	Description		Default
0010	[7..0]	Bit7-0(HDL)	Horizontal start pulse adjustment function	80H

Bit7-0	HDL function
00h	$T_{HE} = T_{HEtyp}$ - 128 CLK period.
80h	$T_{HE} = T_{HEtyp}$. **(default)**
FFh	$T_{HE} = T_{HEtyp}$ + 127 CLK period.

d. R3 setting

Address	Bit	Description		Default
0011	[8..0]	Bit8	AUO Internal Use	0
		Bit7	AUO Internal Use	0
		Bit6	AUO Internal Use	0
		Bit5	AUO Internal Use	0
		Bit4	AUO Internal Use	0
		Bit3-0(VDL)	Vertical start pulse adjustment function	1000

Bit3-0	VDL function
0000	$T_{VE} = T_{VEtyp}$ – 8 Hs period.
0001	$T_{VE} = T_{VEtyp}$ – 7 Hs period.
0010	$T_{VE} = T_{VEtyp}$ – 6 Hs period.
0011	$T_{VE} = T_{VEtyp}$ – 5 Hs period.
0100	$T_{VE} = T_{VEtyp}$ – 4 Hs period.
0101	$T_{VE} = T_{VEtyp}$ – 3 Hs period.
0110	$T_{VE} = T_{VEtyp}$ – 2 Hs period.
0111	$T_{VE} = T_{VEtyp}$ – 1 Hs period.
1000	$T_{VE} = T_{VEtyp.}$ (default)
1001	$T_{VE} = T_{VEtyp}$ – 1 Hs period.
1010	$T_{VE} = T_{VEtyp}$ – 2 Hs period.
1011	$T_{VE} = T_{VEtyp}$ – 3 Hs period.
1100	$T_{VE} = T_{VEtyp}$ – 4 Hs period.
1101	$T_{VE} = T_{VEtyp}$ – 5 Hs period.
1110	$T_{VE} = T_{VEtyp}$ – 6 Hs period.
1111	$T_{VE} = T_{VEtyp}$ – 7 Hs period.

e. R6 setting

Address	Bit	Description		Default
0110	[9..0]	Bits9	AUO Internal Use	0
		Bits8(EnGB12)	Gamma buffer Enable for V9	1
		Bits7(EnGB11)	Gamma buffer Enable for V8	1

		Bits6(EnGB10)	Gamma buffer Enable for V7	1
		Bits5	AUO Internal Use	0
		Bits4	AUO Internal Use	0
		Bits3(EnGB5)	Gamma buffer Enable for V4	1
		Bits2(EnGB4)	Gamma buffer Enable for V3	1
		Bits1(EnGB3)	Gamma buffer Enable for V2	1
		Bits0	AUO Internal Use	0

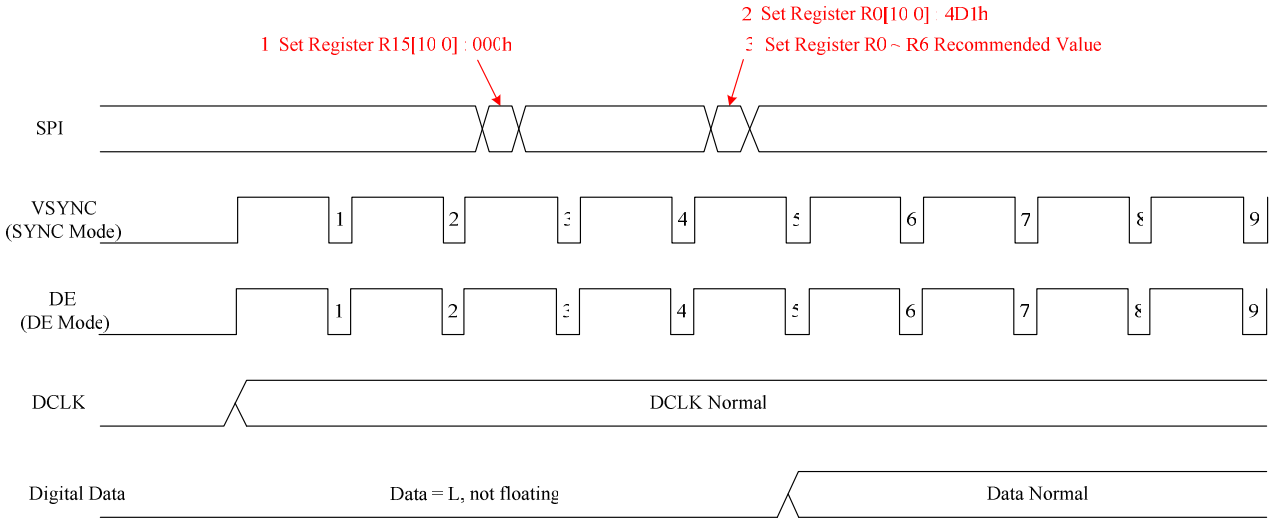
Bitx	EnGBx function
0	Gamma buffer for VX is disabled (High Z).
1	Gamma buffer is enabled. VX must be connected externally.

Recommended Power On Register Setting

Reg No.	ADDRESS				R/W	DATA										
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	10		01		1	0	1	0	0	1	1
R1	0	0	0	1	0	0	01		01		2Fh					
R2	0	0	1	0	0	0	0	0	80h							
R3	0	0	1	1	0	0	0	0	0	0	0	0	1000			
R4	0	1	0	0	0	0	0	1	1	00		1	1111			
R6	0	1	1	0	0	0	0	1	1	1	0	0	1	1	1	0

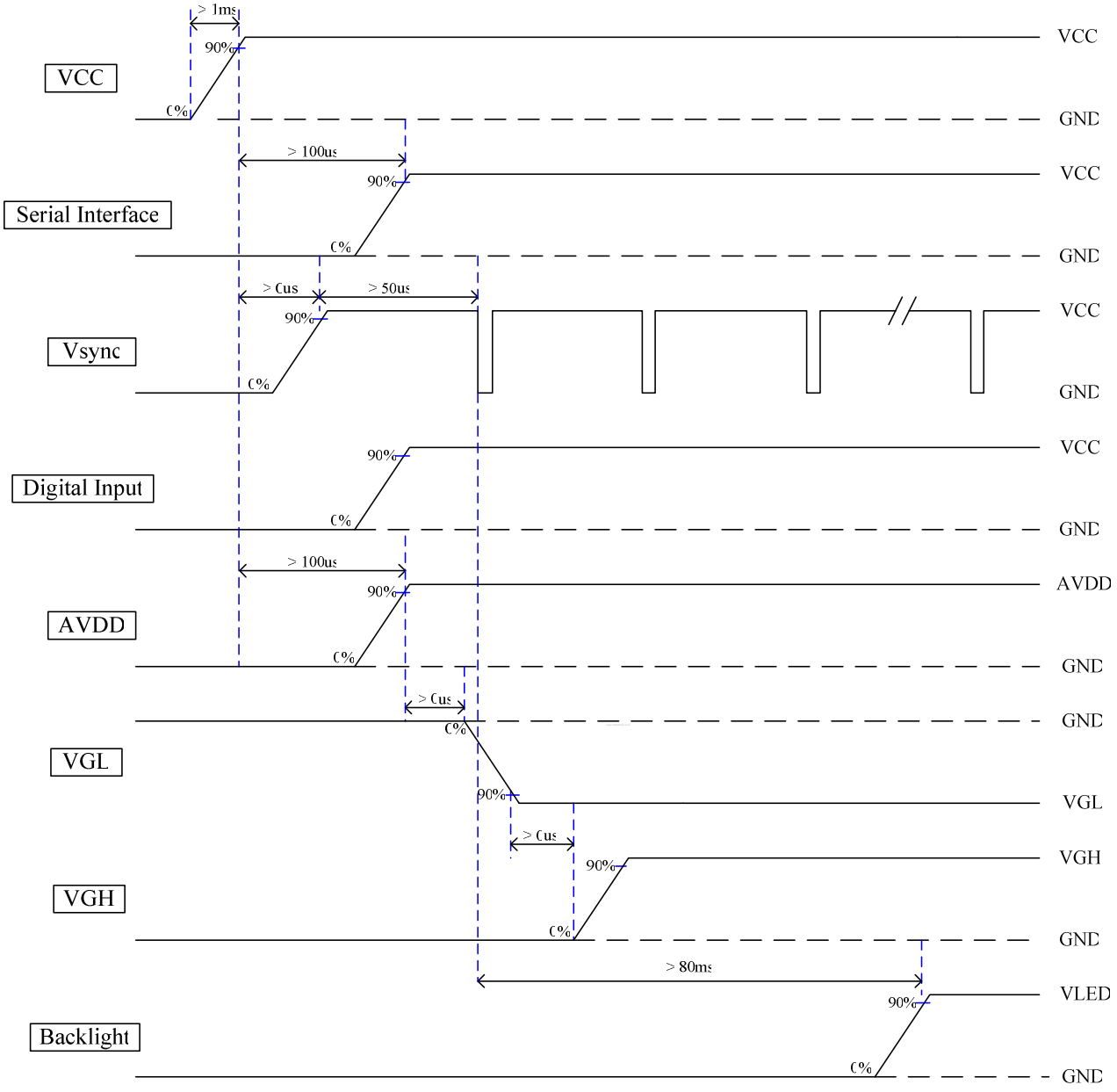
Note : Start to provide SPI commend at least after 2 frame.

1. Send R15 : 000h(Normal register bank) at first.
2. Wait at least after more than one frame, send R0 : 4D1h(Global Reset)
3. After send Global Reset, start to send R0 to R6 recommend register value.

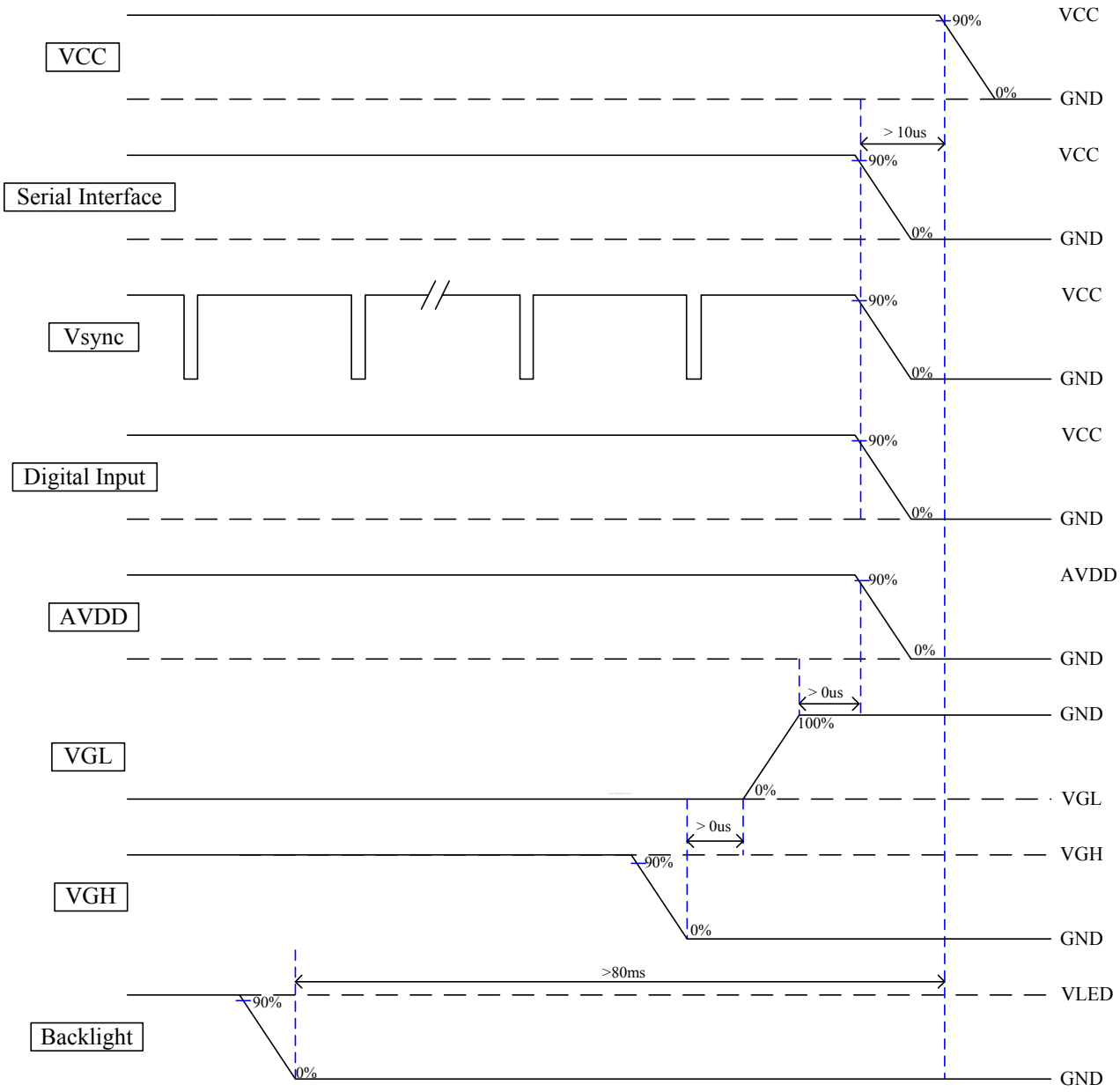


10. Power Sequence

a. Power on sequence



b. Power off sequence



C. Optical specification (Note 1, Note 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise Fall	Tr Tf	θ=0°	- -	12 18	24 36	ms ms	Note 3,5
Contrast ratio		CR	At optimized Viewing angle	300	500	-		Note 4, 5
Viewing angle	Top Bottom Left Right		CR□10	40 50 65 65	50 60 75 75	- - - -	deg.	Note 5, 6
Brightness		Y_L	V_L = 12V	220	250	-	cd/m^2	Note 7
White chromaticity		X	θ=0°	0.26	0.31	0.36		Note 7
		y	θ=0°	0.28	0.33	0.38		
Red chromaticity		X	θ=0°	0.574	0.609	0.644		
		y	θ=0°	0.312	0.347	0.382		
Green chromaticity		X	θ=0°	0.270	0.305	0.340		
		y	θ=0°	0.525	0.560	0.595		
Blue chromaticity		X	θ=0°	0.106	0.141	0.176		
		y	θ=0°	0.068	0.103	0.138		

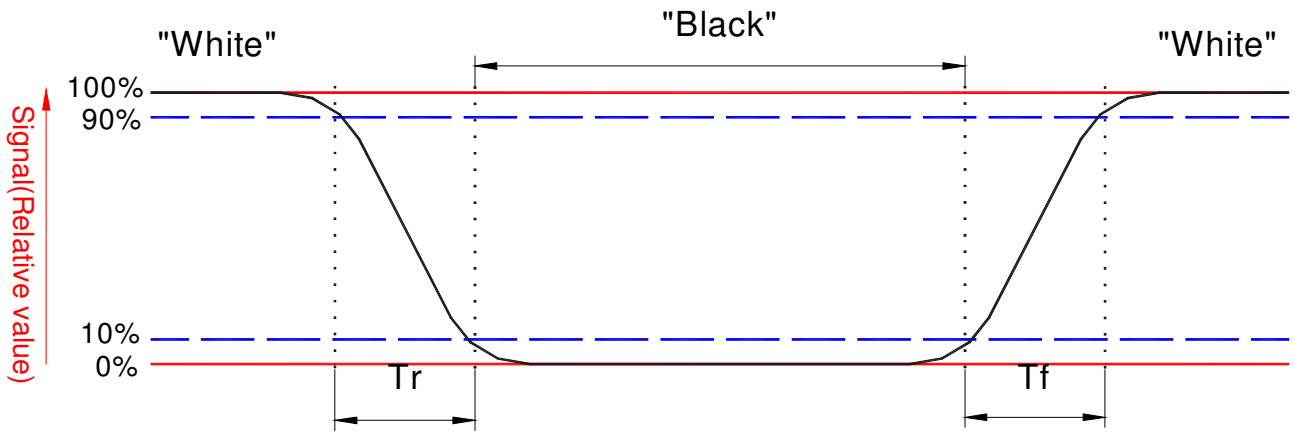
Note 1 : Ambient temperature =25℃, and lamp current I_L = 6.5 mArms. To be measured in the dark room. DC/AC inverter driving frequency: 58 kHz.

Note 2 :To be measured on the center area of panel with a viewing cone of 1°by Topcon luminance meter BM-5A, after 15 minutes operation.

Note 3. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 4. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 5. White $Vi=V_{i50} + 1.5V$

Black $Vi=V_{i50} \pm 2.0V$

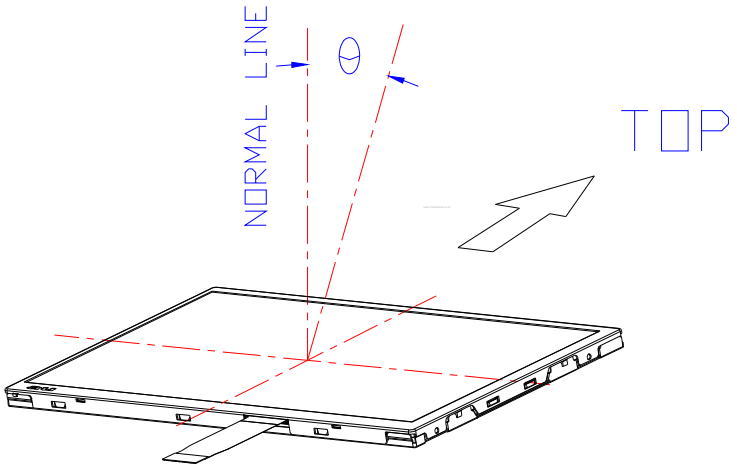
“±” means that the analog input signal swings in phase with V_{COM} signal.

“$\overline{+}$” means that the analog input signal swings out of phase with V_{COM} signal.

V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6. Definition of viewing angle, Refer to figure as below.



Note 7. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

D. Reliability test conditions (Note 2):

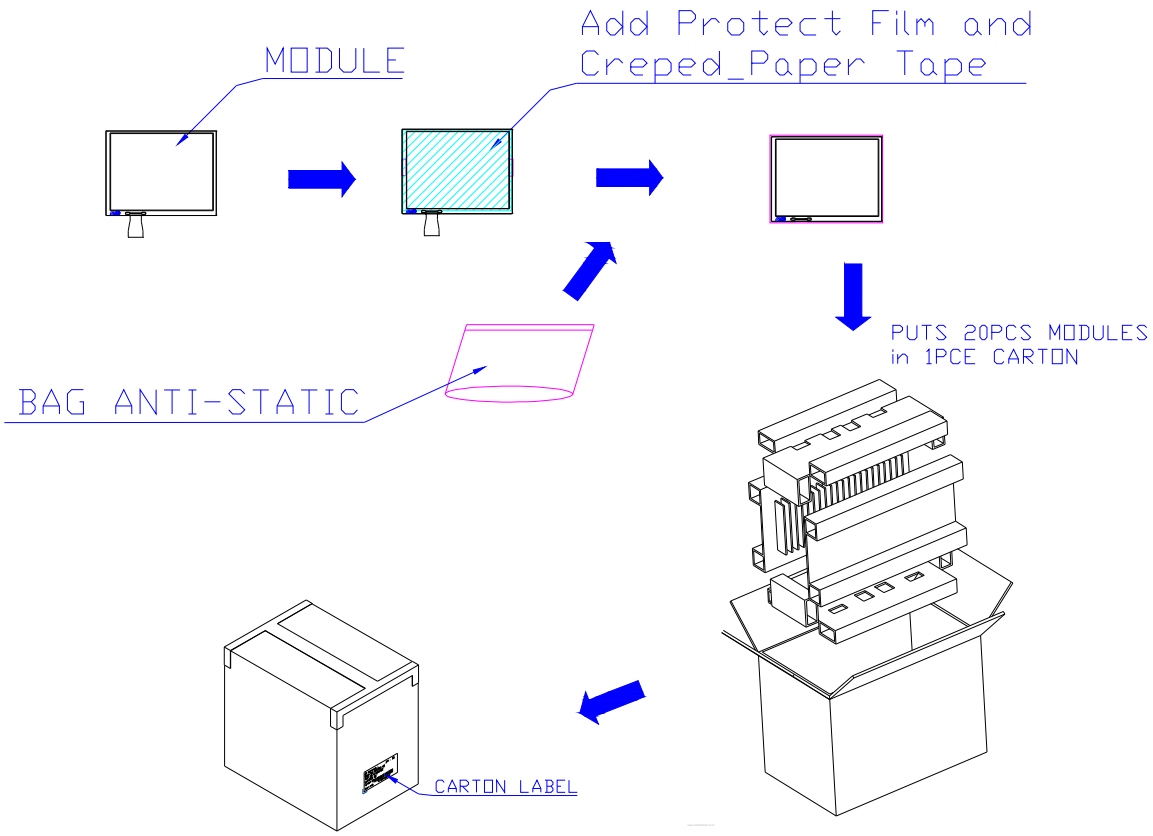
No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 70□ 240Hrs	
2	Low temperature storage	Ta= -20□ 240Hrs	
3	High temperature operation	Tp= 60□ 240Hrs	
4	Low temperature operation	Ta= -10□ 240Hrs	
5	High temperature and high humidity	Tp= 50□, 80% RH 240Hrs	Operation
6	Heat shock	-10□~60□/ 100 cycles 1Hrs/cycle	Non-operation
7	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10 ~ 55 ~ 10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	JIS C7021, A-10 Condition A
8	Mechanical shock	100G, 6ms, ±X,±Y,±Z 3 times for each direction	JIS C7021, A-7 Condition C
9	Vibration (with carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	JIS Z0202

Note1: Ta: Ambient temperature.

Note2: Tp: Panel Surface Temperature

Note3: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

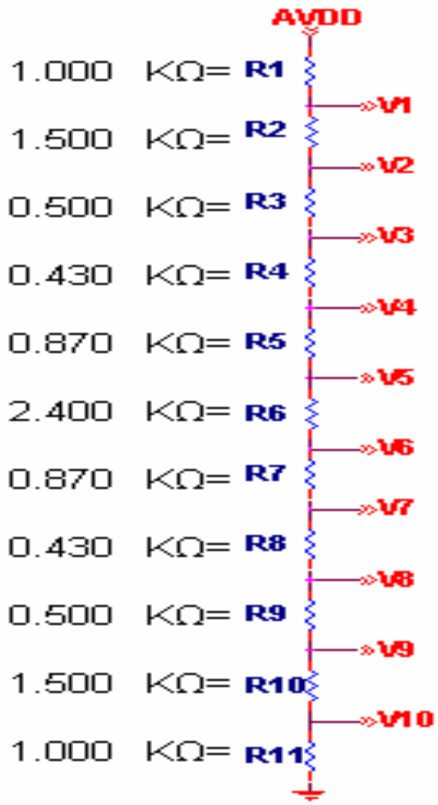
E. Packing form



MAX. CAPACITY: 20MODULES
MAX. WEIGHT: 11 kg
CARTON Dim.:483(L)mm*296(W)mm*355(H)mm

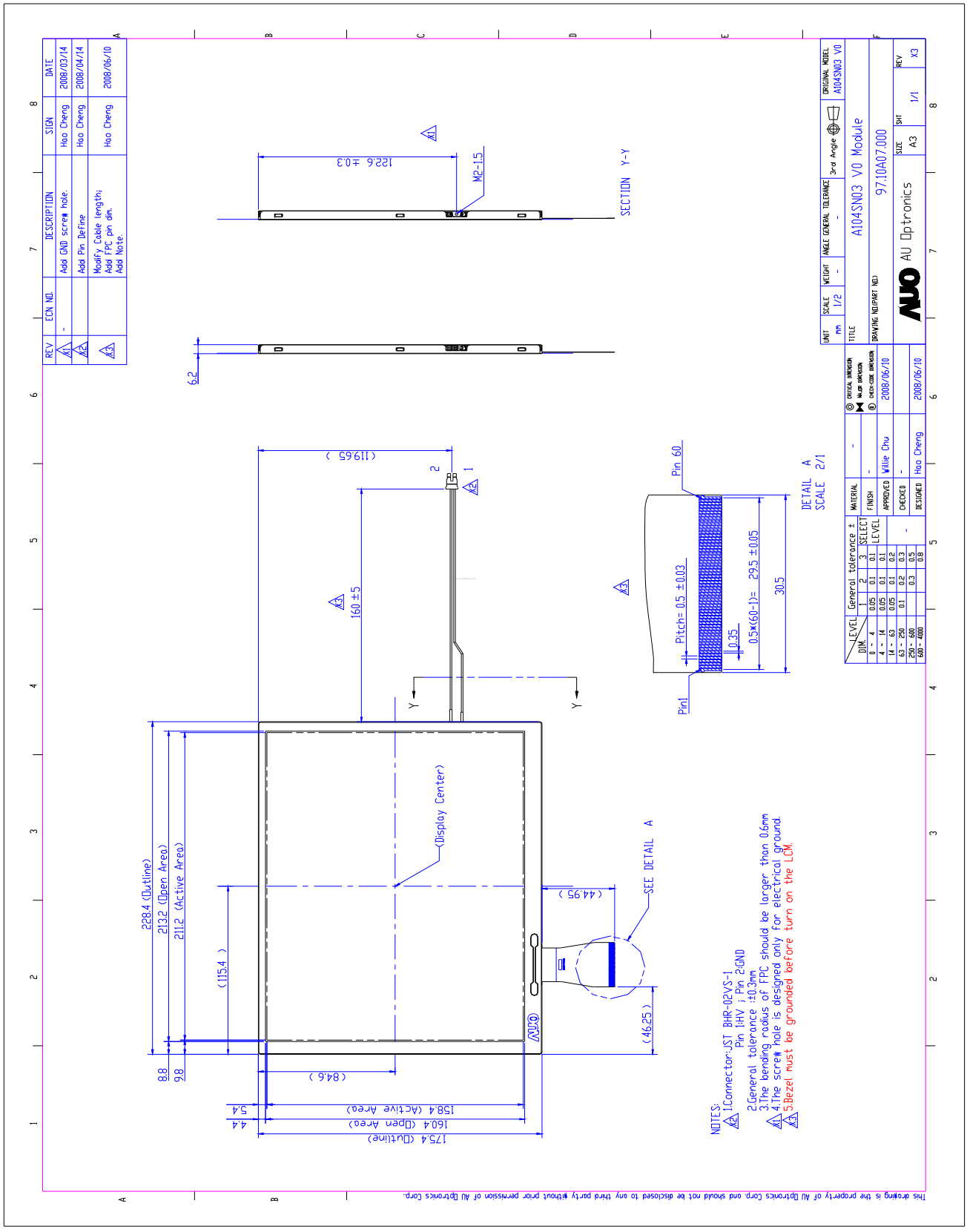
F. Suggested Gamma Voltage

	Test condition	
	AVDD	11
	V1	10
	V2	8.5
	V3	8
	V4	7.57
	V5	6.7
	V6	4.3
	V7	3.43
	V8	3
	V9	2.5
	V10	1

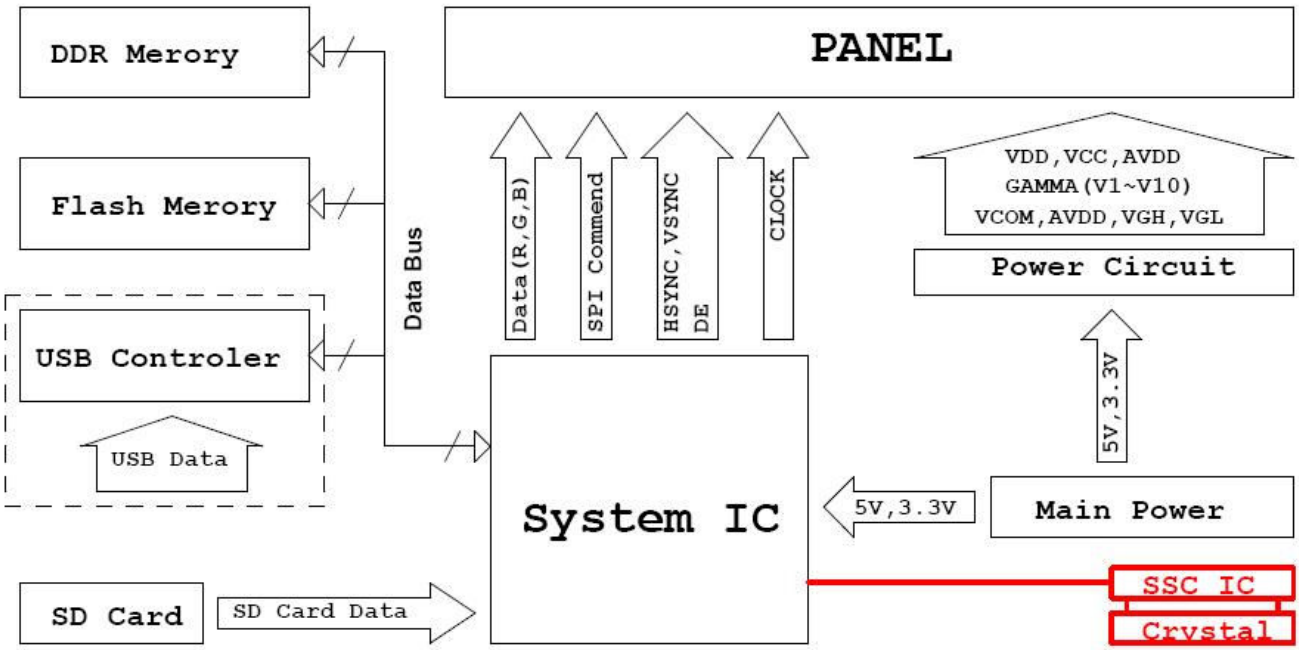


Appendix:

Fig.1-(a) Outline dimension of TFT-LCD module (Front side)



G. Suggestion- System block



According to there are some risks of EMI issue.
Please refer to this function block before design.
If add SSC (Spread Spectrum Clocking) IC on the clock of system may cause USB abnormal work. Please add USB controller to control USB data.