CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**A090VW01 V3**
CUSTOMER APPROVED	Title : Name :

☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.____)**

☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.____)**

☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver.____)**

☐ **CUSTOMER REMARK :**

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Product Specification

9.0" COLOR TFT-LCD MODULE

Model Name：	**A090VW01 V3**
Planned Lifetime:	From 2009/Mar To 2010/Dec
Phase-out Control:	From 2010/Jul To 2010/Dec
EOL Schedule:	2010/Jul

< □ >Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2008/09/03	All	First Draft
0.1	**2009/06/22**	**11**	**Update current consumption**
		14.15	**Add Timing diagram**
		23	**Update Reliability Test Items**
		30	**Update application circuit**

Contents

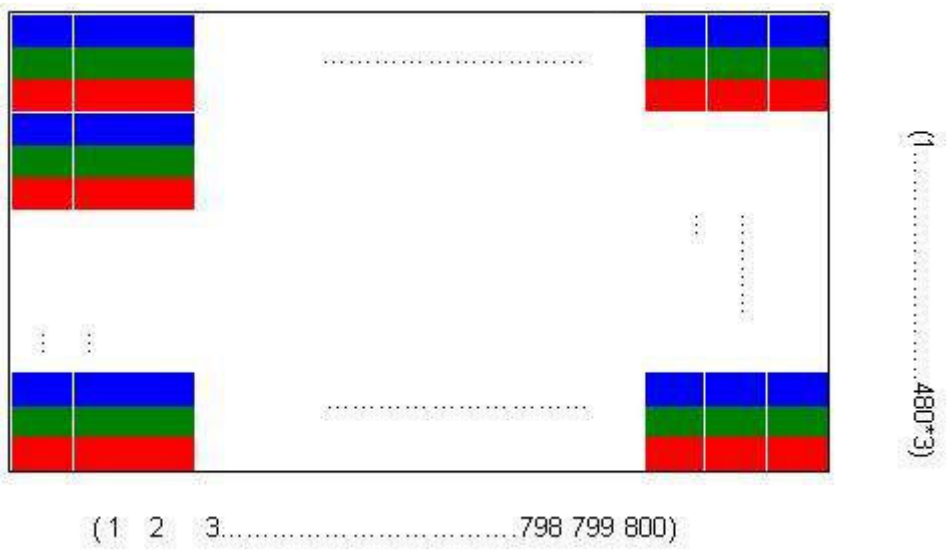
A. General Information

This product is for portable DVD and digital photo frame application.

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	9.0(Diagonal)	
2	Display Resolution	dot	800×480RGB(V)	
3	Overall Dimension	mm	211.7(H) × 125(V) × 4.6(T)	Note 1
4	Active Area	mm	199.2(H)×110.16(V)	
5	Pixel Pitch	mm	0.249(H)×0.2295(V)	
6	Color Configuration	--	R. G. B. Stripe	Note 2
7	Color Depth	--	16.7M Colors	Note 3
8	NTSC Ratio	%	48%	
9	Display Mode	--	Normally White	
10	Panel surface Treatment	--	Anti-Glare, 3H	
11	Weight	g	220	
12	LCD Module Power Consumption	W	2.1W	
13	Viewing direction		6 o'clock (gray inversion)	

Note 1: Not include backlight cable and FPC. Refer next page to get further information.

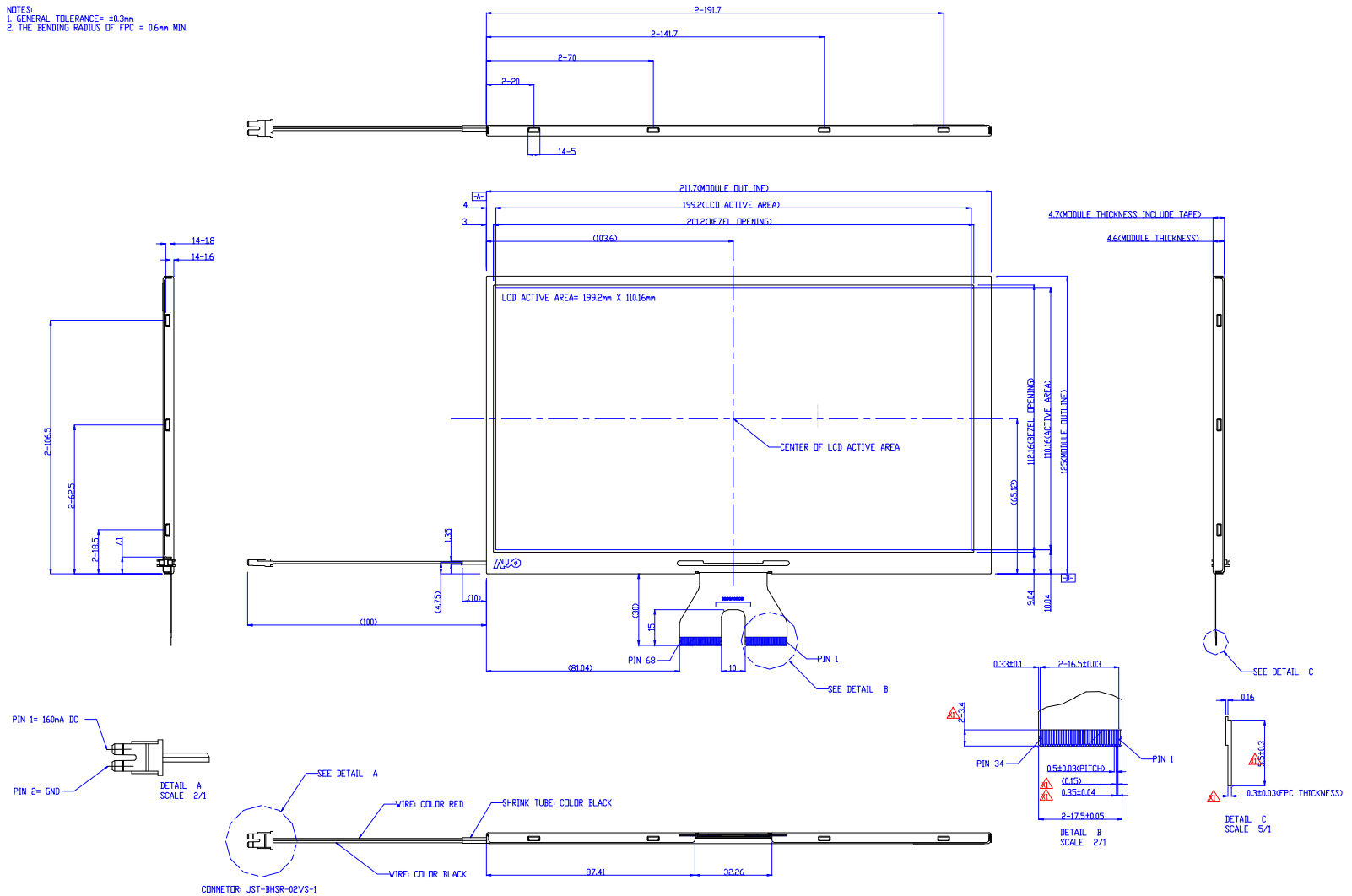
Note 2: Below figure shows dot stripe arrangement.



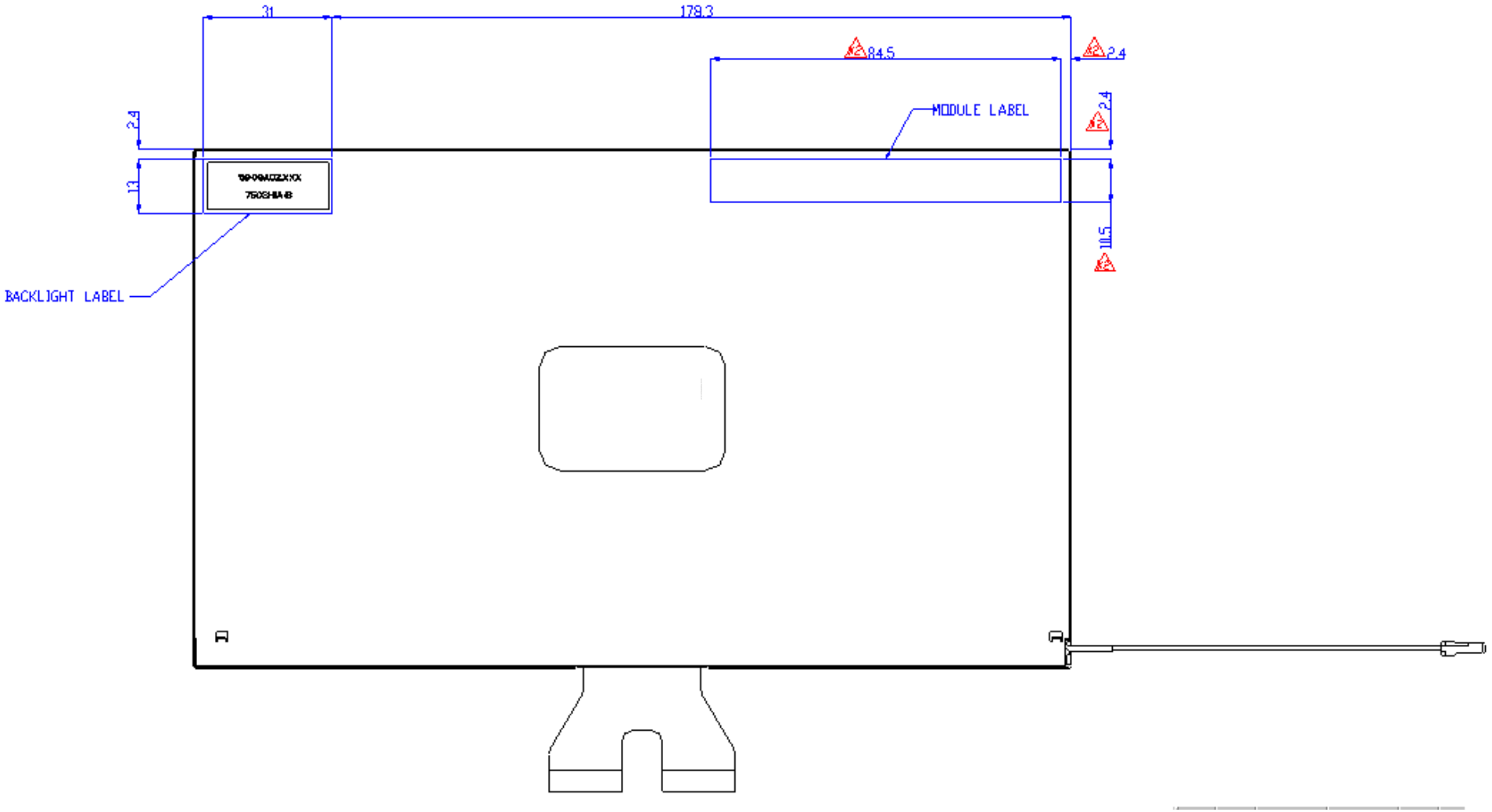
Note 3: The full color display depends on 24-bit data signal (pin 44~67).

B. Outline Dimension

1. TFT-LCD Module – Front View



2. TFT-LCD Module – Rear View



C. Electrical Specifications

1. TFT LCD Panel Pin Assignment

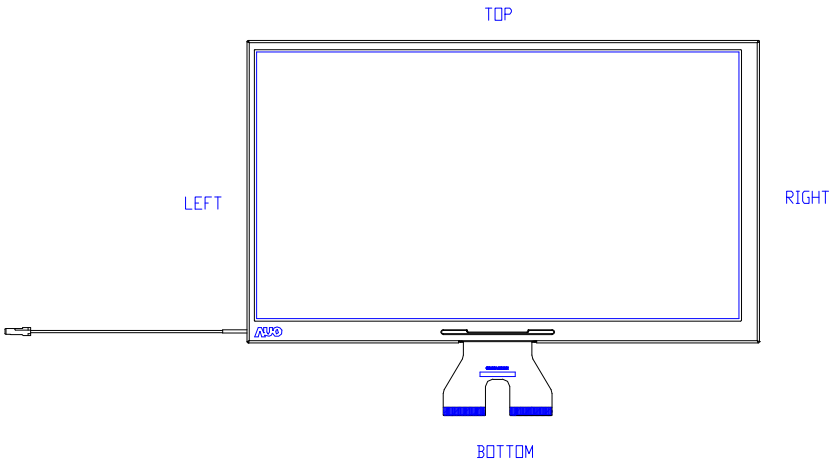
Recommended connector : JST 34FLZX-RSM1-A-TB

Pin no	Symbol	I/O	Description	Remark
1	VCOM	I	Common electrode driving voltage	
2	VGL	P	Negative power supply voltage for Gate driver	
3	VGH	P	Positive power supply voltage for Gate driver	
4	VDPA	P	Positive power supply voltage for Source driver	Note1
5	AGND	P	ground for analog circuit	
6	VDNA	P	Negative power supply voltage for Source driver	Note1
7	GND	P	Ground for digital circuit	
8	VCC	P	supply voltage for digital circuit	
9	DRV_BLU	O	LED driver dimming signal	
10	CABC_EN	I	CABC function enable When CABC_EN=”L”, CABC enabled or not is controlled by S/W register setting (default is disable.) When CABC_EN=”H”, CABC function is enable.	
11	CHUD	I	Vertical shift direction setting When CHUD =“L”, display from up to down. When CHUD =“H”, display from down to up.	
12	CHLR	I	Horizontal shift direction setting When CHLR =“L”, display from left to right. When CHLR =“H”, display from right to left.	
13	EXT_GAMMA	I	Enable external voltage correction voltage V1~V14 When EN_EXT_GAMMA=”H”, use external gamma voltage to fit gamma 2.2.	
14	GRB	I	global reset pin (active low) When GRB = “L”, The controller is reset. When GRB = “H”, Normal operation. Default setting.	
15	NAVDD	C	Pins to connect capacitance for power circuitry Power supply for negative analog circuit.	
16	V14	I	gamma reference voltage	
17	V13	I	gamma reference voltage	
18	V12	I	gamma reference voltage	
19	V11	I	gamma reference voltage	
20	V10	I	gamma reference voltage	
21	V9	I	gamma reference voltage	
22	V8	I	gamma reference voltage	
23	V7	I	gamma reference voltage	
24	V6	I	gamma reference voltage	
25	V5	I	gamma reference voltage	
26	V4	I	gamma reference voltage	

27	V3	I	gamma reference voltage	
28	V2	I	gamma reference voltage	
29	V1	I	gamma reference voltage	
30	PAVDD	C	Pins to connect capacitance for power circuitry Power supply for positive analog circuit.	
31	NVDD	C	Pins to connect capacitance for power circuitry	
32	VCC	P	supply voltage for digital circuit	
33	VDDD	C	Pins to connect capacitance for power circuitry IC internal logic power.	
34	GND	P	Ground for digital circuit	
35	CS	I	Chip select (Low active) of SPI	
36	SDA	I/O	Data input/output of SPI	
37	SCL	I	Clock input of SPI	
38	HSYNC	I	Horizontal sync input	
39	VSYNC	I	Vertical sync input	
40	GND	P	Ground for digital circuit	
41	DCLK	I	Data clock Input	
42	GND	P	Ground for digital circuit	
43	DE	I	Data enable Input (Low active)	
44	DB7	I	Blue data input	
45	DB6	I	Blue data input	
46	DB5	I	Blue data input	
47	DB4	I	Blue data input	
48	DB3	I	Blue data input	
49	DB2	I	Blue data input	
50	DB1	I	Blue data input	
51	DB0	I	Blue data input	
52	DG7	I	Green data input	
53	DG6	I	Green data input	
54	DG5	I	Green data input	
55	DG4	I	Green data input	
56	DG3	I	Green data input	
57	DG2	I	Green data input	
58	DG1	I	Green data input	
59	DG0	I	Green data input	
60	DR7	I	Red data input	
61	DR6	I	Red data input	

62	DR5	I	Red data input	
63	DR4	I	Red data input	
64	DR3	I	Red data input	
65	DR2	I	Red data input	
66	DR1	I	Red data input	
67	DR0	I	Red data input	
68	VCOM	I	Common electrode driving voltage	

I: Input pin; P: Power pin; G: Ground pin; C: capacitor pin



Note 1. Pin 4 and Pin 6 are power pins. Please refer to page 10 for the minimum and maxium value.

2. Backlight Pin Assignment

Recommended connector : JST-BHSR-02VS-1

Pin no	Symbol	I/O	Description	Remark
1	VLED	P	LED power supply	
2	GNDLED	P	LED ground	

3. Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VCC	GND=0	-0.5	5	V	Digital power
	VDPA	GND=0	-0.5	**5.8**		Postive Analog power
	VDNA	GND=0	**-5.8**	+0.5	V	Analog Negative power
	VGH - VGL	GND=0	-0.3	40	V	Gate driver supply voltage
Input signal voltage	Data	GND=0	-0.3	VCC+0.3	V	Digital Signals

Note 1: Functional operation should be restricted under ambient temperature (25℃).

Note 2: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

3. Electrical DC Characteristics

a. Typical Operation Condition (AGND =GND = 0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Voltage		VCC	3.0	3.3	3.6	V	Digital power
		VDPA	5.3	5.5	**5.7**	V	Positive analog Power
		VDNA	**-5.7**	-5.5	-5.3	V	Negative analog Power
		VGH	9	10	11	V	Positive power supply for gate driver
		VGL	-11.5	-13	-14.5	V	Negative power supply for gate driver
Output Signal Voltage	H Level	VOH	VCCx0.8	--	VCC	V	IOH=400uA, IOL=400uA
	L Level	VOL	GND	--	GNDx0.2	V	
Input Signal Voltage	H Level	VIH	0.7xVCC	--	VCC	V	
	L Level	VIL	GND	--	0.3x VCC	V	
Gamma reference voltage		VCOM1	-1.75	-1.55	-1.35	V	Detail Gamma voltage please refer to page 29.
		VCOM2	-2.7	-2.5	-2.3	V	
		V1	--	4.86	--	V	
		V2	--	4.7	--		
		V3	--	2.95	--		
		V4	--	2.43	--		
		V5	--	2.08	--		
		V6	--	1.57	--		
		V7	--	1.27	--		
		V8	--	-0.9	--		
		V9	--	-1.19	--		
		V10	--	-1.94	--		
		V11	--	-2.43	--		
		V12	--	-3.07	--		
		V13	--	-4.9	--		
		V14	--	-5.0	--		

Note 1: VCOM1 when CHUD =“L”, display from up to down.
VCOM2 when CHUD =“H”, display from down to up.

b. Current Consumption (AGND=GND=0V)

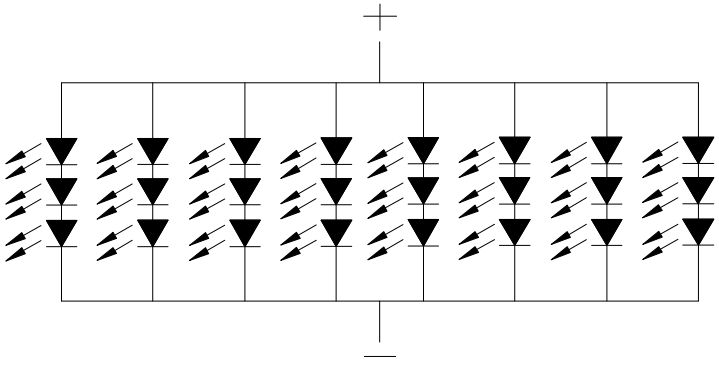
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input current for VCC	I_{VDD}	VCC=3.3V	-	3.7		mA	
Input current for VDPA	I_{VDPA}	VDPA=5.5V	-	29		mA	
Input current for VDNA	I_{VDNA}	VDNA=-5.5	-	9.2		mA	
Input current for VGH	I_{VGH}	**VGH=10V**	**-**	**0.5**	**5**	mA	
Input current for VGL	I_{VGL}	**VGL= -13V**		**0.5**	**5**	mA	
Input current for VCOM	I_{VCOM}	VCOM= -1.85V		0.55		mA	

c. Backlight Driving Conditions

The backlight (LED module, Note 1) is suggested to drive by constant current with typical value.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED light bar Current	I_L	--	200	--	mA	
BL Power Consumption	P_{BL}	--	1.92	--	W	Note 1
LED Life Time	L_L	10,000	--	--	Hr	Note 2, 3

Note 1: The LED driving condition is defined for LED module (24 LED). The voltage range will be 8.5 to 10.4V based on suggested driving current set as 200mA.



Note 2: Define “LED Lifetime”: brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25℃ and LED lightbar current = 200mA.

Note 3: If it uses larger LED lightbar voltage more than 200mA, it maybe decreases the LED lifetime.

4. Electrical AC Characteristics

a. Signal AC Characteristics

t_H: HSYNC period / t_{DCLK}: DCLK period / t_{cw}: the width of DCLK high

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INPUT Signals						
Clock High time	Tch		8	-	-	ns
Clock Low time	Tcl		8	-	-	ns
Hsync setup time	Ths		5			ns
Hsync hold time	Thh		10			ns
Data setup time	Tds		5			ns
Data hold time	Tdh		10			ns
Data enable set-up time	Tes		4			ns
SERIAL Communication						
Serial clock	Tsck		320			ns
SCL pulse duty	Tscw		40%	50%	60%	Tsck
Serial data setup time	Tist		120			ns
Serial data hold time	Tihd		120			ns
Serial clock high/low	Tssw		120			ns
CS setup time	Tcst		120			ns
CS hold time	Tchd		120			ns
Chip select distinguish	Tcd		1			us
Delay from CS to Vsync	Tcv		1			us
Serial data output delay	Tid	CL=20pF	-	-	60	ns

Figure : Input timing details

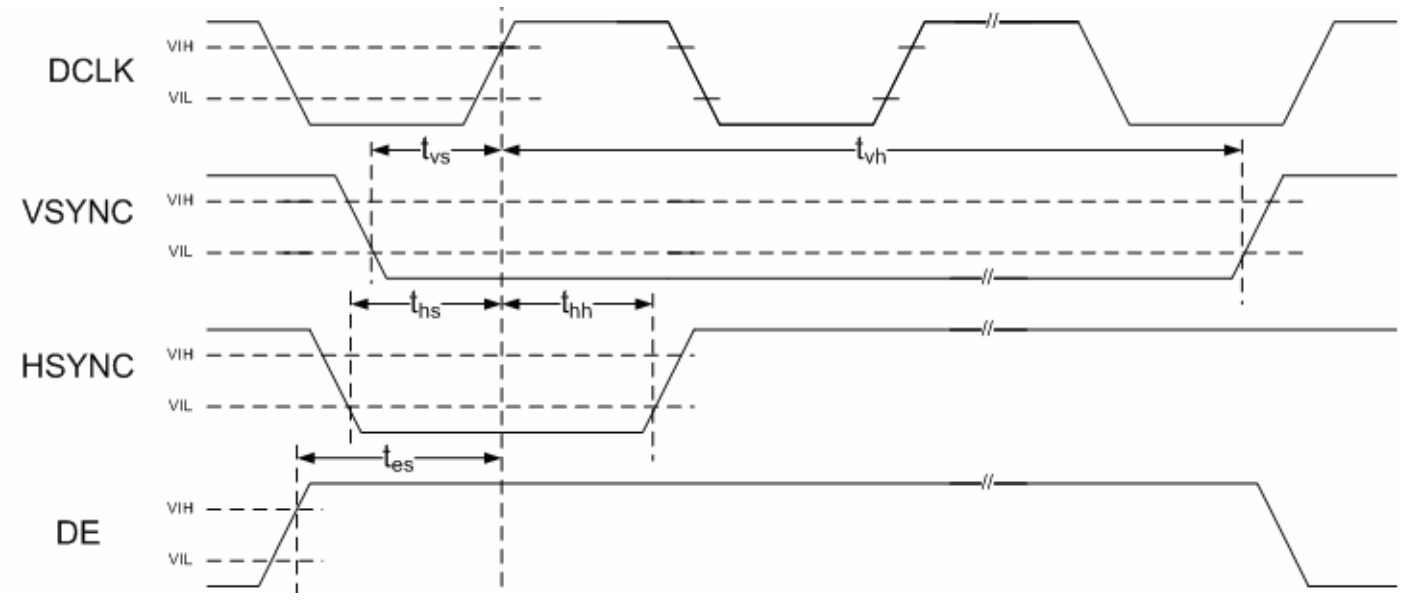


Figure : Input timing details

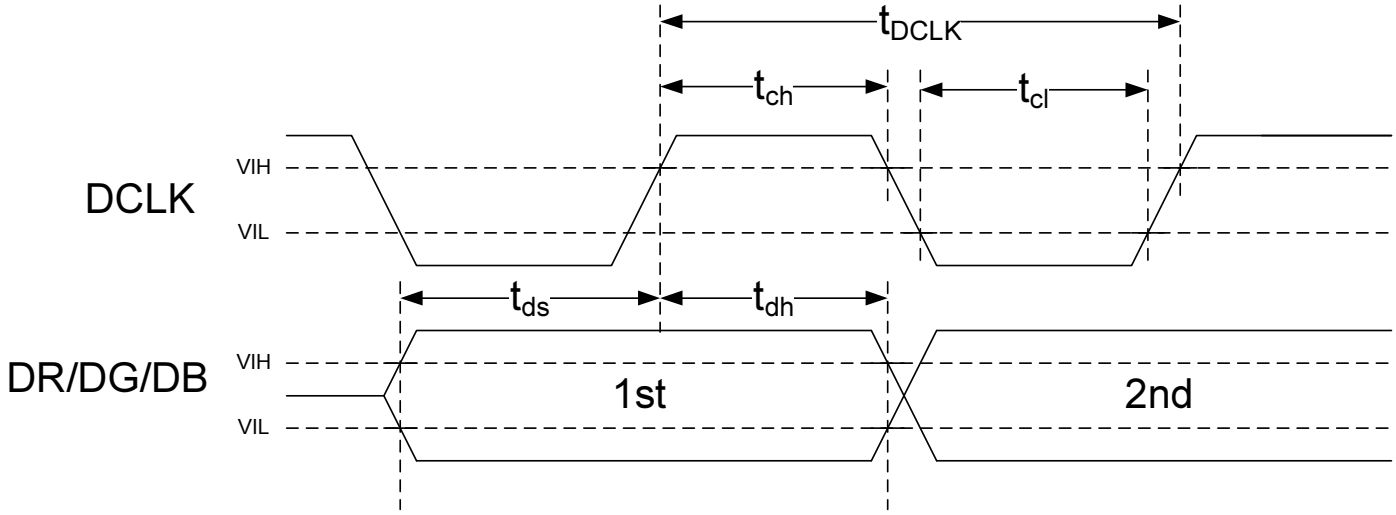


Figure : AC serial interface write mode timings

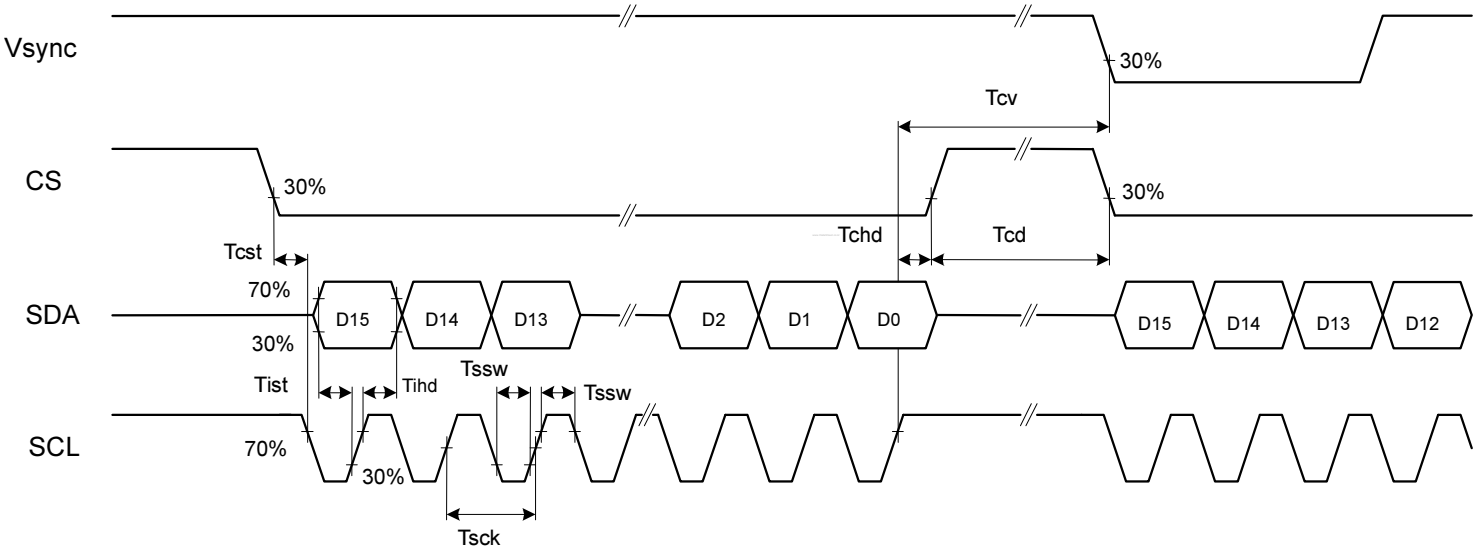
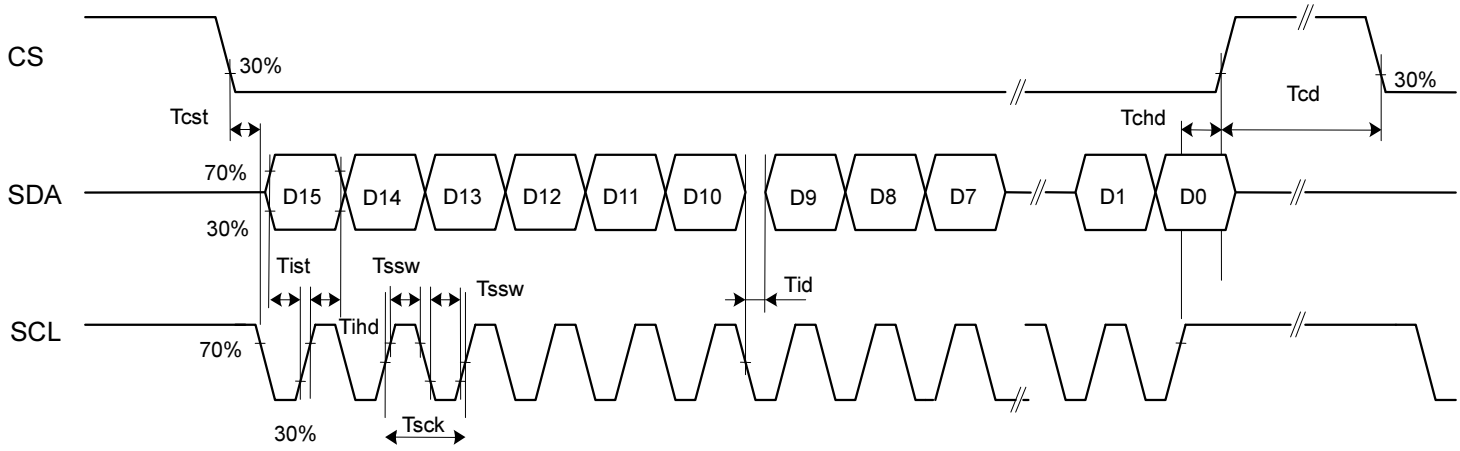


Figure : AC serial interface read mode timings



c. Input Timing Setting

DE Mode:

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCLK frequency	F_{DCLK}		30.3	33.26	37.8	MHz
Horizontal blanking (= Thf+ The)	Thbl		186	256	383	T_{DCLK}
Vertical blanking (=Tvf + Tve)	Tvbl		37	45	52	Th

HV Mode:

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCLK frequency	F_{DCLK}		30.3	33.26	37.8	MHz
DCLK period	T_{DCLK}		26.5	30.06	33.0	ns
Hsync Period (= Thd + Thbl)	Th		986	1056	1183	T_{DCLK}
Active Area	Thd		-	800	-	T_{DCLK}
Horizontal blanking (=Thf + The)	Thbl		186	256	383	T_{DCLK}
Hsync front porch	Thf			40	-	T_{DCLK}
Delay from Hsync to 1st data input (= Thw + Thb)	The	Function of HDL[7:0] settings	146	216	343	T_{DCLK}
Hsync pulse width	Thw		1	128	136	T_{DCLK}
Hsync back porch	Thb		10	88	342	T_{DCLK}
Vsync period (= Tvd + Tvbl)	Tv		517	525	532	Th
Active lines	Tvd		-	480	-	Th
Vertical blanking (=Tvf + Tve)	Tvbl		37	45	52	Th
Vsync front porch	Tvf		-	13	-	Th
GD start pulse delay	Tve	Function of VDL[3:0] settings	24	32	39	Th
Vsync pulse width	Tvw		1	3	-	Th

Figure: Vertical input timing. (HV mode)

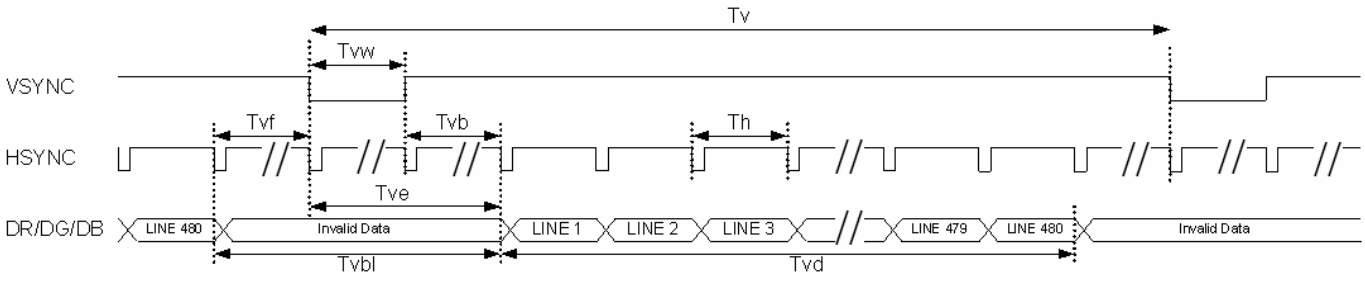


Figure: RGB parallel horizontal input timing. (HV mode)

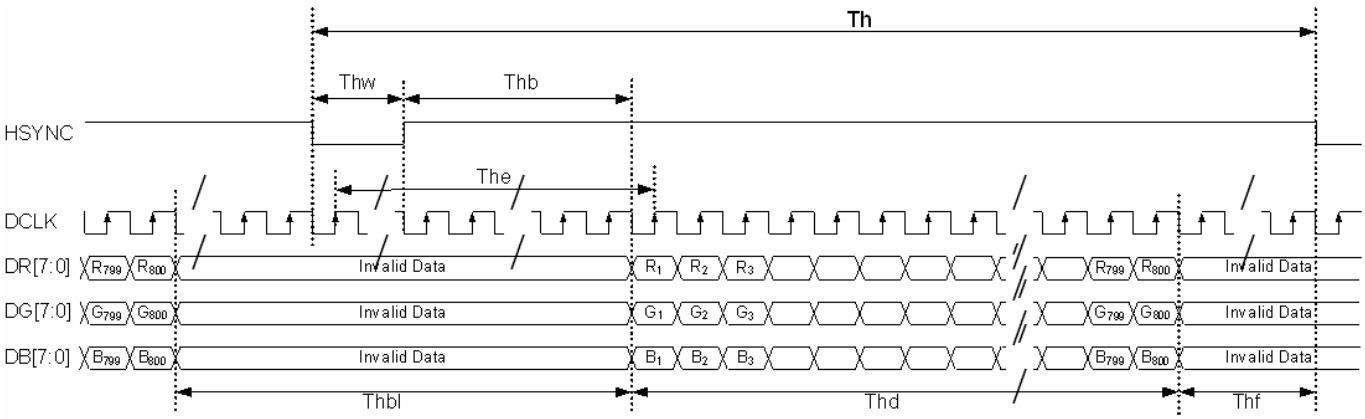


Figure : Vertical input timing. (DE mode)

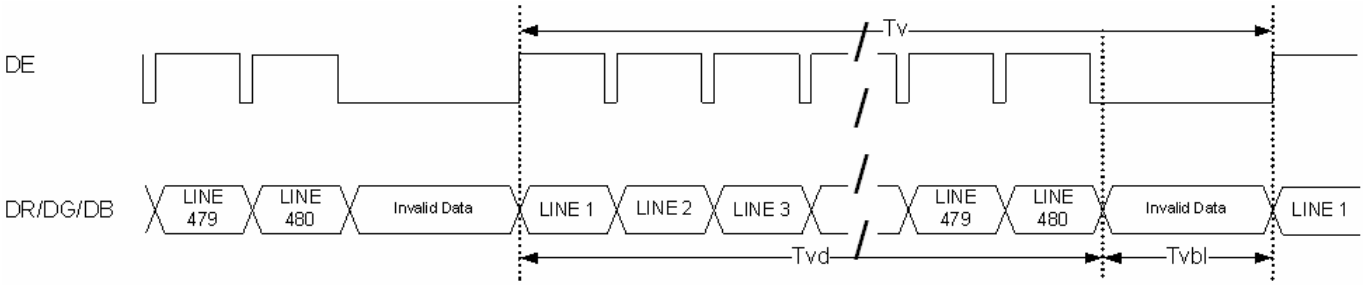
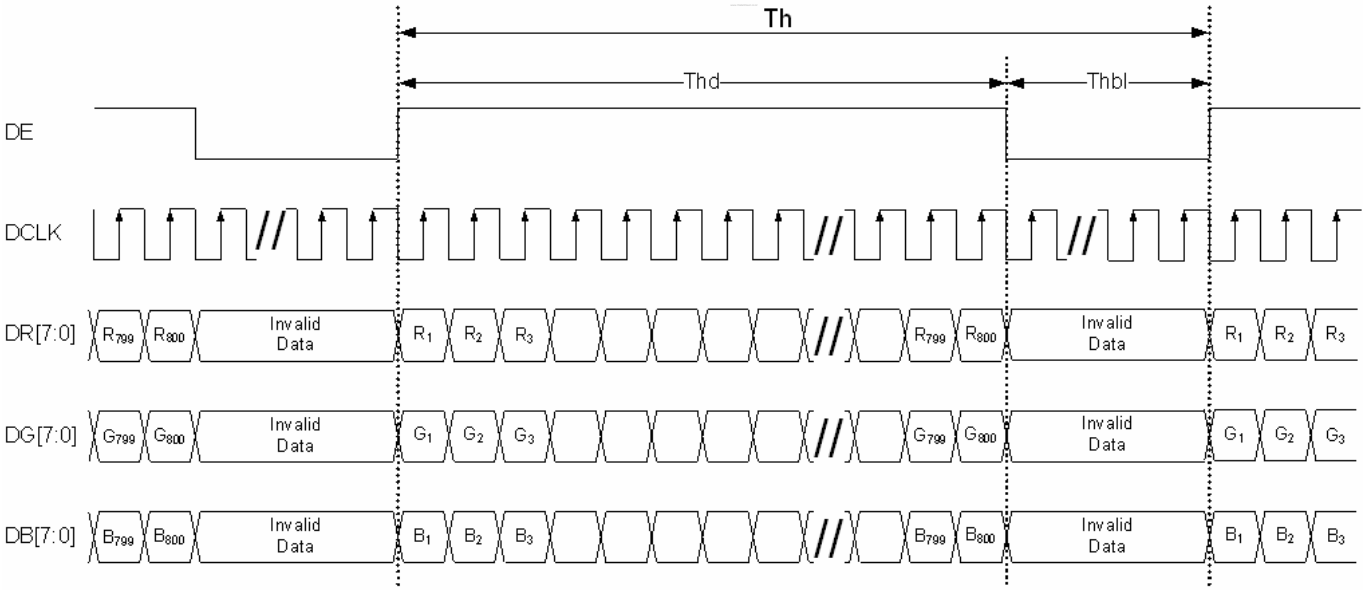


Figure : RGB parallel horizontal input timing. (DE mode)



5. Serial Interface Characteristics

a. Serial Control Interface AC Characteristic

A totally 16-bit register including 7-bit address D[15:9], 1-bit R/W bit D[8] and 8-bit data D[7:0] can be set via 3-wire serial peripheral interface. Below figure is for a detail description of the parameters.

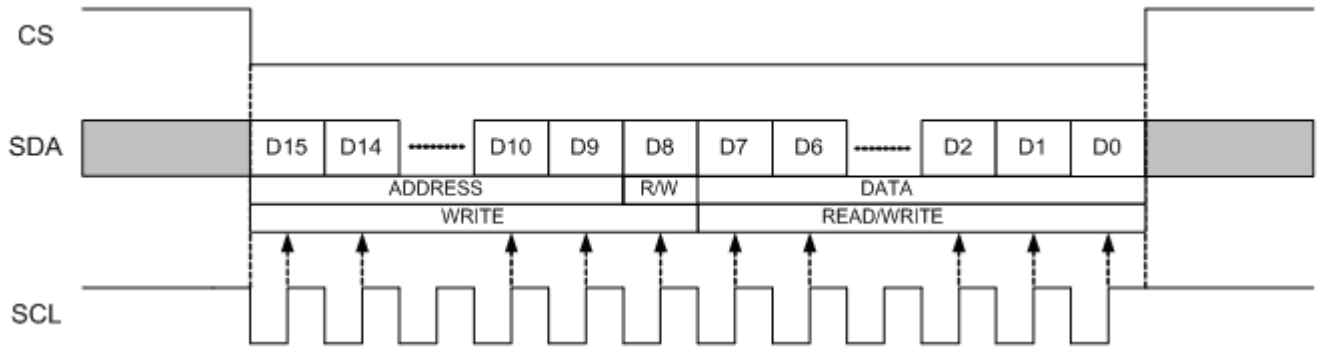


Figure: Serial interface write/read sequence

- Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.
- Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.
- The serial control block is operational after power on reset, but commands are established by the following Vsync(HV mode) or the following rising edge of the End Frame(DE mode). If command is transferred multiple times for the same register, the last command before the following Vsync(HV mode) or the following rising edge of the End Frame(DE mode) is valid, except for some special registers (ex. GRB, etc.).
- If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
  - The write operation is cancelled.
  - The read operation is interrupt.
- If 16 bits or more of SCL are input while CS is low, the first 16 bits of transferred data in the duration of CS="L" are valid data.
- Serial block operates with the SCL clock.
- Serial data can be accepted in the standby (power save) mode.
- Register R/W setting: D8 = "L" → write mode; D8 = "H" → read mode.
- It is suggested that Vsync, Hsync, DCLK(for HV mode) or DE,DCLK(for DE mode) always exists in the same time. But if Hsync, DE, DCLK stops, only Vsync operating, the register setting is still valid.

b Serial Interface Setting Table.

R0 settings

Address	Bit	Description		Default
0000000	4	NA	Not used in this model	**0**
	3	NA	Not used in this model	**0**
	2	NA	Not used in this model	**0**
	1	STB	Standby mode setting	**0**
	0	GRB	S/W global reset	**1**

Bit 1	STB
0	Normal operation. **(default)**
1	Standby mode. Register data are kept. DAC and DC/DC are off.

S/W STB	H/W STB	Operation mode
0	0	Normal operation
0	1	Standby mode
1	0	Standby mode
1	1	Standby mode

Bit 0	GRB
0	S/W global reset. Reset all registers to default value.
1	Normal operation. **(default)**

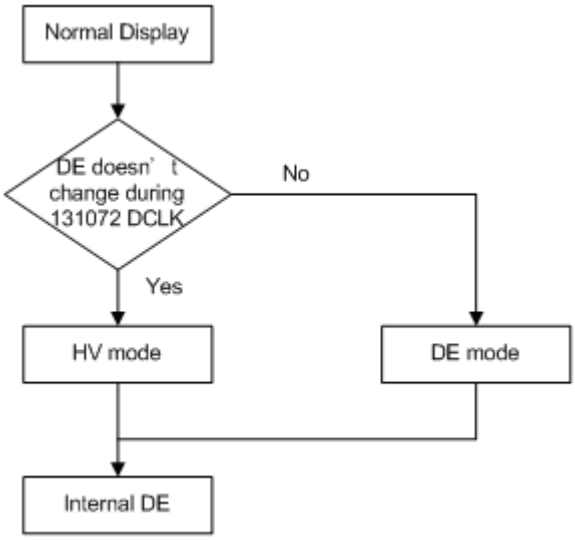
S/W GRB	H/W GRB	Operation mode
0	0	H/W reset
0	1	Execute S/W reset procedure
1	0	H/W reset
1	1	Normal operation

R4 settings

Address	Bit	Description		Default
0000100	7-6	DEM	DE/HV mode setting	**00**
	3-0	VDL	Vertical start pulse adjustment function	**1000**

Bit 7-6	DEM
0x	Auto detection. **(default)**
10	HV mode.
11	DE mode. If DE mode is set, it should be executed immediately.

Figure: DE auto detection flow chart



R13 settings

Address	Bit	Description		Default
0001101	1	NA	NA	**0**
	0	EN_EXT_GAMMA	Enable gamma external voltage input (V1~V14)	**0**

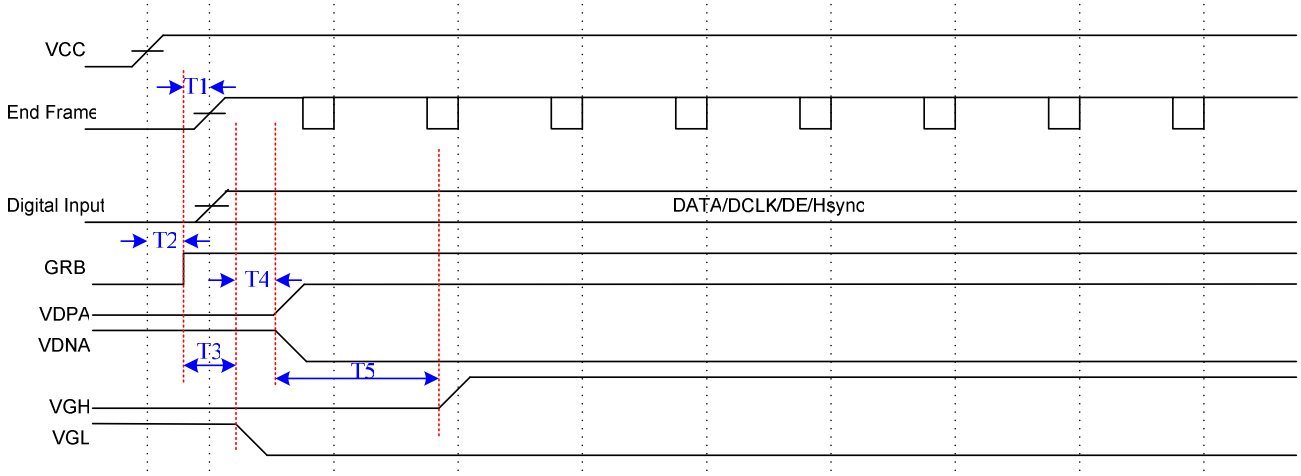
Bit 0	EN_EXT_GAMMA
0	Disable gamma external voltage input (V1~V14). **(default)**
1	Enable gamma external voltage input (V1~V14).

S/W EN_EXT_GAMMA	H/W EN_EXT_GAMMA	External gamma correction voltage V1~V14
0	0	Disable external V1~V14
0	1	Enable external V1~V14
1	0	Enable external V1~V14
1	1	Enable external V1~V14

6. Power On/Off Characteristics

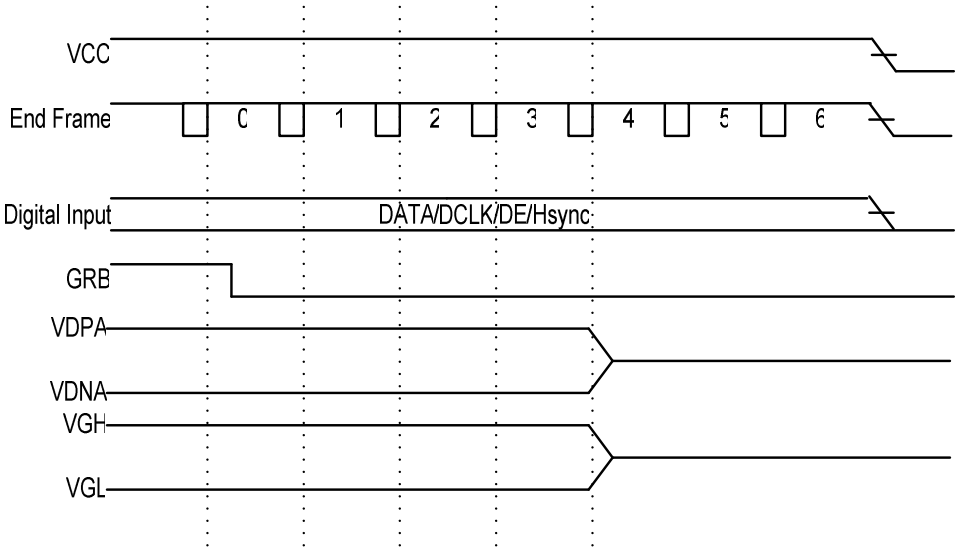
This IC may be damaged by a large current flow when an incorrect power sequence is applied. The recommended power-on sequence is to first connect the logical power (VCC&GND), then the digital signal (DCLK,HSYNC,VSYNC,DE), and then the global reset (GRB). After GRB rise up, five frames time is necessary and then the VGL is produced. Finally, VDPA,VDPA and VGH are produced. Under the power on sequence, panel can normally start up.

a. Recommended Power On Register Setting



T1 > 0us; T2 ≧ 10us ; T3 ≧ 0us ; T4 > 0us ; T5 > 0us

b. Recommended Power Off Sequence



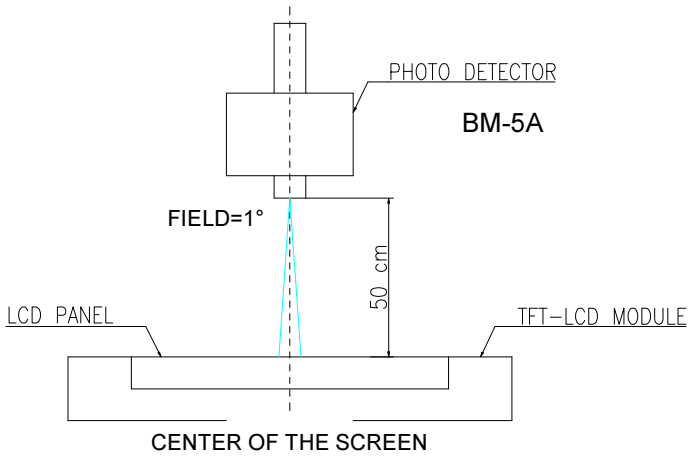
D. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall	 Tr Tf	θ=0°	 -- --	 4 12	 TBD TBD	 ms ms	Note 3
Contrast ratio	CR	At optimized viewing angle	300	500	--		Note 4
Viewing Angle Top Bottom Left Right		CR≥10	40 55 55 55	55 70 70 70	-- -- -- --	deg.	Note 5
Brightness	Y_L	θ=0°	200	250	--	cd/m^2	Note 6
Chromaticity White	X	θ=0°	0.25	0.30	0.35		
	Y	θ=0°	0.27	0.32	0.37		
Uniformity	ΔY_L	%	70	75	--	%	Note 7

Note 1: Ambient temperature =25℃, and LED lightbar current I_L = 200 mA. To be measured in the dark room.

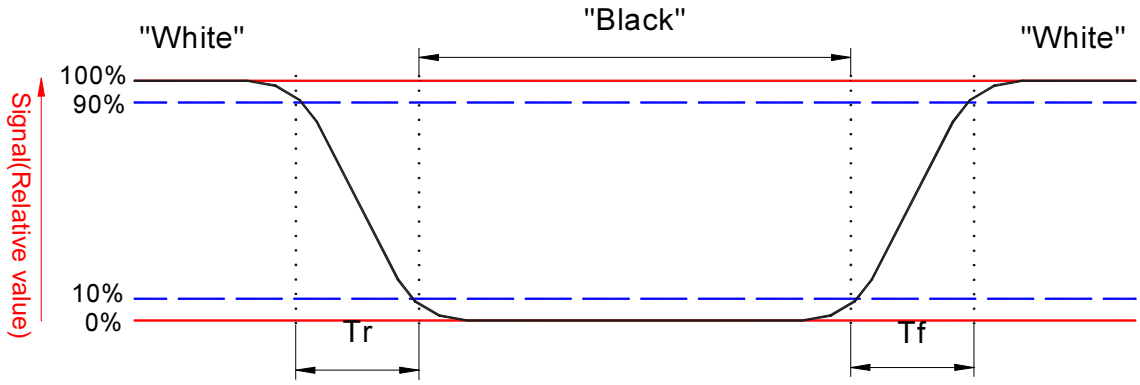
Note 2: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 15 minutes operation.



Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

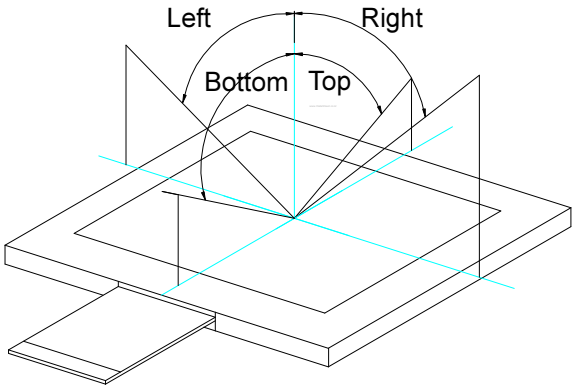


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

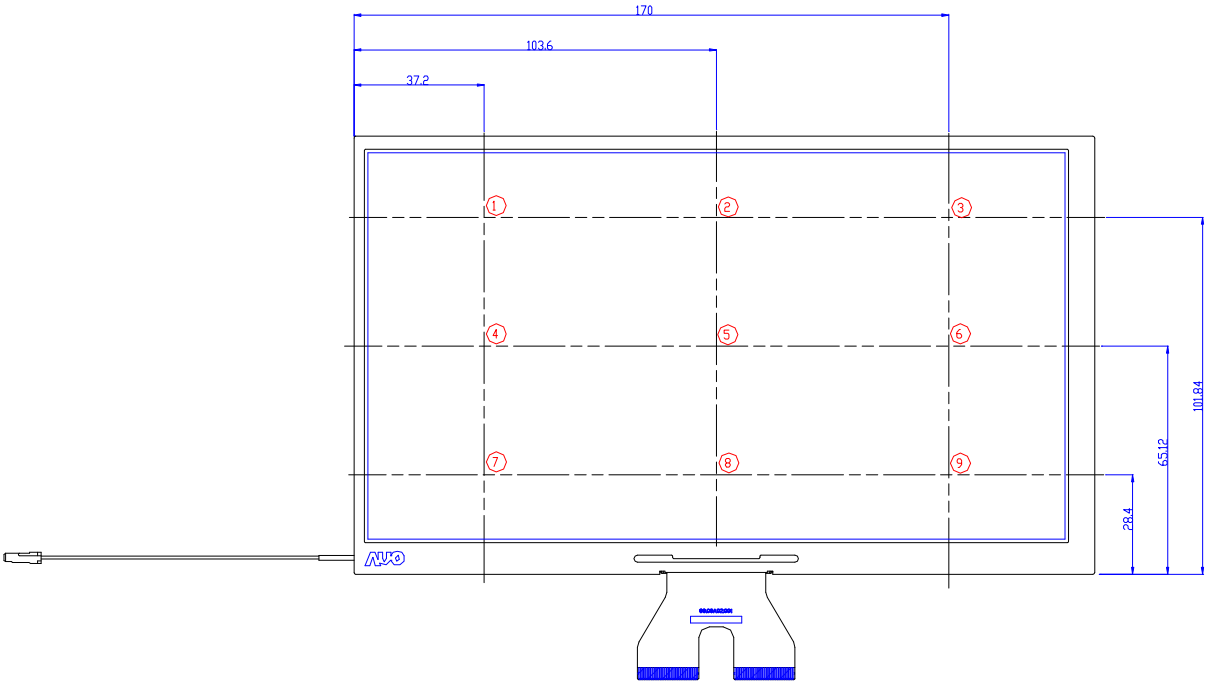
$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.



Note 6. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 7: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

E. Reliability Test Items

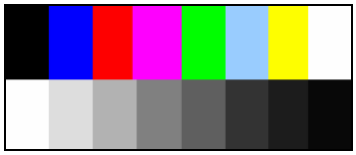
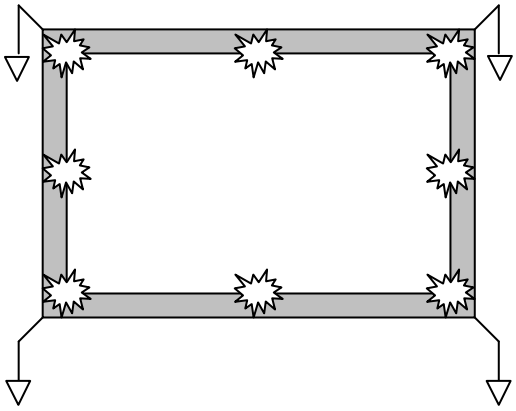
No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 70□ 240Hrs	
2	Low Temperature Storage	Ta= -20□ 240Hrs	
3	High Ttemperature Operation	Tp= 60□ 240Hrs	
4	Low Temperature Operation	Ta= -10□ 240Hrs	
5	High Temperature & High Humidity	Tp= 50□. 80% RH 240Hrs	Operation
6	Heat Shock	-30℃/0.5hr~70℃/0.5hr, 50 cycle	Non-operation
7	Electrostatic Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B	Note 4
8	Image Sticking	25□, 6hrs	Note 5
9	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10Hz ~55Hz-10Hz 2 hours for each direction of X,Y,Z	Non-operation JIS C7021, A-10 condition A : 15 minutes
10	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
11	Vibration (With Carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
12	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	
13	Pressure	5kg, 5sec	Note 6

Note 1: Ta: Ambient Temperature. Tp: Panel Surface Temperature

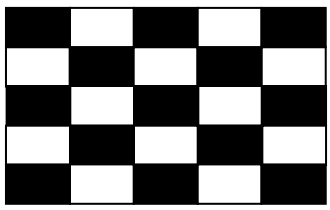
Note 2: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 3: All the cosmetic specification is judged before the reliability stress.

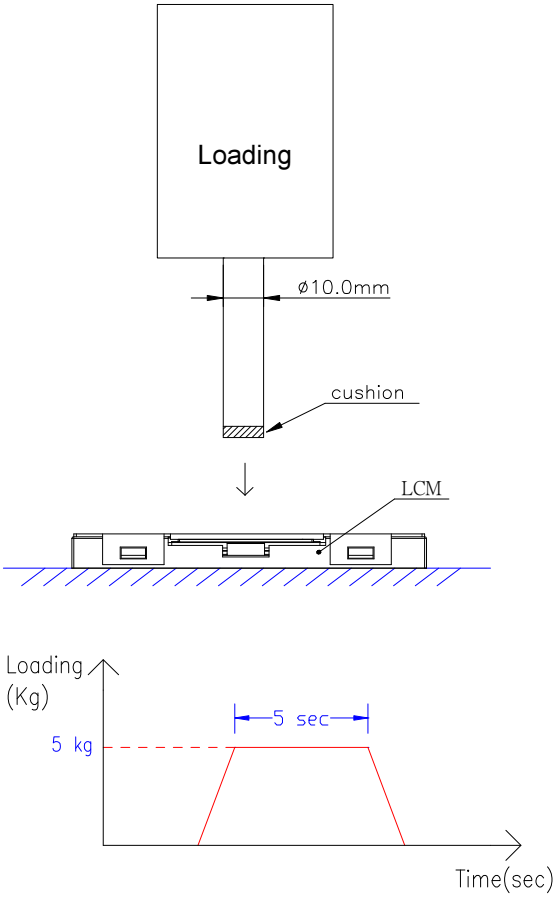
Note 4 : All test techniques follow IEC6100-4-2 standard.

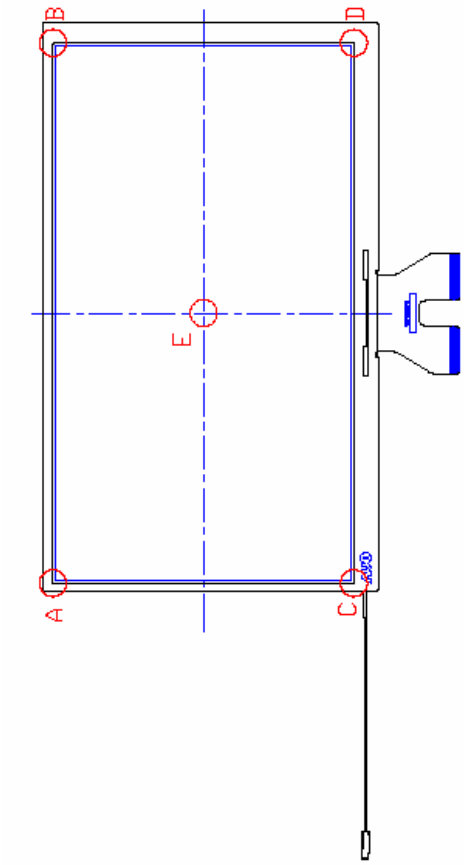
Test Condition		Note
Pattern		
Procedure And Set-up	Contact Discharge：330Ω, 150pF, 1sec, 8 point, 25times/point Air Discharge：330Ω, 150pF, 1sec, 8 point, 25times/point 	
Criteria	B – Some performance degradation allowed. No data lost. Self-recoverable hardware failure.	
Others	1. Gun to Panel Distance 2. No SPI command, keep default register settings.	

Note 5: Operate with 5 x 5 chess board pattern as figure and light on 6 hrs. Then modify to 32 degree gray pattern. After 20 minutes, the mura is less than JND 2.5



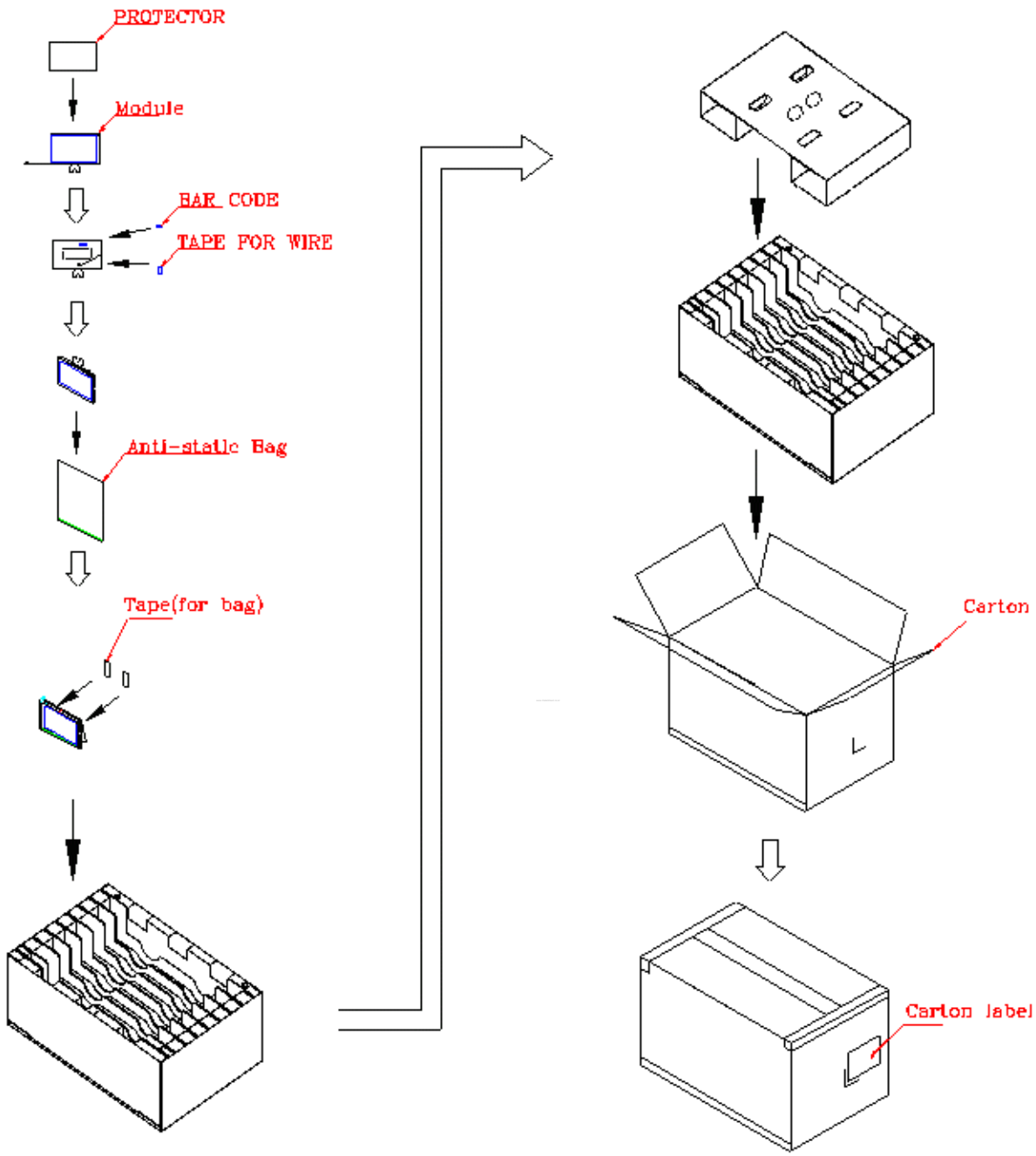
Note 6: The panel is tested as figure. The jig is ϕ 10 mm made by Cu with rubber and the loading speed is 3mm/min on position A~E. After the condition, no glass crack will be found and panel function check is OK.(no guarantee LC mura、LC bubble)





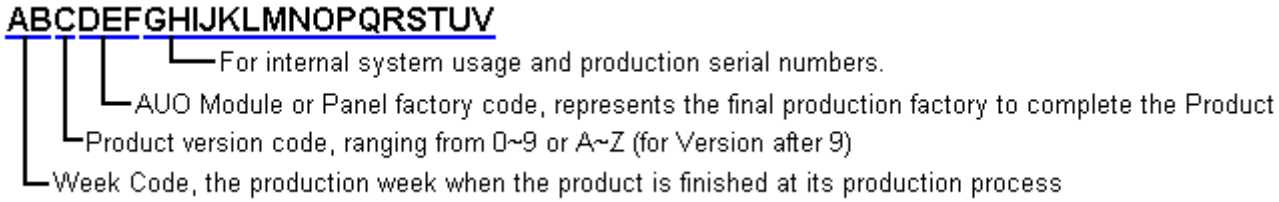
F. Packing and Marking

1. Packing Form



2. Module/Panel Label Information

The module/panel (collectively called as the “Product”) will be attached with a label of Shipping Number which represents the identification of the Product at a specific location. Refer to the Product outline drawing for detailed location and size of the label. The label is composed of a 22-digit serial number and printed with code 128 with the following definition:



Example:

501M06ZL06123456781Z05:

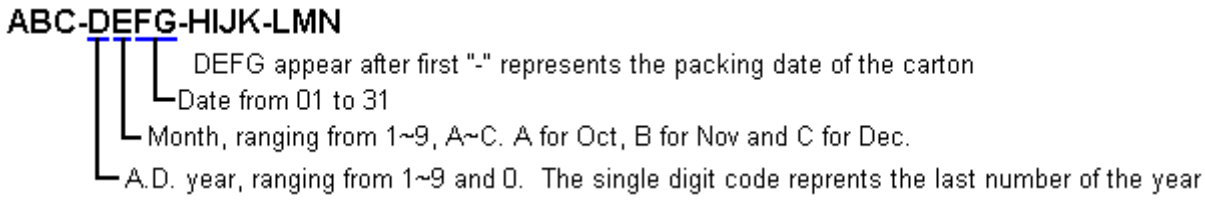
Product Manufacturing Week Code: WK50

Product Version: Version 1

Product Manufactuing Factory: M06

3. Carton Label Information

The packing carton will be attached with a carton label where packing Q’ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed. The Carton Number is apparing in the following format:

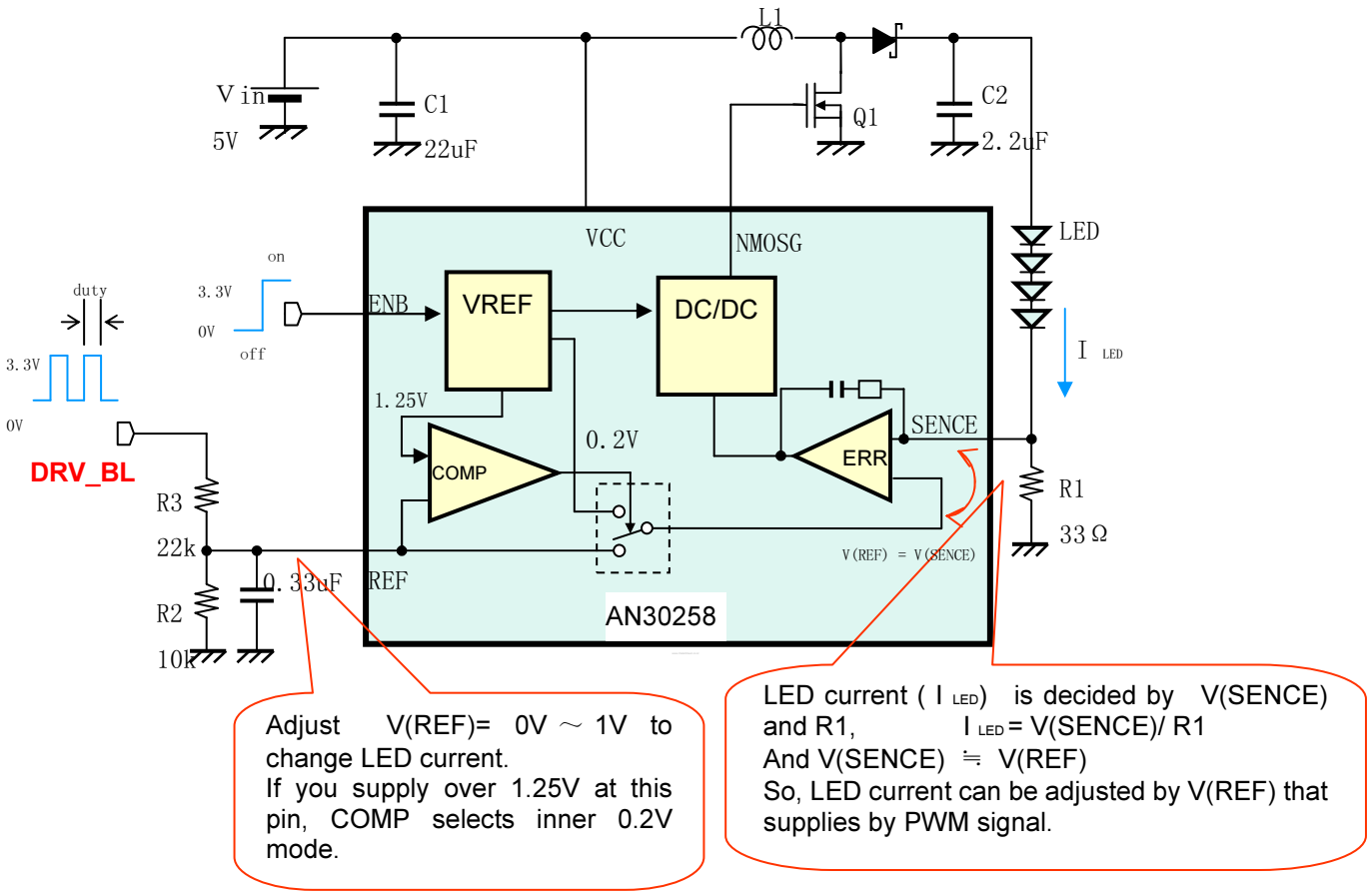


Refer to the drawing of packing format for the location and size of the carton label.

G. Application Note

1. Content-based Automatic Backlight Control (CABC) reference circuit

It is used in a step-up DCDC converter that drives an external NMOS power transistor using a constant frequency PWM architecture. With 2 current modes (Dimmi Mode / Normal Mode) selectable.

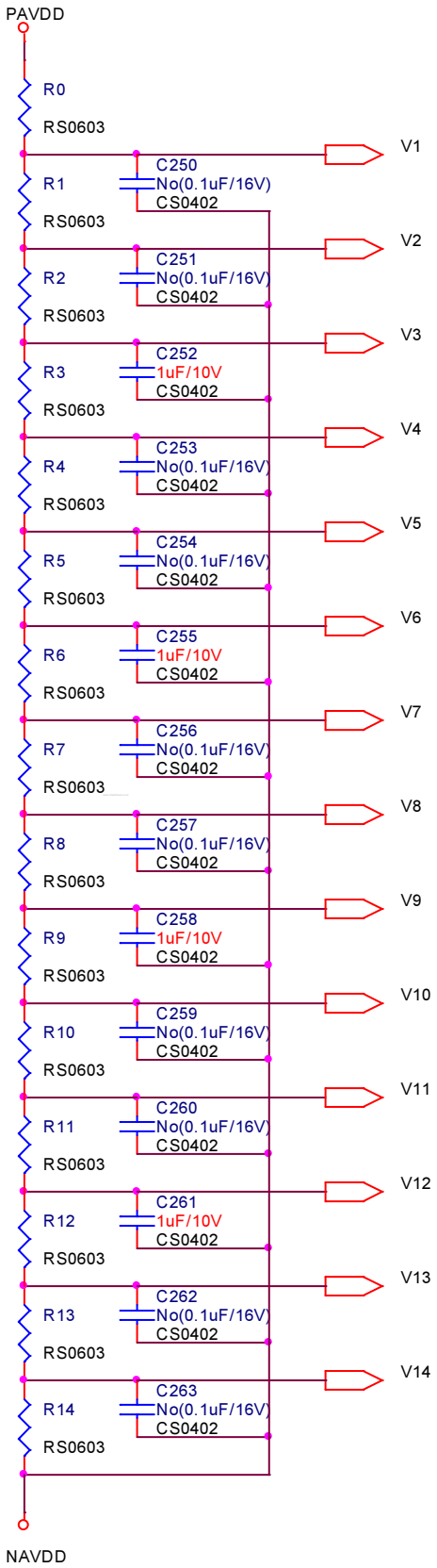


2. Recommended Gamma Voltage

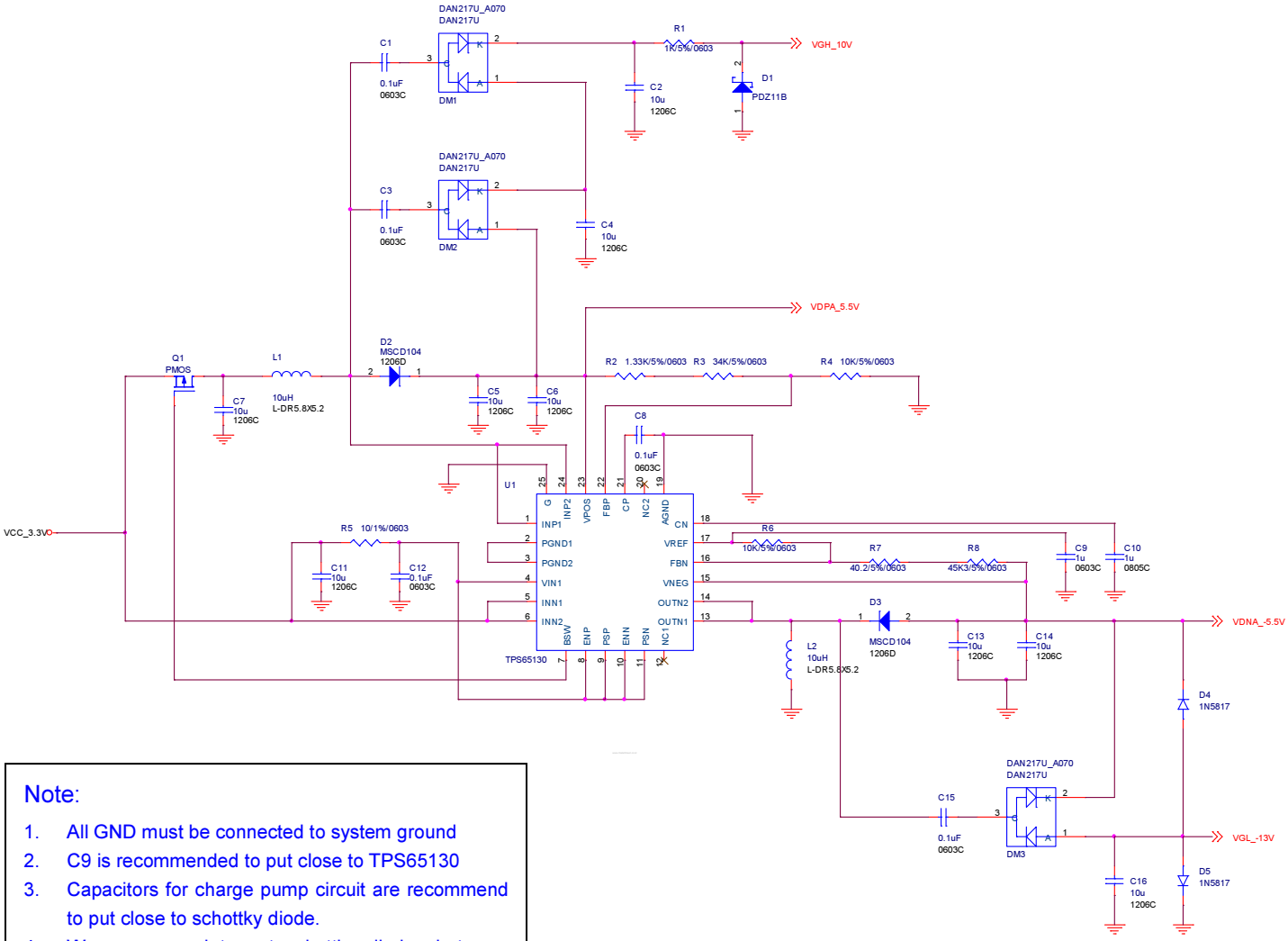
Symbol	Value (V)
V1	4.86
V2	4.7
V3	2.95
V4	2.43
V5	2.08
V6	1.57
V7	1.27
V8	-0.9
V9	-1.19
V10	-1.94
V11	-2.43
V12	-3.07
V13	-4.9
V14	-5.0
PAVDD	5.18
NAVDD	-5.22
VCOM	-1.55

Recommend resister value:

Symbol	Value (Ohm)
R0	1100
R1	549
R2	6190
R3	1800
R4	1210
R5	1780
R6	1050
R7	7500
R8	1000
R9	2610
R10	1690
R11	2210
R12	6490
R13	348
R14	768



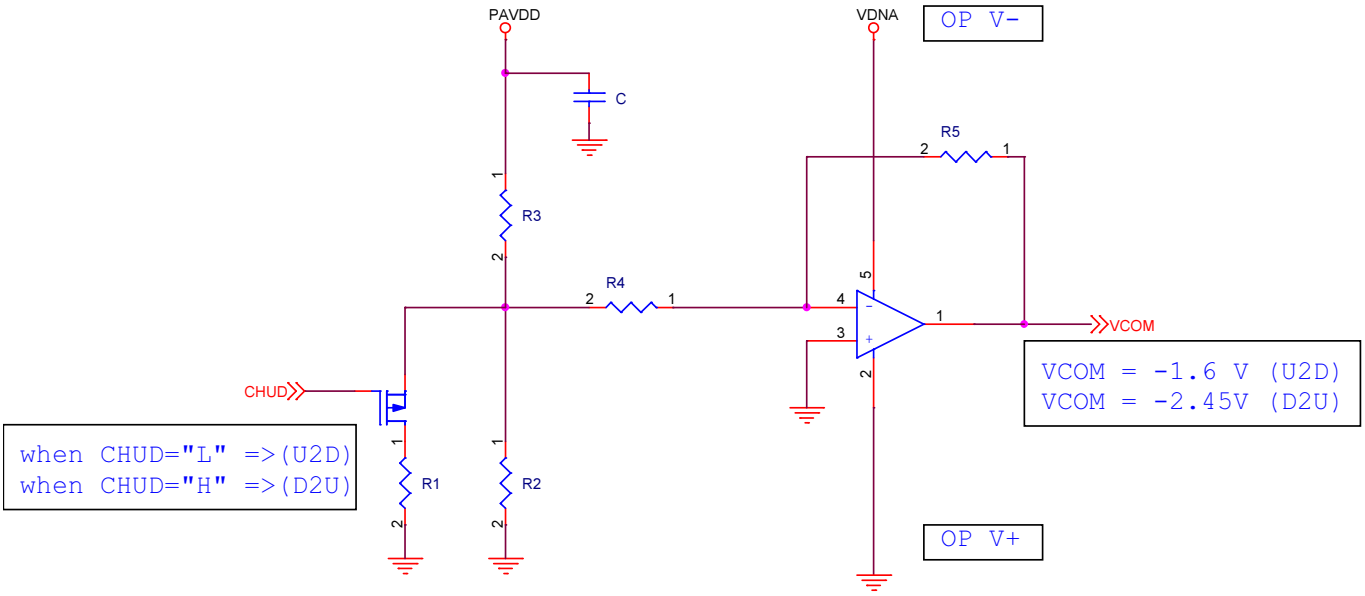
3. Application Circuit



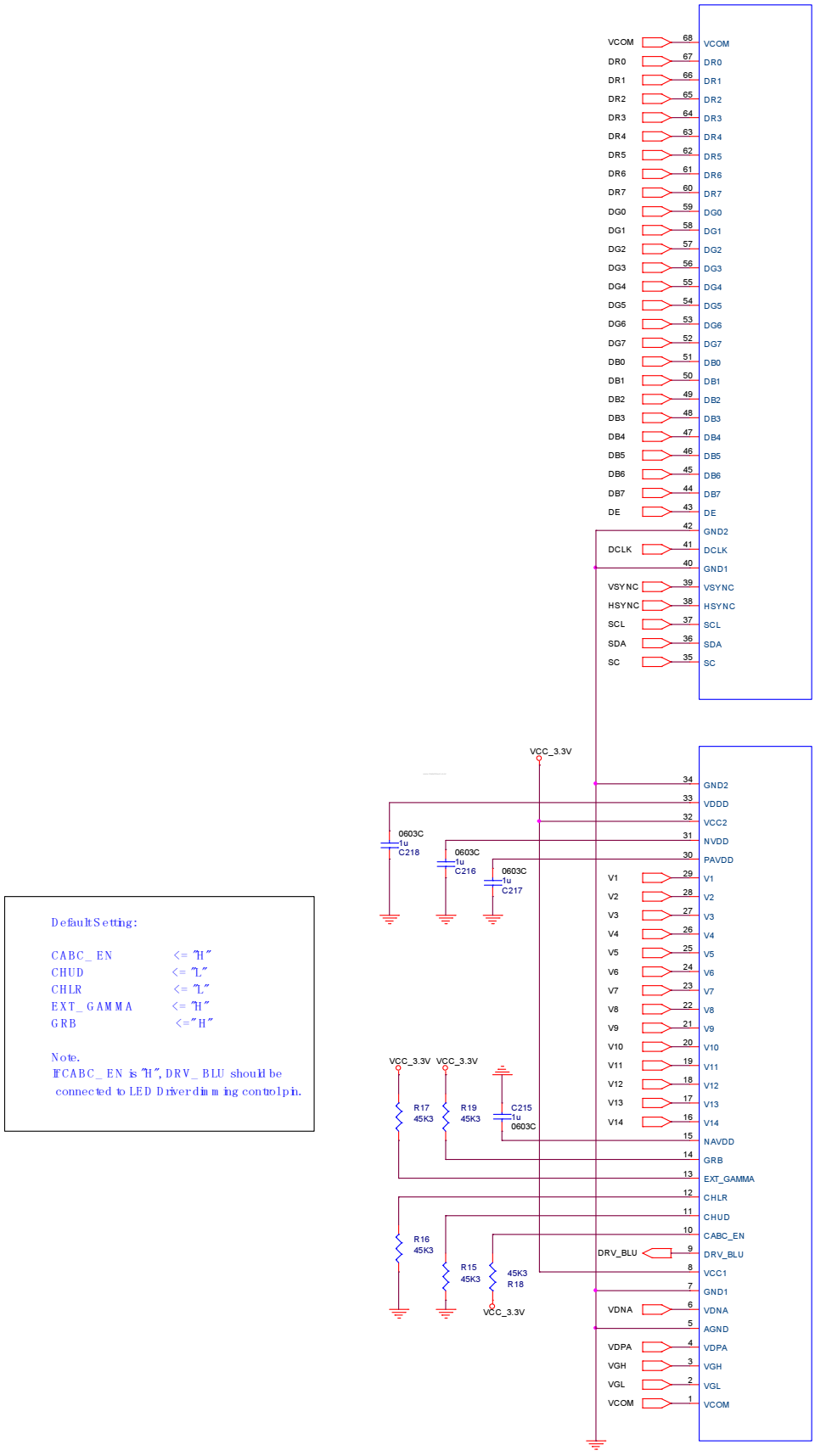
Note:

1. All GND must be connected to system ground
2. C9 is recommended to put close to TPS65130
3. Capacitors for charge pump circuit are recommend to put close to schottky diode.
4. We recommend to put schottky diodes between VGL to GND and VGL to VDNA.

VCOM Circuit for U/D reverse



- R1 =6.34K ohm ; R2= 6.65K ohm ; R3= 6.8K ohm ; R4 = R5 = 100K ohm (All 1% tolerance)
- C = 100nF
- PMOS : CHM2301 PT (Vendor : Chenmko 立勤) /
- OP: G1520F11U (Vendor : GMT 致新) /



Default Setting:

CABC_EN	<= "H"
CHUD	<= "L"
CHLR	<= "L"
EXT_GAMMA	<= "H"
GRB	<= "H"

Note.
If CABC_EN is "H", DRV_BLU should be connected to LED Driver dimming control pin.

H. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.