# 2-Output 1.8V PCIe Gen1/2/3 Zero Delay / Fanout Buffer with Zo=100ohms

9DBV0241

DATASHEET

## Description

The 9DBV0241 is a member of IDT's 1.8V Very-Low-Power (VLP) PCIe family. The device has 2 output enables for clock management.

## Recommended Application

1.8V PCIe Gen1/2/3 Zero-Delay/Fan-out Buffer (ZDB/FOB)

## Output Features

- 2 - 1-200MHz Low-Power (LP) HCSL DIF pairs w/ZO=100Ω

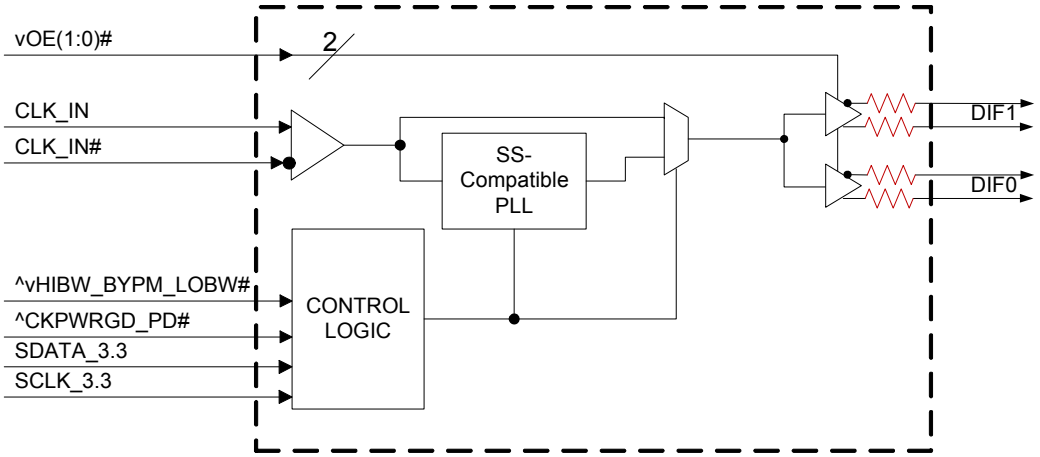
## Key Specifications

- DIF cycle-to-cycle jitter <50ps
- DIF output-to-output skew <50ps
- DIF *additive* phase jitter is <100fs rms for PCIe Gen3
- DIF *additive* phase jitter <300fs rms (12k-20MHz)

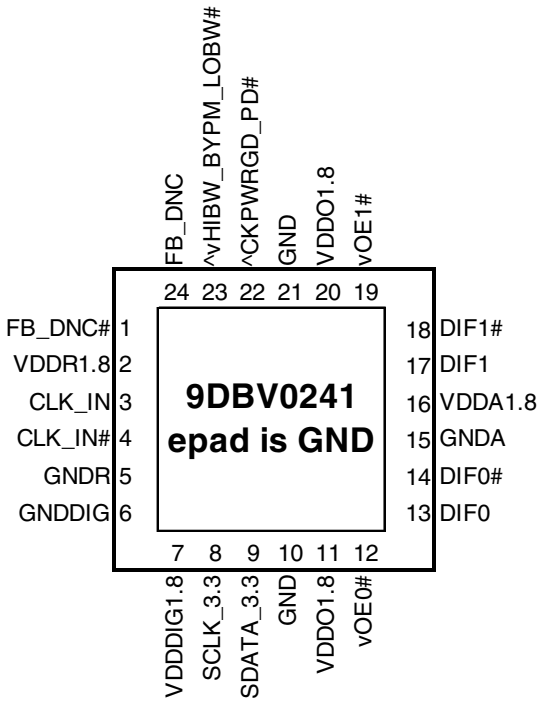
## Features/Benefits

- LP-HCSL outputs with Zo=100Ω; saves 8 resistors compared to standard HCSL outputs
- 35mW typical power consumption in PLL mode; reduced thermal concerns
- Spread Spectrum (SS) compatible; allows use of SS for EMI reduction
- OE# pins; support DIF power management
- HCSL compatible differential input; can be driven by common clock sources
- SMBus-selectable features; optimize signal integrity to application
  - slew rate for each output
  - differential output amplitude
- Pin/software selectable PLL bandwidth and PLL Bypass; optimize PLL to application
- Outputs blocked until PLL is locked; clean system start-up
- Device contains default configuration; SMBus interface not required for device control
- 3.3V tolerant SMBus interface; works with legacy controllers
- Space saving 24-pin 4x4mm VFQFPN; minimal board space

## Block Diagram



## Pin Configuration




**24-pin VFQFPN, 4x4 mm, 0.5mm pitch**

^ prefix indicates internal 120KOhm pull up resistor

^v prefix indicates internal 120KOhm pull up AND pull down resistor (biased to VDD/2)

v prefix indicates internal 120KOhm pull down resistor

### Power Management Table

| CKPWRGD_PD# | CLK_IN | SMBus OEx bit | OEx# Pin | DIFx | | PLL |
|---|---|---|---|---|---|---|
| | | | | True O/P | Comp. O/P | |
| 0 | X | X | X | Low | Low | Off |
| 1 | Running | 0 | X | Low | Low | On[1] |
| 1 | Running | 1 | 0 | Running | Running | On[1] |
| 1 | Running | 1 | 1 | Low | Low | On[1] |

1. If Bypass mode is selected, the PLL will be off, and outputs will be running.

### Power Connections

| Pin Number | | Description |
|---|---|---|
| VDD | GND | |
| 2 | 5 | Input receiver analog |
| 7 | 6 | Digital Power |
| 11,20 | 10,21 | DIF outputs |
| 16 | 15 | PLL Analog |

### Frequency Select Table

| FSEL Byte3 [4:3] | CLK_IN (MHz) | DIFx (MHz) |
|---|---|---|
| **00 (Default)** | 100.00 | CLK_IN |
| 01 | 50.00 | CLK_IN |
| 10 | 125.00 | CLK_IN |
| 11 | Reserved | Reserved |

### PLL Operating Mode

| HiBW_BypM_LoBW# | MODE | Byte1 [7:6] Readback | Byte1 [4:3] Control |
|---|---|---|---|
| 0 | PLL Lo BW | 00 | 00 |
| M | Bypass | 01 | 01 |
| 1 | PLL Hi BW | 11 | 11 |

### SMBus Address

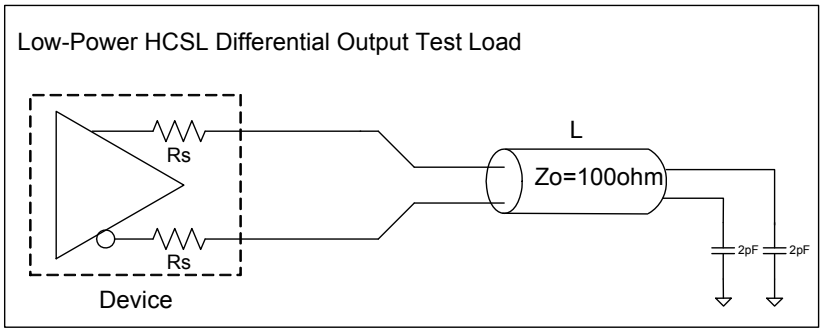
| Address | + Read/Write bit |
|---|---|
| 1101101 | x |

## Pin Descriptions

| Pin# | Pin Name | Type | Pin Description |
|---|---|---|---|
| 1 | FB_DNC# | DNC | Complement clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin. |
| 2 | VDDR1.8 | PWR | 1.8V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately. |
| 3 | CLK_IN | IN | True Input for differential reference clock. |
| 4 | CLK_IN# | IN | Complementary Input for differential reference clock. |
| 5 | GNDR | GND | Analog Ground pin for the differential input (receiver) |
| 6 | GNDDIG | GND | Ground pin for digital circuitry |
| 7 | VDDDIG1.8 | PWR | 1.8V digital power (dirty power) |
| 8 | SCLK_3.3 | IN | Clock pin of SMBus circuitry, 3.3V tolerant. |
| 9 | SDATA_3.3 | I/O | Data pin for SMBus circuitry, 3.3V tolerant. |
| 10 | GND | GND | Ground pin. |
| 11 | VDDO1.8 | PWR | Power supply for outputs, nominally 1.8V. |
| 12 | vOE0# | IN | Active low input for enabling DIF pair 0. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 13 | DIF0 | OUT | Differential true clock output |
| 14 | DIF0# | OUT | Differential Complementary clock output |
| 15 | GNDA | GND | Ground pin for the PLL core. |
| 16 | VDDA1.8 | PWR | 1.8V power for the PLL core. |
| 17 | DIF1 | OUT | Differential true clock output |
| 18 | DIF1# | OUT | Differential Complementary clock output |
| 19 | vOE1# | IN | Active low input for enabling DIF pair 1. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 20 | VDDO1.8 | PWR | Power supply for outputs, nominally 1.8V. |
| 21 | GND | GND | Ground pin. |
| 22 | ^CKPWRGD_PD# | IN | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor. |
| 23 | ^vHIBW_BYPM_LOBW# | LATCHED IN | Trilevel input to select High BW, Bypass or Low BW mode. This pin is biased to VDD/2 (Bypass mode) with internal pull up/pull down resistors. See PLL Operating Mode Table for Details. |
| 24 | FB_DNC | DNC | True clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin. |
| 25 | epad | GND | GND |

NOTE: DNC indicates Do Not Connect anything to this pin.

## Test Loads




L = 5 inches

## Alternate Terminations

The 9DBV family can easily drive LVPECL, LVDS, and CML logic. See "AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs" for details.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBV0241. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| 1.8V Supply Voltage | VDDxx | Applies to all VDD pins | -0.5 | | 2.5 | V | 1,2 |
| Input Voltage | $V_{IN}$ | | -0.5 | | $V_{DD}$+0.5V | V | 1, 3 |
| Input High Voltage, SMBus | $V_{IHSMB}$ | SMBus clock and data pins | | | 3.6V | V | 1 |
| Storage Temperature | Ts | | -65 | | 150 | °C | 1 |
| Junction Temperature | Tj | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 2.5V.

## Electrical Characteristics–Clock Input Parameters

TA = $T_{COM}$ or $T_{IND;}$ Supply Voltage per VDD of normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Input Common Mode Voltage - DIF_IN | $V_{COM}$ | Common Mode Input Voltage | 150 | | 1000 | mV | 1 |
| Input Swing - DIF_IN | $V_{SWING}$ | Differential value | 300 | | 1450 | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | $I_{IN}$ | $V_{IN} = V_{DD}$ , $V_{IN}$ = GND | -5 | | 5 | uA | |
| Input Duty Cycle | $d_{tin}$ | Measurement from differential wavefrom | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | $J_{DIFIn}$ | Differential Measurement | 0 | | 125 | ps | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2]Slew rate measured through +/-75mV window centered around differential zero

# Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = $T_{AMB}$, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | VDDx | Supply voltage for core and analog | 1.7 | 1.8 | 1.9 | V | |
| Ambient Operating Temperature | $T_{AMB}$ | Commmercial range | 0 | 25 | 70 | °C | |
| | | Industrial range | -40 | 25 | 85 | °C | |
| Input High Voltage | $V_{IH}$ | Single-ended inputs, except SMBus | 0.75 $V_{DD}$ | | $V_{DD}$ + 0.3 | V | |
| Input Mid Voltage | $V_{IM}$ | Single-ended tri-level inputs ('_tri' suffix) | 0.4 $V_{DD}$ | | 0.6 $V_{DD}$ | V | |
| Input Low Voltage | $V_{IL}$ | Single-ended inputs, except SMBus | -0.3 | | 0.25 $V_{DD}$ | V | |
| Input Current | $I_{IN}$ | Single-ended inputs, $V_{IN}$ = GND, $V_{IN}$ = VDD | -5 | | 5 | uA | |
| | $I_{INP}$ | Single-ended inputs<br>$V_{IN}$ = 0 V; Inputs with internal pull-up resistors<br>$V_{IN}$ = VDD; Inputs with internal pull-down resistors | -200 | | 200 | uA | |
| Input Frequency | $F_{ibyp}$ | Bypass mode | 1 | | 200 | MHz | 2 |
| | $F_{ipll}$ | 100MHz PLL mode | 60 | 100.00 | 140 | MHz | 2 |
| | $F_{ipll}$ | 125MHz PLL mode | 75 | 125.00 | 175 | MHz | 2 |
| | $F_{ipll}$ | 50MHz PLL mode | 30 | 50.00 | 65 | MHz | 2 |
| Capacitance | $C_{IN}$ | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | $C_{INDIF\_IN}$ | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,5 |
| | $C_{OUT}$ | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | $T_{STAB}$ | From $V_{DD}$ Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1 | ms | 1,2 |
| Input SS Modulation Frequency PCIe | $f_{MODINPCIe}$ | Allowable Frequency for PCIe Applications (Triangular Modulation) | 30 | | 33 | kHz | |
| Input SS Modulation Frequency non-PCIe | $f_{MODIN}$ | Allowable Frequency for non-PCIe Applications (Triangular Modulation) | 0 | | 66 | kHz | |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion<br>DIF stop after OE# deassertion | 1 | | 3 | clocks | 1,3 |
| Tdrive_PD# | $t_{DRVPD}$ | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | $t_F$ | Fall time of single-ended control inputs | | | 5 | ns | 2 |
| Trise | $t_R$ | Rise time of single-ended control inputs | | | 5 | ns | 2 |
| SMBus Input Low Voltage | $V_{ILSMB}$ | $V_{DDSMB}$ = 3.3V, see note 4 for $V_{DDSMB}$ < 3.3V | | | 0.6 | V | |
| SMBus Input High Voltage | $V_{IHSMB}$ | $V_{DDSMB}$ = 3.3V, see note 5 for $V_{DDSMB}$ < 3.3V | 2.1 | | 3.6 | V | 4 |
| SMBus Output Low Voltage | $V_{OLSMB}$ | @ $I_{PULLUP}$ | | | 0.4 | V | |
| SMBus Sink Current | $I_{PULLUP}$ | @ $V_{OL}$ | 4 | | | mA | |
| Nominal Bus Voltage | $V_{DDSMB}$ | Bus Voltage | 1.7 | | 3.6 | V | |
| SCLK/SDATA Rise Time | $t_{RSMB}$ | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | $t_{FSMB}$ | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | $f_{MAXSMB}$ | Maximum SMBus operating frequency | | | 400 | kHz | 6 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

[4] For $V_{DDSMB}$ < 3.3V, $V_{IHSMB}$ >= 0.8x$V_{DDSMB}$

[5]DIF_IN input

[6]The differential input clock must be running for the SMBus to be active

## Electrical Characteristics–DIF 0.7V Low Power HCSL Outputs

TA = $T_{AMB}$, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Slew rate | dV/dt | Scope averaging on, fast setting | 1.6 | 2.8 | 4 | V/ns | 1,2,3 |
| | dV/dt | Scope averaging on, slow setting | 1.1 | 2.0 | 3 | V/ns | 1,2,3 |
| Slew rate matching | ß dV/dt | Slew rate matching, Scope averaging on | | 7 | 20 | % | 1,2,4 |
| Voltage High | $V_{HIGH}$ | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 736 | 850 | mV | 7 |
| Voltage Low | $V_{LOW}$ | | -150 | 32 | 150 | | 7 |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. (Scope averaging off) | | 769 | 1150 | mV | 7 |
| Min Voltage | Vmin | | -300 | 21 | | | 7 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 250 | 391 | 550 | mV | 1,5 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off | | 13 | 140 | mV | 1,6 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

## Electrical Characteristics–Current Consumption

TA = $T_{AMB}$, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Operating Supply Current | $I_{DDA}$ | VDDA+VDDR, PLL Mode, @100MHz | | 4.4 | 6 | mA | 1 |
| | $I_{DD}$ | VDD, All outputs active @100MHz | | 14.2 | 18 | mA | 1 |
| Powerdown Current | $I_{DDAPD}$ | VDDA+VDDR, PLL Mode, @100MHz | | 0.01 | 1 | mA | 1, 2 |
| | $I_{DDPD}$ | VDD, Outputs Low/Low | | 0.9 | 1.4 | mA | 1, 2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Input clock stopped.

## Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| PLL Bandwidth | BW | -3dB point in High BW Mode | 2 | 2.7 | 4 | MHz | 1,5 |
| | | -3dB point in Low BW Mode | 1 | 1.4 | 2 | MHz | 1,5 |
| PLL Jitter Peaking | $t_{JPEAK}$ | Peak Pass band Gain | | 1.05 | 2 | dB | 1 |
| Duty Cycle | $t_{DC}$ | Measured differentially, PLL Mode | 45 | 50 | 55 | % | 1 |
| Duty Cycle Distortion | $t_{DCD}$ | Measured differentially, Bypass Mode @100MHz | -1 | -0.1 | 1 | % | 1,3 |
| Skew, Input to Output | $t_{pdBYP}$ | Bypass Mode, $V_T$ = 50% | 2800 | 3623 | 4500 | ps | 1 |
| | $t_{pdPLL}$ | PLL Mode $V_T$ = 50% | 0 | 112 | 200 | ps | 1,4 |
| Skew, Output to Output | $t_{sk3}$ | $V_T$ = 50% | | 33 | 50 | ps | 1,4 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | PLL mode | | 13 | 50 | ps | 1,2 |
| | | *Additive* Jitter in Bypass Mode | | 0.1 | 5 | ps | 1,2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[4] All outputs at default slew rate

[5] The MIN/TYP/MAX values of each BW setting track each other, i.e., Low BW MAX will never occur with Hi BW MIN.

## Electrical Characteristics–Phase Jitter Parameters

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | INDUSTRY LIMIT | UNITS | Notes |
|---|---|---|---|---|---|---|---|---|
| Phase Jitter, PLL Mode | $t_{jphPCIeG1}$ | PCIe Gen 1 | | 32 | 52 | 86 | ps (p-p) | 1,2,3,5 |
| | $t_{jphPCIeG2}$ | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.8 | 1.4 | 3 | ps (rms) | 1,2,3,5 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 2.4 | 2.5 | 3.1 | ps (rms) | 1,2,3,5 |
| | $t_{jphPCIeG3}$ | PCIe Gen 3 (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz) | | 0.5 | 0.6 | 1 | ps (rms) | 1,2,3,5 |
| | $t_{jphSGMII}$ | 125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz | | 1.9 | 2 | NA | ps (rms) | 1,6 |
| Additive Phase Jitter, Bypass Mode | $t_{jphPCIeG1}$ | PCIe Gen 1 | | 0.1 | 5 | N/A | ps (p-p) | 1,2,3,5 |
| | $t_{jphPCIeG2}$ | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.2 | 0.3 | N/A | ps (rms) | 1,2,3,4, 5 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 0.00 | 0.1 | N/A | ps (rms) | 1,2,3,4 |
| | $t_{jphPCIeG3}$ | PCIe Gen 3 (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz) | | 0.00 | 0.1 | N/A | ps (rms) | 1,2,3,4 |
| | $t_{jphSGMII}$ | 125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz | | 165 | 200 | N/A | ps (rms) | 1,6 |
| | $t_{jphSGMII}$ | 125MHz, 12kHz to 20MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz | | 251 | 300 | N/A | ps (rms) | 1,6 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] See http://www.pcisig.com for complete specs

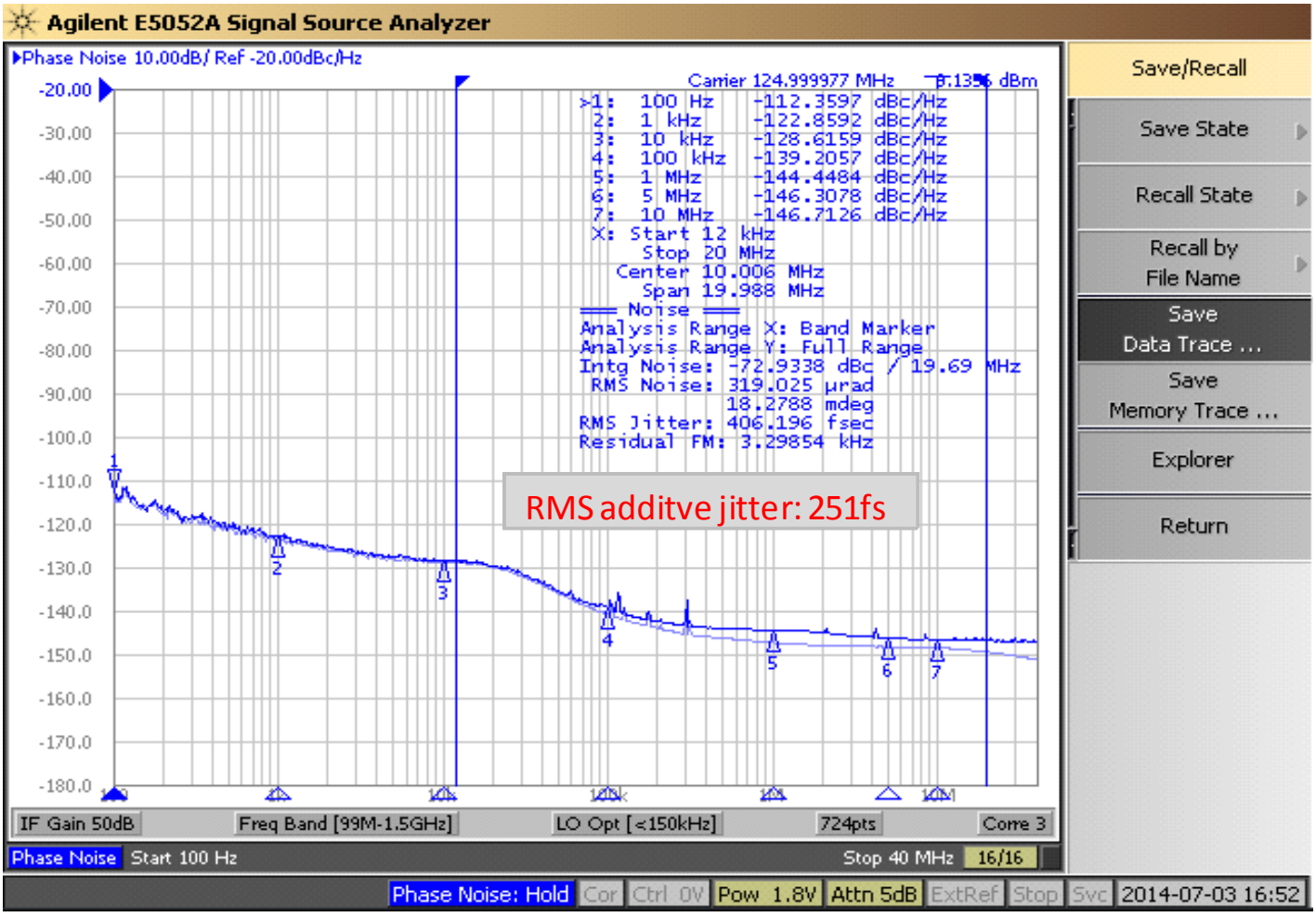
[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)^2 - (input jitter)^2]

[5] Driven by 9FG432 or equivalent

[6] Rohde&Schartz SMA100

## Additive Phase Jitter Plot: 125M (12kHz to 20MHz)



# General SMBus Serial Interface Information

## How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | | |
|---|---|---|---|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

**Note: SMBus Address is 1101101x, where x is the read/write bit.**

## How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|---|---|---|---|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | |
| | | | Data Byte Count=X |
| ACK | | | |
| | | X Byte | Beginning Byte N |
| ACK | | | |
| | | | O |
| O | | | O |
| O | | | O |
| O | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

**SMBus Table: Output Enable Register** [1]

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 1 |
| Bit 6 | Reserved | | | | | 1 |
| Bit 5 | DIF OE1 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 4 | Reserved | | | | | 1 |
| Bit 3 | DIF OE0 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 2 | Reserved | | | | | 1 |
| Bit 1 | Reserved | | | | | 1 |
| Bit 0 | Reserved | | | | | 1 |

1. A low on these bits will overide the OE# pin and force the differential output Low/Low

**SMBus Table: PLL Operating Mode and Output Amplitude Control Register**

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | PLLMODERB1 | PLL Mode Readback Bit 1 | R | See PLL Operating Mode Table | | Latch |
| Bit 6 | PLLMODERB0 | PLL Mode Readback Bit 0 | R | | | Latch |
| Bit 5 | PLLMODE_SWCNTRL | Enable SW control of PLL Mode | RW | Values in B1[7:6] set PLL Mode | Values in B1[4:3] set PLL Mode | 0 |
| Bit 4 | PLLMODE1 | PLL Mode Control Bit 1 | RW[1] | See PLL Operating Mode Table | | 0 |
| Bit 3 | PLLMODE0 | PLL Mode Control Bit 0 | RW[1] | | | 0 |
| Bit 2 | Reserved | | | | | 1 |
| Bit 1 | AMPLITUDE 1 | Controls Output Amplitude | RW | 00 = 0.6V | 01 = 0.7V | 1 |
| Bit 0 | AMPLITUDE 0 | | RW | 10= 0.8V | 11 = 0.9V | 0 |

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

**SMBus Table: DIF Slew Rate Control Register**

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 1 |
| Bit 6 | Reserved | | | | | 1 |
| Bit 5 | SLEWRATESEL DIF1 | Slew Rate Selection | RW | Slow setting | Fast setting | 1 |
| Bit 4 | Reserved | | | | | 1 |
| Bit 3 | SLEWRATESEL DIF0 | Slew Rate Selection | RW | Slow setting | Fast setting | 1 |
| Bit 2 | Reserved | | | | | 1 |
| Bit 1 | Reserved | | | | | 1 |
| Bit 0 | Reserved | | | | | 1 |

**SMBus Table: Frequency Select Control Register**

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 1 |
| Bit 6 | Reserved | | | | | 1 |
| Bit 5 | FREQ_SEL_EN | Enable SW selection of frequency | RW | SW frequency change disabled | SW frequency change enabled | 0 |
| Bit 4 | FSEL1 | Freq. Select Bit 1 | RW[1] | See Frequency Select Table | | 0 |
| Bit 3 | FSEL0 | Freq. Select Bit 0 | RW[1] | | | 0 |
| Bit 2 | Reserved | | | | | 1 |
| Bit 1 | Reserved | | | | | 1 |
| Bit 0 | SLEWRATESEL FB | Adjust Slew Rate of FB | RW | Slow setting | Fast setting | 1 |

1. B3[5] must be set to a 1 for these bits to have any effect on the part.

**Byte 4 is Reserved and reads back 'hFF**

**SMBus Table: Revision and Vendor ID Register**

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | RID3 | Revision ID | **R** | A rev = 0000 | | 0 |
| **Bit 6** | RID2 | | **R** | | | 0 |
| **Bit 5** | RID1 | | **R** | | | 0 |
| **Bit 4** | RID0 | | **R** | | | 0 |
| **Bit 3** | VID3 | VENDOR ID | **R** | 0001 = IDT | | 0 |
| **Bit 2** | VID2 | | **R** | | | 0 |
| **Bit 1** | VID1 | | **R** | | | 0 |
| **Bit 0** | VID0 | | **R** | | | 1 |

**SMBus Table: Device Type/Device ID**

| Byte 6 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | Device Type1 | Device Type | **R** | 00 = FGx, 01 = DBx, 10 = DMx, 11= Reserved | | 0 |
| **Bit 6** | Device Type0 | | **R** | | | 1 |
| **Bit 5** | Device ID5 | Device ID | **R** | 000100 binary or 02 hex | | 0 |
| **Bit 4** | Device ID4 | | **R** | | | 0 |
| **Bit 3** | Device ID3 | | **R** | | | 0 |
| **Bit 2** | Device ID2 | | **R** | | | 0 |
| **Bit 1** | Device ID1 | | **R** | | | 1 |
| **Bit 0** | Device ID0 | | **R** | | | 0 |

**SMBus Table: Byte Count Register**

| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | Reserved | | | | | 0 |
| **Bit 6** | Reserved | | | | | 0 |
| **Bit 5** | Reserved | | | | | 0 |
| **Bit 4** | BC4 | Byte Count Programming | RW | Writing to this register will configure how many bytes will be read back, default is = 8 bytes. | | 0 |
| **Bit 3** | BC3 | | RW | | | 1 |
| **Bit 2** | BC2 | | RW | | | 0 |
| **Bit 1** | BC1 | | RW | | | 0 |
| **Bit 0** | BC0 | | RW | | | 0 |

## Marking Diagrams



Notes:

1. 'LOT' is the lot number.
2. 'YYWW' is the last two digits of the year and week that the part was assembled.
3. 'L' denotes RoHS compliant package.
4. 'I' denotes industrial temperature grade.

## Thermal Characteristics

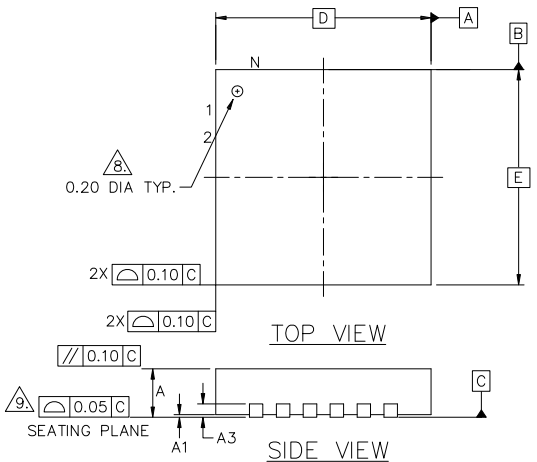
| PARAMETER | SYMBOL | CONDITIONS | PKG | TYP VALUE | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Thermal Resistance | $\theta_{JC}$ | Junction to Case | NLG20 NLG24 | 62 | °C/W | 1 |
| | $\theta_{Jb}$ | Junction to Base | | 5.4 | °C/W | 1 |
| | $\theta_{JA0}$ | Junction to Air, still air | | 50 | °C/W | 1 |
| | $\theta_{JA1}$ | Junction to Air, 1 m/s air flow | | 43 | °C/W | 1 |
| | $\theta_{JA3}$ | Junction to Air, 3 m/s air flow | | 39 | °C/W | 1 |
| | $\theta_{JA5}$ | Junction to Air, 5 m/s air flow | | 38 | °C/W | 1 |

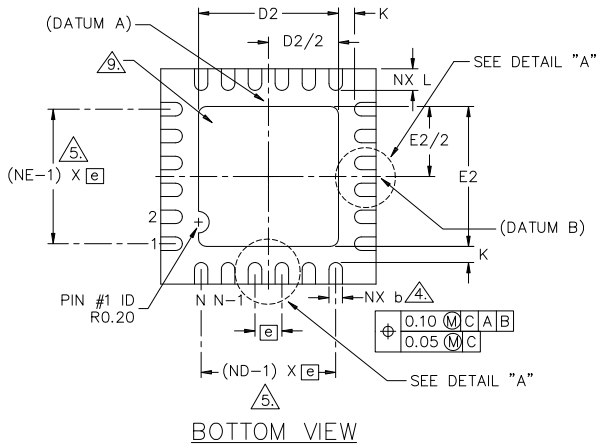
[1]ePad soldered to board

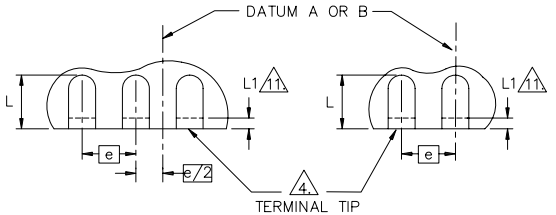
# Package Outline and Dimensions (NLG24)



| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 10/15/08 | RAC |
| 01 | ADD LAND PATTERN | 11/19/10 | JG |




NOTES :

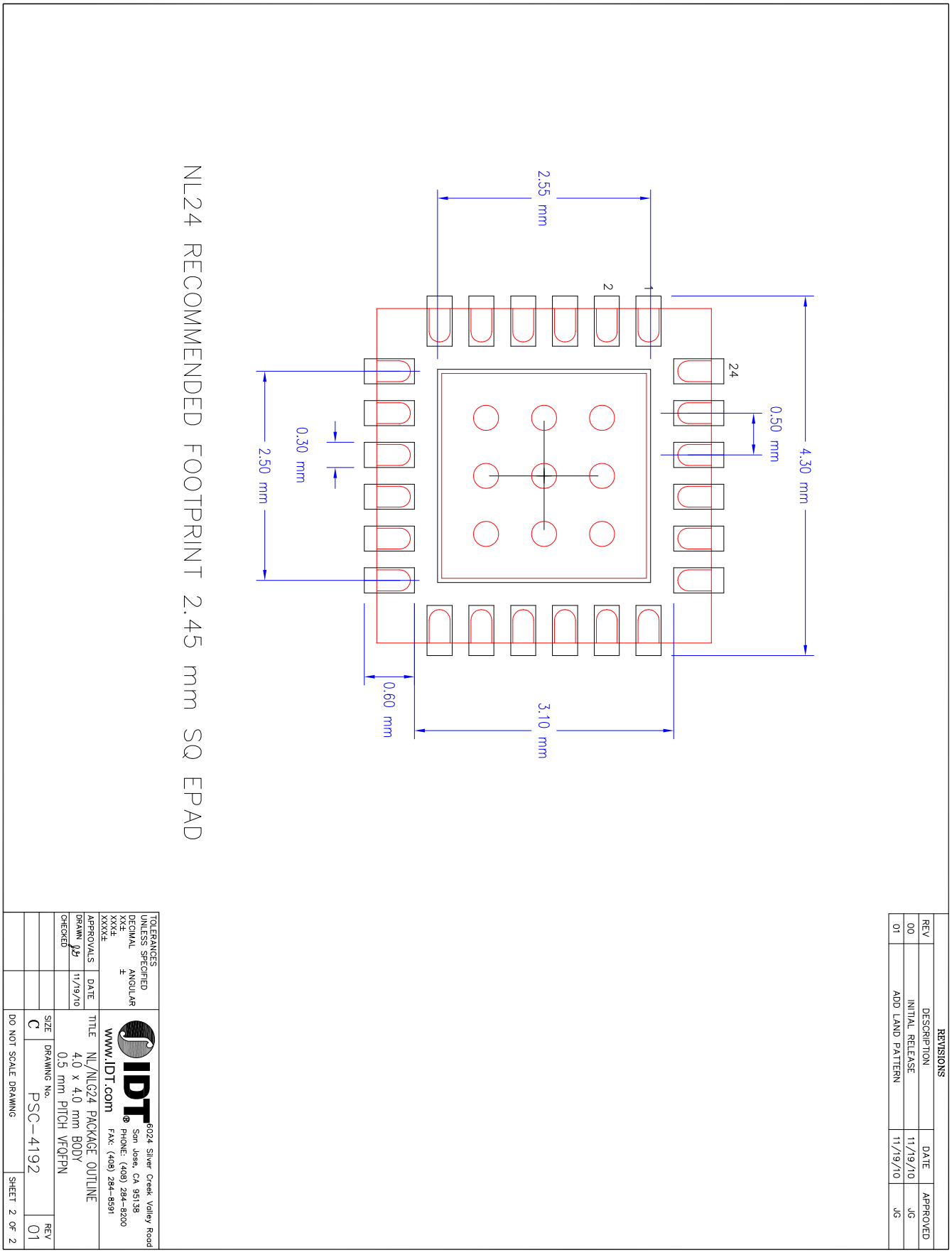
1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220
11. DEPENDING ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, PULLBACK (L1) MAYBE PRESENT
12. PULLBACK DESIGN OPTION IS FOR 0.50mm NOMINAL LANDLENGTH ONLY.

| SYMBOL | MIN. | NOM. | MAX. |
|---|---|---|---|
| e | | 0.50 BSC. | |
| N | | 24 | |
| ND | | 6 | |
| NE | | 6 | |
| L | 0.30 | 0.40 | 0.50 |
| b | 0.18 | 0.25 | 0.30 |
| D2 | 2.30 | 2.45 | 2.60 |
| E2 | 2.30 | 2.45 | 2.60 |

| SYMBOL | DIMENSIONS | | | NOTE |
|---|---|---|---|---|
| | MIN. | NOM. | MAX. | |
| A | 0.80 | 0.90 | 1.0 | |
| A1 | 0.00 | 0.02 | 0.05 | |
| A3 | | 0.20 REF. | | |
| θ | 0 | — | 12 | 2 |
| K | | 0.20 MIN. | | |
| D | | 4.0 BSC | | |
| E | | 4.0 BSC | | |
| L1 | | 0.15 mm MAX | | 11. |

| | | | |
|---|---|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | | IDT® www.IDT.com | 6024 Silver Creek Valley Road<br>San Jose, CA 95138<br>PHONE: (408) 284-8200<br>FAX: (408) 284-8591 |
| APPROVALS | DATE | TITLE | NL/NLG24 PACKAGE OUTLINE<br>4.0 x 4.0 mm BODY<br>0.5 mm PITCH QFN |
| DRAWN RAC | 10/15/08 | | |
| CHECKED | | | |
| | | SIZE C | DRAWING No. PSC-4192 REV 01 |
| | | DO NOT SCALE DRAWING | SHEET 1 OF 2 |

# Package Outline and Dimensions (NLG24), cont.



## Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---|---|---|---|
| 9DBV0241AKLF | Tubes | 24-pin VFQFPN | 0 to +70° C |
| 9DBV0241AKLFT | Tape and Reel | 24-pin VFQFPN | 0 to +70° C |
| 9DBV0241AKILF | Tubes | 24-pin VFQFPN | -40 to +85° C |
| 9DBV0241AKILFT | Tape and Reel | 24-pin VFQFPN | -40 to +85° C |

**"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.**

**“A” is the device revision designator (will not correlate with the datasheet revision).**

## Revision History

| Rev. | Initiator | Issue Date | Description | Page # |
|---|---|---|---|---|
| A | RDW | 8/13/2012 | 1. Updated electrical characteristics tables.<br>2. Move to final. | 5-8 |
| B | RDW | 9/6/2014 | 1. Changed VIH min. from 0.65*VDD to 0.75*VDD<br>2. Changed VIL max. from 0.35*VDD to 0.25*VDD<br>3. Added missing mid-level input voltage spec (VIM) of 0.4*VDD to 0.6*VDD.<br>4. Changed Shipping Packaging from "Trays" to Tubes".<br>5. Reformatted to new template | Various |
| C | RDW | 8/10/2015 | 1. Updated front page text for family consistency<br>2. Updated block diagram for family consistency<br>3. Updated pin configuration to indicate that paddle is ground<br>4. Added epad as pin 25 to pin descritptions<br>5. Replaced "Driving LVDS" with "Alternate Terminations", adding reference to AN-891.<br>6. Updated "Clock Input Parameters Table" correcting inconsistency with PCIe SIG specifications.<br>7. Widened allowable input frequency at each PLL mode frequency.<br>8. Updated phase jitter parameters with 12k-20M additive phase jitter and added additive phase jitter graph.<br>9. Updated NLG24 package drawing with actual package info instead of generic drawing. | 1,2,4,5, 6,7,8, 14 |
| D | RDW | 9/11/2015 | 1. Corrected block diagram from clock generator to ZDB buffer | 1 |
| E | RDW | 11/4/2015 | 1. Minor typographical corrections throughout the data sheet<br>2. Updated test load diagram to generic diagram. Length of test load listed outside the drawing.<br>3. Minor updates to electrical tables for formatting. Removed Schmitt trigger info and output high/low voltage specifications for single-ended outputs, since this part does not have any.<br>4. "Low-Power HCSL Outputs" table: corrected inversion of slew rate setting with specifications. Changed reference from 2 V/ns and 3 V/ns to slow setting and fast setting. Also change references in SMBus Bytes[3:2]<br>5. "Low-Power HCSL Outputs" table: Removed Vswing parameter since this is an input parameter and is covered in "Clock Input Parameters" Table.<br>6. Reduced current consumption limits.<br>7. Minor updates to other electrical tables. | Various, 4-8,11 |
| F | RDW | 4/22/2016 | 1. Updated max frequency of 100MHz PLL mode to 140MHz<br>2. Updated max frequency of 125MHz PLL mode to 175MHz<br>3. Updated max frequency of 50MHz PLL mode to 65MHz | 6 |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