FAIRCHILD

A Schlumberger Company

96LS488
General Purpose Interface Bus (GPIB) Circuit

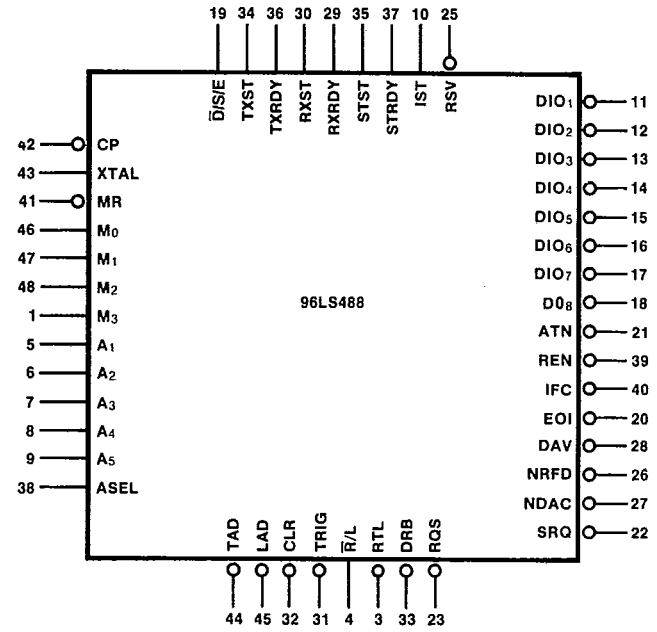
Digital Integrated Circuits

The 96LS488 is a TTL LSI circuit containing all of the logic necessary to interface Talk, Listen and Talk/Listen type instruments and system components in accordance with the IEEE-488 standard for programmable instrumentation. All outputs that drive the IEEE-488 bus are guaranteed to sink 48 mA, and all bus inputs have Schmitt triggers and bus terminating networks. All pins that interface to the instrument logic are LSTTL compatible.

The 96LS488 has programming inputs that determine whether it is to be a talker, listener or both, single or dual address, high or low speed, etc., according to the instrument and system requirements. It operates with a minimum of external support logic and readily interfaces with most microprocessors. It operates from a single 5.0 V supply and a 10 MHz single phase clock and is capable of operating the bus handshake at the full 1 MHz data rate. It offers a variety of handshaking and status connections to the instrument logic for versatility and ease of design.

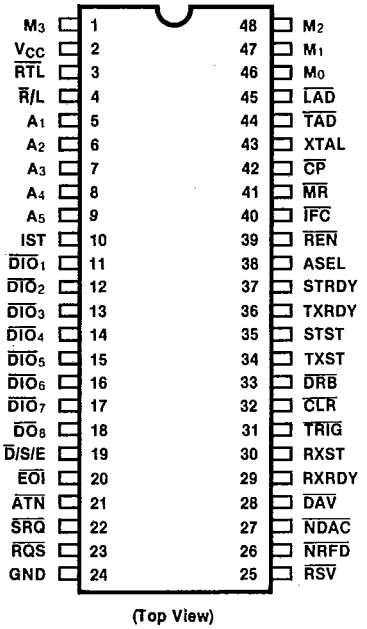
- SINGLE 5.0 V SUPPLY
- COMPLETE SOURCE AND ACCEPTOR HANDSHAKE LOGIC
- SAME OR SEPARATE TALK AND LISTEN ADDRESS
- SECONDARY ADDRESS CAPABILITY
- TALK ONLY OR LISTEN ONLY CAPABILITY
- SOURCE HANDSHAKE DELAY PROGRAMMABLE FOR LOW OR HIGH SPEED
- SERIAL POLL CAPABILITY
- PARALLEL POLL CAPABILITY
- SYNC TRIGGER AND DEVICE CLEAR OUTPUTS
- IMPLEMENTS REMOTE/LOCAL FUNCTION
- ON-CHIP CLOCK OSCILLATOR
- SERVICE REQUEST INTERRUPT FACILITY
- ALL BUS I/O SIGNALS COMPLY WITH THE IEEE-488 (1980) AND IEC-625-1 INPUT THRESHOLD, TERMINATION AND OUTPUT SPECIFICATIONS
- ALL INSTRUMENT INTERFACE SIGNALS ARE LSTTL COMPATIBLE
- GPIB PINS PRESENT NO ELECTRICAL LOAD WHEN DEVICE IS POWERED OFF

Logic Symbol



V_{CC} = Pin 2
Gnd = Pin 24

Connection Diagram
48-Pin DIP



(Top View)

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Input Loading/Fan-Out

Pin Names	Description	96LS (U.L.)** HIGH/LOW
A_1–A_5	Address Inputs	0.5/0.25
$\overline{ATN}$	Attention Input (Active LOW)	T*/1.4
$\overline{CP}$	Clock Input (Active Falling Edge)	0.5/0.25
$\overline{IFC}$	Interface Clear Input (Active LOW)	T*/1.4
IST	Instrument Status Input	0.5/0.25
$M_0 - M_3$	Mode Control Inputs	0.5/0.25
$\overline{MR}$	Master Reset Input (Active LOW)	0.5/0.25
$\overline{REN}$	Remote Enable Input (Active LOW)	T*/1.4
$\overline{RSV}$	Request Service Input (Active LOW)	0.5/0.25
$\overline{RTL}$	Return to Local Input (Active LOW)	0.5/0.25
RXRDY	Receiver Ready Input (Active HIGH)	0.5/0.25
STRDY	Status Ready Input (Active HIGH)	0.5/0.25
TXRDY	Transmitter Ready Input (Active HIGH)	0.5/0.25
$\overline{DAV}$	Data Valid Input (Active LOW)	T*/1.4
	as Output (Active LOW)	130/30
$\overline{DIO}_1$–$\overline{DIO}_7$	Data Inputs	T*/1.4
	as Outputs (Active LOW)	T*/30
$\overline{DO}_8$	Data Output (Active LOW)	T*/30
$\overline{EOI}$	End or Identify Input (Active LOW)	T*/1.4
$\overline{NDAC}$	Not Data Accepted Input (Active LOW)	T*/1.4
	as Output (Active LOW)	T*/30
$\overline{NRFD}$	Not Ready for Data Input	T*/1.4
	as Output (Active LOW)	T*/30
ASEL	Address Select Output	10/5.0 (2.5)
$\overline{CLR}$	Device Clear Output (Active LOW)	10/5.0 (2.5)
$\overline{D}$/S/E	Data/Status Output (Active LOW)	10/5.0 (2.5)
	End-of-String Output (Active HIGH)	10/5.0 (2.5)
$\overline{DRB}$	Bus Drive Enable Output (Active LOW)	10/5.0 (2.5)
$\overline{LAD}$	Listen Address Status Output (Active LOW)	10/5.0 (2.5)
$\overline{RQS}$	Requested Service Status Output (Active LOW)	130/30
RXST	Receiver Strobe Output (Active HIGH)	10/5.0 (2.5)
$\overline{R}$/L	Remote/Local Output	10/5.0 (2.5)
$\overline{SRQ}$	Service Request Output (Active LOW)	T*/30
STST	Status Strobe Output (Active HIGH	10/5.0 (2.5)
$\overline{TAD}$	Talk Address Status Output (Active LOW)	10/5.0 (2.5)
TXST	Transmitter Strobe Output (Active HIGH)	10/5.0 (2.5)
$\overline{TRIG}$	Device Trigger Output (Active LOW)	10/5.0 (2.5)
XTAL	Crystal Output	10/5.0 (2.5)

*T = Resistive Termination per IEEE-488 Standard.

**Unit Load (U.L.) definitions
LOW State: 1.6 mA = 1 U.L.
HIGH State: 40 μA = 1 U.L.
Where two sets of output LOW loading factors are shown, the one in parentheses applies over the Military V_{CC} and temperature ranges.

1693 8-08

GPIB Protocol

A full description and specification of the GPIB system is published in the IEEE document 'IEEE Standard Interface for Programmable Instrumentation" IEEE Std 488–1978 and is used as the reference in this description.

The standard is a 16-wire interface that can transmit byte serial data at rates of up to 1 megabyte/second. Using this standard up to 15 individual devices (instruments or system components) may be interconnected in a star or linear network, with a maximum cable length of 20 m and automatically controlled or programmed. Data may be exchanged between instruments or between a controller and instruments. The use of a bus extender or a controller which can handle a number of separate instrument buses allows more than 15 instruments to be used in a system:

Talkers—These instruments can only transmit data (when addressed), e.g., a timer or counter.

Listeners—These instruments can only receive information, e.g., a programmable power supply or a printer.

Talker/Listeners—These instruments can receive data or functional instructions and later transmit data, e.g., a programmable DVM or multichannel a/d converter.

Controller—A device that is able to generate control instructions for instruments on the bus, e.g., a mini-computer or programmable calculator.

The 96LS488 is designed for use in any of the first three types of devices.

The 16-wire bus is organized as 3 functional groups *(Figure 1).* The 8-line Data bus, $\overline{DIO}_1$–$\overline{DIO}_7$, $\overline{DO}_8$, is used to transfer commands in bit parallel/byte serial form from Talkers to Listeners. The 3-line Data Byte Transfer Control bus, $\overline{NRFD}$, $\overline{NDAC}$ and $\overline{DAV}$, implements a data handshake which ensures that information transfer proceeds as fast as the device will allow but no faster than the slowest device currently addressed as active *(Figure 2).* The 5-line General Interface Management bus $\overline{ATN}$, $\overline{REN}$, $\overline{EOI}$, $\overline{IFC}$ and $\overline{SRQ}$ is principally used by the Controller.

In its simplest configuration the GPIB can consist of only two instruments, a Talker and a Listener; in its most complex configuration up to 961 instruments could be controlled by one or more mini-computers. A bus controller dictates the role of each device by making the $\overline{ATN}$ line LOW and sending Talk and/or Listen Addresses on the bus data lines. Those devices with matching addresses are activated accordingly. Device addresses are set by switches or PC board jumpers. In single address mode each device has a 5-bit address allowing up to 31 different addresses (one code is used as an unaddress command). In extended address mode each device has a 10-bit address, allowing up to 961 different addresses and the Controller must send two bytes in order to activate a device.

In the configuration shown in *Figure 1* a sequence to initiate a data transfer from device A to device D would proceed as follows:

Controller sends $\overline{ATN}$ (attention) command; whenever the $\overline{ATN}$ line goes LOW, devices using the Data bus immediately stop all operations. The Controller keeps the $\overline{ATN}$ line LOW during the remainder of this sequence.

Controller sends UNL (unlisten) command; this instruction disables any devices that are in Listen mode.

Controller sends Talk Address command to device A; this instruction puts device A into Talk mode and disables any other devices that had been in that mode.

Controller sends Listen Address command to device D, putting it in Listen mode.

When the Controller stops sending $\overline{ATN}$, the bus will be released for data transfer functions and device A will begin transmitting to device D.

The $\overline{SRQ}$ line allows any device to interrupt the Controller and request service. The Controller can identify the interrupting devices by conducting a Serial Poll. To do this it issues an Unlisten (UNL) command followed by a Serial Poll Enable (SPE) command and then the Talk Address of each device in turn. The interrupting device will optionally drive $\overline{DIO}_7$ LOW. Alternatively the Controller can conduct a Parallel Poll by making both $\overline{EOI}$ and $\overline{ATN}$ LOW. Devices will then return one bit of status on a $\overline{DIO}$ line previously assigned via a Parallel Poll Enable (PPE) command.

The $\overline{REN}$ line allows the Controller to put all Listen addressed instruments into remote control mode, while the $\overline{IFC}$ line allows the Controller to initialize the system.

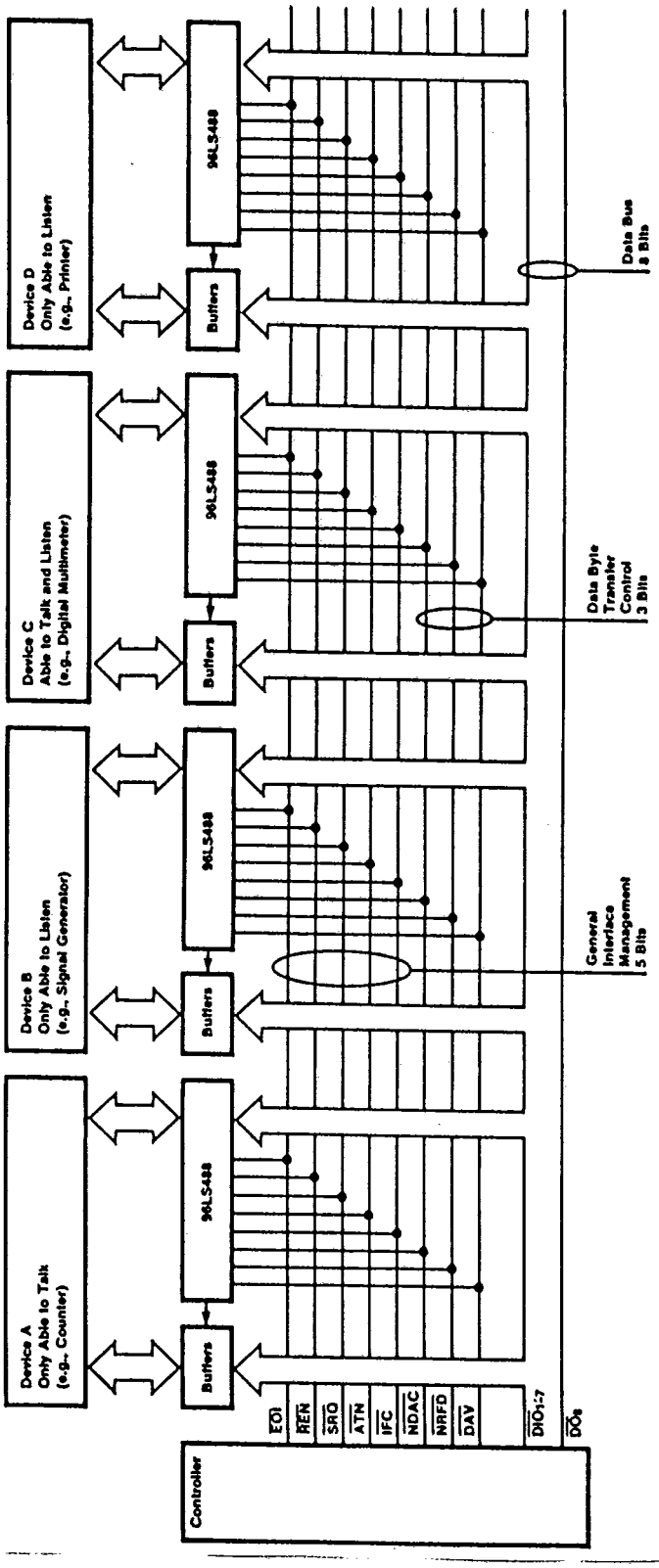
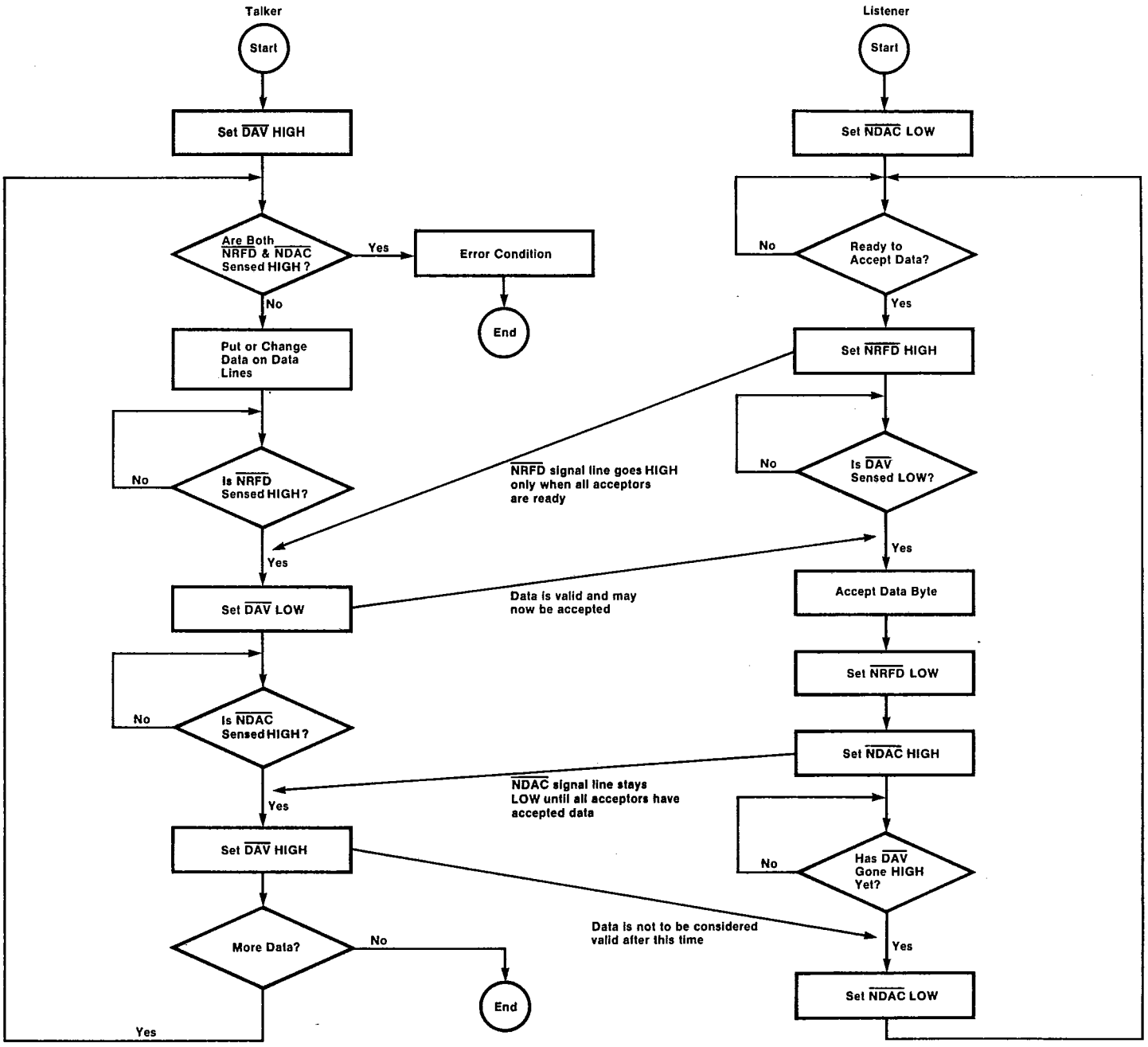
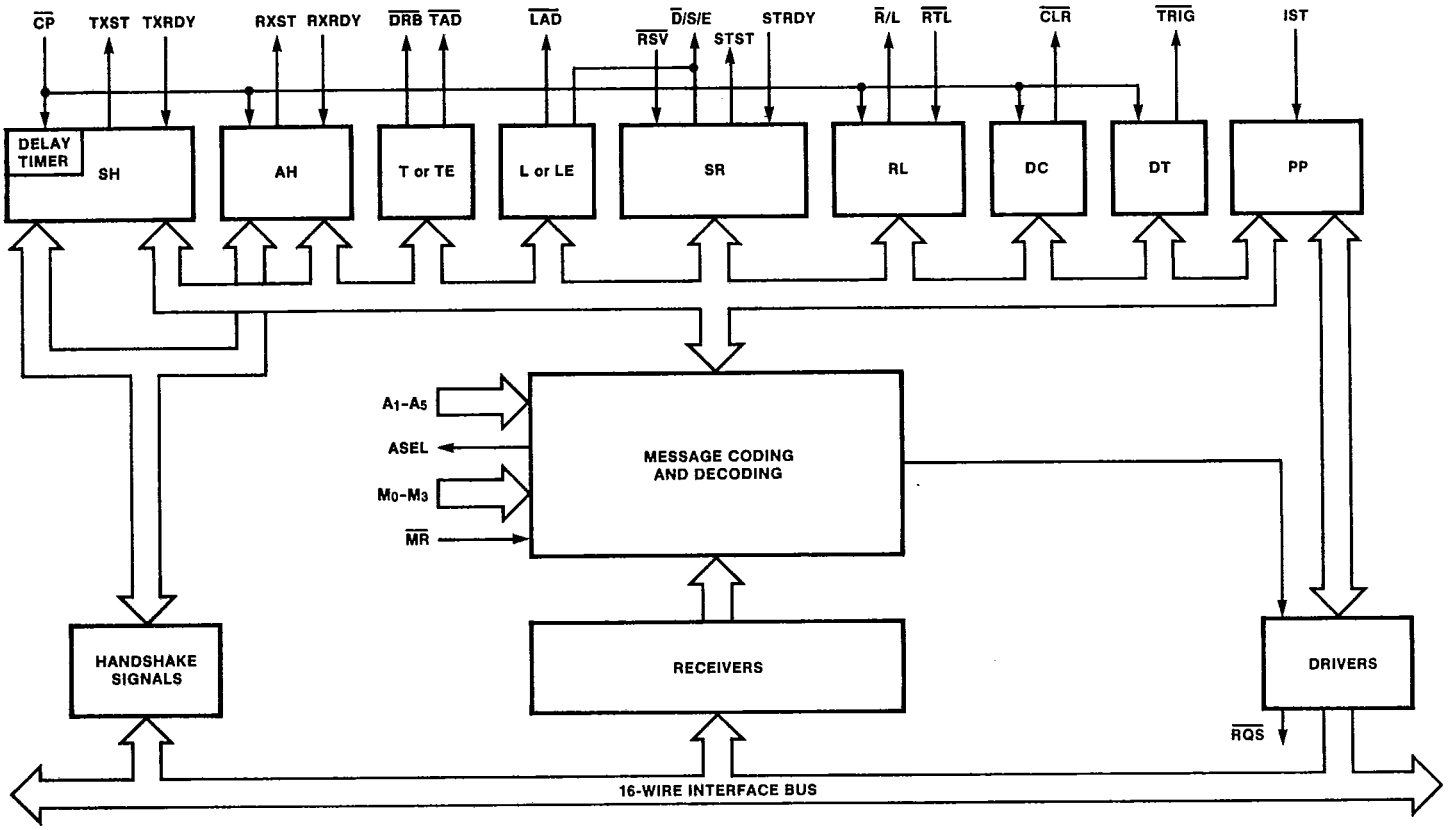


Fig. 1 Interface Capabilities and Bus Structure

Fig. 2 Source and Acceptor Handshake Logic



96LS488 Functional Block Diagram



Functions Implemented by the 96LS488

Acceptor Handshake (AH)
Controls the acquisition of addresses, interface commands and data bytes from the bus. The AH passes data bytes to the instrument logic via a 2-wire handshake (RXST, RXRDY) and a status output ($\overline{LAD}$).

Source Handshake (SH)
Controls the passing of data bytes and status information from the instrument to the bus. The SH communicates with the instrument via a 2-wire handshake (TXST, TXRDY) and a status output ($\overline{TAD}$). It has two operating speeds, selectable via the M_0-M_3 inputs. Low speed is used with open collector data drivers and gives a settling delay of 2.0 μs. High speed is used with 3-state bus drivers and gives a settling delay of 1.1 μs for the first byte sent and 0.5 μs for the subsequent bytes (clock frequency 10 MHz).

Listener, Extended Listener (L or LE)
Either the single or extended address L function can be selected by the M_0-M_3 inputs. The 96LS488 flags the listener addressed status via the $\overline{LAD}$ output. The listen address is defined by the A_1-A_5 inputs and, where the extended address feature is used, the ASEL output controls an external multiplexer to select the primary or secondary address as required.

Talker, Extended Talker (T OR TE)
Either the single or extended address T function can be selected. The T function employes the M_0-M_3 and A_1-A_5 inputs in the same manner as the L function. The 96LS488 flags the talker addressed status via the $\overline{TAD}$ output. The T function also incorporates the Serial Poll Function.

Talker/Listener, Extended Talker/Listener
For instruments with both talk and listen capabilities, the 96LS488 implements both the T and L functions. In this mode, the "Untalk if My Listen Address" and "Unlisten if My Talk Address" feature is standard. Where the single address mode is selected, different Talk and Listen addresses can be used. In the extended address mode, the Talk and Listen addresses must be identical.

Device Trigger, Device Clear (DT, DC)
These functions generate a pulse on the Trigger or Clear output upon receipt of the relevant bus command.

Remote Local (RL)
The complete RL function is implemented, including the Local Lock-Out feature.

Talk Only, Listen Only
The 96LS488 can operate in either of these two modes via the M_0-M_3 input code selection.

Service Request (SR)
The 96LS488 initiates an SR on receipt of the $\overline{RSV}$ input and returns its status on the $\overline{RQS}$ line when serial polled. The $\overline{RQS}$ output can be used to drive the $\overline{DIO}_7$ bus line directly.

Parallel Poll (PP)
The Controller assigns, via the PPE command, one of the eight data lines for use as the Parallel Poll Response output. When the Controller issues the IDY command, the 96LS488 compares the state of the IST input with the state defined by the last PPE command. If the comparison is True, the previously assigned $\overline{DIO}$ line is driven LOW by the 96LS488.

Pin Functions

488 Bus Signals
All bus inputs have Schmitt trigger buffers, and all bus outputs can sink 48 mA. Each bus signal is terminated with a resistive load and meets the dc load characteristics specified in section 3.5.3 of the IEEE Std 488 – 1978 specification.

$\overline{DIO}_1$-$\overline{DIO}_7$ (Data Input/Output)—These are used as inputs to receive addresses and interface commands. They are used as outputs, along with $\overline{DO}_8$ to provide Parallel Poll response.

$\overline{ATN}$ (Attention)—This is an input from the GPIB Controller. When $\overline{ATN}$ is LOW the 96LS488 interprets the data on $\overline{DIO}_1$-$\overline{DIO}_7$ lines as commands or addresses. If the 96LS488 is interrupted by $\overline{ATN}$ while sending data, it will relinquish control of the Data and Management lines within 200 ns.

$\overline{DAV}$ (Data Valid)—A bidirectional signal with a 3-state output driver, $\overline{DAV}$ is part of the handshake system and is driven LOW by current talker when a valid data byte, command or address is on the GPIB. $\overline{DAV}$ is treated as an input when the 96LS488 is addressed to Listen, or is receiving $\overline{ATN}$. It is an output when the 96LS488 is addressed to Talk and $\overline{ATN}$ is HIGH.

$\overline{NRFD}$ (Not Ready for Data)—A bidirectional signal with an open-collector output driver, $\overline{NRFD}$ is part of the handshake system and is driven LOW to indicate that an instrument is not ready to receive data. The 96LS488 drives $\overline{NRFD}$ HIGH when addressed as a Listener and the instrument is ready to accept a data byte or when $\overline{ATN}$ is LOW and the 96LS488 is ready to accept an address or interface command. $\overline{NRFD}$ is treated as an input when the 96LS488 is addressed to Talk.

$\overline{NDAC}$ (Not Data Accepted)—A bidirectional signal with an open-collector output driver, $\overline{NDAC}$ is part of the handshake system and is pulled LOW to indicate that a device has not yet accepted a data byte. $\overline{NDAC}$ is treated as an input when the 96LS488 is addressed to Talk. It is an output and is driven LOW when the 96LS488 is addressed to Listen and the instrument has not accepted a data byte or when receiving $\overline{ATN}$ and the 96LS488 has not accepted an address or interface command.

$\overline{SRQ}$ (Service Request)—This is an open-collector output driven LOW when the instrument requests service (via $\overline{RSV}$) from the Controller.

$\overline{RQS}$ (Requested Service)—A 48 mA 3-state output, enabled during a Serial Poll response and driven LOW if the 96LS488 initiated an $\overline{SRQ}$, $\overline{RQS}$ can be directly connected to $\overline{DIO}_7$ in applications where it is the only status information to be sent.

$\overline{EOI}$ (End or Identify)—This is an input from the GPIB Controller used to elicit a Parallel Poll response, or from the current active talker to indicate the End-of-string (END) message.

$\overline{REN}$ (Remote Enable)—This is an input driven by the Controller. The Controller drives it LOW when it needs to remotely program an instrument.

$\overline{IFC}$ (Interface Clear)—This is an input from the Controller, driven LOW to clear the interface logic. (See *Figure 18.*)

Instrument Interface and Auxiliary Pins
Instrument Logic Signals—All instrument logic signals are standard low-power Schottky compatible.

$\overline{CP}$ (10 MHz Clock)—Used to clock internal-state flip-flops and is divided down internally to generate the SH data settling delay. All output changes are synchronous with the negative clock edge. The $\overline{CP}$ input can be driven by an external oscillator or used in conjunction with XTAL output, as an RC or a crystal oscillator. (See *Figure 6.*)

XTAL (Crystal)—Used to connect a crystal or external RC timing components for the on-chip oscillator. (See *Figure 6.*)

$\overline{MR}$ (Active-LOW Master Reset)—Initializes all internal latches and is completely asynchronous. After a reset, all outputs to the GPIB are passive HIGH and $\overline{RQS}$ is in the high-Z state; R/L, $\overline{TRIG}$, $\overline{CLR}$, $\overline{DRB}$, ASEL, $\overline{TAD}$ and $\overline{LAD}$ are HIGH; D/S/E, RXST, STST and TXST are LOW.

M_0-M_3 (Mode Control Inputs)—Define 1 of 14 possible operating modes for the 96LS488. M_0-M_3 are HIGH-true inputs.

A_1-A_5 (Device Address Inputs)—Define the instrument address and originate from switches, PC jumpers or software-loaded register. Where different Talk and Listen addresses are required or when the secondary address feature is used, these inputs must be externally multiplexed, using the ASEL output to control the multiplexer. A_1-A_5 are HIGH-true inputs (H = 1, L = 0) and thus have the opposite polarity of the $\overline{DIO}_1$-$\overline{DIO}_5$ addresses.

ASEL (Address Select Output)—Selects, via an external multiplexer, the Talk/Listen or primary/secondary address input, depending on the operating mode selected; LOW for Talk or primary address; HIGH for Listen or secondary address. (See *Figure 11.*)

$\overline{LAD}$, $\overline{TAD}$ (Address Status Outputs)—Indicate the Listen-Address or Talk-Address status respectively. They are also activated in the Talk-Only and Listen-Only modes. The outputs are active-LOW to facilitate driving LED indicator lamps. (See *Figures 7, 10.*)

RXST (Receiver Strobe Output)—Forms part of the handshake logic to pass data bytes to the instrument. When addressed to Listen, the 96LS488 takes RXST HIGH when a valid data byte is on the bus and holds it HIGH until the instrument signals (via the RXRDY input) that it has processed the byte. RXST may be inverted and connected to RXRDY, in which case the 96LS488 will receive data bytes from the bus at a data rate determined solely by the bus handshake. (See *Figure 8.*)

TXST (Transmit Strobe Output)—Forms part of the handshake logic to pass data bytes from the instrument to the bus. When addressed to Talk, the 96LS488 takes TXST HIGH to signal the instrument that the bus has accepted the data. TXST does not go LOW again until the instrument has acknowledged that the byte has been accepted (via the TXRDY INPUT). TXST may be inverted and connected to TXRDY, in which case the 96LS488 will transmit data bytes to the bus at a data rate determined solely by the bus handshake. (See *Figure 9.*)

STST (Status Strobe Output)—Forms part of the handshake logic to pass a status byte from the instrument to the bus during a Serial Poll sequence. It operates in conjunction with the STRDY input in the same way as the TXST and TXRDY signals. STST may be inverted and connected to STRDY, in which case the status byte will be repeated as long as the 96LS488 is addressed to Talk. (See *Figure 16.*)

RXRDY (Receiver Ready Input)—Forms part of the handshake logic controlling the passing of data from the bus to the instrument. RXRDY is driven HIGH when the instrument is ready to receive a data byte and LOW to acknowledge receipt of a data byte. (See *Figure 8.*)

TXRDY (Transmitter Ready Input)—Forms part of the handshake logic controlling the passing of data from the instrument to the bus. When the 96LS488 is addressed to Talk, TXRDY is driven HIGH when the instrument has a data byte to send and LOW to acknowledge that the byte has been accepted by the bus. (See *Figure 9.*)

STRDY (Status Ready Input)—Forms part of the handshake logic controlling the passing of a status byte to the bus during a Serial Poll sequence. It operates in a similar fashion to TXRDY. (See *Figure 16.*)

$\overline{RSV}$ (Request Service Input)—Is pulled LOW by the instrument to request service and initiate an $\overline{SRQ}$ interrupt to the controller. This interrupt will be cleared if $\overline{RSV}$ goes HIGH before it is serviced, but once the $\overline{SRQ}$ is serviced, $\overline{RSV}$ must, after exiting SPAS, go HIGH then LOW to initiate another service request. (See *Figure 16.*)

$\overline{CLR}$ (Clear Output)—Issues a negative pulse when the 96LS488 receives a Device Clear (DC) command, or when it is addressed to Listen and receives a Selected Device Clear. The $\overline{CLR}$ Output will stay LOW during Accept Data State (ACDS) or until $\overline{ATN}$ goes HIGH. (See *Figure 13.*)

$\overline{TRIG}$ (Trigger Output)—Issues a negative pulse when the 96LS488 is addressed to Listen and receives a DT command. The $\overline{TRIG}$ output will stay LOW during ACDS or until $\overline{ATN}$ goes HIGH. (See *Figure 13.*)

$\overline{DRB}$ (Drive Bus Output)—Taken LOW to enable an external data bus driver when the 96LS488 is addressed to Talk and is in the Talker Active State. $\overline{DRB}$ will go LOW one clock period after $\overline{ATN}$ goes HIGH, and will go HIGH asynchronously within 200 ns (typically 70 ns) after $\overline{ATN}$ goes LOW. (See *Figures 9, 10, 11.*) $\overline{DRB}$ can also be used to tell the instrument logic to fetch the first byte.

$\overline{RQS}$ (Requested Service Output)—A 48 mA 3-state output, enabled during a Serial Poll response and driven LOW if the 96LS488 initiated an $\overline{SRQ}$. $\overline{RQS}$ can be directly connected to $\overline{DIO_7}$ in applications where it is the only status information to be sent. (See *Figures 4, 5, 16.*)

$\overline{D}$/S/E (Data/Status or END Output)—Valid during the Talk Addressed state and indicates to the instrument logic whether the information to be sent via the bus is to be data or status (LOW for data, HIGH for status). A status byte is sent only in response to a Serial Poll, and, in this case, $\overline{D}$/S/E may be used to control a multiplexer to select data or status as the source to the bus data drivers. (See *Figures 4, 5, 16.*) Valid during the Listener Active State (LACS) to indicate that the current talker is sending the END message; a HIGH output indicates that the END message is true.

$\overline{R}$/L (Remote/Local Output)—Goes LOW when the Controller puts the instrument into Remote mode via the $\overline{REN}$ command. (See *Figures 14, 15.*)

$\overline{RTL}$ (Return to Local Input)—Taken LOW to request return of the instrument to local control. $\overline{RTL}$ will set $\overline{R}$/L HIGH unless the Controller has put the 96LS488 into Local Lock-out state. (See *Figure 14.*)

IST (Instrument Status Input)—Used by the Parallel Poll logic, IST is compared with the logic state defined by $\overline{DIO_4}$ during the last PPE command. If IST is in the defined state, the 96LS488 will make an affirmative response to the next IDY message by making the assigned $\overline{DIO}$ line LOW. Note that IST is a HIGH-true input while $\overline{DIO_4}$ is LOW-true. (See *Figure 17.*)

Operating Modes

The 96LS488 has 14 operating modes, defined by a 4-bit input code M_0-M_3 which would normally be selected by switches or PC board jumpers.

Table 1 defines the input codes and operating modes.

Table 1

Mode Inputs				Operating Mode	Function
M_0	M_1	M_2	M_3		
L	L	L	L	Off Line	The device cannot take part in any GPIB operations
L	L	L	H	TON (LOW Speed)[1]	The device goes directly to the talk addressed state and can source data to the bus
L	L	H	L	LON	The device goes directly to the listen addressed state and can receive data from the bus
L	L	H	H	TON (HIGH Speed)[1]	As for TON (LOW Speed)
L	H	L	L	T (LOW Speed)[1]	Talker Only, single address mode
L	H	L	H	TE (LOW Speed)[1]	Talker Only, extended address mode
L	H	H	L	T (HIGH Speed)[1]	Talker Only, single address mode
L	H	H	H	TE (HIGH Speed)[1]	Talker Only, extended address mode
H	L	L	L	L	Listener Only, single address mode
H	L	L	H	LE	Listener Only, extended address mode
H	H	L	L	T/L (LOW Speed)[1, 2]	Talker/Listener, dual address mode
H	H	L	H	TE/LE (LOW Speed)[1]	Talker/Listener, extended address mode
H	H	H	L	T/L (HIGH Speed)[1, 2]	Talker/Listener, dual address mode
H	H	H	H	TE/LE (HIGH Speed)[1]	Talker/Listener, extended address mode

Notes

1. The LOW speed talker option is selected where open-collector data drivers are used. The delay from putting valid data on the GPIB to $\overline{DAV}$ going true is 2.0 μs. The HIGH speed option is selected where 3-state drivers are used. The settling delay (data to $\overline{DAV}$) is 1.1 μs for the first byte sent after a LOW to HIGH transition of $\overline{ATN}$ and 500 ns for subsequent bytes.
2. For dual address Talker/Listener modes the Talk and Listen addresses can be different.

Table 2

$\overline{DO_8}$	$\overline{DIO_7}$	$\overline{DIO_6}$	$\overline{DIO_5}$	$\overline{DIO_4}$	$\overline{DIO_3}$	$\overline{DIO_2}$	$\overline{DIO_1}$	
X	H	L	$\overline{A}_5$	$\overline{A}_4$	$\overline{A}_3$	$\overline{A}_2$	$\overline{A}_1$	Primary Listen Address
X	H	L	L	L	L	L	L	Unlisten
X	L	H	$\overline{A}_5$	$\overline{A}_4$	$\overline{A}_3$	$\overline{A}_2$	$\overline{A}_1$	Primary Talk Address
X	L	H	L	L	L	L	L	Untalk
X	L	L	$\overline{S}_5$	$\overline{S}_4$	$\overline{S}_3$	$\overline{S}_2$	$\overline{S}_1$	Secondary Address

Addresssing Modes

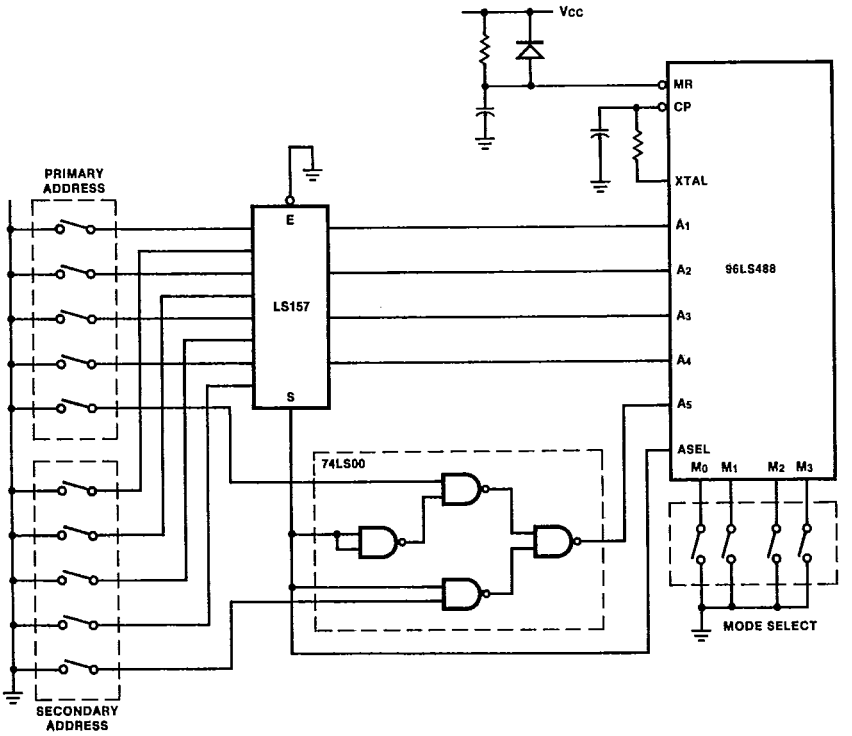
Where extended addressing or different Talk and Listen addresses are required, the address codes must be externally multiplexed, using ASEL. (See *Figure 3.*) In the extended address modes, ASEL is LOW for the primary address and HIGH for the secondary address. (See *Figure 11.*) In the dual address modes, ASEL is HIGH for the Listen address and LOW for the Talk address.

In single address mode the 96LS488 will go into the addressed state on receipt of the primary address. In extended address mode it will go to the addressed state on receipt of its secondary address if, and only if, it has received its primary address. If a device is addressed to Talk and receives its Listen address it will un-address as a Talker and go to Listener addressed state, and vice versa. A Talker Addressed device will un-address if it receives a non-matching talk address. The 96LS488 indicates its address status on the $\overline{TAD}$, $\overline{LAD}$ and $\overline{D}$/S/E outputs. (See *Table 3.*)

Table 3
Status Codes

$\overline{TAD}$	$\overline{LAD}$	$\overline{D}$/S/E	State
H	H	L	Off Line
H	L	L	Addressed to Listen (LADS)
L	H	L	Addressed to Talk (TADS)
L	H	H	Serial Poll Mode (SPM)
H	L	H	Receiving END Message (LACS)

Fig. 3 Address Multiplexer



Status Response

In Serial Poll Active State (SPAS) the instrument is requested to return a status byte, via the usual handshake, to the Controller. Seven bits are defined by the instrument. Bit 7 denotes the Request Service Status ($\overline{RQS}$) and is provided by the 96LS488 on the $\overline{RQS}$ output. If the instrument provides no status, other than $\overline{RQS}$, then the $\overline{RQS}$ output can drive the bus directly *(Figure 4)*. If the instrument provides status information this can be multiplexed to the bus using $\overline{D}$/S/E *(Figure 5)*. After the bus handshake, the instrument can send a second status byte by making STRDY LOW then HIGH again, which starts the handshake. This sequence can be repeated to send additional bytes, as long as $\overline{ATN}$ remains HIGH. *(Figure 16.)*

Fig. 4 Status Bit Driven Direct by RQS

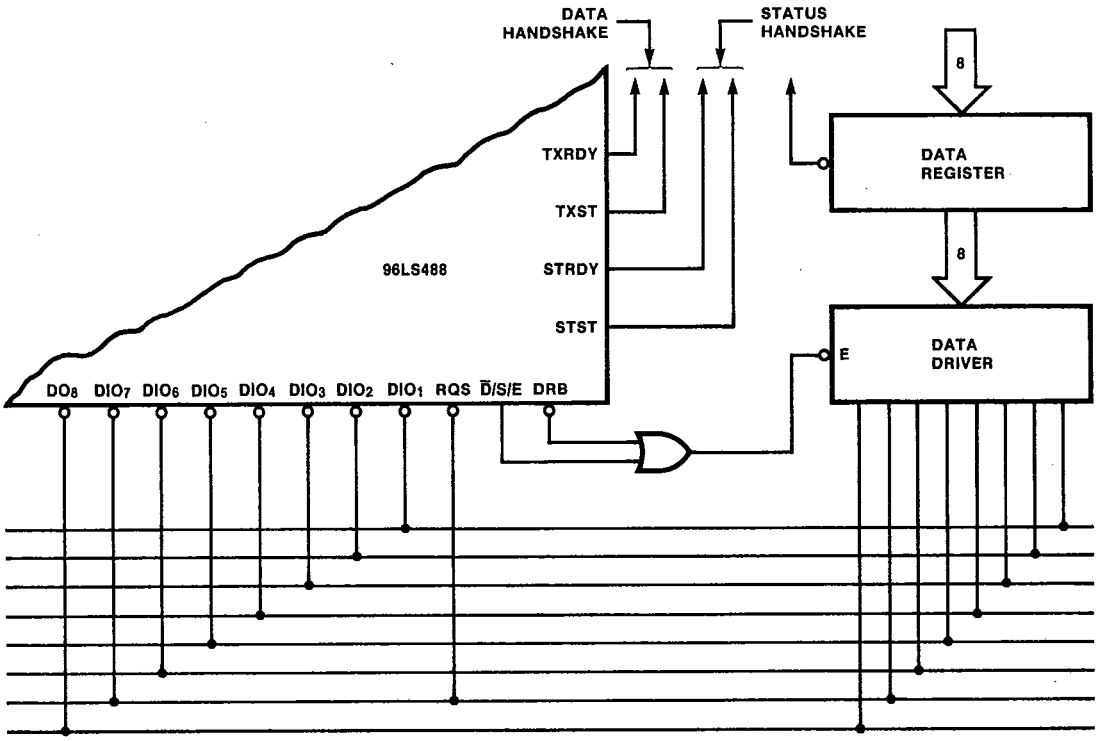
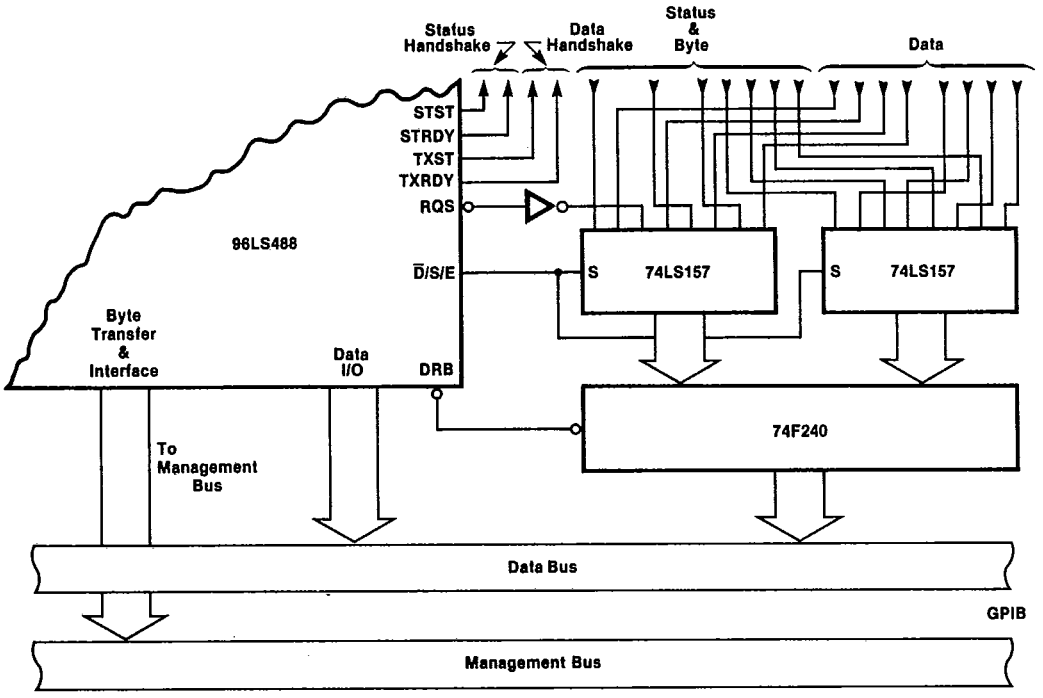


Fig. 5 Status Byte Multiplexing



Clock Input

The $\overline{CP}$ and XTAL inputs allow the 96LS488 either to accept external clock pulses or to generate its own clock. (See *Figure 6.*)

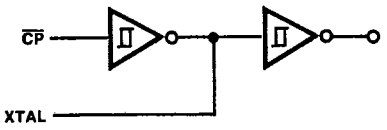
(a) An external clock can drive $\overline{CP}$. The XTAL pin may be used as an inverted buffered version of the external clock.

(b) The Schmitt-trigger buffer-inverter between the $\overline{CP}$ and XTAL pins can be used as a relaxation oscillator by connecting an RC network to provide feedback. The frequency of oscillation is variable up to 10 MHz. XTAL may be used to clock external circuits provided it is buffered.

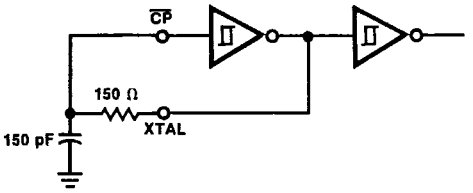
(c) The $\overline{CP}$ and XTAL pins will form a stable crystal oscillator by connecting a 10 MHz crystal and an RC network to provide positive feedback. XTAL may be used to clock external circuits provided it is buffered.

Fig. 6 Clock Timing Component Connections

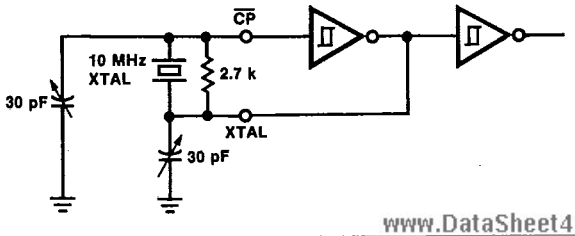
a



b



c



Timing Sequences

A 10 MHz clock frequency is recommended to give the correct Source Handshake delays. The 96LS488 can be clocked at a slower rate if the GPIB is not running at its maximum data rate of 1M byte. The lowest clock frequency allowable is dependent on the GPIB speed.

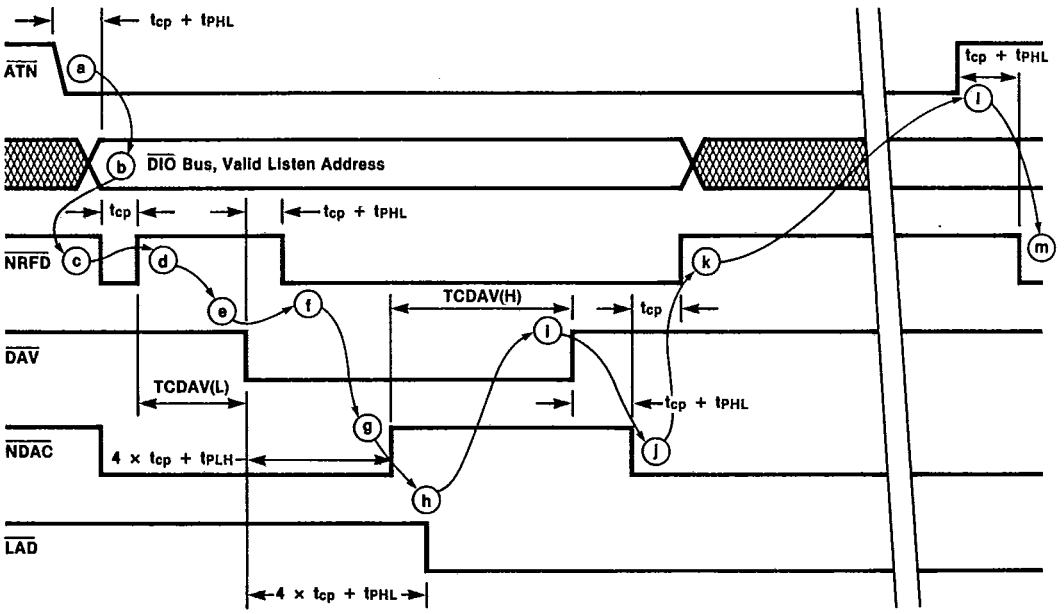
Regardless of clock frequency, the 96LS488 will respond to $\overline{ATN}$ within 200 ns by disabling $\overline{NRFD}$, $\overline{NDAC}$ and $\overline{DAV}$ while forcing $\overline{DRB}$ HIGH to disable the data drivers. In Parallel Poll sequences the relevant $\overline{DIO}$ line will be enabled or disabled within 200 ns of an IDY transition.

Since the internal logic of the 96LS488 is synchronous with the $\overline{CP}$ input, while in general all inputs are asynchronous, the precise timing of all responses to external signals is subject to a maximum uncertainty equal to one clock period. This is illustrated in the following timing diagrams, where some delays are defined as $t_{cp} + t_x$ (i.e., clock period + propagation delay).

Listen Address Sequence (See *Figure 7*)

a. Controller takes $\overline{ATN}$ line LOW followed by
b. putting the Listen address on the GPIB
c. Within ($t_{cp} + t_{PHL}$) the 96LS488 takes $\overline{NRFD}$ and $\overline{NDAC}$ LOW
d. and a t_{cp} later takes $\overline{NRFD}$ HIGH, indicating that the 96LS488 is ready for data
e. After a delay TCDAV(L) (determined by the Controller logic) the Controller takes $\overline{DAV}$ LOW
f. Within ($t_{cp} + t_{PHL}$) the 96LS488 takes $\overline{NRFD}$ LOW and
g. 3 clock periods later $\overline{NDAC}$ goes HIGH, indicating that the 96LS488 has accepted the data
h. followed by $\overline{LAD}$ indicating listen addressed status
i. After a Controller dependent delay, TCDAV(H), the $\overline{DAV}$ line goes HIGH and
j. within ($t_{cp} + t_{PHL}$) the 96LS488 takes $\overline{NDAC}$ LOW
k. A t_{cp} later the 96LS488 allows $\overline{NRFD}$ to go HIGH. $\overline{NRFD}$ stays HIGH until the Controller takes $\overline{ATN}$ HIGH, unless a further command is sent over the GPIB when a similar handshake sequence takes place
l. $\overline{ATN}$ goes HIGH followed by
m. $\overline{NRFD}$ going LOW within ($t_{cp} + t_{PHL}$). This occurs if the instrument is not ready to receive data (RXRDY LOW). If RXRDY is HIGH, $\overline{NRFD}$ will stay HIGH allowing a data transfer to take place

Fig. 7 Timing Diagram for Listen Address Sequence



Note: $\overline{ATN}$, $\overline{DIO}$ Bus & $\overline{DAV}$ driven by controller
$\overline{NRFD}$, $\overline{NDAC}$ Driven by 96LS488

Data Transfer from Bus to Listener (See *Figure 8*)
Assuming the instrument logic responds to RXST within one clock period. (See *Figure 8a.*)

a. The instrument signals it is ready to receive a byte by taking RXRDY HIGH (keeping RXRDY LOW constitutes an "$\overline{\text{NRFD}}$ hold").
b. Provided the 96LS488 is in the Listen Addressed State (LADS), $\overline{\text{NRFD}}$ is taken HIGH within (t_{cp} + t_{PHL})
c. When the current Talker sees the $\overline{\text{NRFD}}$ line HIGH it takes $\overline{\text{DAV}}$ LOW after a settling delay TTDAV(L).
d. The 96LS488 takes RXST HIGH within (t_{cp} + t_{PLH}) to inform the instrument that the GPIB data is valid and takes $\overline{\text{NRFD}}$ LOW
e. Assuming the instrument responds by pulsing RXRDY LOW within one clock period (t_{PRX} < t_{cp}) then RXST will remain HIGH only for one clock
f. At the same time as RXST returns LOW, $\overline{\text{NDAC}}$ is taken HIGH to inform the Talker that data has been accepted
g. After a delay TTDAV(H) determined by the Talker the $\overline{\text{DAV}}$ line goes HIGH
h. Within (t_{cp} + t_{PHL}) $\overline{\text{NDAC}}$ goes LOW
i. Followed by $\overline{\text{NRFD}}$ going HIGH one clock later

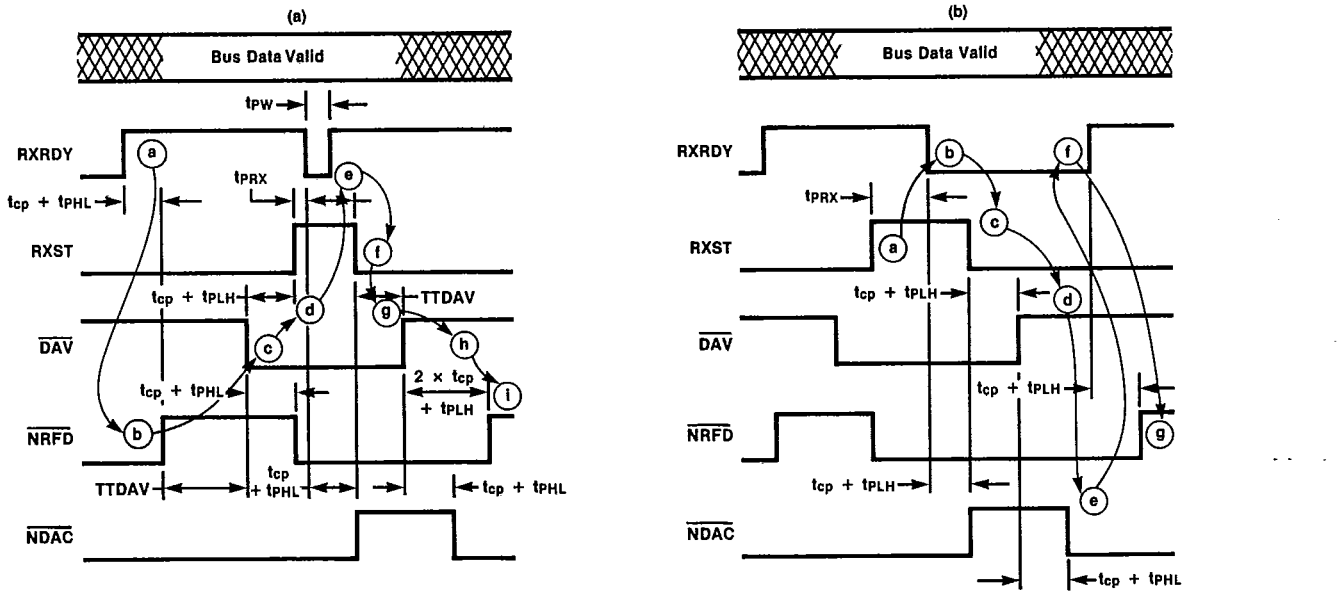
Note
In applications where the bus data can be latched by the RXST rising edge and handshaking is not necessary, RXRDY can be driven by RXST via an Inverter.

Assuming the instrument logic is slow and requires more than one clock period to process a data byte. (See *Figure 8b.*)

The timing sequence is identical to *Figure 8a* until RXST goes HIGH

a. After RXST goes HIGH the instrument delays t_{PRX} (>1 clock cycle) before taking RXRDY LOW
b. RXST will remain HIGH and $\overline{\text{NDAC}}$ will remain LOW during this period, causing the bus data to be maintained valid
c. RXST goes LOW, and $\overline{\text{NDAC}}$ goes HIGH within (t_{cp} + t_{PHL}) of RXRDY
d. After a delay TTDAV(H) the Talker takes $\overline{\text{DAV}}$ HIGH
e. Within (t_{cp} + t_{PHL}) $\overline{\text{NDAC}}$ goes LOW
f. Assuming the instrument is not ready (i.e., is holding RXRDY LOW) the 96LS488 holds $\overline{\text{NRFD}}$ LOW preventing another data transfer from starting
g. Within (t_{cp} + t_{PLH}) of RXRDY going HIGH, $\overline{\text{NRFD}}$ goes HIGH and the next data transfer cycle can start

Fig. 8 Timing Diagram, Data Transfer from Bus to Listener



Data Transfer from Talker to GPIB (See *Figure 9*)

a. $\overline{ATN}$ goes HIGH after completion of a Talk address sequence; $\overline{TAD}$ (not shown) is already LOW.

b. Within (t_{cp} + t_{PHL}) $\overline{DRB}$ goes LOW to enable the bus drivers

c. At a time determined by the instrument logic, TXRDY goes HIGH

d. If $\overline{NRFD}$ is already HIGH, the 96LS488 drives $\overline{DAV}$ LOW after delay T1 (11 × t_{cp} + t_{PHL} in high or 20 × t_{cp} + t_{PHL} in low speed). If $\overline{NRFD}$ is LOW, $\overline{DAV}$ will stay HIGH until $\overline{NRFD}$ goes HIGH (assuming T1 has expired). The $\overline{DAV}$ LOW period corresponds to the Source Transfer State (STRS).

e. The Listener(s) respond by eventually taking $\overline{NDAC}$ HIGH

f. Within (t_{cp} + t_{PLH}) 96LS488 takes $\overline{DAV}$ HIGH and TXST HIGH to inform the instrument that the data has been accepted and a new byte can be presented.

g. The instrument takes TXRDY LOW and holds it there until it has provided a new byte, h or h'. The minimum time TXRDY must be LOW is t_{PWL}

h. If TXRDY pulses LOW within t_{cp} of TXST, TXST(H) will be a minimum of t_{cp} wide. Otherwise TXST goes LOW within (t_{cp} + t_{PHL}) of TXRDY,j. After the first byte is sent, T1 drops from 11 × t_{cp} to 5 × t_{cp} in high speed mode.

i. If TXRDY is HIGH before $\overline{NRFD}$, $\overline{DAV}$ goes LOW within T2 of $\overline{NRFD}$ going HIGH (5 × t_{cp} in high speed or 20 × t_{cp} in low speed)

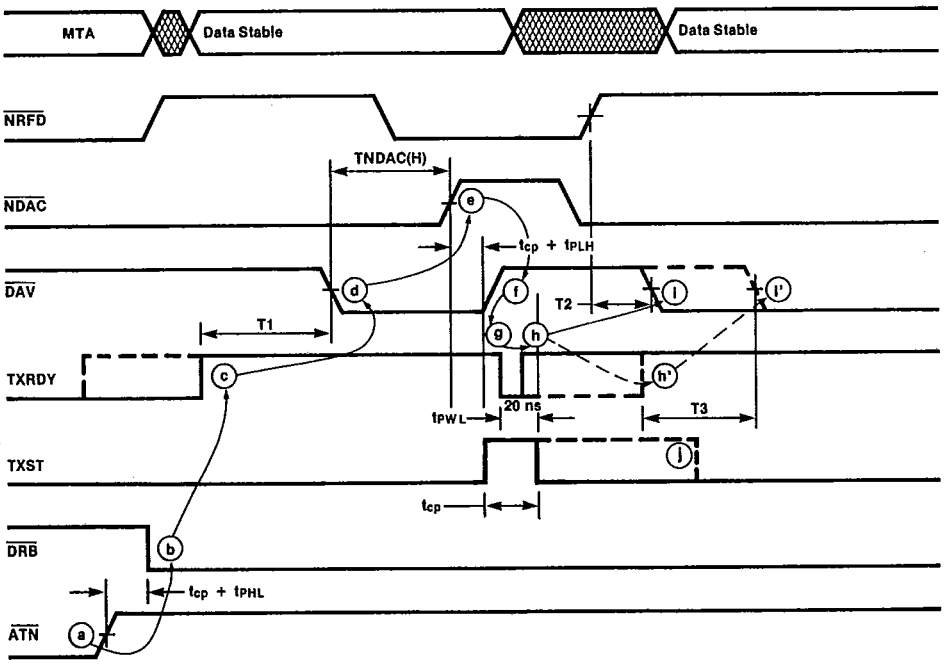
If TXRDY does not go HIGH until h' (after $\overline{NRFD}$ goes HIGH) $\overline{DAV}$ goes LOW T3 later,i'. (T3 = 6 × t_{cp} in HIGH and 21 × t_{cp} in low speed).

If the Talk sequence is interrupted by $\overline{ATN}$, while the instrument is generating a new byte, (between f and h), $\overline{DRB}$ will go HIGH within 200 ns and the $\overline{DAV}$ line will be relinquished. $\overline{DRB}$ will return LOW and the sequence will continue within (t_{cp} + t_{PLH}) of $\overline{ATN}$ going HIGH. If the 96LS488 is in high speed mode the first data byte sent will have a delay T1 = 11 × t_{cp}.

Note

In order to get the source handshake delays specified in IEEE Stad 488 - 1978, t_{cp} must be 100 ns (f_{clock} = 10 MHz).

Fig. 9 Timing Diagram Data Transfer from Talker to Bus



Notes

$\overline{NRFD}$, $\overline{NDAC}$ are driven by the current listener(s) $\overline{DAV}$ is driven by 96LS488.
T1 = 11 × t_{cp} + t_{PHL} in high speed, 20 × t_{cp} + t_{PHL} in low speed
T2 = 5 × t_{cp} + t_{PHL} in high speed, 20 × t_{cp} + t_{PHL} in low speed
T3 = 6 × t_{cp} + t_{PHL} in high speed, 21 × t_{cp} + t_{PHL} in low speed

Talk Address Sequence (See *Figure 10*)
This is similar to the Listen address sequence.

Fig. 10 Talk Address Sequence

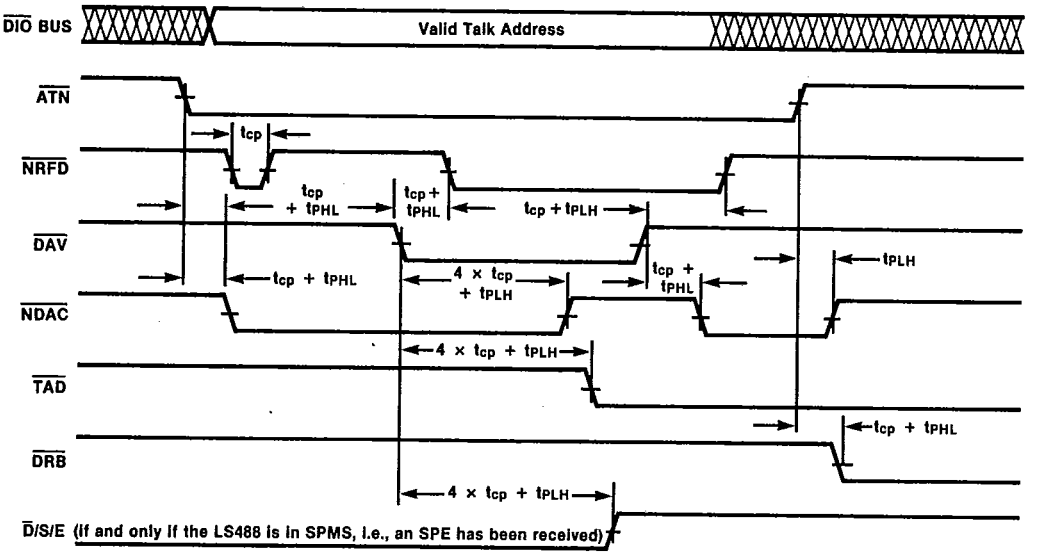


Fig. 11 Timing Diagram for Secondary Address Sequence

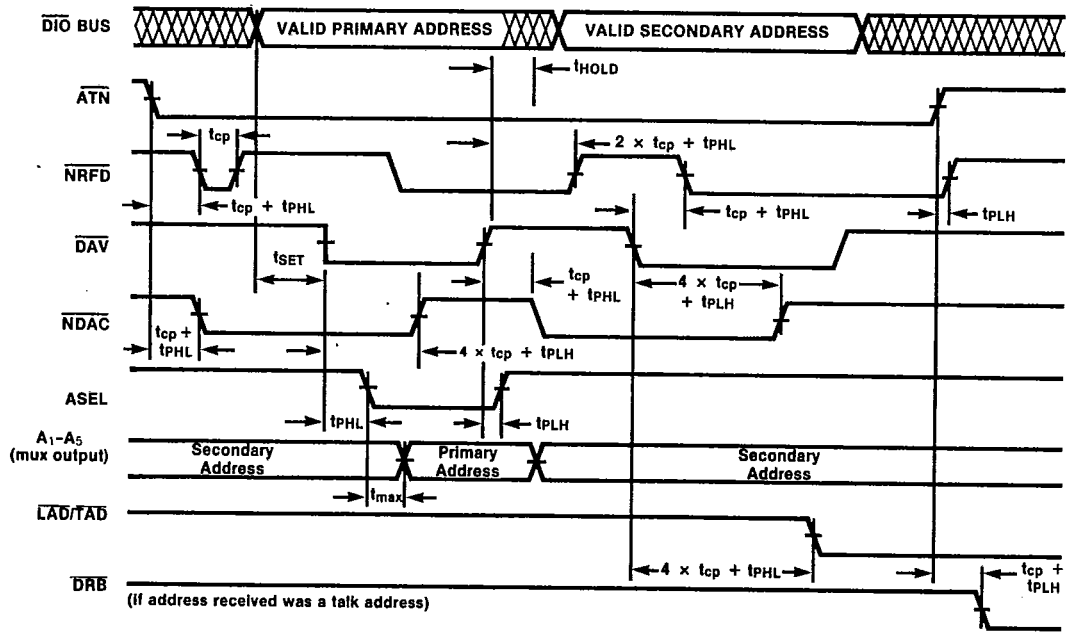
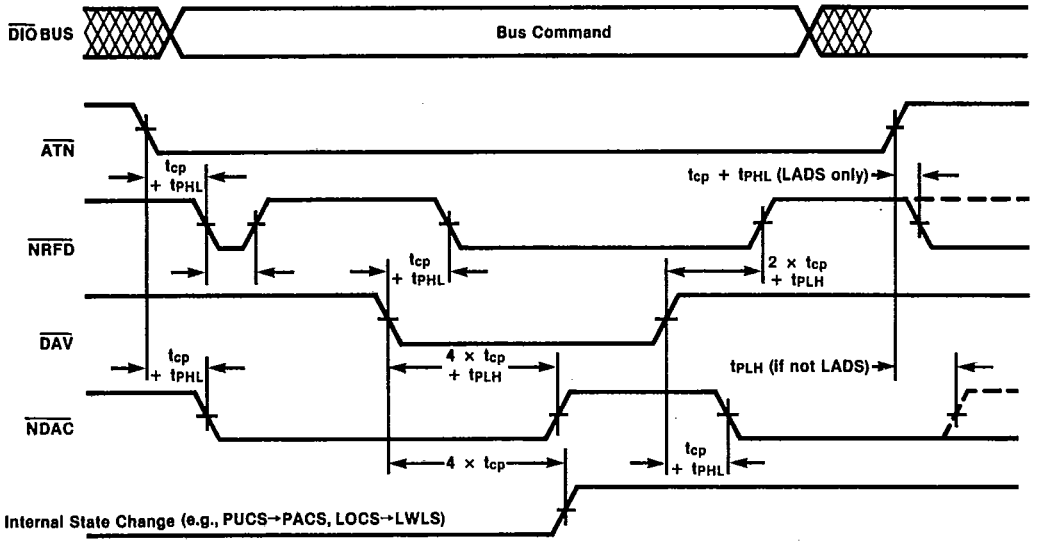


Fig. 12 Timing Diagram for 96LS488 Receiving Bus Commands



Note
Internal state changes do not necessarily change any 96LS488 outputs.

Fig. 13 Timing Diagram for Device Clear and Device Trigger Commands

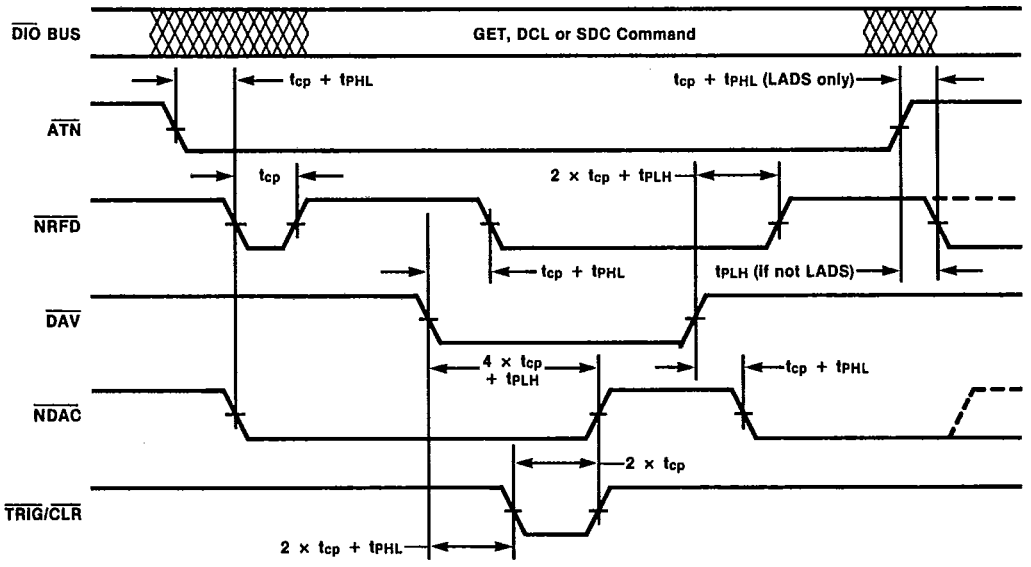
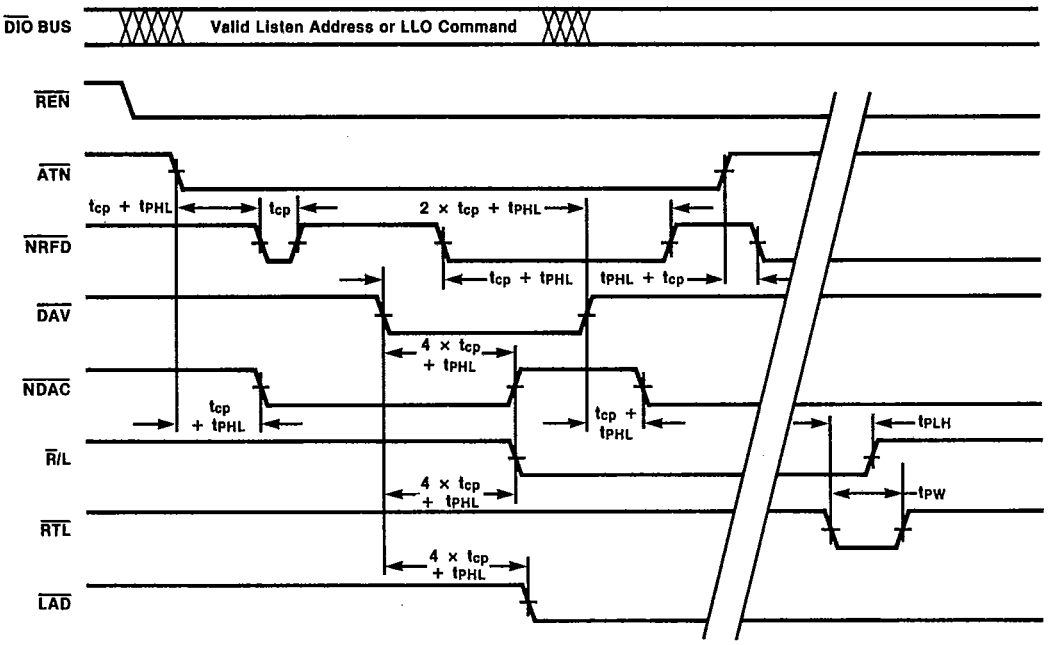
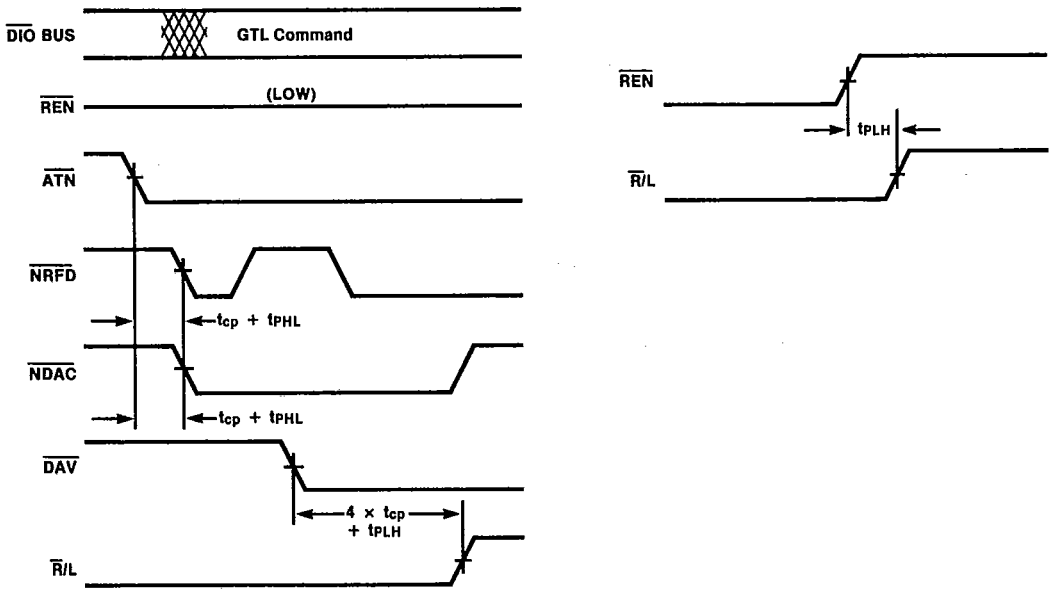


Fig. 14 Timing Diagram for Remote/Local Logic (Starting in LOCAL State)



Note
If LLO has been sent, $\overline{RTL}$ will not cause $\overline{R}/L$ to change.

Fig. 15 Timing Diagram for Remote/Local Logic (Starting in REMOTE State)



Serial Poll Sequence (See *Figure 16*)

a. The Controller has sent the Unlisten (UNL) and Serial Poll Enable (SPE) commands, generally in response to a LOW signal on $\overline{SRQ}$, and places a Talk address on the GPIB. The 96LS488 is sending the Service Request ($\overline{SRQ}$) message, which was caused by the instrument logic making $\overline{RSV}$ LOW.

b. The 96LS488 allows $\overline{NRFD}$ to float passive HIGH to initiate normal handshake routine.

c. The Controller forces $\overline{DAV}$ LOW. Since $\overline{ATN}$ is also LOW, the 96LS488 receives the GPIB information as the message My Talk Address (MTA)

d. $\overline{NRFD}$ is active, acknowledging that the device is receiving a data byte

e. The 96LS488 enters the Talker Addressed State at time ($4 \times t_{cp} + t_{PHL}$) after $\overline{DAV}$ was forced LOW

f. $\overline{D}$/S/E goes HIGH at time ($4 \times t_{cp} + t_{PLH}$) after $\overline{DAV}$ was forced LOW. This indicates that the 96LS488 is in the Serial Poll Mode.

g. $\overline{NDAC}$ is allowed to float passive HIGH, indicating that the command data byte has been received

h. The Controller takes $\overline{DAV}$ HIGH

i. $\overline{NDAC}$ is pulled LOW, showing that the 96LS488 is ready for a new handshake cycle

j. The Controller allows the bus to float

k. The Controller releases $\overline{ATN}$. Because the 96LS488 is in the Serial Poll Mode, it now enters the Serial Poll Active State (SPAS), which prevails until the Controller makes $\overline{ATN}$ LOW again.

l. $\overline{DRB}$ goes active LOW, allowing the instrument to place its status byte on the bus. $\overline{DRB}$ goes LOW at time ($t_{cp} + t_{PHL}$) after $\overline{ATN}$ goes HIGH

m. When the 96LS488 enters SPAS, $\overline{SRQ}$ goes HIGH at time t_{PLH} after $\overline{ATN}$ goes HIGH

n. The instrument indicates that a status byte is ready by taking STRDY HIGH. This may occur earlier than shown, without affecting any of the foregoing

o. $\overline{DRB}$ enables the 3-state output $\overline{RQS}$ when in SPAS. $\overline{RQS}$ goes LOW at time ($t_{cp} + t_{PZL}$) after $\overline{ATN}$ is released

p. The Controller has taken $\overline{NRFD}$ HIGH, acknowledging that it is ready for the status byte

q. The 96LS488 takes $\overline{DAV}$ LOW after the time interval T_1, which starts either at the rising edge of STRDY or the falling edge of $\overline{DRB}$, whichever occurs later. The $\overline{DAV}$ LOW period corresponds to the Source Transfer State (STRS).

r. The Controller takes $\overline{NRFD}$ LOW

s. The instrument may release $\overline{RSV}$ at any time after the 96LS488 enters SPAS

t. The Controller takes $\overline{NDAC}$ HIGH, acknowledging that it has received the status byte

u. The 96LS488 releases $\overline{DAV}$ at time ($t_{cp} + t_{PLH}$) after $\overline{NDAC}$ goes HIGH

v. STST goes HIGH at time ($t_{cp} + t_{PLH}$) after $\overline{NDAC}$ goes HIGH. This tells the instrument that the status byte has been accepted. The instrument takes STRDY LOW to indicate that the data is no longer valid and to allow STST to go LOW again one t_{cp} after STRDY goes LOW

w. The Controller takes $\overline{NDAC}$ LOW once more after $\overline{DAV}$ goes HIGH

x. The data on the bus is no longer valid. If the $\overline{ATN}$ line remains HIGH, the instrument can provide another status byte by making STRDY HIGH to indicate valid data and to start the handshake

y. At the completion of the Serial Poll of this instrument, the Controller assumes control of the bus by forcing $\overline{ATN}$ LOW

z. $\overline{DRB}$ goes HIGH at time t_{PLH} after $\overline{ATN}$ goes LOW. This places the bus drivers of this instrument in the high-impedance (3-state output) or off (open-collector outputs) state

aa. Since $\overline{DRB}$ is no longer valid, the $\overline{RQS}$ output reverts to its high-impedance state

bb. $\overline{NRFD}$ goes HIGH, indicating that devices are ready to receive a command from the bus

cc. The Controller forces $\overline{DAV}$ LOW to show that it has placed a control byte on the bus

dd. $\overline{NRFD}$ goes LOW to acknowledge $\overline{DAV}$

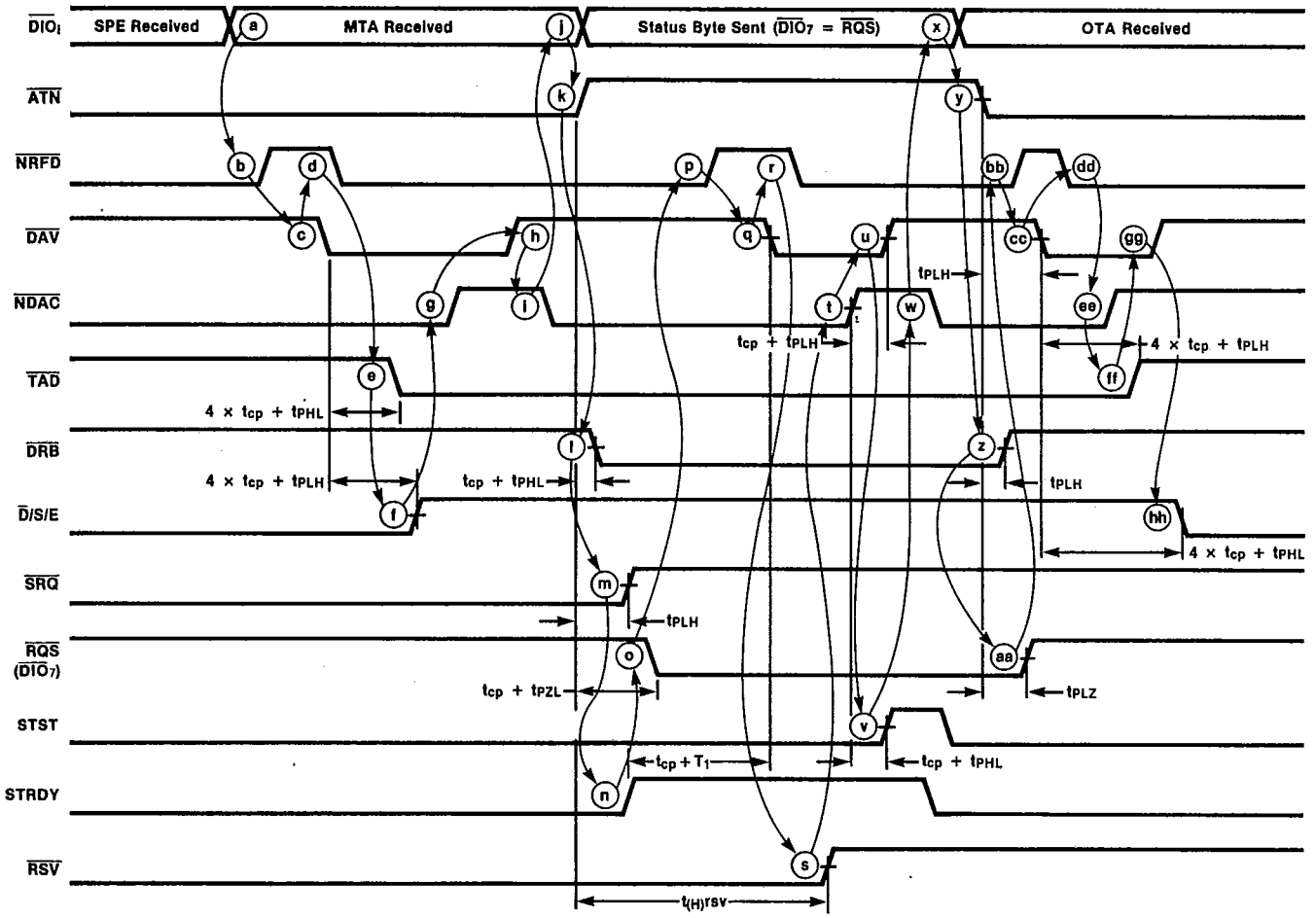
ee. $\overline{NDAC}$ goes HIGH when devices all acknowledge acceptance of the command byte

ff. The 96LS488 has received the Other Talk Address (OTA) command and reverts to its unaddressed state. $\overline{TAD}$ goes HIGH at time ($4 \times t_{cp} + t_{PLH}$) after $\overline{DAV}$ went LOW

gg. $\overline{DAV}$ is set HIGH by the Controller

hh. Because the 96LS488 has been unaddressed it is no longer in the Serial Poll Active State (SPAS). The $\overline{D}$/S/E output goes LOW at time ($4 \times t_{cp} + t_{PHL}$) after $\overline{DAV}$ went HIGH. The 96LS488 is still in the Serial Poll Mode State (SPMS), however, and will return to SPAS ($\overline{D}$/S/E HIGH, STST and STRDY valid) if subsequently addressed to talk. The 96LS488 enters the Serial Poll Idle State (SPIS) when the Controller either issues the Serial Poll Disable (SPD) command or makes $\overline{IFC}$ LOW.

Fig. 16 Timing Diagram for Serial Poll Sequence



Parallel Poll Sequence (See *Figure 17*)

a. The Controller sends the instrument's listen address

b. Then Controller issues the Parallel Poll Configure command: this enables the 96LS488 to receive a subsequent PPE command.

c. The Controller issues the Parallel Poll Enable command. Bits $\overline{D}_1$–$\overline{D}_3$ of the command byte determine which data output ($\overline{DIO}_j$) will be valid when the IDY command is sent. Bit $\overline{D}_4$ of the command is compared with IST (Instrument Status) during the IDY command.

d. The Controller issues the Unlisten command. The 96LS488 will now not respond to further PPE commands, allowing the Controller to configure other instruments.

e. The Instrument Status bit (IST) is set by the instrument before an IDENTIFY command is received. IST must be in a stable state when IDY is received so the setup and hold times must be observed (t_s IST and t_h IST).

f. During the IDY command the Controller releases the data lines $\overline{DIO}_1$–$\overline{DIO}_7$, $\overline{DO}_8$. The assigned data line $\overline{DIO}_j$ will be taken active LOW by the 96LS488 if IST compares with bit $\overline{D}_4$ of the PPE command.

g. The IDY message is received (IDY = $\overline{EOI} \cdot \overline{ATN}$). At this time the Instrument Status bit IST is latched in the 96LS488, and the output data $\overline{DIO}_j$ is true if IST compares with bit $\overline{D}_4$ of the PPE command. $\overline{DIO}_j$ is LOW if $\overline{D}_4$ was LOW and IST was HIGH, or if $\overline{D}_4$ was HIGH and IST was LOW.

h. The 96LS488 enables data bit $\overline{DIO}_j$ after a delay t_{PHL} from the time $\overline{EOI}$ goes active LOW. $\overline{DIO}_j$ remains valid while IDY is active. Note that this is an asynchronous message sent and is not governed by the handshake protocol.

i. IST may be altered not less than time t_h IST after IDY is active. Because IST is latched by IDY it will not affect the status byte sent during this IDY routine.

j. IDY is false and the 96LS488 stops sending a status byte. Outputs $\overline{DIO}_1$-$\overline{DIO}_7$, $\overline{DO}_8$ again float passive HIGH.

k. The status bit $\overline{DIO}_j$ floats passive HIGH at a time not greater than t_{PLH} after IDY goes FALSE.

l. The Controller can now place information on the data bus.

m. Once the 96LS488 has been configured via steps a-c, the Controller can examine IST at any time by issuing the IDY command. To change the $\overline{D}_1$-$\overline{D}_4$ assignment of a particular 96LS488, the Controller must address it to listen, issue the PPC command, then the Parallel Poll Disable (PPD) command (which clears the $\overline{D}_1$-$\overline{D}_4$ latches), then the PPE command with the revised $\overline{D}_1$-$\overline{D}_4$ assignment. The $\overline{D}_1$-$\overline{D}_4$ assignment will also be cleared by the universal Parallel Poll Unconfigure (PPU) command or by $\overline{MR}$, but not by $\overline{IFC}$. PPU, $\overline{MR}$ or the MLA/PPC/PPD sequence puts the 96LS488 in the Parallel Poll Idle State (PPIS) and it will not respond to IDY until it is subsequently reconfigured.

Fig. 17 Timing Diagram for Parallel Poll Sequence

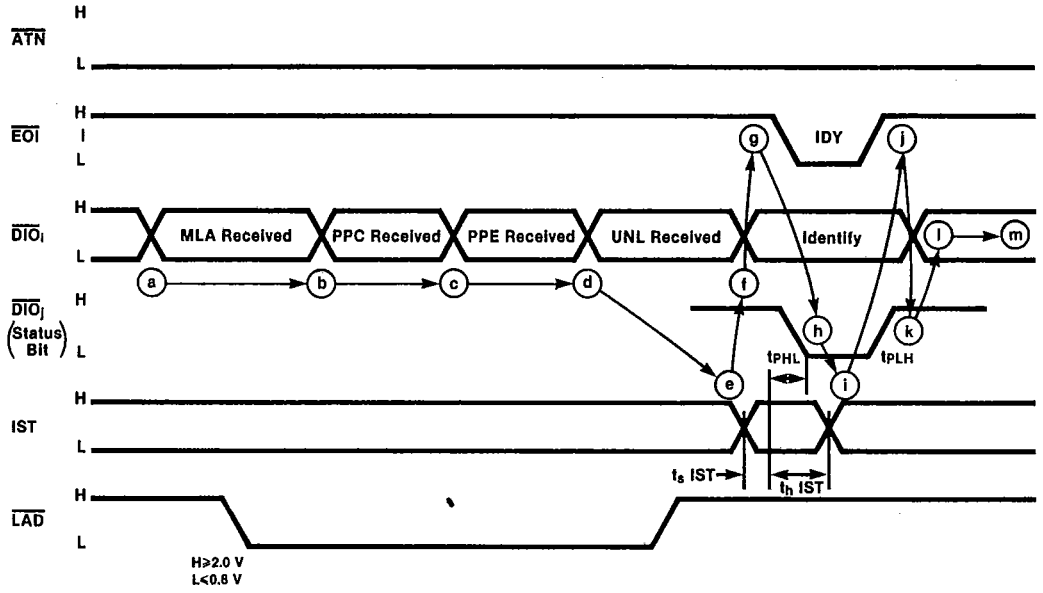
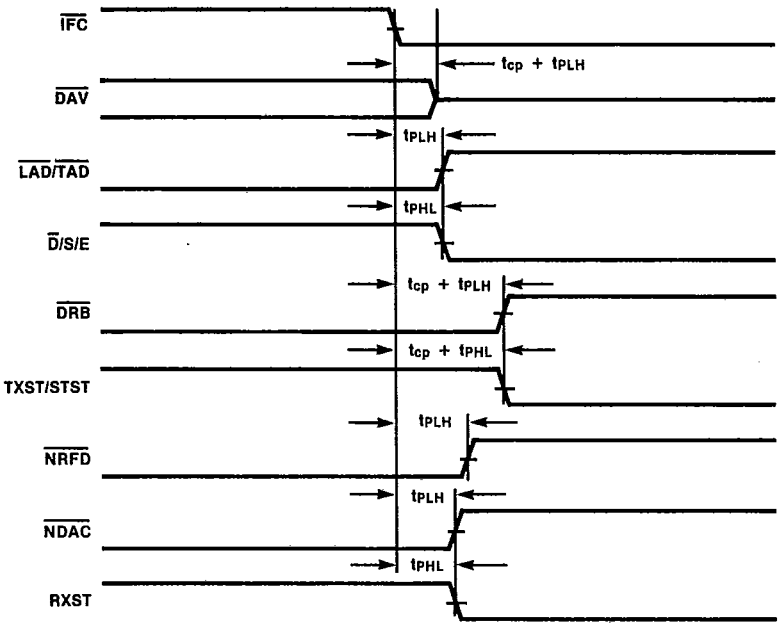


Fig. 18 IFC Timing Diagram



Absolute Maximum Ratings
(above which the useful life may be impaired)

Storage Temperature	−65 °C to +150 °C
Temperature (Ambient) Under Bias	−55 °C to +125 °C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

DC Characteristics

Symbol	Parameter	Min	Max	Unit	V_{CC}	Condition
V_{IH}	Input HIGH Voltage All Inputs	2.0		V		Recognized as a HIGH Signal Over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage DM All Inputs DC		0.7 0.8	V		Recognized as a LOW Signal Over Recommended V_{CC} and T_A Range
$V_{T+}-V_{T-}$	Hysteresis Voltage	0.4		V		All Bus Inputs
V_{CD}	Input Clamp Diode Voltage		1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage $\overline{RQS}$, $\overline{DAV}$	2.5		V	Min	I_{OH} = −5.2 mA
	$\overline{DIO}_1 - \overline{DIO}_7$, $\overline{DO}_8$, $\overline{SRQ}$, $\overline{NRFD}$, $\overline{NDAC}$	2.5	3.7	V	Min	Open-Collector Bus Pins I_{OH} = 0 mA
	$\overline{R}$/L, $\overline{D}$/S/E, $\overline{RXST}$, $\overline{TXST}$, $\overline{STST}$, $\overline{CLR}$, $\overline{TRIG}$, $\overline{DRB}$, ASEL, XTAL, $\overline{LAD}$, $\overline{TAD}$	2.5		V	Min	I_{OH} = −0.4 mA
V_{OL}	Output LOW Voltage $\overline{DIO}_1 - \overline{DIO}_7$, $\overline{DO}_8$, $\overline{SRQ}$, $\overline{RQS}$, $\overline{NRFD}$, $\overline{NDAC}$, $\overline{DAV}$		0.5	V	Min	I_{OL} = 48 mA
	All Other Outputs DM, DC		0.4	V	Min	I_{OL} = 4.0 mA
	DC		0.5	V	Min	I_{OL} = 8.0 mA
I_{IH}	0.5 U.L. Input HIGH Current 1.0 U.L. n U.L.		20 40 n(40)	μA	Max	I_{IH} = 40 μA Multiplied by Input HIGH U.L. Shown on Data Sheet; V_{IN} = 2.7 V
I_{IL}	0.25 U.L. Input LOW Current 0.5 U.L. n U.L.		−0.4 −0.8 n(−1.6)	mA	Max	I_{IL} = −1.6 mA Multiplied by Input LOW U.L. Shown on Data Sheet; V_{IN} = 0.4 V
I_{POFS}	Leakage into GPIB Pins in Powered-off State		100	μA	0	V_{IN} = 2.5 V
I_{OZH}	3-State Output OFF Current HIGH		40	μA	Max	V_{OUT} = 2.4 V
I_{OZL}	3-State Output OFF Current LOW		−40	μA	Max	V_{OUT} = 0.4 V
I_{CC}	Power Supply Current	*	250	mA	Max	Any 3 Bus Outputs in LOW State

*Typical Value for I_{CC} is 180 mA.

AC Characteristics V_{CC} = 5.0 V, T_A = +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Fig. No.	Condition
f_{max}	Maximum Clock Frequency	12	15		MHz		For correct timing for SH or AH, $\overline{CP}$ must be 10 MHz.
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{NRFD}$		150 90		ns ns	7, 8, 10, 11 12, 13, 14	C_L = 300 pF, R_L = 200 Ω
t_{PLH}	Propagation Delay $\overline{ATN}$ to $\overline{NRFD}$		150		ns	11	C_L = 300 pF, R_L = 200 Ω
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{NDAC}$		150 90		ns ns	7, 8, 10, 11 12, 13, 14	C_L = 300 pF, R_L = 200 Ω
t_{PLH}	Propagation Delay $\overline{ATN}$ to $\overline{NDAC}$		150		ns	10, 12, 13	C_L = 300 pF, R_L = 200 Ω
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{DAV}$		100 90		ns ns	9	C_L = 300 pF, R_L = 200 Ω
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{ATN}$ to $\overline{DAV}$		100 100		ns ns	9	C_L = 300 pF, R_L = 200 Ω
t_{PZL} t_{PZH}	Output Enable Time $\overline{CP}$ to $\overline{DAV}$		100 100		ns ns	9	C_L = 300 pF, R_L = 200 Ω
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{CP}$ to $\overline{DAV}$		100 100		ns ns		C_L = 300 pF, R_L = 200 Ω
t_{PLH}	Propagation Delay $\overline{IFC}$ to $\overline{NRFD}$ or $\overline{NDAC}$		180		ns	18	C_L = 300 pF, R_L = 200 Ω
t_{PHL}	Propagation Delay $\overline{IFC}$ to RXST		160		ns	18	C_L = 15 pF
t_{PHL}	Propagation Delay, $\overline{IFC}$ to $\overline{D}$/S/E		100		ns	18	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{LAD}$ or $\overline{TAD}$		150 150		ns ns	7, 8, 10	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay $M_0 - M_3$ to $\overline{LAD}$ or $\overline{TAD}$		60 60		ns ns		C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to RXST, TXST or STST		75 75		ns ns	8, 9	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{DRB}$		85 85		ns ns	9, 11	C_L = 15 pF
t_{PLH}	Propagation Delay, $\overline{ATN}$ to $\overline{DRB}$		70		ns	9	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{TRIG}$ or $\overline{CLR}$		130 130		ns ns	13	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{DAV}$ to ASEL		25 25		ns ns	11	C_L = 15 pF

AC Characteristics V_{CC} = 5.0 V, T_A = +25°C (Cont'd)

Symbol	Parameter	Min	Typ	Max	Unit	Fig. No.	Condition
t_{PHL}	Propagation Delay, $\overline{MR}$ to RXST, TXST, STST, $\overline{D}$/S/E		100		ns		C_L = 15 pF
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{LAD}$, $\overline{TAD}$ or $\overline{R}$/L		50		ns		C_L = 15 pF
t_{PLH}	Propagation Delay, $\overline{MR}$ to $\overline{NRFD}$, $\overline{NDAC}$, $\overline{DAV}$, $\overline{DIO_1}$-$\overline{DIO_7}$, $\overline{DO_8}$ or $\overline{SRQ}$		100		ns		C_L = 300 pF, R_L = 200 Ω
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to XTAL		15 15		ns ns	6	C_L = 15 pF, $\overline{CP}$ driven from ext. oscillator
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to $\overline{R}$/L		150 150		ns ns	14, 15	C_L = 15 pF
t_{PLH}	Propagation Delay, $\overline{RTL}$ to $\overline{R}$/L		150		ns	14	C_L = 15 pF
t_{PLH}	Propagation Delay, $\overline{REN}$ to $\overline{R}$/L		45		ns	14	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to $\overline{D}$/S/E		140 140		ns ns	16	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, $\overline{RSV}$ to $\overline{SRQ}$		90 30		ns ns		C_L = 300 pF, R_L = 200 Ω
t_{PLH}	Propagation Delay, $\overline{ATN}$ to $\overline{SRQ}$		150		ns	16	C_L = 300 pF, R_L = 200 Ω
t_{PZL} t_{PZH}	Output Enable Time, $\overline{CP}$ to $\overline{RQS}$		100 100		ns ns	16	C_L = 300 pF, R_L = 200 Ω
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{ATN}$ to $\overline{RQS}$		85 85		ns ns	16	C_L = 300 pF, R_L = 200 Ω
t_{PLH} t_{PHL}	Propagation Delay $\overline{EOI}$ to $\overline{DIO_1}$-$\overline{DIO_7}$, $\overline{DO_8}$		110 50		ns ns	17	C_L = 300 pF, R_L = 200 Ω
t_{PLH} t_{PHL}	Propagation Delay $\overline{EOI}$ to $\overline{D}$/S/E		30 30		ns ns		C_L = 15 pF

AC Operating Requirements V_{CC} = 5.0 V, T_A = +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Fig. No.	Condition
t_s (L) t_s (H)	Setup Time, HIGH or LOW IST to $\overline{EOI}$	20 20			ns ns	17	
t_h (L) t_h (H)	Hold Time, HIGH or LOW IST to $\overline{EOI}$	5.0 5.0			ns ns	17	
t_s (L)	Setup Time, $\overline{RSV}$ to $\overline{ATN}$		−50		ns		Device about to enter SPAS on next L to H $\overline{ATN}$ transition.
t_h (L)	Hold Time, $\overline{RSV}$ to $\overline{ATN}$		−50		ns		Device about to enter SPAS on next L to H $\overline{ATN}$ transition.
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{DIO_1}$-$\overline{DIO_7}$ to $\overline{DAV}$	100 100			ns ns	11	
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{DIO_1}$-$\overline{DIO_7}$ to $\overline{DAV}$	0 0			ns ns	11	
t_m (H) t_m (L)	Delay in external address mux from ASEL to valid address			100 100	ns ns	11	
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width	30 30			ns ns		
t_w (L)	Pulse Width RXRDY, TXRDY or STRDY	20			ns	8, 9, 16	
t_w (L)	$\overline{MR}$ Pulse Width	50			ns		
t_w (L)	$\overline{RTL}$ Pulse Width	60			ns	14	

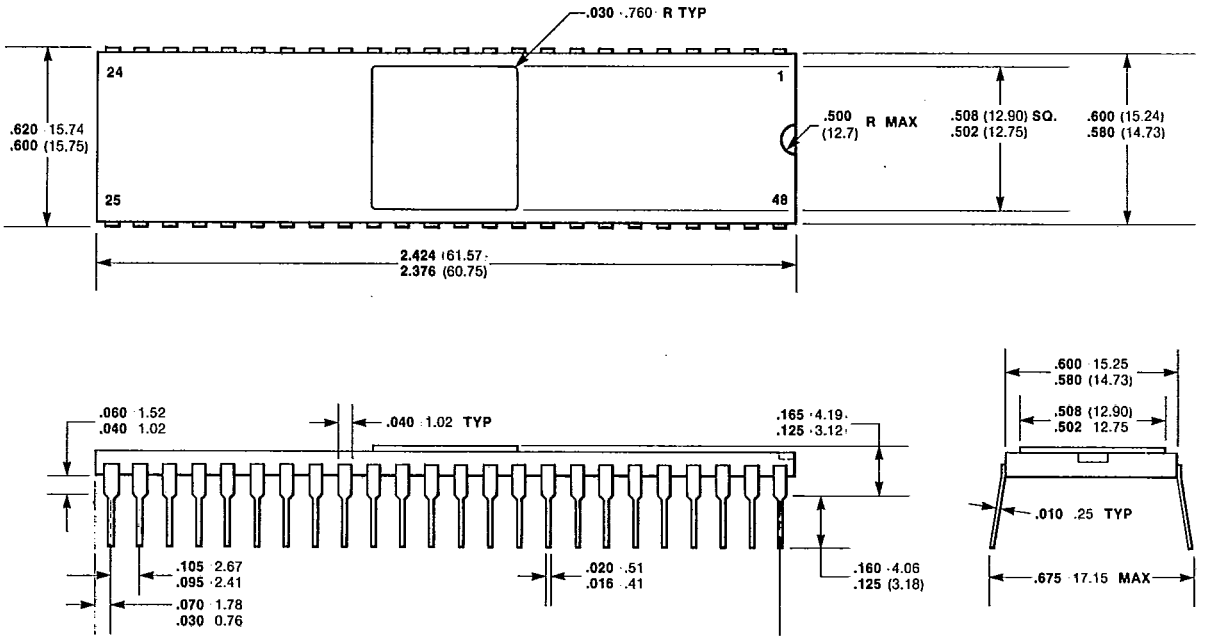
Ordering Information

Order Code	Package	Temperature*
96LS488DC	Ceramic DIP	Commercial
96LS488DM	Ceramic DIP	Military

*C = 0°C to +70°C
M = −55°C to +125°C

Package Outlines

48-Pin Side-brazed Package



Notes
All dimensions in inches **bold** and millimeters in parentheses
Pin material is nickel, gold-plated kovar or alloy 42
Cap is kovar or alloy 42
Base is ceramic
Cavity size is **.310 × .310** (7.874 × 7.874)
Package weight is 7.7 grams