Datasheet

8V97052

High Resolution Wideband RF Synthesizer / PLL

The 8V97052 is a high-performance wide-band RF synthesizer / PLL that offers a high resolution of 32-bit fractional and modulus. It is ideal for use in instrumentation, test equipment, satellite equipment, or applications that require very fine adjustments of the output frequency. It is also optimal for use as a traditional Local Oscillator (LO) in Multi-Carrier, Multi-mode FDD, and TDD Base Station radio card.

The 8V97052 offers an integrated Voltage Controlled Oscillator (VCO) and output divider that supports a continuous output frequency range of 34.375MHz to 4400MHz. This large frequency tuning range can provide multi-band local oscillator (LO) frequency synthesis, thus, limiting the use of multiple narrow band RF synthesizers and reducing the BOM complexity and cost. The RF_OUT output driver has an independently programmable output power ranging from -4dBm to +11.5dBm. The RF_OUT output can be muted via a SPI command or mute pin.

Integrated low noise Low Dropout Regulators (LDOs) are used for superior power supply noise immunity. The operation of the 8V97052 is controlled by writing to registers through a 3-wire SPI interface. The device also has an option that allows users to read back values from registers by configuring the MUX_OUT pin as a SDO for the SPI interface. The SPI interface is compatible with 1.8V logic and tolerant to 3.3V.

The device also includes features such as fast lock, programmable charge pump current, electable DSM types and orders, output mute, lock detection, MUX_OUT, and phase adjust that can help with specific system requirements, optimization, or power savings. In RF applications, very low noise oscillators are required to generate a large variety of frequencies to the mixers while maintaining excellent phase noise performance and low power.

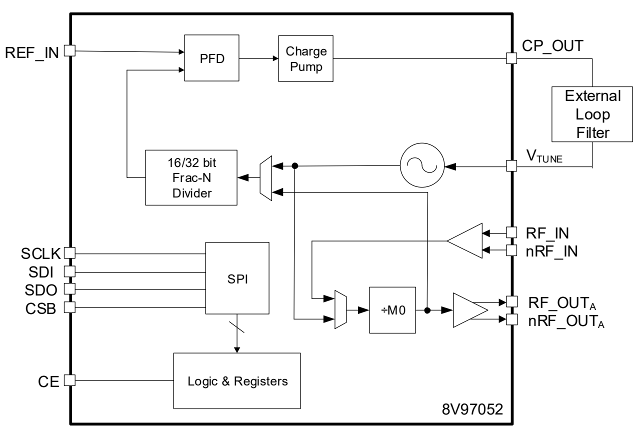
Applications

- Wireless infrastructure
- Instrumentation equipment
- Test equipment
- CATV equipment
- Military and aerospace
- Wireless LAN
- Clock generation

Features

- Supports on-chip VCO or external VCO
- Single differential output with frequency range: 34.375MHz to 4400MHz (continuous range)
- RF output divide by 1, 2, 4, 8, 16, 32, 64
- Open drain output (see Output Distribution Section)
- Fractional-N synthesizer (also supports Integer-N mode)
- 16-bit integer and 32-bit fractional/32-bit modulus
- 3- or 4-wire SPI interface (compatible with 3.3V and 1.8V)
- Single 3.3V supply
- Programmable output power level: -4dBm to +11.5dBm
- Mute function
- Ultra low phase noise for 2GHz LO: -133dBc/Hz at 1MHz offset, (typical)
- Normalized phase noise floor: -228dBc/Hz
- Lock detect Indicators
- Input reference frequency: 5MHz to 310MHz
- Power consumption: 380mW (typical)
- 5 × 5 mm, 32-VFQFPN package
- Automatic VCO band selection (Autocal feature)
- -40°C to +85°C ambient operating temperature
- Supports case temperature ≤ 105°C operations
- Lead-free (RoHS 6) packaging

Simplified Block Diagram



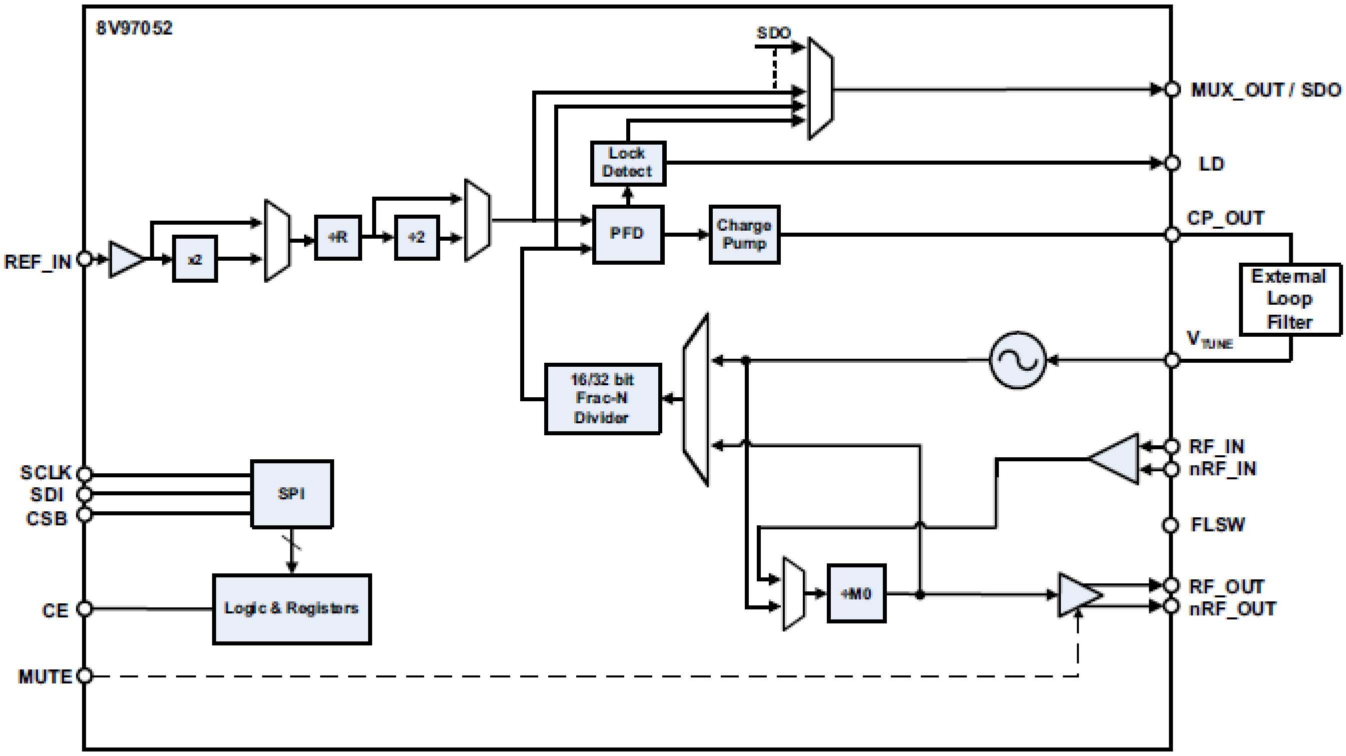
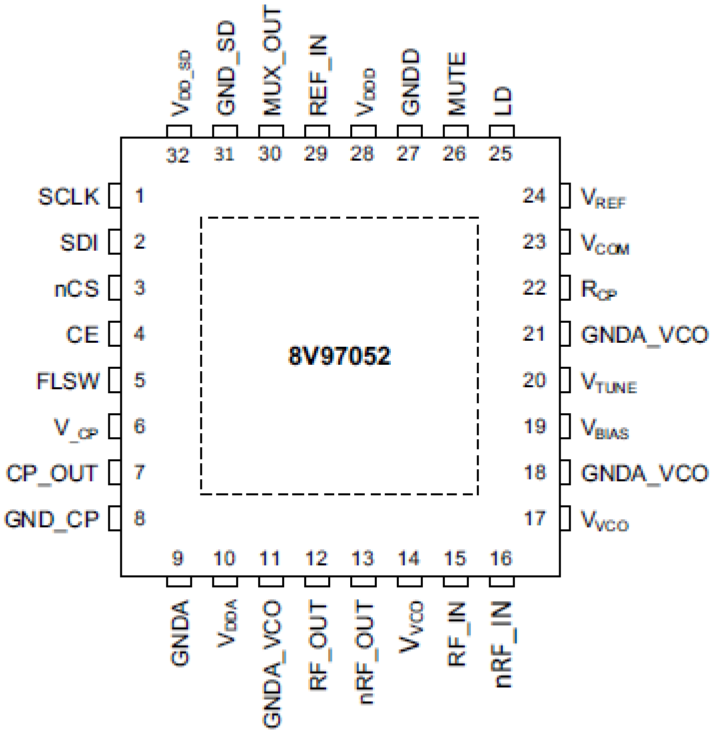


Figure 1. Block Diagram

Contents

1. Pin Information

1.1 Pin Assignments



1.2 Pin Descriptions

Table 1. Pin Descriptions[1]

Pin	Name	Type		Description
1	SCLK	LVCMOS input	Pull-down	Serial clock input. High-Impedance CMOS input. 1.8V logic. 3.3V tolerant.
2	SDI	LVCMOS input	Pull-up	Serial data input. High-Impedance CMOS input. 1.8V logic. 3.3V tolerant.
3	nCS	LVCMOS input	Pull-down	Load enable. High-Impedance CMOS input. 1.8V logic. 3.3V tolerant. Active low.
4	CE	LVCMOS input	Pull-up	Chip enable. On logic low, powers down the device and puts the charge pump into High-Impedance mode. Powers up the device on logic High.
5	FLSW	Analog		Fast lock switch. A connection should be made from the loop filter to this pin when using the fast lock mode.
6	$V_{\_CP}$	Power		Charge pump power supply. $V_{\_CP}$ must have the same value as V_{DDA}. Place decoupling capacitors to the ground plane as close to this pin as possible.
7	CP_OUT	Analog		Charge pump output. When enabled, this output provides ±ICP to the external loop filter. The output of the loop filter is connected to V_{TUNE} to drive the internal VCO.
8	GND_CP	Ground		Charge pump power supply ground.
9	GNDA	Ground		VCO analog power supply ground.
10	V_{DDA}	Power		Analog supply. This pin ranges from 3.3V ±5%. V_{DDA} must have the same value as V_{DDD}.

Table 1. Pin Descriptions[1] (Cont.)

Pin	Name	Type		Description
11	GNDA_VCO	Ground		VCO analog power supply ground.
12	RF_OUT	Output		RF output pair. The output level is programmable.
13	nRF_OUT	Output		RF output pair. The output level is programmable.
14, 17	V_{VCO}	Power		VCO supply. This pin ranges from 3.3V ±5%. V_{VCO} must have the same value as V_{DDA}.
15	RF_IN	Input		RF input pair.
16	nRF_IN	Input		RF input pair.
18	GNDA_VCO	Ground		VCO analog power supply ground.
19	V_{BIAS}	Analog		Place decoupling capacitors (≥0.1µF) to ground, as close to this pin as possible.
20	V_{TUNE}			Control input to tune the VCO.
21	GNDA_VCO	Ground		VCO analog power supply ground.
22	R_{CP}	Analog		Sets the charge pump current. Requires external resistor.
23	V_{COM}	Analog		Place decoupling capacitors (≥0.1µF) to ground, as close to this pin as possible.
24	V_{REF}	Analog		Place decoupling capacitors (≥0.1µF) to ground, as close to this pin as possible.
25	LD	LVCMOS output		Lock detect. Logic high indicates PLL lock. Logic low indicates loss of PLL lock.
26	MUTE	LVCMOS input	Pull-up	RF_OUT_A power-down. A logic low on this pin mutes the RF_OUT outputs and puts them in High-Impedance.
27	GNDD	Ground		Digital power supply ground.
28	VDDD	Power		Digital supply. V_{DDD} must have the same value as V_{DDA}.
29	REF_IN	LVCMOS input	Analog	Reference input. This CMOS input has a nominal threshold of $V_{DDA}/2$ and a DC equivalent input resistance of 100kΩ. This input can be driven from a TTL or CMOS crystal oscillator, or it can be AC-coupled.
30	MUX_OUT	LVCMOS output		Multiplexed output and serial data out. Refer to Table 6.
31	GND_SD	Ground		Digital Sigma Delta Modulator power supply ground.
32	V_{DD_SD}	Power		Digital Sigma Delta Modulator supply. V_{DD_SD} must have the same value as V_{DDA}.
EP	Exposed Pad	Ground		Must be connected to GND.

1. *Pull-up and Pull-down* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
C_{in}	Input Capacitance			4		pF
R_{OUT}	LVCMOS Output Impedance	MUX_OUT & LD		38		Ω
R_{PULLUP}	Input Pull-up Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pull-down Resistor			51		kΩ

Table 3. Supply Pins and Associated Current Return Paths

Power Supply Pin Number	Power Supply Pin Name	Associated Ground Pin Number	Associated Ground Pin Name
10	V_{DDA}	9	GNDA
28	V_{DDD}	27	GNDD
32	V_{DD_SD}	31	GND_SD
14, 17	V_{VCO}	11, 18, 21	GNDA_VCO
6	$V_{\_CP}$	8	GND_CP

2. Principles of Operation

2.1 Synthesizer Programming

The Fractional-N architecture is implemented via a cascaded programmable dual modulus prescaler. The N divider offers a division ratio in the feedback path of the PLL, and is given by programming the value of INT, FRAC and MOD in the following equation:

$$N = INT + FRAC/MOD \quad (1)$$

INT is the divide ratio of the binary 16-bits counter (see Table 11).

FRAC is the numerator value of the fractional divide ratio. It is programmable from 0 to (MOD – 1) (see Table 12.)

MOD is the 32-bit modulus. It is programmable from 2 to 4,294,967,295 (see Table 17).

The **VCO** frequency (f_{VCO}) at RF_OUT is given by the following equation: $f_{VCO} = f_{PFD} \times (INT + FRAC/MOD)$ (2)

f_{PFD} is the frequency at the input of the Phase and Frequency Detector (PFD).

The 8V97052 offers an Integer mode. To enable that mode, the user has to program the FRAC value to 0.

The device's integrated VCO features three VCO band-splits to cover the entire range with sufficient margin for process, voltage, and temperature variations. These are automatically selected by invoking the Autocal feature. The charge pump current is also programmable via the ICP SETTING register for maximum flexibility.

Via register 4, one can enable RF_OUT. Similarly, one can disable RF_OUT.

Valid reference clock needs to be input to the 8V97052 before it is programmed.

2.2 Reference Input Stage

The 8V97052 features one single-ended reference clock input (REF_IN). This single-ended input can be driven by an ac-coupled sine wave or square wave.

In Power-down mode this input is set to High-Impedance to prevent loading of the reference source.

The reference input signal path also includes an optional doubler.

2.3 Reference Doubler

To improve the phase noise performance of the device, the reference doubler can be used. By using the doubler, the PFD frequency is also doubled. This allows the VCO frequency to be adjusted more often and typically improves the performance of the device. When operating the device in Fractional mode with the SSMF-II Sigma Delta modulator type, the speed of the N counter is limited to 80MHz, which is also the maximum PFD frequency that can be used in the Fractional mode. When operating the device in Fractional mode with the SSMF-B Sigma

Delta modulator type, the maximum speed of the N counter and PFD is 80MHz. When the part operates in Integer-N mode, the PFD frequency is limited to 310MHz.

The user has the possibility to select a higher PFD frequency (up to 310MHz in Integer mode) by doing the following steps:

1. The user needs to set the size of the band select clock divider ratio (12 bits) to divide down to a frequency lower than 500kHz and higher than 125kHz.
   - Increase the lock detect precision for a faster PFD frequency.

The lock detect window should be set as large as possible but less than a period of the phase detector. The phase detector frequency should be greater than 500kHz.

Table 4. Lock Detect Precision (LDP)

LDP_Ext2 (D27 of Register 6)	LDP_Ext1 (D26 of Register 6)	LDP (D7 of Register 2)	LDP Value (ns)
0	0	0	10
0	0	1	6
0	1	0	3
0	1	1	3
1	0	0	4
1	0	1	4.5
1	1	0	1.5
1	1	1	1.5

2.4 Feedback Divider

The feedback divider N supports fractional division capability in the PLL feedback path. It consists in an integer N divider of 16-bits, and a fractional divider of 32-bits (FRAC) over 32-bits (MOD).

To select an integer mode only, the user sets FRAC to 0.

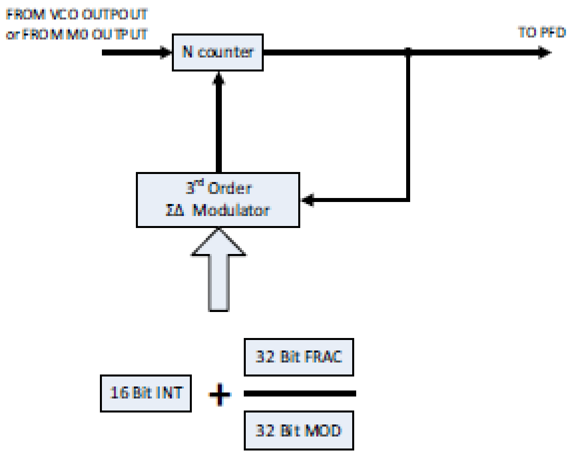


Figure 2. RF Feedback N Divider

The 16 INT bits (Bit [D30:D15] in Register 0) set the integer part of the feedback division ratio.

The 32 FRAC bits (Bit [D14:D3] in Register 0 and Bit [D30:D11] in Register 3) set the numerator of the fraction that goes into the Sigma Delta modulator.

The 32 MOD bits (Bit [D14:D3] in Register 1 and Bit [D22:D3] in Register 5) set the denominator of the fraction that goes into the Sigma Delta modulator.

From the relation (2), the VCO minimum step frequency is determined by (1/MOD) $*$ f_{PFD}.

FRAC values from 0 to (MOD – 1) cover channels over a frequency range equal to the PFD reference frequency.

The PFD frequency is calculated as follows:

$$f_{PFD} = REF_{CLK} \frac{1+D}{R} \qquad (3)$$

Use **2R** instead of R if the reference divide by 2 is used.
REF_{CLK} = the input reference frequency (REF_IN)
D = the input reference doubler (0 if not active or 1 if active)
R = the 10-bits programmable input reference pre-divider

The programmable modulus (MOD) is determined based on the input reference frequency (REF_IN) and the desired channelization (or output frequency resolution). The high resolution provided on the R counter and the modulus allows the user to choose from several configuration (by using the doubler or not) of the PLL to achieve the same channelization. Using the doubler may offer better phase noise performance. The high resolution modulus also allows to use the same input reference frequency to achieve different channelization requirements. Using a unique PFD frequency for several needed channelization requirements allows the user to design a loop filter for the different needed setups and ensure the stability of the loop.

The channelization is given by $\frac{f_{PFD}}{MOD}$ (4)

In low noise mode (dither disabled), the Sigma Delta modulator can generate some fractional spurs that are due to the quantization noise.

The spurs are located at regular intervals equal to f_{PFD}/L where L is the repeat length of the code sequence in the Sigma Delta modulator. That repeat length depends on the MOD value, as described in Table 5.

Table 5. Fractional Spurs Due to the Quantization Noise

Condition (Dither Disabled)	L	Spur Intervals
MOD can be divided by 2, but not by 3	2 × MOD	$f_{PFD}/(2 \times MOD)$
MOD can be divided by 3, but not by 2	3 × MOD	$f_{PFD}/(3 \times MOD)$
MOD can be divided by 6	6 × MOD	$f_{PFD}/(6 \times MOD)$
Other conditions	MOD	f_{PFD}/MOD (channel step)

In order to reduce the spurs, the user can enable the dither function to increase the repeat length of the code sequence in the Sigma Delta modulator. The increased repeat length is 2^{32} cycles so that the resulting quantization error is spread to appear like broadband noise. As a result, the in-band phase noise may be degraded when using the dither function.

When the application requires the lowest possible phase noise and when the loop bandwidth is low enough to filter most of the undesirable spurs, or if the spurs won't affect the system performance, it is recommended to use the low noise mode with dither disabled.

2.5 Phase and Frequency Detector (PFD) and Charge Pump

The phase detector compares the outputs from the R counter and from the N counter and generates an output corresponding to the phase and frequency difference between the two inputs the PFD. The charge pump current is programmable through the serial port (SPI) to several different levels.

The PFD offers an anti-backlash function that helps to avoid any dead zone in the PFD transfer function.

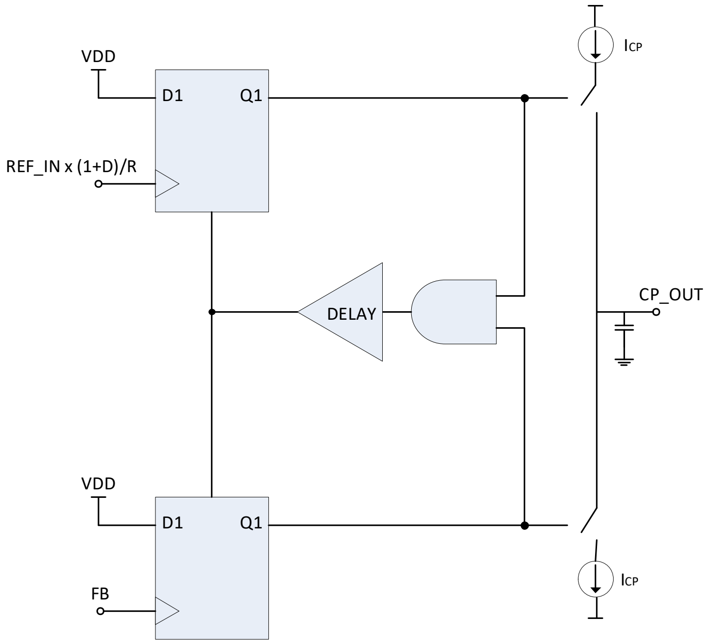


Figure 3. Simplified PFD Circuit using D-type Flip-flop

The band select logic operates between 125kHz and 500kHz. The band select clock divider needs to be set to divide down the PFD frequency to between 125kHz to 500kHz (logic maximum frequency).

2.6 PFD Frequency

The VCO band selection can be used while operating at PFD frequencies up to 310MHz.

If the application requires the PFD frequency to be higher than 100MHz in integer mode, the user can use one of the following two techniques (Technique A is the recommended procedure):

1. The user can use the extended register ExtBndSelDiv[4:1] bits (Bits [D6:D3]) in Register 6. These additional band select divider bits extend the band select divider from 8-bits (available in Register 4) to 12-bits. The four additional band select divider bits in
Register 4 are the most significant bits of the divide value. For proper VCO band selection, the PFD frequency divided by the band select divide value must be ≤500kHz and ≥125kHz.
   - If choosing this second technique, the user must follow the three following steps:
2. Disable the phase adjust function by setting the bit D28 in Register 1 to 0, keep the PFD frequency lower than 125MHz, and program the desired VCO frequency.
3. Enable the phase adjust function by setting BAND_SEL_DISABLE (Bit D28 in Register 1) to 1.
4. Set the desired PFD frequency and program the relevant R divider and N counter values.

In either technique, the lock detect precision should be programmed to be lower than the PFD period using the bit [D7] in Register 2 and the bits [D27:D26] in Register 6 (refer to Table 4).

2.7 External Loop Filter

The 8V97052 requires an external loop filter. The design of that filter is application specific. For additional information, refer to Applications Information.

2.8 Phase Detector Polarity

The phase detector polarity is set by bit D6 in Register 2. This bit should be set to 1 when using a passive loop filter or a non-inverting active loop filter. If an inverting active filter is used, this bit should be set to 0.

2.9 Charge Pump High-Impedance

In order to put the charge pump into three-state mode, the user must set the bit D4 [CP HIGHZ] in Register 2 to 1. This bit should be set to 0 for normal operation.

2.10 Integrated Low Noise VCO

The VCO function of the 8V97052 consists in three separate VCOs. This allows keeping narrow tuning ranges for the VCOs while offering a large frequency tuning range for VCO core. Keeping narrow VCO tuning ranges allows for lower VCO sensitivity (K_{VCO}), which results in the best possible VCO phase noise and spurious performance.

The user does not have to select the different VCO bands. The VCO band select logic of the 8V97052 will automatically select the most suitable band of operation at power up or when Register 0 is written

2.11 RF_IN Input

The 8V97052 offers a RF_IN differential input that can be used with an external VCO with frequencies up to 4.4GHz. The RF_IN input signal can be routed directly to the output driver M0. For more information, see Table 85.

2.12 Output Distribution Section

The 8V97052 device provides an open drain output RF_OUT. The output can generate a frequency f_{VCO} / M0 or RF_IN / M0 for any allowed value of M0.

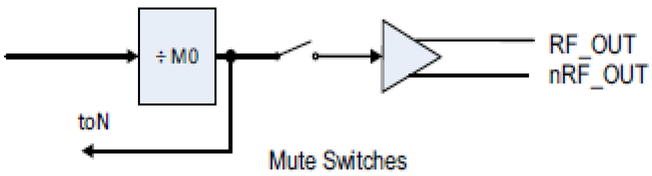


Figure 4. Output Clock Distribution

RF_OUT and nRF_OUT are derived from the drain of an NMOS differential pair driven by the VCO output (or by the M0 divider), as shown in Figure 5.

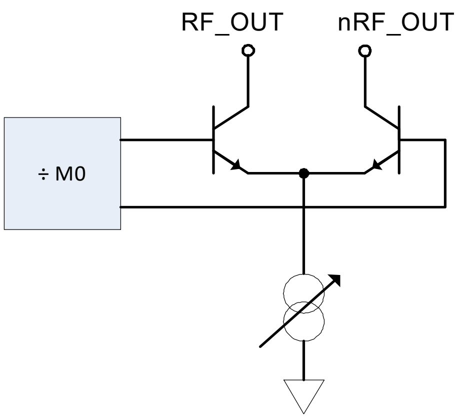


Figure 5. Output Stage

Eight programmable output power levels can be programmed from -4dBm to +11.5dBm (see RF Output Power section).

The supply current to the output stage can be shut down until the part achieves lock. To enable this mode, the user will set the MTLD bit in Register 4. The MUTE pin can be used to mute the output and be used as a similar function.

2.13 Output Matching

The output of the 8V97052 is an open drain output and can be matched in different ways.

A simple broadband matching is to terminate the open drain RF_OUT output with a 50Ω to V_{DDA}, and with an AC coupling capacitor in series. An example of this termination scheme is shown on Figure 6.

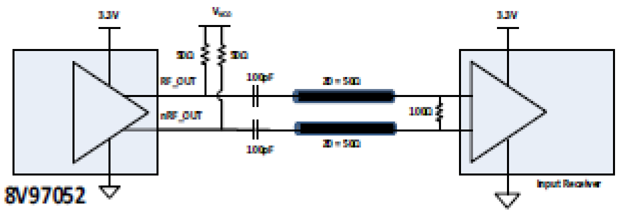


Figure 6. Broadband Matching Termination

This termination scheme allows to provide one of the selected output power on the differential pair when connected to a 50Ω load.
(See the RF Output Power section for more information about the output power selection).

The 50Ω resistor connected to V_{DDA} can also be replaced by a choke, for better performance and optimal power transmission.

The pull up inductor value is frequency dependent. For impedance of 50Ω pull-up, the inductance value can be calculated as
L = 50/(2 × 3.14 × F), where F is operating frequency. In this example,
L = 3.9nF is for an operating frequency of approximately 2GHz.

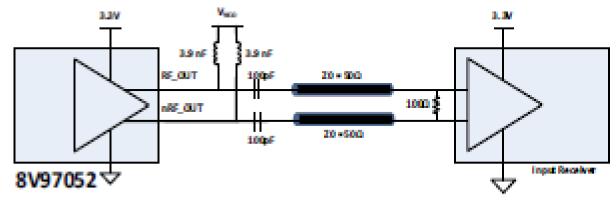


Figure 7. Optimal Matching Termination

For more recommendations on the termination scheme, see Applications Information.

2.14 Band Selection Disable

For a given frequency, the output phase can be adjusted when using the Band_Sel_Disable bit (Bit D28 in Register 1). When this bit is enabled (Bit D28 set to 1), the part does not do a VCO band selection or phase resync after an update to Register 0.

When the Band_Sel_Disable bit is set to 0, and when Register 0 is updated, the part proceeds to a VCO band selection, and to a phase resync if phase_resync is also enabled in Register 7 (Bits [D18:D17] set to D18 = 1 and D17 = 0).

The "Band_Sel_Disable" bit is useful when the user wants to make small changes in the output frequency (<1MHz from the nominal frequency) without recalibrating the VCO and minimizing the settling time.

2.15 Phase Adjust

The output phase is controlled by the 12-bit phase value Bits [D26:D15] in Register 1. The output phase can vary over 360° with a 360° x 2^20 ÷ MOD step. For dynamic adjustments of the phase after an initial phase setting, it is recommended to select the BAND_SEL_DISABLE function by setting the Band_Sel_Disable bit (D28 in Register 1) to 1.

2.16 Phase Resync

The phase alignment function operates based on adjusting the "fractional" phase, so the phase can settle to any one of the MOD phase offsets, MOD being the modulus of the fractional feedback divider.

The phase adjustment can provide a 0° – 360° of phase adjust, assuming that the output divider ratio is set to 1.

The phase step is TVCO/MOD for the normal case of fundamental feedback. TVCO is the period of the VCO.

The feedback select bit (FbkSel bit, Bit D23 in Register 4) gives the choices of fundamental feedback or divided feedback. This bit controls the mux that sends the VCO signal or the output divider signal to the feedback loop. The user can get larger phase steps in the divided mode, but the phase noise may be degraded, especially in fractional mode. Should the user select this option, the phase adjustment step would be ~T_{OUT}/MOD, where T_{OUT} is the output signal period.

When the part is in fractional mode, the device is dithering the feedback divider value. As an example, when using a 4GHz VCO frequency, the feedback divider value may dither between div-by-20 and div-by-21. Since the period is 250ps, there will be 250ps of jitter added to the phase detector. This jitter is filtered by the loop, but can still show up at the output if the loop bandwidth is high. When using a divider before the feedback divider, the effective VCO period is increased. If a div-by-64 is used for example, the period becomes
64×250ps = 16ns. This means that there could be an additional 16ns of jitter at the PFD, rather than 250ps. It is more challenging for the loop to filter this larger amount of jitter and this will degrade the overall performance of the part, unless the user chooses to use a very low loop bandwidth. With normal loop bandwidth configurations (for optimal noise), the phase noise would be degraded when using a divided feedback mode.

The phase resync is controlled by setting Bits [D18:D17] in Register 7 to D18 = 1 and D17 = 0.
When phase resync is used, an internal timer generates sync signals every T_{SYNC} where:

$$T_{SYNC} = \text{ClkDiv} \times \text{MOD} \times T_{PFD} \qquad (5)$$

- **ClkDiv** = the value (from 1 and 4095) programmed in the 12-bit clock counter in Bits [D31:D20] in Register 4. The 12-bit counter is used as a timer for Fast Lock and for the Phase Resync function.
- **MOD** = the modulus value (Bits [D14:D3] of Register 1 and Bits [D22:D3] of Register 5)
- **T_{PFD}** = the PFD period

In *Equation 5*, the minimum of either MOD value or 4095 is used for calculating T_{SYNC}.

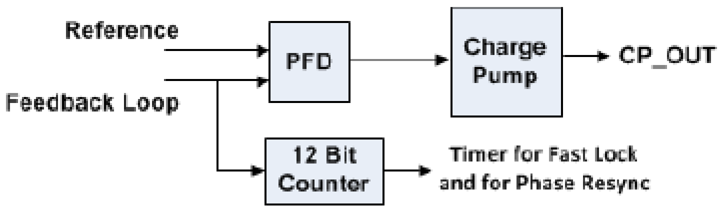


Figure 8. 12-bit Counter for Fast Lock and Phase Resync

After the user program a frequency, the second sync pulse coming from the 12-bit counter, after the nCS is asserted high, is used to resynchronize the output phase to the input phase. To ensure that the PLL is locked before to resynchronize the output phase, TSYNC must be larger than the worst case lock time.

2.17 Fast Lock Function

The device uses a fast-lock mode to decrease lock time.

In order to allow the fast lock mode, the Fast Lock Switch (FLSW) is shorted to ground and the Charge Pump Current (ICP) is changed temporarily until the fast lock mode is disabled.

The loop bandwidth needs to be increased temporarily in order to allow a faster lock time. By doing this, the loop filter needs to be initially designed so that it addresses the risk of instability of having the zero and the poles too close to the actual bandwidth knee, when the user switches to a fast lock mode.

The loop bandwidth is proportional to: RS and ICP (BW ~ RS × ICP)

Where:

- BW = the loop bandwidth
- RS = the damping resistor
- ICP = the programmable charge pump current

In order to enable the fast lock mode, the charge pump current is increased to the maximum value in order to increase the loop bandwidth. In parallel, the FLSW filter is set to ON so that the RS value is ¼ of its initial value in order to maintain the loop stability. By doing so, the zero and the first pole are moved (by a factor of 4x in the example below), so that the zero and the pole are kept at a suitable distance around the loop bandwidth.

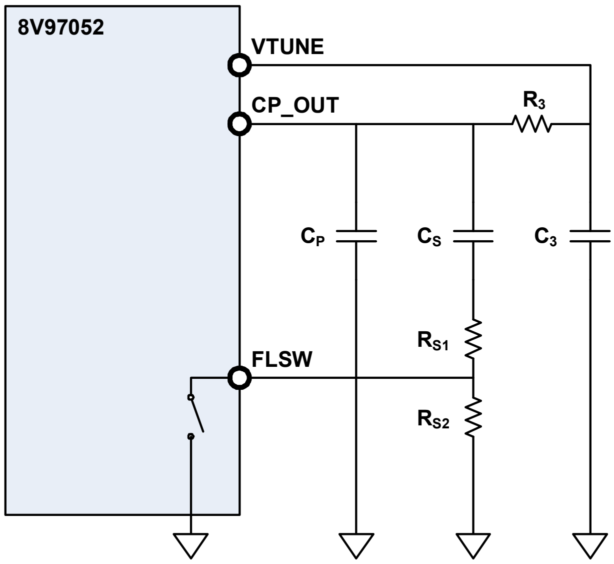


Figure 9. Example of Fast Lock Mode Loop Filter Topology

In the example of Figure 9, the damping resistor RS is equal to:
RS1 + RS2 in normal mode (FSLW switch OFF), with RS2 = 3 × RS1

When the FLSW switch is ON, the damping resistor value is reduced by ¼ of its initial value (RS = RS1).

The second pole defined by R3 and C3 need needs to be designed so that there is no risk of instability when widening the loop bandwidth.

2.18 RF Output Power

For RF_OUT the output power can be programmed from -4dBm to +11.5dBm.

Refer to Table 44 and Table 45 in the Registers section for additional information.

2.19 MUX_OUT

MUX_OUT is a multipurpose output that can be programmed to provide the user with some internal status and values for test and debugging purpose. In addition, MUX_OUT can also be programmed to provide an additional serial data out pin for a 4-wire SPI interface when needed. The MUX_OUT function is described in the Table 6 and can be programmed in Bits [D28:D26] in Register 2.

Table 6. MUX_OUT Pin Configuration

MUX_OUT Register Value	MUX_OUT Function
000	High-Impedance output
001	V_{DDD}
010	GNDD
011	R counter output
100	N counter output
101	Reserved
110	Lock detect
111	MUX_OUT configured as SDO

2.20 Power-Down Mode

When power-down is activated, the following events occur:

1. Counters are forced to their load state conditions
   - VCO is powered down
   - Charge pump is forced into three-state mode
   - Digital lock detect circuitry is reset
   - RF_OUT buffers are disabled
   - The input stage is powered down and set to High-Impedance
   - Input registers remain active and capable of loading and latching data

2.21 Default Power-Up Conditions

All the RF outputs are muted at power up until the loop is locked. Refer to Registers for default values in registers.

2.22 Program Modes

Table 7 and Registers indicates how the program modes are set up in the 8V97052.

Table 7. Control Bits Configuration

Control Bits (CB)			Register
C3	C2	C1	
0	0	0	Register 0
0	0	1	Register 1
0	1	0	Register 2
0	1	1	Register 3
1	0	0	Register 4
1	0	1	Register 5
1	1	0	Register 6
1	1	1	Register 7

2.23 Double Buffering

The following bits are doubled buffered:

1. PHASE (Bits[D26:D15] in Register 1)
   - MOD (Bits [D14:D3] in Register 1 and Bits [D22:D3] in Register 5)
   - REF DOUBLER (Bit D25 in Register 2)
   - REF DIV2 (Bit D24 in Register 2)
   - R COUNTER (Bits [D23:D14] in Register 2)
   - ICP SETTING (Bits [D12:D9] in Register 2)
   - CALIB_VC (Bits [D20:D19] in Register 7)
   - CP_BCC (Bits D[29:25] in Register 5)

The user must proceed to the following steps before any value written in these bits are used.

1. The new values are written in the double buffered bits
   - A new Write is performed on Registers 0.

The RF DIVIDER value in Register 7 (Bits [D14:D12]) is also double buffered by the DOUBLE BUFFER bit (Bit D13 in Register 2) is set to 1.

3. Timing Characteristics

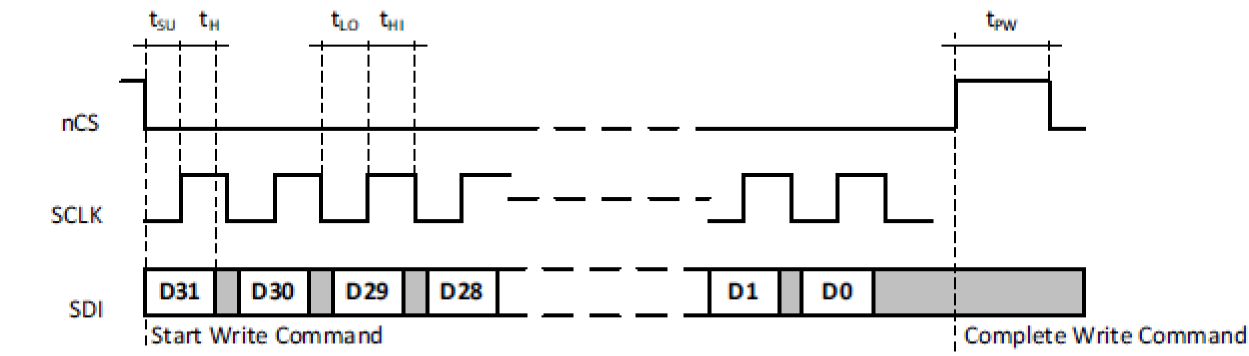


Figure 10. SPI Write Cycle Timing Diagram

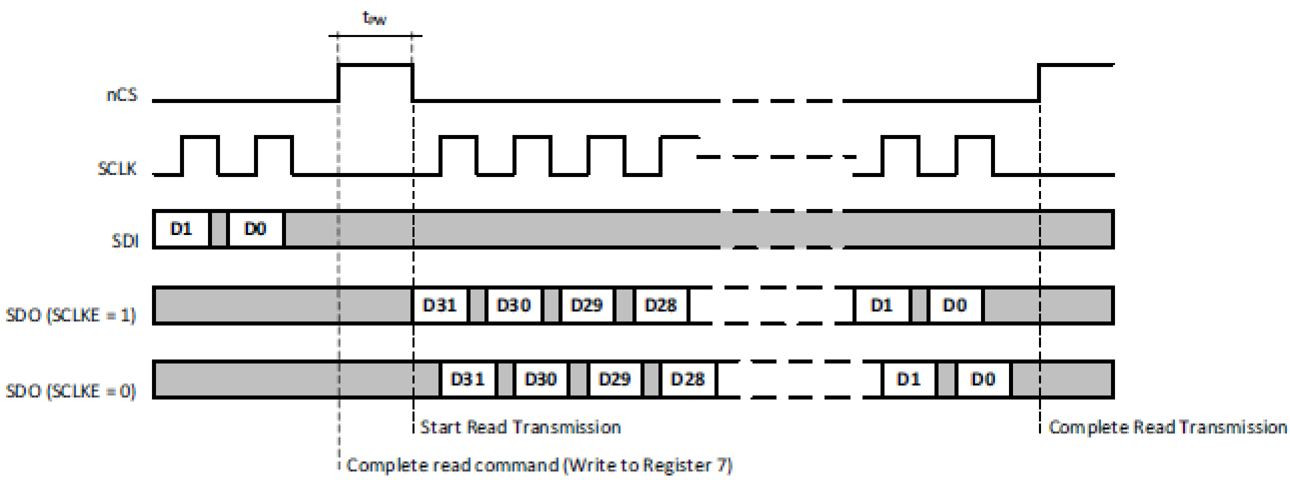


Figure 11. SPI Read Cycle Timing Diagram

Table 8. SPI Read / Write Cycle Timing Parameters

Symbol	Parameter	Minimum	Maximum	Unit
f_{CLK}	SCLK frequency	—	20	MHz
t_{SU}	nCS, SDI setup time to SCLK	10	—	ns
t_H	SCLK to nCS, SDI hold time	10	—	ns
t_{LO}	SCLK low pulse width	25	—	ns
t_{HI}	SCLK high pulse width	25	—	ns
t_{PW}	nCS De-asserted pulse width	20	—	ns

4. 3- or 4-Wire SPI Interface Description

The 8V97052 has a serial control port capable of responding as a slave in an SPI compatible configuration to allow access to any of the internal registers (see Registers) for device programming or examination of internal status. See the specific sections for each register for details on meanings and default conditions.

SPI mode slave operation requires that a device external to the 8V97052 has performed any necessary serial bus arbitration and/or address decoding at the level of the board or system. The 8V97052 begins a cycle by detecting an asserted (low) state on the nCS input at a rising edge of SCLK. This is also coincident with the first bit of data being shifted into the device. In SPI mode, the first bit is the Most Significant Bit (MSB) of the data word being written. Data must be written in 32-bit words, with nCS remaining asserted and one data bit being shifted in to the 8V97052 on every rising edge of SCLK. If nCS is de-asserted (high) at any time except after the complete 32nd SCLK cycle, this is treated as an error, and the shift register contents are discarded. No data is written to any internal registers. If nCS is de-asserted (high) as expected at a time at least t_{SU} after the 32nd falling edge of SCLK, then this will result in the shift register contents being acted on according to the control bit in it.

It is recommended to write the registers in reverse sequential order, starting with the highest register number first and ending with Register 0.

The word format of the 32-bit quantity in the shift register is shown in Table 9. The register fields in the 8V97052 have been organized so that the three LSBs in each 32-bit register row are not used for data transfer. These bits will represent the base address for the 32-bit register row.

Table 9. SPI Mode Serial Word Structure

<table>
<tr><th rowspan="2">Bit #</th><th>MSB</th><th colspan="6"></th><th>LSB</th></tr>
<tr><th>31</th><th>...</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>Meaning</td><td colspan="5">D[31:3]</td><td colspan="3">Control Bits</td></tr>
<tr><td>Width</td><td colspan="5">29</td><td colspan="3">3</td></tr>
</table>

To perform a register Read, the user needs set the MUX_OUT bits (Bits [D28:D26]) in Register 2 to 111 to configure the MUX_OUT pin as SDO. Register 7 (Instruction register) needs to be set for Read operation. Bit D3 of Register 7 will set the Read or Write command, and Bits [D4:D6] determine the read back address.

If a read operation is requested, 32-bits of read data will be provided in the immediately subsequent access. nCS must be de-asserted (high) for at least $t_{PW,}$ and then reasserted (low).

If SCLKE = 1 (default condition), one data bit will be transmitted on the SDO output at the falling edge of nCS and each falling edge of SCLK as long as nCS remains asserted (low), and the master device should capture data on the rising edge of SCLK. If SCLKE = 0, one data bit will be transmitted on the SDO output at each rising edge of SCLK as long as nCS remains asserted (low), and the master device should capture data on the falling edge of SCLK.

If nCS is de-asserted (high) before 32-bits of read data have been shifted out, the read cycle will be considered to be completed. If nCS remains asserted (low) longer than 32-bit times, then the data during those extra clock periods will be undefined. The MSB of the data will be presented first.

5. Registers

5.1 Register 0

Table 10. Register 0 Bit Allocation

BITS	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Reserved	Ndiv16	Ndiv15	Ndiv14	Ndiv13	Ndiv12	Ndiv11	Ndiv10	Ndiv9	Ndiv8	Ndiv7	Ndiv6	Ndiv5	Ndiv4	Ndiv3	Ndiv2	Ndiv1	Fdiv32	Fdiv31	Fdiv30	Fdiv29	Fdiv28	Fdiv27	Fdiv26	Fdiv25	Fdiv24	Fdiv23	Fdiv22	Fdiv21	CB3	CB2	CB1
DESCRIPTION	RESERVED	FEEDBACK INTEGER VALUE (INT)																FEEDBACK DIVIDER VALUE (FRAC) (12 UPPER BITS OF THE 32 BITS FRAC VALUE)												CONTROL BITS		

Table 11. Register 0: 16-bit Feedback Divider Integer Value (INT). Function Description

Name	Description	Factory Defaults	Function
NDiv[16:1]	Feedback Divider Integer Value (INT)	0000 0000 0110 0100 (INT = 100)	0000 0000 0000 0000 = Not allowed 0000 0000 0000 0001 = Not allowed … 0000 0000 0000 0111 = Not allowed 0000 0000 0000 1000 = 8 … 0000 0000 0001 0111 = 23 0000 0000 0001 1000 = 24 … 1111 1111 1111 1111 = 65,535

Table 12. Register 0: 12 Last Bit Feedback Divider Fractional Value (FRAC). Function Description[1]

Name	Description	Factory Defaults		Function		
		Register 0 FRAC (FDiv[32:21])	Register 3 FRAC (FDiv[20:1])	Register 0 FRAC (FDiv[32:21])	Register 3 FRAC (FDiv[20:1])	Value
FDiv[32:1]	Feedback Divider Fractional Value (FRAC)	0000 0000 0000	0000 0000 0000 0000 0000	0000 0000 0000	0000 0000 0000 0000 0000	0
					0000 0000 0000 0000 0001	1
					0000 0000 0000 0000 0010	2
					…	
					1111 1111 1111 1111 1111	(2^20)-1 = 1,048,575
				0000 0000 0001	0000 0000 0000 0000 0000	2^20 = 1,048,576
					…	
					1111 1111 1111 1111 1111	(2^21)-1
				…		
				1111 1111 1111	0000 0000 0000 0000 0000	(2^20) * (2^12 - 1)
					…	
					1111 1111 1111 1111 1111	2^32 - 1

1. This table is used along with Register 3 FRAC value in order to complete the 32 bits of FRAC.

Table 13. Register 0: 3-bit Control Bits. Function Description[1]

Name	Description	Function
CB[3:1]	Control bits	000 = Register 0 is programmed

1. The user has to set CB[3:1] to 000 in order to Write to Register 0.

5.2 Register 1

Table 14. Register 1 Bit Allocation

BITS	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Reserved	Reserved	Reserved	Band_Sel_Disable	Unused	Phase12	Phase11	Phase10	Phase9	Phase8	Phase7	Phase6	Phase5	Phase4	Phase3	Phase2	Phase1	Mod32	Mod31	Mod30	Mod29	Mod28	Mod27	Mod26	Mod25	Mod24	Mod23	Mod22	Mod21	CB3	CB2	CB1
DESCRIPTION	RESERVED			BAND_SEL_DISABLE	UNUSED	PHASE												MODULUS VALUE (MOD) (12 LAST BITS OF THE 32 BITS MOD VALUE)												CONTROL BITS		

Table 15. Register 1: 1-Bit BAND_SEL_DISABLE. Function Description

Name	Description	Factory Defaults	Function
Band_Sel_ Disable	BAND_SEL_DISABLE	0	0 = VCO Band Selection occurs after a Write to Register 0 1 = VCO Band selection is not active and hold to previous VCO band selection

Table 16. Register 1: 12-bit Phase Value (PHASE). Function Description

Name	Description	Factory Defaults	Function
Phase [12:1]	PHASE	0000 0000 0001	0000 0000 0000 = 0 0000 0000 0001 = 1 = 2^20 (Recommended) … 1111 1111 1111 = 4,293,918,270

Table 17. Register 1: 12 Last Bits Modulus Value (MOD). Function Description[1]

Name	Description	Factory Defaults		Function		
		Register 1 MOD (FDiv[32:21])	Register 5 MOD (FDiv[20:1])	Register 1 MOD (FDiv[32:21])	Register 5 MOD (FDiv[20:1])	Value
Mod[32:1]	MODULUS VALUE (MOD)	0000 0000 0000	0000 0000 0000 0000 0010	0000 0000 0000	0000 0000 0000 0000 0000	Not Allowed
					0000 0000 0000 0000 0001	Not Allowed
					0000 0000 0000 0000 0010	2
					…	
					1111 1111 1111 1111 1111	(2^20) – 1 = 1,048,575
				0000 0000 0001	0000 0000 0000 0000 0000	2^20 = 1,048,576
					…	
					1111 1111 1111 1111 1111	(2^21) – 1
				…		
				1111 1111 1111	0000 0000 0000 0000 0000	2^20*(2^12 –1)
					…	
					1111 1111 1111 1111 1111	2^32 – 1

1. This table is used along with Register 5 MOD value in order to complete the 32 bits of MOD.

Table 18. Register 1: 3-Bit Control Bits. Function Description[1]

Name	Description	Function
CB[3:1]	Control bits	001 = Register 1 is programmed

1. The user has to set CB[3:1] to 001 in order to write to Register 1.

5.3 Register 2

Table 19. Register 2 Bit Allocation

BITS	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Reserved	ModeNoise2	ModeNoise1	MUX_OUT3	MUX_OUT2	MUX_OUT1	RefDoub	RDiv2	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	DoubBuff	ChrgPmp4	ChrgPmp3	ChrgPmp2	ChrgPmp1	LDF	LDP	PD_pol	PwrDwn	CP_HIGHZ	Unused	CB3	CB2	CB1
DESCRIPTION	RESERVED	NOISE MODE		MUX_OUT			REF DOUBLER	REF DIV2	R COUNTER										DOUBLE BUFFER	ICP SETTING				LDF	LDP	PD POLARITY	POWER DOWN	CP HIGHZ	UNUSED	CONTROL BITS		

Table 20. Register 2: 2-bit NOISE MODE. Function Description

Name	Description	Factory Defaults	Function
ModeNoise[2:1]	NOISE MODE	00	00 = Low Noise Mode (Dither OFF) 01 = Reserved 10 = Reserved 11 = Low Spur Mode (Dither Enabled)

Table 21. Register 2: 3-bit MUX_OUT. Function Description

Name	Description	Factory Defaults	Function
MUX_OUT[3:1]	MUX_OUT	000	000 = High-Impedance output 001 = VDDD 010 = GNDD 011 = R counter output 100 = N counter output 101 = Reserved 110 = Lock Detect 111 = MUX_OUT configured as SDO

Table 22. Register 2: 1-bit REF DOUBLER. Function Description

Name	Description	Factory Defaults	Function
RefDoub	REF DOUBLER	0	0 = Disabled 1 = Enabled

Table 23. Register 2: 1-bit REF DIV2. Function Description

Name	Description	Factory Defaults	Function
RDIV2	REF DIV2	0	0 = Disabled 1 = Enabled

Table 24. Register 2: 10-bit R COUNTER (R). Function Description

Name	Description	Factory Defaults	Function
R[10:1]	R	00 0000 0001	00 0000 0000 = Not Allowed 00 0000 0001 = 1 00 0000 0010 = 2 … 11 1111 1111 = 1023

Table 25. Register 2: 1-bit DOUBLE BUFFER. Function Description

Name	Description	Factory Defaults	Function
DoubBuff	DOUBLE BUFFER	0	0 = Disabled 1 = Enabled

Table 26. Register 2: 4-bit Charge Pump Setting (ICP SETTING). Function Description

Name	Description	Factory Defaults	Function
ChrgPmp[4:1]	ICP SETTING	0000	Icp (mA) assuming RCP = 5.1kΩ 0000 = 0.31 0001 = 0.63 0010 = 0.94 0011 = 1.25 0100 = 1.56 0101 = 1.88 0110 = 2.19 0111 = 2.50 1000 = 2.81 1001 = 3.13 1010 = 3.44 1011 = 3.75 1100 = 4.06 1101 = 4.38 1110 = 4.69 1111 = 5.00

Table 27. Register 2: 1-bit Lock Detect Function (LDF). Function Description

Name	Description	Factory Defaults	Function[1]
LDF	LDF	0	0 = 40 consecutive cycles (recommended for FRAC-N mode) 1 = 5 consecutive cycles (recommended for INT-N mode)

1. LDF controls the number of PFD cycles that needs to be considered by the lock detect function to decide if the part has achieved lock.

Table 28. Register 2: 1-bit Lock Detect Precision. Function Description

Name	Description	Factory Defaults	Function
LDP	LDP	0	0 = 10ns 1 = 6ns

Table 29. Register 2: 1-bit Phase Detector Polarity. Function Description

Name	Description	Factory Defaults	Function
PD_Pol	PD POLARITY	1	0 = Negative 1 = Positive

Table 30. Register 2: 1-bit Power Down. Function Description

Name	Description	Factory Defaults	Function
PwrDwn	POWER DOWN	0	0 = Disabled 1 = Enabled

Table 31. Register 2: 1-bit Charge Pump High-Impedance. Function Description

Name	Description	Factory Defaults	Function
CP_HIGHZ	CP HIGHZ	0	0 = Disabled 1 = Enabled

Table 32. Register 2: 3-bit Control Bits. Function Description

Name	Description	Function[1]
CB[3:1]	Control bits	010 = Register 2 is programmed

1. The user has to set CB[3:1] to 010 in order to Write to Register 2.

5.4 Register 3

Table 33. Register 3 Bit Allocation

BITS	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Reserved	Fdiv20	Fdiv19	Fdiv18	Fdiv17	Fdiv16	Fdiv15	Fdiv14	Fdiv13	Fdiv12	Fdiv11	Fdiv10	Fdiv9	Fdiv8	Fdiv7	Fdiv6	Fdiv5	Fdiv4	Fdiv3	Fdiv2	Fdiv1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CB3	CB2	CB1
DESCRIPTION	RESERVED	FEEDBACK DIVIDER VALUE (FRAC) (20 FIRST BITS OF THE 32 BITS FRAC VALUE)																				RESERVED								CONTROL BITS		

Table 34. Register 3: 20 First Bits Feedback Divider Fractional Value (FRAC). Function Description

Name	Description	Factory Defaults		Function[1]		
		Register 0 FRAC (FDiv[32:21])	Register 3 FRAC (FDiv[20:1])	Register 0 FRAC (FDiv[32:21])	Register 3 FRAC (FDiv[20:1])	Value
FDiv[32:1]	Feedback Divider Fractional Value (FRAC)	0000 0000 0000	0000 0000 0000 0000 0000	0000 0000 0000	0000 0000 0000 0000 0000	0
					0000 0000 0000 0000 0001	1
					0000 0000 0000 0000 0010	2
					...	
					1111 1111 1111 1111 1111	(2^20)-1 = 1,048,575
				0000 0000 0001	0000 0000 0000 0000 0000	2^20 = 1,048,576
					...	
					1111 1111 1111 1111 1111	(2^21)-1
					...	
				1111 1111 1111	0000 0000 0000 0000 0000	(2^20) * (2^12 - 1)
					...	
					1111 1111 1111 1111 1111	2^32 - 1

1. This table is used along with Register 0 FRAC value in order to complete the 32 bits of FRAC.

Table 35. Register 3: 1-Bit SCLKE. Function Description

Name	Description	Function[1]
CB[3:1]	Control bits	011 = Register 3 is programmed

1. The user has to set CB[3:1] to 011 in order to Write to Register 3.

5.5 Register 4

Table 36. Register 4 Bit Allocation

BITS	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	ClkDiv12	ClkDiv11	ClkDiv10	ClkDiv9	ClkDiv8	ClkDiv7	ClkDiv6	ClkDiv5	ClkDiv4	ClkDiv3	ClkDiv2	ClkDiv1	BndSelDiv8	BndSelDiv7	BndSelDiv6	BndSelDiv5	BndSelDiv4	BndSelDiv3	BndSelDiv2	BndSelDiv1	VCOPwrDwn	MTLD	RF_IN_En	Reserved	Sel_M0_Mux	Sel_RF_IN_Route_Mux	RF_Out_En	RF_OUT_Pwr2	RF_OUT_Pwr1	CB3	CB2	CB1
DESCRIPTION	CLOCK COUNTER VALUE												BAND SELECT CLOCK COUNTER								VCO POWER DOWN	MTLD	RF_IN_ENABLE	RESERVED	SEL_M0_MUX	RF_IN ROUTE SELECT	RF_OUT ENABLE	RF_OUT OUTPUT POWER		CONTROL BITS		

Table 37. Register 4: 12-bit Clock Divider Value (CLOCK COUNTER VALUE). Function Description

Name	Description	Factory Defaults	Function
ClkDiv[12:1]	CLOCK COUNTER VALUE	0000 0000 0001	0000 0000 0000 = Not allowed 0000 0000 0001 = 1 0000 0000 0010 = 2 … 1111 1111 1111 = 4095

Table 38. Register 4: 8-bit Band Select Clock Counter. Function Description

Name	Description	Factory Defaults	Function[1]
BndSelDiv[8:1]	BAND SELECT CLOCK COUNTER	0000 0001	0000 0000 = Not Allowed 0000 0001 = 1 0000 0010 = 2 ... 1111 1111 = 255

1. BAND SELECT CLOCK COUNTER sets the value of the divider for the band select logic clock input. By default, the output frequency of the R counter is used to clock the band select logic. If this frequency is larger than 125kHz, the band Select Clock counter can be used to divide the R counter output to a smaller frequency suitable for the band selection logic.

Table 39. Register 4: 1-bit VCO Power Down. Function Description

Name	Description	Factory Defaults	Function
VCOPwrDwn	VCO POWER DOWN	0	0 = VCO Powered Up 1 = VCO Powered Down

Table 40. Register 4: 1-bit Mute Till Lock Detect. Function Description

Name	Description	Factory Defaults	Function
MTLD	MTLD	0	0 = Mute Disabled 1 = Mute Enabled

Table 41. Register 4: 1-bit RF_IN Enable. Function Description

Name	Description	Factory Defaults	Function
RF_IN_En	RF_IN_ENABLE	0	0 = RF_IN Disabled 1 = RF_IN Enabled

Table 42. Register 4: 1-bit VCO or RF_IN. Function Description

Name	Description	Factory Defaults	Function
Sel_M0_Mux	SEL_M0_Mux	0	0 = Select input from Internal VCO routed to M0 [1] 1 = Select input coming from RF_IN_ROUTE_MUX (RF_IN) routed to M0 [2]

Table 43. Register 4: 1-bit RF_IN Route Select. Function Description

Name	Description	Factory Defaults	Function
Sel_RF_IN_Route_Mux	RF_IN ROUTE SELECT	0	0 = RF_IN unused 1 = RF_IN signal routed to M0 Mux

Table 44. Register 4: 1-bit RF_OUTA Enable. Function Description

Name	Description	Factory Defaults	Function
RF_OUT_En	RF_OUT ENABLE	0	0 = Disabled (High-Impedance) 1 = Enabled

Table 45. Register 4: 1-bit RF_OUTA Output Power. Function Description

Name	Description	Factory Defaults	Function[1]
RF_OUT_Pwr[2:1]	RF_OUT OUTPUT POWER	10	00 = -4dBm 01 = 0dBm 10 = +2.5dBm 11 = +6dBm

1. f_{RF_OUT} = 250MHz.

Table 46. Register 4: 3-bit Control Bits. Function Description

Name	Description	Function[1]
CB[3:1]	Control bits	100 = Register 4 is programmed

1. The user has to set CB[3:1] to 100 in order to write to Register 4.

5.6 Register 5

Table 47. Register 5 Bit Allocation

BITS	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDPInMode2	LDPInMode1	Mod20	Mod19	Mod18	Mod17	Mod16	Mod15	Mod14	Mod13	Mod12	Mod11	Mod10	Mod9	Mod8	Mod7	Mod6	Mod5	Mod4	Mod3	Mod2	Mod1	CB3	CB2	CB1
DESCRIPTION	Reserved							LD PIN MODE		MODULUS VALUE (MOD) (20 FIRST BITS OF THE 32 BITS MOD VALUE)																				CONTROL BITS		

Table 48. Register 5: 2-bit LD (Lock Detect) Pin Mode. Function Description

Name	Description	Factory Defaults	Function
LDPInMode[2:1]	LD PIN MODE	01	00 = Low 01 = Digital Lock Detect 10 = Low 11 = High

Table 49. Register 5: 20 First Bits Modulus Value (MOD). Function Description

Name	Description	Factory Defaults		Function[1]		
		Register 1 MOD (Fdiv[32:21])	Register 5 MOD (Fdiv[20:1])	Register 1 MOD (Fdiv[32:21])	Register 5 MOD (Fdiv[20:1])	Value
Mod[32:1]	MODULUS VALUE (MOD)	0000 0000 0000	0000 0000 0000 0000 0010	0000 0000 0000	0000 0000 0000 0000 0000	Not Allowed
					0000 0000 0000 0000 0001	Not Allowed
					0000 0000 0000 0000 0010	2
					…	
					1111 1111 1111 1111 1111	(2^20)-1 = 1,048,575
				0000 0000 0001	0000 0000 0000 0000 0000	2^20 = 1,048,576
					…	
					1111 1111 1111 1111 1111	(2^21)-1
					…	
				1111 1111 1111	0000 0000 0000 0000 0000	2^20*(2^12-1)
					…	
					1111 1111 1111 1111 1111	2^32 - 1

1. This table is used along with Register 1 MOD value in order to complete the 32 bits of MOD.

Table 50. Register 5: 3-bit Control Bits. Function Description

Name	Description	Function[1]
CB[3:1]	Control bits	101 = Register 5 is programmed

1. The user has to set CB[3:1] to 101 in order to write to Register 5.

5.7 Register 6

Table 51. Register 6 Bit Allocation[1][2][3]

BITS	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	DigLock	Band_select_done	band_select_acc2	band_select_acc1	LDP_Ext2	LDP_Ext1	Reserved	rfout_hi_pwr	SDMOrder2	SDMOrder1	DitherG	ShapeDitherEn	SDMType2	Reserved	Band9	Band8	Band7	Band6	Band15	Band4	Band3	Band2	Band1	Band0	ManuBandEn	ExtBndSelDiv4	ExtBndSelDiv3	ExtBndSelDiv2	ExtBndSelDiv1	CB3	CB2	CB1
DESCRIPTION	DIGITAL LOCK (RO)	BAND_SELECT_DONE (RO)	BAND_SELECT_ACC		LDP_EXT		RESERVED	RF_OUT_HI_PWR	SDM_ORDER		DITHER GAIN	SHAPE_DITHER_EN	SDM_TYPE	RESERVED	BAND										MANU_BAND_EN	EXT_BND_SEL_DIV				CONTROL BITS		

NOTE 1. It is recommended that the user writes to Register 0 after writing to Register 6.

NOTE 2. Bit D7 must be set to 0 for correct operation

NOTE 3. RO bits are Read Only bits.

Table 52. Register 6: 1-bit Digital Lock Detect. Function Description

Name	Description	Function
DigLock	DIGITAL LOCK	0 = PLL Not Locked 1 = PLL Locked (according LDF and LDP in Register 2)

Table 53. Register 6: 1-bit Band Select Status (Read Only). Function Description

Name	Description	Function
Band_select_done	BAND_SELECT_DONE	0 = Band Selection Not Complete 1 = Band Selection Complete

Table 54. Register 6: 2-bit Extra Lock Detect Precision. Function Description

Name	Description	Factory Defaults	Function[1]		
			Extra Bit	LDP Bits in Register 2	Value
LDP_Ext[2:1]	LDP_EXT Extra Lock Detect Precision	00	00	0	10ns
				1	6ns
			01	0	3ns
				1	3ns
			10	0	4ns
				1	4.5ns
			11	0	1.5ns
				1	1.5ns

1. LDP_Ext[2:1] are Extra Lock Detect Precision bits. When these bits are set to 00, then the precision of the Lock Detect precision only relies on the LDP bit in Register 2, so that the lock detect window is 10ns or 6ns, depending on the LDP bit in Register 2. For high PFD frequencies, the 6ns window may be larger than the entire ref/FB period. The LDP_ext bits reduce the size of the lock detect window allowing an accurate lock detection with higher PFD frequencies.

Table 55. Register 6: 1-bit Extra Bit of RF_OUTA Power. Function Description

Name	Description	Factory Defaults	Function[1][2]		
			Extra Bit	RF_OUT OUTPUT POWER Bits in Register 4	Value (dBm)
rfout_hi_pwr	RF_OUT_HI_PWR	0	0	00	-4
				01	0
				10	+2.5
				11	+6
			1	00	+5
				01	+7.5
				10	+11
				11	+11.5

1. RF_OUT_HI_PWR is an Extra Bit of RF_OUT Power that increases the output power to the RF_OUT output.
2. f_{RF_OUT} = 250MHz.

Table 56. Register 6: 2-bit Sigma Delta Modulator Order Configuration. Function Description

Name	Description	Factory Defaults	Function
SDMOrder[2:1]	SDM_ORDER	11	00 = OFF. The device operates in integer mode and the fractional part is ignored. 01 = 1st order 10 = 2nd order 11 = 3rd order

Table 57. Register 6: 2-bit Dither Gain Configuration. Function Description

Name	Description	Factory Defaults	Function
DitherG	DITHER GAIN	0	0 = Dither Noise Shaping Disabled; LSB Dither (Recommended) 1 = Dither Noise Shaping Enabled (LSB x4 Dither)

Table 58. Register 6: 1-bit Dither Noise Shaping Configuration. Function Description

Name	Description	Factory Defaults	Function
ShapeDitherEn	SHAPE_DITHER_EN	1	0 = Dither Noise Shaping Disabled 1 = Dither Noise Shaping Enabled

Table 59. Register 6: 1-bit Sigma Delta Modulator Type Configuration. Function Description

Name	Description	Factory Defaults	Function[1]
SDMType	SDM_TYPE	0	0 = SSMF-II 1 = SSMF-B[1]

1. The PFD frequency must be limited to 88MHz when using the SSMFB DSM type (SDMType = 1).

Table 60. Register 6: 2-bit VCO Band Selection Accuracy Configuration. Function Description

Name	Description	Factory Defaults	Function
band_select_acc[2:1]	BAND_SELECT_ACC	00	00 = 1 cycle of the band select clock (output of the Band Select Divider) 01 = 2 cycles 10 = 4 cycles 11 = Reserved

Table 61. Register 6: 8-Bit Current VCO Band. Function Description

Name	Description	Factory Defaults	Function
Band	Current VCO band.	0 0000 0000	Will display the currently selected band. Can be written to in order to overwrite the band as long as manu_band_en = 1.

Table 62. Register 6: 1-Bit Manual Band Select Enable. Function Description

Name	Description	Factory Defaults	Function
MANU_BAND_EN	Manual band select enable	0	0 = Use band value computed by band select logic 1 = Use values in band registers

Table 63. Register 6: 4-Bit Extra Most Significant Bits of Band Select Divider. Function Description

Name	Description	Factory Defaults	Value	Function
ExtBndSelDiv[4:1]	EXT_BND_SEL_DIV	0000	BSCC_R4 + [EXT_BND_SEL_DIV]x256	0000 = [BSCC_R4]
				0001 =[BSCC_R4]+256
				0010 = [BSCC_R4] + 512
				…
				1111 = [BSCC_R4]+3840

Table 64. Register 6: 3-bit Control Bits. Function Description

Name	Description	Function[1]
CB[3:1]	Control bits	110 = Register 6 is programmed

1. The user has to set CB[3:1] to 110 in order to write to Register 6.

5.8 Register 7

Table 65. Register 7 Bit Allocation[1][2]

BITS	NAME	DESCRIPTION
D31	Loss_Dig_Lock	LOSS_DIG_LOCK (SB)
D30	Loss_Anlg_Lock	LOSS_ANLG_LOCK (SB)
D29	Spi_error	SPI_ERROR (SB)
D28	Reserved	RESERVED
D27	Rev_ID3	REV_ID
D26	Rev_ID2	
D25	Rev_ID1	
D24	Dev_ID4	DEV_ID (RO)
D23	Dev_ID3	
D22	Dev_ID2	
D21	Dev_ID1	
D20	Calib_Vc2	CALIB_VC2
D19	Calib_Vc1	CALIB_VC1
D18	ClkDivMode2	CLK DIV MODE
D17	ClkDivMode1	
D16	BandSelCM	BAND SELECT
D15	FbkSel	FEEDBACK SELECT
D14	RFDiv3	RF DIVIDER
D13	RFDiv2	
D12	RFDiv1	
D11	Reserved	RESERVED
D10	Reserved	
D9	Reserved	
D8	Reserved	
D7	sclke	SCLKE
D6	Rd_Addr3	READBACK_ADDR
D5	Rd_Addr2	
D4	Rd_Addr1	
D3	SPI_R_WN	SPI_R_WN
D2	CB3	CONTROL BITS
D1	CB2	
D0	CB1	

NOTE 1. SB bits are Sticky bits and need to be cleared.
NOTE 2. RO bits are Read Only bits.

Table 66. Register 7: 1-bit Loss of Digital Lock. Function Description

Name	Description	Function[1]
Loss_Dig_Lock	LOSS_DIG_LOCK	0 = Locked since last time register was cleared 1 = Loss of Digital Lock since last time register was cleared

1. This bit is a sticky bit and needs to be cleared with a SPI write of 1 to detect further Loss of Digital Lock occurrences.

Table 67. Register 7: 1-bit Loss of Analog Lock. Function Description

Name	Description	Function[1]
Loss_Anlg_Lock	LOSS_ANLG_LOCK	0 = Band Selection remained the same since last time register was cleared 1 = Band selection occurred since last time register was cleared

1. This bit is a sticky bit and needs to be cleared with a SPI write of 1 to detect further Band Selection occurrences.

Table 68. Register 7: 1-bit SPI Error. Function Description

Name	Description	Function[1]
Spi_error	SPI_ERROR	0 = No SPI write error detection 1 = SPI Write error

1. Spi_error Bit goes high if the SPI interface detects a cycle with the incorrect number of SCLK cycles between nCS asserted Low and nCS asserted High. The SPI interface expects 32 clock cycles between nCS asserted Low and nCS asserted High. Any Read/Write via the SPI interface with more or less than 32 clock cycles will result in the Spi_error Bit switched to 1. This bit is a sticky and needs to be cleared with a SPI write of 1 in order to detect further possible SPI Write/Read errors.

Table 69. Register 7: 3-bit Revision ID. Function Description

Name	Description	Factory Default
Rev_ID[3:1]	REV_ID	010

Table 70. Register 7: 4-bit Device ID. Function Description

Name	Description	Factory Default
Dev_ID[4:1]	DEV_ID	0111

Table 71. Register 7: 2-bit CALIB_VC Control Voltage Selection. Function Description

Name	Description	Factory Default	Function
Calib_Vc[2:1]	CALIB_VC Control Voltage Selection During Calibration	0	00 = VCC/2 01 = VCC × 0.366 10 = VCC × 0.63 11 = High-Z

Table 72. Register 7: 2-bit Clock Divider Mode. Function Description

Name	Description	Factory Defaults	Function
ClkDivMode[2:1]	CLK DIV MODE	00	00 = Clock Divider OFF 01 = Fast Lock Enabled 10 = Resync Enabled 11 = Reserved

Table 73. Register 7: 1-bit Band Select Clock Mode. Function Description

Name	Description	Factory Defaults	Function[1]
BandSelCM	BAND SELECT (CLOCK RATE)	0	0 = LOW (125kHz) 1 = HIGH (up to 500kHz logic sequence for Faster Lock applications)

1. BAND SELECT (CLOCK RATE) selects the speed of the logic sequence for the band selection. BandSelCM = 1 sets the logic sequence rate faster, which is recommended for fast lock operation and when high PFD frequencies are used. BandSelCM = 0 is recommended when low PFD frequencies (125kHz) are used. When using BandSelCM = 1, the value of the BAND SELECT CLOCK COUNTER (BndSelDiv[8:1]) must be less than or equal to 254.

Table 74. Register 7: 1-bit Feedback Select. Function Description

Name	Description	Factory Defaults	Function
FbkSel	FEEDBACK SELECT	1	0 = Divided (only allowed when RF_IN is not used, and when Sel_M0_Mux is set to 0) 1 = Fundamental

Table 75. Register 7: 3-bit RF Output Divider (÷M0) Select. Function Description

Name	Description	Factory Defaults	Function
RFDiv[3:1]	RF OUTPUT DIVIDER	000	000 = Div by 1 001 = Div by 2 010 = Div by 4 011 = Div by 8 100 = Div by 16 101 = Div by 32 110 = Div by 64 111 = Reserved

Table 76. Register 7: 1-bit SCLKE. Function Description

Name	Description	Factory Default	Function
Sclke	SCLKE	1	0 = Output Data in a Read Cycle on a Rising Edge of SCLK 1 = Output Data in a Read Cycle on a Falling Edge of SCLK

Table 77. Register 7: 1-bit READBACK_ADDR. Function Description

Name	Description	Function[1]
Rd_Addr[3:1]	READBACK_ADDR	000 = Register 0 001 = Register 1 010 = Register 2 011 = Register 3 100 = Register 4 101 = Register 5 110 = Register 6 111 = Register 7

1. In order to Read a register, the user must set the SPI_R_WN Bit to 1 (READ) and indicate the address of the register to read in the READBACK_ADDR Bit (Bits[D6:D4]).

Table 78. Register 7: 1-bit SPI_R_WN. Function Description

Name	Description	Function[1]
SPI_R_WN	SPI_R_WN	0 = WRITE 1 = READ

1. Writing this bit to a ‘1’ will allow the user to read back the register selected in READBACK_ADDR on the next 32 SCLK cycle. This bit will revert back to ‘0’ once it is written with ‘1’ and will not retain the ‘1’ value.

Table 79. Register 7: 3-bit Control Bits. Function Description

Name	Description	Function[1]
CB[3:1]	Control bits	111 = Register 7 is programmed

1. The user has to set CB[3:1] to 111 in order to write to Register 7.

6. Specifications

6.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8V97052 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 80. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DDX}[1]	3.63V
Analog Supply Voltage, V_{DDA}	3.63V
Input, V_I REF_IN Other Inputs (MUTE, SDI, FLSW, V_{TUNE})	-0.5 to V_{DDA} +0.5V
Outputs, V_O RF_OUT, nRF_OUT	-0.5 to V_{DDA} +0.5V
Outputs, V_O (SCLK, LD, nCS, MUX_OUT)	-0.5 to V_{DDA} +0.5V
Outputs, I_O Continuous Current Surge Current	 40mA 65mA
Outputs, IO (SCLK, LD, nCS, MUX_OUT) Continuous Current Surge Current	 8mA 13mA
Junction Temperature, T_J	125°C
Storage Temperature, TSTG	-65°C to 150°C

1. V_{DDX} denotes V_{DDD}, $V_{\_CP}$, V_{DD_SD}, V_{VCO}.

6.2 DC Electrical Characteristics

Table 81. Power Supply DC Characteristics, V_{DDX} = V_{DDA} = 3.3V ±5%, T_A = -40°C to +85°C[1][2][3]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{DDX}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DDX}	Power Supply Current[4]			72	91	mA
I_{DDA}	Analog Supply Current[5]	RF_OUT – active		61	76	mA
		RF_OUT – muted		37	47	mA
I_{VCO}	VCO Supply Current			37	47	mA
–	Power-down mode[6]	CE = 0 or Register 2, bit D5 = 1		7	9	mA

1. V_{DDX} denotes V_{DDD}, $V_{\_CP}$, V_{DD_SD}, V_{VCO}.
2. RF outputs terminated 50Ω ±1% to V_{DDA}.
3. Output power set to +2.5dBm.
4. I_{DDX} denotes I_{DDD} + $I_{\_CP}$ + I_{DD_SD} + I_{VCO}.
5. I_{DDA} is dependent on the value of the M0 output divider. The numbers indicated for I_{DDA} show the current consumption when using the output divider M0 = 64, for which input frequency = 40MHz, doubler is enabled, feedback divider = 50, and $I_{\_CP}$ = 2.19mA.
6. In power-down mode, VCO calibration by writing to register 0 should not be performed. Doing so will increase power-down current by 10mA. CE pin must be pulled high before powering up the device.

Table 82. Output Divider Incremental Current[1]

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Output Divider Supply Current	Divide by 2		6		mA
	Divide by 4		6		mA
	Divide by 8		1		mA
	Divide by 16		1		mA
	Divide by 32		2		mA
	Divide by 64		2		mA

1. RF output divider (÷MO) has an incremental increase in current as the divider value increases. This specification is the incremental current change per output divider step. For example, current of divide-by-2 is 6.5mA more than divide-by-1, current of divide-by-4 is 7mA more than divide-by-2, and so on. The total increase from ÷1 to ÷64 is 6.5mA + 7mA + 1mA + 1.5mA + 2mA + 2mA = 20mA.

Table 83. Typical Current by Power Domain[1]

Pin Name	Pin Number	Typical Current	Unit
$V_{\_CP}$	6	27	mA
V_{VCO}	16, 17	37	mA
V_{DDD}	28	1	mA
V_{DD_SD}	32	6	mA
V_{DDA}	10	61	mA

1. Operating conditions are:
   REF_IN = 40MHz
   D = 1 (Ref Doubler is on)
   INT = 50 (integer mode)
   RF divider = ÷2
   RF_OUT = 2GHz
   RF_{POWER} = +2.5dBm
   Charge pump = 2.19mA

Table 84. LVCMOS DC Characteristics, $V_{DDX} = V_{DDA} = 3.3V \pm 5\%$, T_A = -40°C to 85°C[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage	MUTE, CE		1.8		V_{DDx}	V
		SDI, SCLK, nCS		1.5		V_{DDx}	V
V_{IL}	Input Low Voltage			-0.3		0.6	V
I_{IH}	Input High Current	SDI, MUTE, CE	V_{DDx} = 3.465V, V_{IN} = 1.8V			5	µA
		SCLK, nCS	V_{DDx} = 3.465V, V_{IN} = 1.8V			150	µA
I_{IL}	Input Low Current	SDI, MUTE, CE	V_{DDx} = 3.465V, V_{IN} = 0V	-150			µA
		SCLK, nCS	V_{DDx} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage	MUX_OUT, LD	V_{DDx} = 3.465V; I_{OH} = -500µA		V_{DDX} – 0.4		V
V_{OL}	Output Low Voltage	MUX_OUT, LD	V_{DDx} = 3.465V; I_{OL} = 500µA		0.4		V

1. V_{DDX} denotes V_{DDD}, $V_{\_CP}$, V_{DD_SD}, V_{VCO}.

6.3 AC Electrical Characteristics

Table 85. AC Characteristics, $V_{DDX} = V_{DDA} = 3.3V \pm 5\%$, T_A = -40°C to 85°C[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
REF_IN	Input Reference Frequency[2]		Ref doubler disabled	5		310	MHz
			Ref doubler enabled	5		100	MHz
V_{PP}	Input Sensitivity	REF_IN	Biased at $V_{DDA}/2$[3]	0.7		V_{DDA}	V
f_{VCO}	VCO Frequency		Fundamental VCO mode	2200		4400	MHz
RF_IN_{CLK}	External Clock provided to RF_IN		SEL_M0_Mux set to 1	5[4]		4400	MHz
V_{PP}	Input Sensitivity	RF_IN	Biased at $V_{DDA}/2$[3]		1		V
f_{RF_OUT}	Output Frequency		Divider values: 1, 2, 4, 8, 16, 32, 64	34.375		4400	MHz
f_{PFD}	PFD Frequency		Fractional mode: SDM type = SSMF-II			110	MHz
			Fractional mode: SDM type = SSMF-B			88	MHz
			Integer mode			310	MHz
K_{VCO}	VCO Sensitivity				69		MHz/V
t_{LOCK}	PLL Lock Time		Time from low to high nCS until low to high LD		86		µs
–	Output Power Variation				±1		dB
–	RF Output Power		Muted		<-80		dBm
–	Min/Max VCO tuning voltage				0.5 / 2.5		V

1. V_{DDX} denotes V_{DDD}, $V_{\_CP}$, V_{DD_SD}, V_{VCO}.
2. For REF_IN < 10MHz, the slew rate must be > 21V/µs.
3. AC-coupling the reference signal ensures $V_{DDA}/2$ biasing.
4. For RF_IN < 5MHz, the slew rate must be > 1000V/µs.

Table 86. $RF\_OUT_{[A:B]}$ Phase Noise and Jitter Characteristics, $V_{DDX} = V_{DDA} = 3.3V \pm 5\%$, T_A = -40°C to 85°C[1][2][3]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
tjit(Ø)	RMS Phase Jitter (random)	f = 2GHz Integration range: 12kHz – 20MHz	155	181	209	fs
$\varphi_N(100)$	RF Output Phase Noise Performance at 2GHz	100Hz offset from carrier	-107	-97	-87	dBc/Hz
$\varphi_N(1k)$		1kHz offset from carrier	-114	-106	-98	dBc/Hz
$\varphi_N(10k)$		10kHz offset from carrier	-108	-105	-102	dBc/Hz
$\varphi_N(100k)$		100kHz offset from carrier	-113	-111	-109	dBc/Hz
$\varphi_N(1M)$		1M offset from carrier	-135	-133	-131	dBc/Hz

Table 86. $RF\_OUT_{[A:B]}$ Phase Noise and Jitter Characteristics, $V_{DDX} = V_{DDA} = 3.3V \pm 5\%$, T_A = -40°C to 85°C[1][2][3] (Cont.)

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
tjit(Ø)	RMS Phase Jitter (random)	f = 201.5MHz Integration range: 12kHz – 20MHz		372		fs
$\varphi_N(100)$	RF Output Phase Noise Performance at 201.5MHz	100Hz offset from carrier		-104		dBc/Hz
$\varphi_N(1k)$		1kHz offset from carrier		-119		dBc/Hz
$\varphi_N(10k)$		10kHz offset from carrier		-128		dBc/Hz
$\varphi_N(100k)$		100kHz offset from carrier		-132		dBc/Hz
$\varphi_N(1M)$		1M offset from carrier		-141		dBc/Hz
$\varphi_N(SYNTH)$	Normalized Phase Noise Floor			-228		dBc/Hz
$\varphi_N(1/f)$	Normalized 1/f Noise[4]	10kHz offset; normalized to 1GHz		-122		dBc/Hz

1. Internal VCO is used.
2. V_{DDX} denotes V_{DDD}, $V_{\_CP}$, V_{DD_SD}, V_{VCO}.
3. Output power setting = +11.5dBm.
4. $\varphi_N(1/f) = \varphi_N(RF\_OUT) - 10 \text{ Log}(10kHz/f) - 10 \text{ Log }(f_{RF\_OUT}/1GHz)$ where $\varphi_N(1/f)$ is the 1/f noise contribution at a RF_OUT frequency (f_{RF_OUT}) and at a frequency offset f.

Table 87. $RF\_OUT_{[A:B]}$ Phase Noise and Jitter Characteristics, $V_{DDX} = V_{DDA} = 3.3V \pm 5\%$, T_A = -40°C to 85°C[1][2][3]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
tjit(Ø)	RMS Phase Jitter (random)	f = 3.5GHz Integration range: 12kHz – 20MHz		179		fs
$\varphi_N(100)$	RF Output Phase Noise Performance at 3.5GHz	100Hz offset from carrier		-91		dBc/Hz
$\varphi_N(1k)$		1kHz offset from carrier		-99		dBc/Hz
$\varphi_N(10k)$		10kHz offset from carrier		-103		dBc/Hz
$\varphi_N(100k)$		100kHz offset from carrier		-107		dBc/Hz
$\varphi_N(1M)$		1M offset from carrier		-121		dBc/Hz
tjit(Ø)	RMS Phase Jitter (random)	f = 4.3GHz Integration range: 12kHz – 20MHz		103		fs
$\varphi_N(100)$	RF Output Phase Noise Performance at 4.3MHz	100Hz offset from carrier		-89		dBc/Hz
$\varphi_N(1k)$		1kHz offset from carrier		-99		dBc/Hz
$\varphi_N(10k)$		10kHz offset from carrier		-105		dBc/Hz
$\varphi_N(100k)$		100kHz offset from carrier		-112		dBc/Hz
$\varphi_N(1M)$		1M offset from carrier		-123		dBc/Hz

1. Internal VCO is used.
2. V_{DDX} denotes V_{DDD}, $V_{\_CP}$, V_{DD_SD}, V_{VCO}.
3. Output power setting = +11.5dBm.

7. Phase Noise Plots

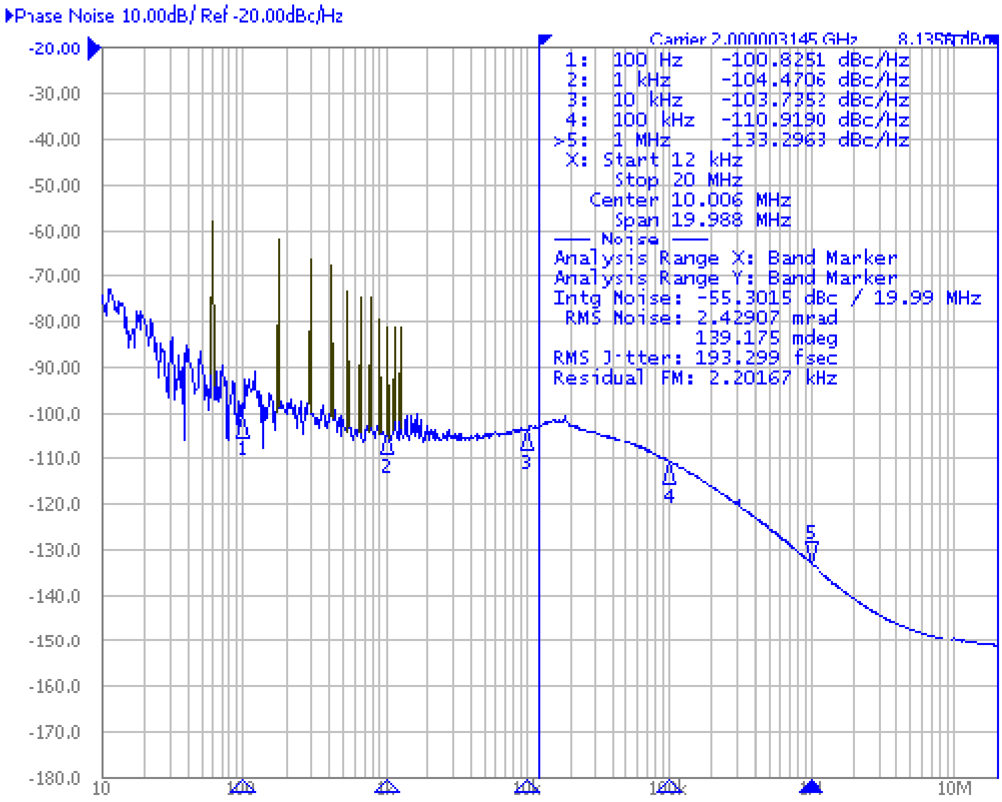


Figure 12. Phase Noise at 2GHz (3.3V)

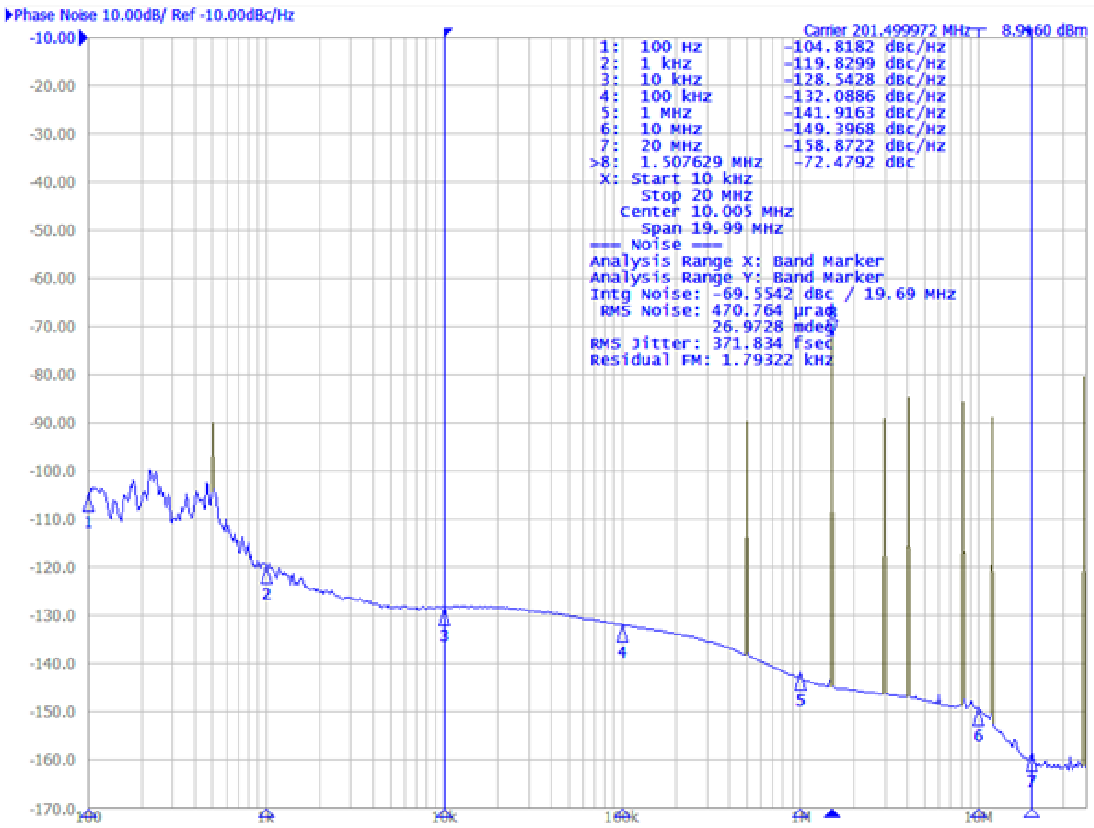


Figure 13. Phase Noise at 201.5 MHz (3.3V)

8. Applications Information

8.1 Loop Filter Calculations

8.2 2nd Order Loop Filter

This section helps design a 2nd order loop filter for the 8V97052. A general 2nd order loop filter is shown in Figure 14. Step-by-step calculations to determine Rz, Cz and Cp values for a desired loop bandwidth are described below. Required parameters are provided. A spreadsheet for calculating the loop filter values is also available.

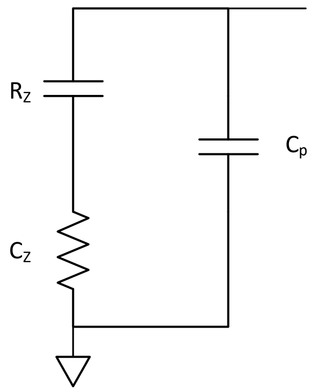


Figure 14. Typical 2nd Order Loop Filter

1. Determine desired loop bandwidth fc.
2. Calculate Rz:

$$Rz = \frac{2 * \pi * fc * N}{Icp * Kvco}$$

Where,

Icp is charge pump current. Icp is programmable from 310µA to 5mA.

N is effective feedback divider. N must be programmed into the following value.

$$N = \frac{Fvco}{Fpd}$$

F_{VCO} is VCO frequency.

VCO frequency range: 2200MHz to 4400MHz

Fpd is phase detector input frequency.

$$Fpd = \frac{F\_ref}{Pv}$$

F_ref is reference clock (REF_IN) input frequency.

Pv is overall pre-divider setting.

Kvco is VCO gain. Kvco = 40MHz/V

3. Calculate Cz:

$$Cz = \frac{\alpha}{2 * \pi * fc * Rz}$$

Where,

α = fc/ fz, user can determine an α number.
α >6 is recommended.

fz is frequency at zero.

4. Calculate Cp:

$$Cp = \frac{Cz}{\alpha * \beta}$$

Where,

β = fp/fc, user can determine β number.
β >4 is recommended.

fp is frequency at pole.

5. Verify Phase Margin (*PM)*

$$PM = \arctan\left(\frac{b-1}{2 * \sqrt{b}}\right)$$

Where,

$$b = 1 + \frac{Cz}{Cp}$$

The phase margin (PM) should be greater than 50°.

A spreadsheet for calculating the loop filter component values is available at www.renesas.com. To use the spreadsheet, the user simply enters the following parameters:

fc, F_ref, P_V, Icp, F_{VCO}, α and β.

The spreadsheet will provide the component values, Rz, Cz, and Cp as the result. The spreadsheet also calculates the maximum phase margin for verification.

8.3 3rd Order Loop Filter

This section helps design a 3rd order loop filter for the 8V97052. A general 3rd order loop filter is shown in Figure 15.

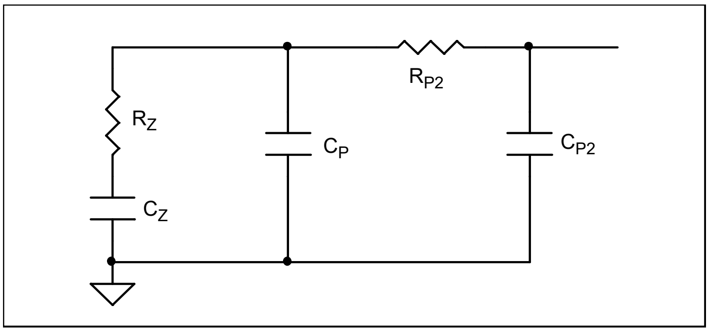


Figure 15. Typical 3rd Order Loop Filter

The Rz, Cz and Cp can be calculated as 2nd order loop filter.
The following equation help determine the 3rd order loop filter Rp2 and Cp2.

Pick an Rp2 value. Rp2 ~ 1.5xRz is suggested.

$$C_{P2} = \frac{R_Z * C_P}{R_{P2} * \gamma}$$

Where,

γ is ratio between the 1st pole frequency and the 2nd pole frequency. γ >4 is recommended.

8.4 Recommendations for Unused Input and Output Pins

8.4.1 Inputs

8.4.1.1 LVCMOS Control Pins

All control pins have internal pull-up and pull-down resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

8.4.2 Outputs

8.4.2.1 Output Pins

For any unused output, it can be left floating and disabled.

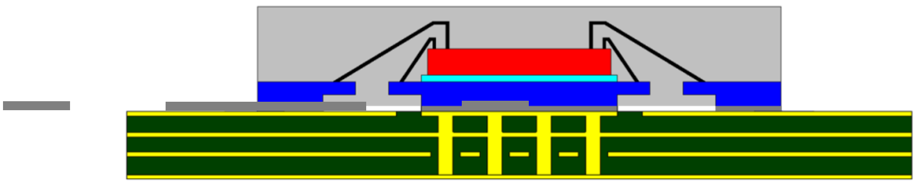
8.5 Case Temperature Considerations

This device supports applications in a natural convection environment which does not have any thermal conductivity through ambient air. The Printed Circuit Board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters which is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter Ψ_{JB} (Psi-JB) to calculate the junction temperature (T_J) and ensure it does not exceed the maximum allowed junction temperature in the Absolute Maximum Rating table.

The junction-to-board thermal characterization parameter, Ψ_{JB}, is calculated using the following equation:

$T_J = T_{CB} + \Psi_{JB} \times P_d$, Where

- **T_J =** Junction temperature at steady state condition in (°C).
- **T_{CB} =** Case temperature (Bottom) at steady state condition in (°C).
- **Ψ_{JB} =** Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.
- **P_d =** power dissipation (W) in desired operating configuration.



The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. It's critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC case temperature (T_{CB}). A good connection ensures that temperature at the exposed pad (T_{CB}) and the board temperature (T_B) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

Example calculation for junction temperature (T_J): $T_J = T_{CB} + \Psi_{JB} \times P_d$

Package type:	32-Lead VFQFPN
Body size:	3 × 3 × 0.9 mm
ePad size:	3.15 × 3.15 mm
Thermal via:	4 × 4 matrix
Ψ_{JB}	0.34ºC/W
T_{CB}	105ºC
P_d	0.6618W

For the variables above, the junction temperature is equal to 105.2ºC. Since this is below the maximum junction temperature of 125ºC, there are no long term reliability concerns.

9. Reliability Information

Table 88. θ_{JA} vs. Air Flow Table for a 32-VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	34.34°C/W	30.7°C/W	29.12°C/W

Table 89. θ_{JB} vs. Air Flow Table for a 32-VFQFN

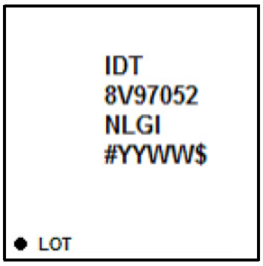
θ_{JB}[1] vs. Air Flow	
Meters per Second	**0**
Multi-Layer PCB, JEDEC Standard Test Boards	0.472°C/W

1. θ_{JB} is independent of airflow.

10. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

11. Marking Diagram

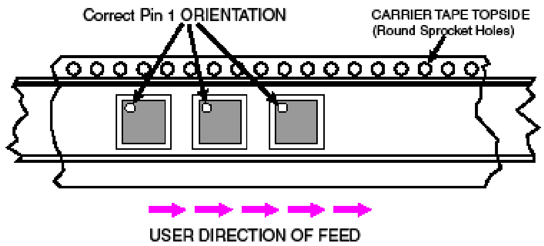


- Line 1 denotes the part number prefix.
- Line 2 and 3 indicate the part number.
- Line 4 denotes the following:
  - "YYWW" is the last digit of the year and week that the part was assembled.
  - "$" denotes mark code

12. Ordering Information

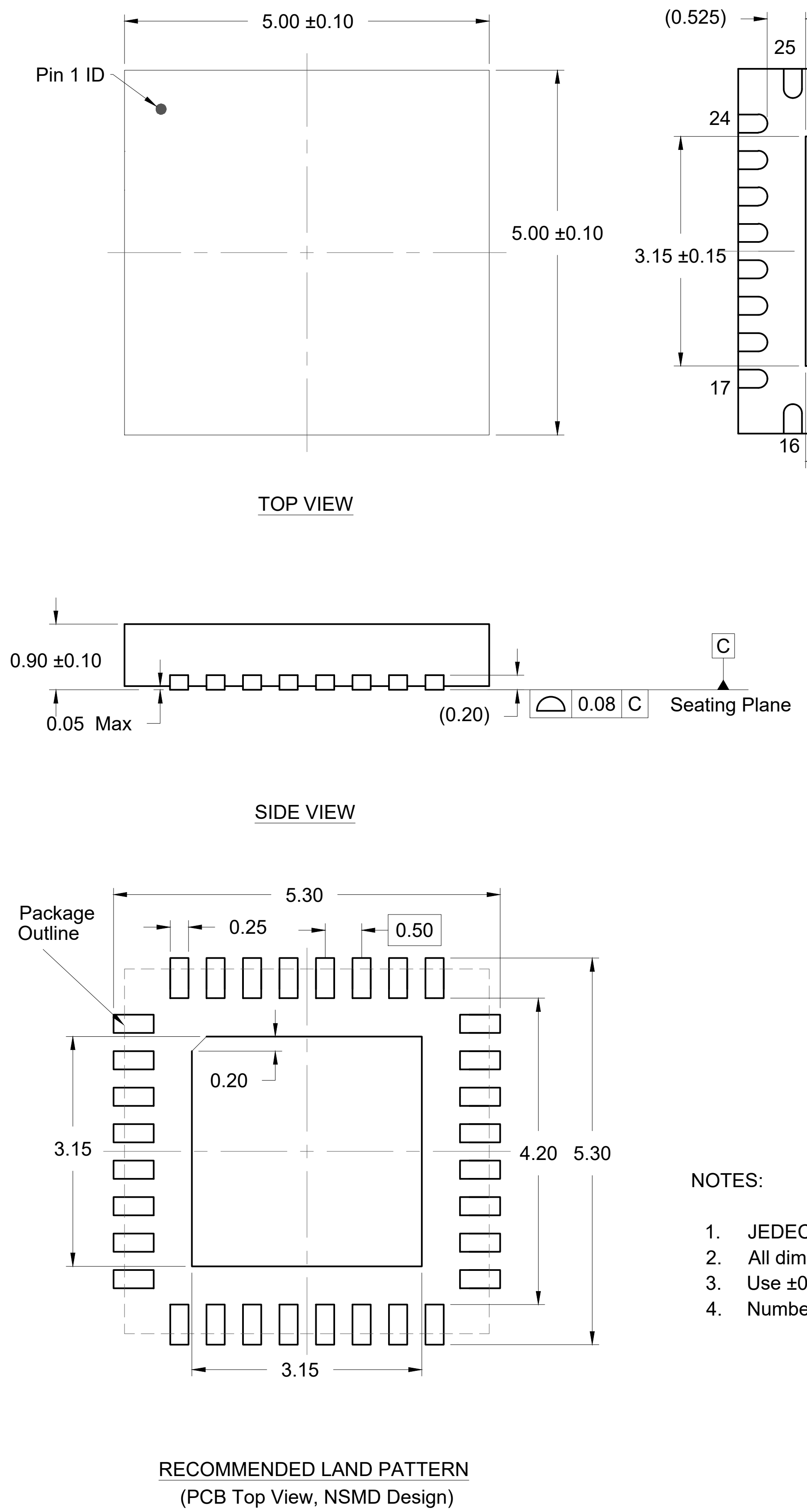
Part Number	Marking	Package	Carrier Type	Temp. Range
8V97052NLGI	IDT8V97052NLGI	32-VFQFPN, Lead Free	Tray	-40°C to +85°C
8V97052NLGI8	IDT8V97052NLGI	32-VFQFPN, Lead Free	Tape and Reel	-40°C to +85°C

Table 90. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
NLGI8	Quadrant 1 (EIA-481-C)	

13. Revision History

Revision	Date	Description
-	Feb 6, 2023	Updated POD links in Ordering Information.
1.1	May 20, 2021	▪ Updated Features, RF_IN Input, RF_IN Input, and DC Electrical Characteristics ▪ Completed other minor changes
1.0	Apr 29, 2021	Initial release.



NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

IMPORTANT NOTICE AND DISCLAIMER

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