# DATA SHEET

**NOTICE**
PLEASE SEE THE P87C552 DATA SHEET FOR NEW DESIGN-INS

# 87C552

# 80C51 8-bit microcontroller

8K/256 OTP, 8 channel 10 bit A/D, I$^2$C, PWM, capture/compare, high I/O

**PHILIPS**

# 80C51 8-bit microcontroller

## 8K/256 OTP, 8 channel 10 bit A/D, I2C, PWM, capture/compare, high I/O

## 87C552

## DESCRIPTION

The 87C552 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 87C552 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C552—8k bytes mask programmable ROM

- 80C552—ROMless version of the 83C552

- 87C552—8k bytes EPROM

The 87C552 contains a 8k × 8 a volatile 256 × 8 read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I2C-bus), a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 87C552 can be expanded using standard TTL compatible memories and logic.

In addition, the 87C552 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte, and 17 three-byte. With a 16MHz crystal, 58% of the instructions are executed in 0.75μs and 40% in 1.5μs. Multiply and divide instructions require 3μs.

## FEATURES

- 80C51 central processing unit

- 8k × 8 EPROM expandable externally to 64k bytes

- An additional 16-bit timer/counter coupled to four capture registers and three compare registers

- Two standard 16-bit timer/counters

- 256 × 8 RAM, expandable externally to 64k bytes

- Capable of producing eight synchronized, timed outputs

- A 10-bit ADC with eight multiplexed analog inputs

- Two 8-bit resolution, pulse width modulation outputs

- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs

- I2C-bus serial I/O port with byte oriented master and slave functions

- Full-duplex UART compatible with the standard 80C51

- On-chip watchdog timer

- 16MHz speed

- Extended temperature ranges

- OTP package available

## ORDERING INFORMATION

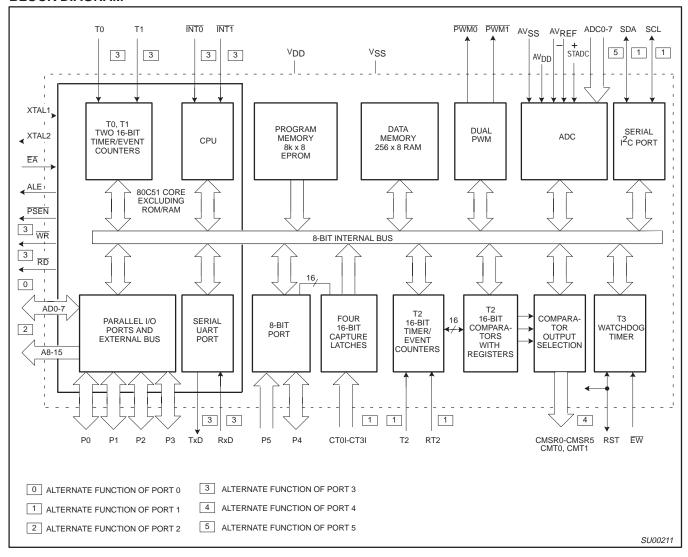| EPROM | TEMPERATURE °C AND PACKAGE | FREQ MHz | DRAWING NUMBER |
|---|---|---|---|
| S87C552-4A68 | 0 to +70, Plastic Leaded Chip Carrier | 16 | SOT188-3 |
| S87C552-4BA | 0 to +70, Plastic Quad Flat Pack | 16 | SOT318-2 |
| S87C552-5A68 | −40 to +85, Plastic Leaded Chip Carrier | 16 | SOT188-3 |

**NOTE:**
1. For ROM and ROMless see data sheet 80C552/83C552

## 80C51 8-bit microcontroller

8K/256 OTP, 8 channel 10 bit A/D, I2C, PWM, capture/compare, high I/O
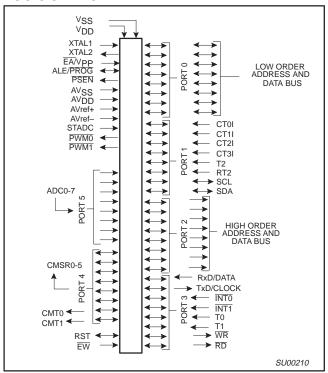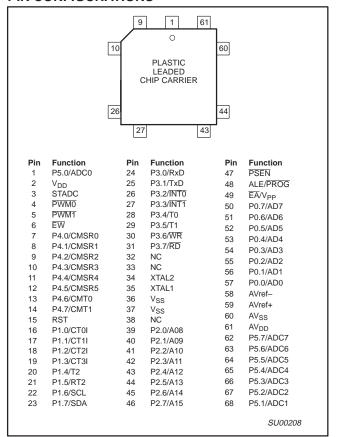
**87C552**

## BLOCK DIAGRAM



| 0 | ALTERNATE FUNCTION OF PORT 0 | 3 | ALTERNATE FUNCTION OF PORT 3 |
| 1 | ALTERNATE FUNCTION OF PORT 1 | 4 | ALTERNATE FUNCTION OF PORT 4 |
| 2 | ALTERNATE FUNCTION OF PORT 2 | 5 | ALTERNATE FUNCTION OF PORT 5 |

SU00211

# 80C51 8-bit microcontroller

## 8K/256 OTP, 8 channel 10 bit A/D, I²C, PWM, capture/compare, high I/O

**87C552**

## LOGIC SYMBOL



SU00210

## PIN CONFIGURATIONS



PLASTIC LEADED CHIP CARRIER

| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | P5.0/ADC0 | 24 | P3.0/RxD | 47 | $\overline{PSEN}$ |
| 2 | V$_{DD}$ | 25 | P3.1/TxD | 48 | ALE/$\overline{PROG}$ |
| 3 | STADC | 26 | P3.2/$\overline{INT0}$ | 49 | $\overline{EA}$/V$_{PP}$ |
| 4 | $\overline{PWM0}$ | 27 | P3.3/$\overline{INT1}$ | 50 | P0.7/AD7 |
| 5 | $\overline{PWM1}$ | 28 | P3.4/T0 | 51 | P0.6/AD6 |
| 6 | $\overline{EW}$ | 29 | P3.5/T1 | 52 | P0.5/AD5 |
| 7 | P4.0/CMSR0 | 30 | P3.6/$\overline{WR}$ | 53 | P0.4/AD4 |
| 8 | P4.1/CMSR1 | 31 | P3.7/$\overline{RD}$ | 54 | P0.3/AD3 |
| 9 | P4.2/CMSR2 | 32 | NC | 55 | P0.2/AD2 |
| 10 | P4.3/CMSR3 | 33 | NC | 56 | P0.1/AD1 |
| 11 | P4.4/CMSR4 | 34 | XTAL2 | 57 | P0.0/AD0 |
| 12 | P4.5/CMSR5 | 35 | XTAL1 | 58 | AVref– |
| 13 | P4.6/CMT0 | 36 | V$_{SS}$ | 59 | AVref+ |
| 14 | P4.7/CMT1 | 37 | V$_{SS}$ | 60 | AV$_{SS}$ |
| 15 | RST | 38 | NC | 61 | AV$_{DD}$ |
| 16 | P1.0/CT0I | 39 | P2.0/A08 | 62 | P5.7/ADC7 |
| 17 | P1.1/CT1I | 40 | P2.1/A09 | 63 | P5.6/ADC6 |
| 18 | P1.2/CT2I | 41 | P2.2/A10 | 64 | P5.5/ADC5 |
| 19 | P1.3/CT3I | 42 | P2.3/A11 | 65 | P5.4/ADC4 |
| 20 | P1.4/T2 | 43 | P2.4/A12 | 66 | P5.3/ADC3 |
| 21 | P1.5/RT2 | 44 | P2.5/A13 | 67 | P5.2/ADC2 |
| 22 | P1.6/SCL | 45 | P2.6/A14 | 68 | P5.1/ADC1 |
| 23 | P1.7/SDA | 46 | P2.7/A15 | | |

SU00208

## PLASTIC QUAD FLAT PACK PIN FUNCTIONS



PQFP

| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|---|---|
| 1 | P4.1/CMSR1 | 21 | NC | 41 | P2.3/A11 | 61 | AV$_{SS}$ |
| 2 | P4.2/CMSR2 | 22 | NC | 42 | P2.4/A12 | 62 | NC |
| 3 | NC | 23 | P3.3/$\overline{INT1}$ | 43 | NC | 63 | AV$_{DD}$ |
| 4 | P4.3/CMSR3 | 24 | P3.4/T0 | 44 | NC | 64 | P5.7/ADC7 |
| 5 | P4.4/CMSR4 | 25 | P3.5/T1 | 45 | P2.5/A13 | 65 | P5.6/ADC6 |
| 6 | P4.5/CMSR5 | 26 | P3.6/$\overline{WR}$ | 46 | P2.6/A14 | 66 | P5.5/ADC5 |
| 7 | P4.6/CMT0 | 27 | P3.7/$\overline{RD}$ | 47 | P2.7/A15 | 67 | P5.4/ADC4 |
| 8 | P4.7/CMT1 | 28 | NC | 48 | $\overline{PSEN}$ | 68 | P5.3/ADC3 |
| 9 | RST | 29 | NC | 49 | ALE/$\overline{PROG}$ | 69 | P5.2/ADC2 |
| 10 | P1.0/CT0I | 30 | NC | 50 | $\overline{EA}$/V$_{PP}$ | 70 | P5.1/ADC1 |
| 11 | P1.1/CT1I | 31 | XTAL2 | 51 | P0.7/AD7 | 71 | P5.0/ADC0 |
| 12 | P1.2/CT2I | 32 | XTAL1 | 52 | P0.6/AD6 | 72 | V$_{DD}$ |
| 13 | P1.3/CT3I | 33 | IC | 53 | P0.5/AD5 | 73 | IC |
| 14 | P1.4/T2 | 34 | V$_{SS}$ | 54 | P0.4/AD4 | 74 | STADC |
| 15 | P1.5/RT2 | 35 | V$_{SS}$ | 55 | P0.3/AD3 | 75 | $\overline{PWM0}$ |
| 16 | P1.6/SCL | 36 | V$_{SS}$ | 56 | P0.2/AD2 | 76 | $\overline{PWM1}$ |
| 17 | P1.7/SDA | 37 | NC | 57 | P0.1/AD1 | 77 | $\overline{EW}$ |
| 18 | P3.0/RxD | 38 | P2.0/A08 | 58 | P0.0/AD0 | 78 | NC |
| 19 | P3.1/TxD | 39 | P2.1/A09 | 59 | AVref– | 79 | NC |
| 20 | P3.2/$\overline{INT0}$ | 40 | P2.2/A10 | 60 | AVref+ | 80 | P4.0/CMSR0 |

NC = Not Connected
IC = Internally Connected (do not use)

SU00209

# 80C51 8-bit microcontroller

**87C552**

8K/256 OTP, 8 channel 10 bit A/D, I$^2$C, PWM, capture/compare, high I/O

## PIN DESCRIPTION

| MNEMONIC | PIN NO. PLCC | PIN NO. QFP | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|
| V$_{DD}$ | 2 | 72 | I | **Digital Power Supply:** +5V power supply pin during normal operation, idle and power-down mode. |
| STADC | 3 | 74 | I | **Start ADC Operation:** Input starting analog to digital conversion (ADC operation can also be started by software). |
| $\overline{\text{PWM0}}$ | 4 | 75 | O | **Pulse Width Modulation:** Output 0. |
| $\overline{\text{PWM1}}$ | 5 | 76 | O | **Pulse Width Modulation:** Output 1. |
| $\overline{\text{EW}}$ | 6 | 77 | I | **Enable Watchdog Timer:** Enable for T3 watchdog timer and disable power-down mode. |
| P0.0-P0.7 | 57-50 | 58-51 | I/O | **Port 0:** Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1s. Port 0 is also used to input the code byte during programming and to output the code byte during verification. |
| P1.0-P1.7 | 16-23 | 10-17 | I/O | **Port 1:** 8-bit I/O port. Alternate functions include: |
|  | 16-21 | 10-15 | I/O | **(P1.0-P1.5):** Quasi-bidirectional port pins. |
|  | 22-23 | 16-17 | I/O | **(P1.6, P1.7):** Open drain port pins. |
|  | 16-19 | 10-13 | I | **CT0I-CT3I (P1.0-P1.3):** Capture timer input signals for timer T2. |
|  | 20 | 14 | I | **T2 (P1.4):** T2 event input. |
|  | 21 | 15 | I | **RT2 (P1.5):** T2 timer reset signal. Rising edge triggered. |
|  | 22 | 16 | I/O | **SCL (P1.6):** Serial port clock line I$^2$C-bus. |
|  | 23 | 17 | I/O | **SDA (P1.7):** Serial port data line I$^2$C-bus. Port 1 is also used to input the lower order address byte during EPROM programming and verification. A0 is on P1.0, etc. |
| P2.0-P2.7 | 39-46 | 38-42, 45-47 | I/O | **Port 2:** 8-bit quasi-bidirectional I/O port. Alternate function: High-order address byte for external memory (A08-A15). Port 2 is also used to input the upper order address during EPROM programming and verification. A8 is on P2.0, A9 on P2.1, through A12 on P2.4. |
| P3.0-P3.7 | 24-31 | 18-20, 23-27 | I/O | **Port 3:** 8-bit quasi-bidirectional I/O port. Alternate functions include: |
|  | 24 | 18 |  | **RxD(P3.0):** Serial input port. |
|  | 25 | 19 |  | **TxD (P3.1):** Serial output port. |
|  | 26 | 20 |  | **$\overline{\text{INT0}}$ (P3.2):** External interrupt. |
|  | 27 | 23 |  | **$\overline{\text{INT1}}$ (P3.3):** External interrupt. |
|  | 28 | 24 |  | **T0 (P3.4):** Timer 0 external input. |
|  | 29 | 25 |  | **T1 (P3.5):** Timer 1 external input. |
|  | 30 | 26 |  | **$\overline{\text{WR}}$ (P3.6):** External data memory write strobe. |
|  | 31 | 27 |  | **$\overline{\text{RD}}$ (P3.7):** External data memory read strobe. |
| P4.0-P4.7 | 7-14 | 80, 1-2 4-8 | I/O | **Port 4:** 8-bit quasi-bidirectional I/O port. Alternate functions include: |
|  | 7-12 | 80, 1-2 4-6 | O | **CMSR0-CMSR5 (P4.0-P4.5):** Timer T2 compare and set/reset outputs on a match with timer T2. |
|  | 13, 14 | 7, 8 | O | **CMT0, CMT1 (P4.6, P4.7):** Timer T2 compare and toggle outputs on a match with timer T2. |
| P5.0-P5.7 | 68-62, 1 | 71-64, | I | **Port 5:** 8-bit input port. **ADC0-ADC7 (P5.0-P5.7):** Alternate function: Eight input channels to ADC. |
| RST | 15 | 9 | I/O | **Reset:** Input to reset the 87C552. It also provides a reset pulse as output when timer T3 overflows. |
| XTAL1 | 35 | 32 | I | **Crystal Input 1:** Input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external clock signal when an external oscillator is used. |
| XTAL2 | 34 | 31 | O | **Crystal Input 2:** Output of the inverting amplifier that forms the oscillator. Left open-circuit when an external clock is used. |
| V$_{SS}$ | 36, 37 | 34-36 | I | **Digital ground.** |
| $\overline{\text{PSEN}}$ | 47 | 48 | O | **Program Store Enable:** Active-low read strobe to external program memory. |

# 80C51 8-bit microcontroller

8K/256 OTP, 8 channel 10 bit A/D, I²C, PWM, capture/compare, high I/O

**87C552**

## PIN DESCRIPTION (Continued)

| MNEMONIC | PIN NO. PLCC | PIN NO. QFP | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|
| ALE/$\overline{PROG}$ | 48 | 49 | O | **Address Latch Enable:** Latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods. During an external data memory access, one ALE pulse is skipped. ALE can drive up to eight LS TTL inputs and handles CMOS inputs without an external pull-up. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming. |
| $\overline{EA}$/V$_{PP}$ | 49 | 50 | I | **External Access:** When $\overline{EA}$ is held at TTL level high, the CPU executes out of the internal program ROM provided the program counter is less than 8192. When $\overline{EA}$ is held at TTL low level, the CPU executes out of external program memory. $\overline{EA}$ is not allowed to float. This pin also receives the 12.75V programming supply voltage (V$_{PP}$) during EPROM programming. |
| AV$_{REF-}$ | 58 | 59 | I | **Analog to Digital Conversion Reference Resistor:** Low-end. |
| AV$_{REF+}$ | 59 | 60 | I | **Analog to Digital Conversion Reference Resistor:** High-end. |
| AV$_{SS}$ | 60 | 61 | I | **Analog Ground** |
| AV$_{DD}$ | 61 | 63 | I | **Analog Power Supply** |

**NOTE:**
1. To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher or lower than V$_{DD}$ + 0.5V or V$_{SS}$ − 0.5V, respectively.

## OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

## RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V$_{DD}$ and RST must come up at the same time for a proper start-up.

## IDLE MODE

In the idle mode, the CPU puts itself to sleep while some of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

## POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON. Table 1 shows the state of the I/O ports during low current operating modes.

**Table 1. External Pin Status During Idle and Power-Down Modes**

| MODE | PROGRAM MEMORY | ALE | $\overline{PSEN}$ | PORT 0 | PORT 1 | PORT 2 | PORT 3 | PORT 4 | PWM0/ PWM1 |
|---|---|---|---|---|---|---|---|---|---|
| Idle | Internal | 1 | 1 | Data | Data | Data | Data | Data | High |
| Idle | External | 1 | 1 | Float | Data | Address | Data | Data | High |
| Power-down | Internal | 0 | 0 | Data | Data | Data | Data | Data | High |
| Power-down | External | 0 | 0 | Float | Data | Data | Data | Data | High |

## 80C51 8-bit microcontroller

8K/256 OTP, 8 channel 10 bit A/D, I$^2$C, PWM, capture/compare, high I/O

**87C552**

### Serial Control Register (S1CON) – See Table 2

**S1CON (D8H)**

| CR2 | ENS1 | STA | STO | SI | AA | CR1 | CR0 |
|-----|------|-----|-----|----|----|-----|-----|

**Bits CR0, CR1 and CR2 determine the serial clock frequency that is generated in the master mode of operation.**

### Table 2.  Serial Clock Rates

| CR2 | CR1 | CR0 | BIT FREQUENCY (kHz) AT f$_{OSC}$ | | | f$_{OSC}$ DIVIDED BY |
|-----|-----|-----|-------|--------|--------|----------------------|
| | | | **6MHz** | **12MHz** | **16MHz** | |
| 0 | 0 | 0 | 23 | 47 | 62.5 | 256 |
| 0 | 0 | 1 | 27 | 54 | 71 | 224 |
| 0 | 1 | 0 | 31.25 | 62.5 | 83.3 | 192 |
| 0 | 1 | 1 | 37 | 75 | 100 | 160 |
| 1 | 0 | 0 | 6.25 | 12.5 | 17 | 960 |
| 1 | 0 | 1 | 50 | 100 | 133 [1] | 120 |
| 1 | 1 | 0 | 100 | 200 | 267 [1] | 60 |
| 1 | 1 | 1 | 0.25 < 62.5 | 0.5 < 62.5 | 0.67 < 56 | 96 × (256 – (reload value Timer 1)) |
| | | | 0 to 225 | 0 to 224 | 0 to 223 | Timer 1 in Mode 2. |

**NOTE:**
1.  These frequencies exceed the upper limit of 100kHz of the I$^2$C-bus specification and cannot be used in an I$^2$C-bus application.

### ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

| PARAMETER | RATING | UNIT |
|-----------|--------|------|
| Storage temperature range | –65 to +150 | °C |
| Voltage on $\overline{EA}$/V$_{PP}$ to V$_{SS}$ | –0.5 to +13 | V |
| Voltage on any other pin to V$_{SS}$ | –0.5 to +6.5 | V |
| Input, output DC current on any single I/O pin | 5.0 | mA |
| Power dissipation (based on package heat transfer limitations, not device power consumption) | 1.0 | W |

**NOTES:**
1.  Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2.  This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3.  Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V$_{SS}$ unless otherwise noted.

### DEVICE SPECIFICATIONS

| TYPE | SUPPLY VOLTAGE (V) | | FREQUENCY (MHz) | | TEMPERATURE RANGE (°C) |
|------|-----|-----|-----|-----|------------------------|
| | **MIN** | **MAX** | **MIN** | **MAX** | |
| P87C552-4 | 4.5 | 5.5 | 3.5 | 16 | 0 to +70 |
| P87C552-5 | 4.5 | 5.5 | 3.5 | 16 | –40 to +85 |

## DC ELECTRICAL CHARACTERISTICS

$V_{SS}$, $AV_{SS}$ = 0V

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $I_{DD}$ | Supply current operating: PCA8XC552-5-16 | See notes 1 and 2 $f_{OSC}$ = 16MHz | | 40 | mA |
| $I_{ID}$ | Idle mode: 87C552 | See notes 1 and 3 $f_{OSC}$ = 16MHz | | 7 | mA |
| $I_{PD}$ | Power-down current: 87C552 | See notes 1 and 4; 2V < $V_{PD}$ < $V_{DD}$ max | | 50 | µA |
| **Inputs** | | | | | |
| $V_{IL}$ | Input low voltage, except $\overline{EA}$, P1.6, P1.7 | | −0.5 | 0.2$V_{DD}$−0.1 | V |
| $V_{IL1}$ | Input low voltage to $\overline{EA}$ | | −0.5 | 0.2$V_{DD}$−0.3 | V |
| $V_{IL2}$ | Input low voltage to P1.6/SCL, P1.7/SDA[5] | | −0.5 | 0.3$V_{DD}$ | V |
| $V_{IH}$ | Input high voltage, except XTAL1, RST | | 0.2$V_{DD}$+0.9 | $V_{DD}$+0.5 | V |
| $V_{IH1}$ | Input high voltage, XTAL1, RST | | 0.7$V_{DD}$ | $V_{DD}$+0.5 | V |
| $V_{IH2}$ | Input high voltage, P1.6/SCL, P1.7/SDA[5] | | 0.7$V_{DD}$ | 6.0 | V |
| $I_{IL}$ | Logical 0 input current, ports 1, 2, 3, 4, except P1.6, P1.7 | $V_{IN}$ = 0.45V | | −50 | µA |
| $I_{TL}$ | Logical 1-to-0 transition current, ports 1, 2, 3, 4, except P1.6, P1.7 | See note 6 | | −650 | µA |
| $\pm I_{IL1}$ | Input leakage current, port 0, $\overline{EA}$, STADC, $\overline{EW}$ | 0.45V < $V_I$ < $V_{DD}$ | | 10 | µA |
| $\pm I_{IL2}$ | Input leakage current, P1.6/SCL, P1.7/SDA | 0V < $V_I$ < 6V 0V < $V_{DD}$ < 5.5V | | 10 | µA |
| $\pm I_{IL3}$ | Input leakage current, port 5 | 0.45V < $V_I$ < $V_{DD}$ | | 1 | µA |
| **Outputs** | | | | | |
| $V_{OL}$ | Output low voltage, ports 1, 2, 3, 4, except P1.6, P1.7 | $I_{OL}$ = 1.6mA[7] | | 0.45 | V |
| $V_{OL1}$ | Output low voltage, port 0, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$ | $I_{OL}$ = 3.2mA[7] | | 0.45 | V |
| $V_{OL2}$ | Output low voltage, P1.6/SCL, P1.7/SDA | $I_{OL}$ = 3.0mA[7] | | 0.4 | V |
| $V_{OH}$ | Output high voltage, ports 1, 2, 3, 4, except P1.6/SCL, P1.7/SDA | −$I_{OH}$ = 60µA −$I_{OH}$ = 25µA −$I_{OH}$ = 10µA | 2.4 0.75$V_{DD}$ 0.9$V_{DD}$ | | V V V |
| $V_{OH1}$ | Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$)[8] | −$I_{OH}$ = 400µA −$I_{OH}$ = 150µA −$I_{OH}$ = 40µA | 2.4 0.75$V_{DD}$ 0.9$V_{DD}$ | | V V V |
| $V_{OH2}$ | Output high voltage (RST) | −$I_{OH}$ = 400µA −$I_{OH}$ = 120µA | 2.4 0.8$V_{DD}$ | | V V |
| $R_{RST}$ | Internal reset pull-down resistor | | 50 | 150 | kΩ |
| $C_{IO}$ | Pin capacitance | Test freq = 1MHz, $T_{amb}$ = 25°C | | 10 | pF |
| **Analog Inputs** | | | | | |
| $AV_{DD}$ | Analog supply voltage: 87C552[9] | $AV_{DD}$ = $V_{DD}$±0.2V | 4.5 | 5.5 | V |
| $AI_{DD}$ | Analog supply current: operating: | Port 5 = 0 to $AV_{DD}$ | | 1.2 | mA |
| $AI_{ID}$ | Idle mode: 87C552 | | | 50 | µA |
| $AI_{PD}$ | Power-down mode: 87C552 | 2V < $AV_{PD}$ < $AV_{DD}$ max | | 50 | µA |

# 80C51 8-bit microcontroller

## 8K/256 OTP, 8 channel 10 bit A/D, I²C, PWM, capture/compare, high I/O

**87C552**

## DC ELECTRICAL CHARACTERISTICS (Continued)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|--------|-----------|-----------------|--------|--------|------|
| | | | MIN | MAX | |
| **Analog Inputs (Continued)** | | | | | |
| $AV_{IN}$ | Analog input voltage | | $AV_{SS}-0.2$ | $AV_{DD}+0.2$ | V |
| $AV_{REF}$ | Reference voltage:<br>$AV_{REF-}$<br>$AV_{REF+}$ | | $AV_{SS}-0.2$ | $AV_{DD}+0.2$ | V<br>V |
| $R_{REF}$ | Resistance between $AV_{REF+}$ and $AV_{REF-}$ | | 10 | 50 | kΩ |
| $C_{IA}$ | Analog input capacitance | | | 15 | pF |
| $t_{ADS}$ | Sampling time | | | $8t_{CY}$ | μs |
| $t_{ADC}$ | Conversion time (including sampling time) | | | $50t_{CY}$ | μs |
| $DL_e$ | Differential non-linearity[10, 11, 12] | | | ±1 | LSB |
| $IL_e$ | Integral non-linearity[10, 13] | | | ±2 | LSB |
| $OS_e$ | Offset error[10, 14] | | | ±2 | LSB |
| $G_e$ | Gain error[10, 15] | | | ±0.4 | % |
| $A_e$ | Absolute voltage error[10, 16] | | | ±3 | LSB |
| $M_{CTC}$ | Channel to channel matching | | | ±1 | LSB |
| $C_t$ | Crosstalk between inputs of port 5[17] | 0–100kHz | | −60 | dB |

**NOTES FOR DC ELECTRICAL CHARACTERISTICS:**

1. See Figures 10 through 15 for $I_{DD}$ test conditions.
2. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10ns$; $V_{IL} = V_{SS} + 0.5V$; $V_{IH} = V_{DD} - 0.5V$; XTAL2 not connected; $\overline{EA} = RST = Port\ 0 = \overline{EW} = V_{DD}$; STADC = $V_{SS}$.
3. The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10ns$; $V_{IL} = V_{SS} + 0.5V$; $V_{IH} = V_{DD} - 0.5V$; XTAL2 not connected; Port 0 = $\overline{EW} = V_{DD}$; $\overline{EA}$ = RST = STADC = $V_{SS}$.
4. The power-down current is measured with all output pins disconnected; XTAL2 not connected; Port 0 = $\overline{EW} = V_{DD}$; $\overline{EA}$ = RST = STADC = XTAL1 = $V_{SS}$.
5. The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I²C specification, so an input voltage below 1.5V will be recognized as a logic 0 while an input voltage above 3.0V will be recognized as a logic 1.
6. Pins of ports 1 (except P1.6, P1.7), 2, 3, and 4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when $V_{IN}$ is approximately 2V.
7. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the $V_{OL}$s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. $I_{OL}$ can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
8. Capacitive loading on ports 0 and 2 may cause the $V_{OH}$ on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{DD}$ specification when the address bits are stabilizing.
9. The following condition must not be exceeded: $V_{DD} - 0.2V < AV_{DD} < V_{DD} + 0.2V$.
10. Conditions: $AV_{REF-} = 0V$; $AV_{DD} = 5.0V$. Measurement by continuous conversion of $AV_{IN} = -20mV$ to 5.12V in steps of 0.5mV, derivating parameters from collected conversion results of ADC. $AV_{REF+}$ (87C552) = 4.977V. ADC is monotonic with no missing codes.
11. The differential non-linearity ($DL_e$) is the difference between the actual step width and the ideal step width. (See Figure 1.)
12. The ADC is monotonic; there are no missing codes.
13. The integral non-linearity ($IL_e$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset error. (See Figure 1.)
14. The offset error ($OS_e$) is the absolute difference between the straight line which fits the actual transfer curve (after removing gain error), and a straight line which fits the ideal transfer curve. (See Figure 1.)
15. The gain error ($G_e$) is the relative difference in percent between the straight line fitting the actual transfer curve (after removing offset error), and the straight line which fits the ideal transfer curve. Gain error is constant at every point on the transfer curve. (See Figure 1.)
16. The absolute voltage error ($A_e$) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve.
17. This should be considered when both analog and digital signals are simultaneously input to port 5.

**Figure 1.  ADC Conversion Characteristic**

(1)  Example of an actual transfer curve.
(2)  The ideal transfer curve.
(3)  Differential non-linearity (DL$_e$).
(4)  Integral non-linearity (IL$_e$).
(5)  Center of a step of the actual transfer curve.

$$1 \text{ LSB} = \frac{AV_{REF+} - AV_{REF-}}{1024}$$

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# 80C51 8-bit microcontroller

8K/256 OTP, 8 channel 10 bit A/D, I²C, PWM, capture/compare, high I/O

**87C552**

## AC ELECTRICAL CHARACTERISTICS[1, 2]

| SYMBOL | FIGURE | PARAMETER | 12MHz CLOCK MIN | 12MHz CLOCK MAX | 16MHz CLOCK MIN | 16MHz CLOCK MAX | VARIABLE CLOCK MIN | VARIABLE CLOCK MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $1/t_{CLCL}$ | 2 | Oscillator frequency | | | | | 3.5 | 16 | MHz |
| $t_{LHLL}$ | 2 | ALE pulse width | 127 | | 85 | | $2t_{CLCL}-40$ | | ns |
| $t_{AVLL}$ | 2 | Address valid to ALE low | 28 | | 8 | | $t_{CLCL}-55$ | | ns |
| $t_{LLAX}$ | 2 | Address hold after ALE low | 48 | | 28 | | $t_{CLCL}-35$ | | ns |
| $t_{LLIV}$ | 2 | ALE low to valid instruction in | | 234 | | 150 | | $4t_{CLCL}-100$ | ns |
| $t_{LLPL}$ | 2 | ALE low to $\overline{PSEN}$ low | 43 | | 23 | | $t_{CLCL}-40$ | | ns |
| $t_{PLPH}$ | 2 | $\overline{PSEN}$ pulse width | 205 | | 143 | | $3t_{CLCL}-45$ | | ns |
| $t_{PLIV}$ | 2 | $\overline{PSEN}$ low to valid instruction in | | 145 | | 83 | | $3t_{CLCL}-105$ | ns |
| $t_{PXIX}$ | 2 | Input instruction hold after $\overline{PSEN}$ | 0 | | 0 | | 0 | | ns |
| $t_{PXIZ}$ | 2 | Input instruction float after $\overline{PSEN}$ | | 59 | | 38 | | $t_{CLCL}-25$ | ns |
| $t_{AVIV}$ | 2 | Address to valid instruction in | | 312 | | 208 | | $5t_{CLCL}-105$ | ns |
| $t_{PLAZ}$ | 2 | $\overline{PSEN}$ low to address float | | 10 | | 10 | | 10 | ns |
| **Data Memory** | | | | | | | | | |
| $t_{AVLL}$ | 3, 4 | Address valid to ALE low | 43 | | 23 | | $t_{CLCL}-40$ | | ns |
| $t_{RLRH}$ | 3 | $\overline{RD}$ pulse width | 400 | | 275 | | $6t_{CLCL}-100$ | | ns |
| $t_{WLWH}$ | 3 | $\overline{WR}$ pulse width | 400 | | 275 | | $6t_{CLCL}-100$ | | ns |
| $t_{RLDV}$ | 3 | $\overline{RD}$ low to valid data in | | 252 | | 148 | | $5t_{CLCL}-165$ | ns |
| $t_{RHDX}$ | 3 | Data hold after $\overline{RD}$ | 0 | | 0 | | 0 | | ns |
| $t_{RHDZ}$ | 3 | Data float after $\overline{RD}$ | | 97 | | 55 | | $2t_{CLCL}-70$ | ns |
| $t_{LLDV}$ | 3 | ALE low to valid data in | | 517 | | 350 | | $8t_{CLCL}-150$ | ns |
| $t_{AVDV}$ | 3 | Address to valid data in | | 585 | | 398 | | $9t_{CLCL}-165$ | ns |
| $t_{LLWL}$ | 3, 4 | ALE low to $\overline{RD}$ or $\overline{WR}$ low | 200 | 300 | 138 | 238 | $3t_{CLCL}-50$ | $3t_{CLCL}+50$ | ns |
| $t_{AVWL}$ | 3, 4 | Address valid to $\overline{WR}$ low or $\overline{RD}$ low | 203 | | 120 | | $4t_{CLCL}-130$ | | ns |
| $t_{QVWX}$ | 4 | Data valid to $\overline{WR}$ transition | 23 | | 3 | | $t_{CLCL}-60$ | | ns |
| $t_{DW}$ | 4 | Data before $\overline{WR}$ | 433 | | 288 | | $7t_{CLCL}-150$ | | ns |
| $t_{WHQX}$ | 4 | Data hold after $\overline{WR}$ | 33 | | 13 | | $t_{CLCL}-50$ | | ns |
| $t_{RLAZ}$ | 4 | $\overline{RD}$ low to address float | | 0 | | 0 | | 0 | ns |
| $t_{WHLH}$ | 3, 4 | $\overline{RD}$ or $\overline{WR}$ high to ALE high | 43 | 123 | 23 | 103 | $t_{CLCL}-40$ | $t_{CLCL}+40$ | ns |
| **External Clock** | | | | | | | | | |
| $t_{CHCX}$ | 5 | High time[3] | 20 | | 20 | | 20 | | ns |
| $t_{CLCX}$ | 5 | Low time[3] | 20 | | 20 | | 20 | | ns |
| $t_{CLCH}$ | 5 | Rise time[3] | | 20 | | 20 | | 20 | ns |
| $t_{CHCL}$ | 5 | Fall time[3] | | 20 | | 20 | | 20 | ns |
| **Serial Timing – Shift Register Mode[4]** (Test Conditions: $T_{amb}$ = 0°C to +70°C; $V_{SS}$ = 0V; Load Capaciatnce = 80pF) | | | | | | | | | |
| $t_{XLXL}$ | 6 | Serial port clock cycle time | 1.0 | | 0.75 | | $12t_{CLCL}$ | | µs |
| $t_{QVXH}$ | 6 | Output data setup to clock rising edge | 700 | | 492 | | $10t_{CLCL}-133$ | | ns |
| $t_{XHQX}$ | 6 | Output data hold after clock rising edge | 50 | | 8 | | $2t_{CLCL}-117$ | | ns |
| $t_{XHDX}$ | 6 | Input data hold after clock rising edge | 0 | | 0 | | 0 | | ns |
| $t_{XHDV}$ | 6 | Clock rising edge to input data valid | | 700 | | 492 | | $10t_{CLCL}-133$ | ns |

**NOTES:**
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. $t_{CLCL}$ = $1/f_{OSC}$ = one oscillator clock period.
   $t_{CLCL}$ = 83.3ns at $f_{OSC}$ = 12MHz.
   $t_{CLCL}$ = 62.5ns at $f_{OSC}$ = 16MHz.
4. These values are characterized but not 100% production tested.

## 80C51 8-bit microcontroller

8K/256 OTP, 8 channel 10 bit A/D, I$^2$C, PWM, capture/compare, high I/O

**87C552**

### AC ELECTRICAL CHARACTERISTICS (Continued)

| SYMBOL | PARAMETER | INPUT | OUTPUT |
|---|---|---|---|
| **I$^2$C Interface (Refer to Figure 9)[5]** | | | |
| $t_{HD;STA}$ | START condition hold time | $\geq 14\ t_{CLCL}$ | $> 4.0\mu s$ [1] |
| $t_{LOW}$ | SCL low time | $\geq 16\ t_{CLCL}$ | $> 4.7\mu s$ [1] |
| $t_{HIGH}$ | SCL high time | $\geq 14\ t_{CLCL}$ | $> 4.0\mu s$ [1] |
| $t_{RC}$ | SCL rise time | $\leq 1\mu s$ | $-$ [2] |
| $t_{FC}$ | SCL fall time | $\leq 0.3\mu s$ | $< 0.3\mu s$ [3] |
| $t_{SU;DAT1}$ | Data set-up time | $\geq 250ns$ | $> 20\ t_{CLCL} - t_{RD}$ |
| $t_{SU;DAT2}$ | SDA set-up time (before rep. START cond.) | $\geq 250ns$ | $> 1\mu s$ [1] |
| $t_{SU;DAT3}$ | SDA set-up time (before STOP cond.) | $\geq 250ns$ | $> 8\ t_{CLCL}$ |
| $t_{HD;DAT}$ | Data hold time | $\geq 0ns$ | $> 8\ t_{CLCL} - t_{FC}$ |
| $t_{SU;STA}$ | Repeated START set-up time | $\geq 14\ t_{CLCL}$ | $> 4.7\mu s$ [1] |
| $t_{SU;STO}$ | STOP condition set-up time | $\geq 14\ t_{CLCL}$ | $> 4.0\mu s$ [1] |
| $t_{BUF}$ | Bus free time | $\geq 14\ t_{CLCL}$ | $> 4.7\mu s$ [1] |
| $t_{RD}$ | SDA rise time | $\leq 1\mu s$ | $-$ [2] |
| $t_{FD}$ | SDA fall time | $\leq 0.3\mu s$ | $< 0.3\mu s$ [3] |

**NOTES:**
1. At 100 kbit/s. At other bit rates this value is inversely proportional to the bit-rate of 100 kbit/s.
2. Determined by the external bus-line capacitance and the external bus-line pull-resistor, this must be $< 1\mu s$.
3. Spikes on the SDA and SCL lines with a duration of less than 3 $t_{CLCL}$ will be filtered out. Maximum capacitance on bus-lines SDA and SCL = 400pF.
4. $t_{CLCL} = 1/f_{OSC}$ = one oscillator clock period at pin XTAL1. For 62ns (42s) $< t_{CLCL} <$ 285ns (16MHz (24Hz) $> f_{OSC} >$ 3.5MHz) the SI01 interface meets the I$^2$C-bus specification for bit-rates up to 100 kbit/s.
5. These values are guaranteed but not 100% production tested.

## 80C51 8-bit microcontroller

8K/256 OTP, 8 channel 10 bit A/D, I²C, PWM, capture/compare, high I/O

**87C552**

### EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A  –  Address
C  –  Clock
D  –  Input data
H  –  Logic level high
I  –  Instruction (program memory contents)
L  –  Logic level low, or ALE

P  –  $\overline{\text{PSEN}}$
Q  –  Output data
R  –  $\overline{\text{RD}}$ signal
t  –  Time
V  –  Valid
W  –  $\overline{\text{WR}}$ signal
X  –  No longer a valid logic level
Z  –  Float

**Examples:** $t_{AVLL}$ = Time for address valid to ALE low.
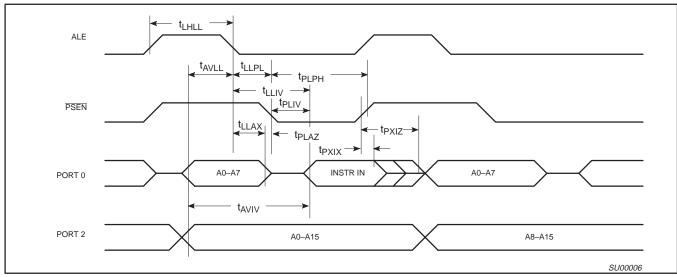$t_{LLPL}$ = Time for ALE low to $\overline{\text{PSEN}}$ low.



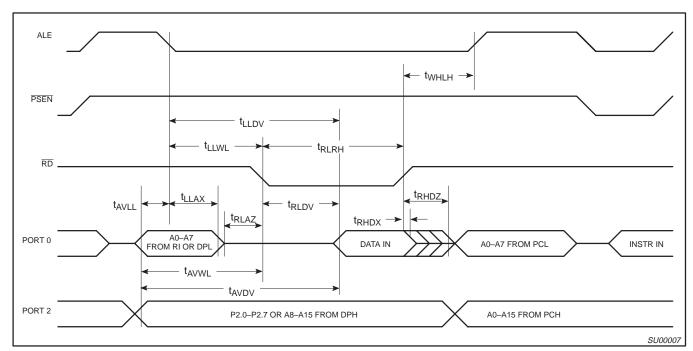**Figure 2.  External Program Memory Read Cycle**



**Figure 3.  External Data Memory Read Cycle**

# 80C51 8-bit microcontroller

8K/256 OTP, 8 channel 10 bit A/D, I2C, PWM, capture/compare, high I/O
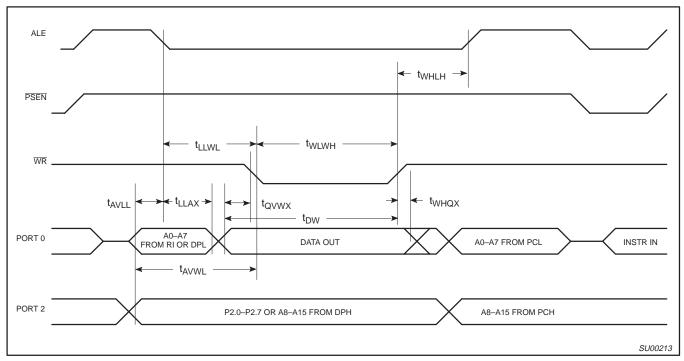
**87C552**
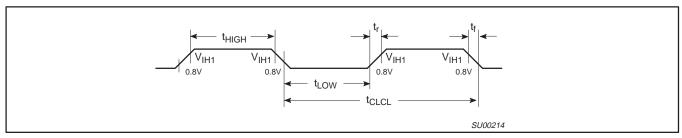


**Figure 4.  External Data Memory Write Cycle**
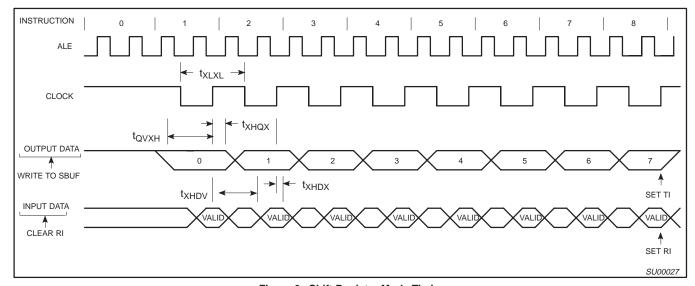


**Figure 5.  External Clock Drive XTAL1**



**Figure 6.  Shift Register Mode Timing**

# 80C51 8-bit microcontroller

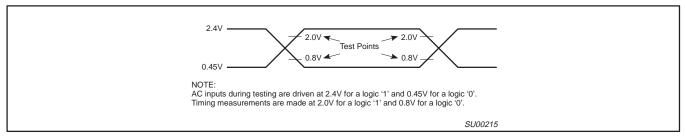8K/256 OTP, 8 channel 10 bit A/D, I²C, PWM, capture/compare, high I/O
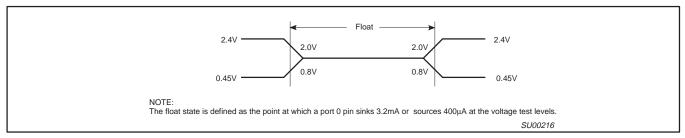
**Figure 7. AC Testing Input/Output**
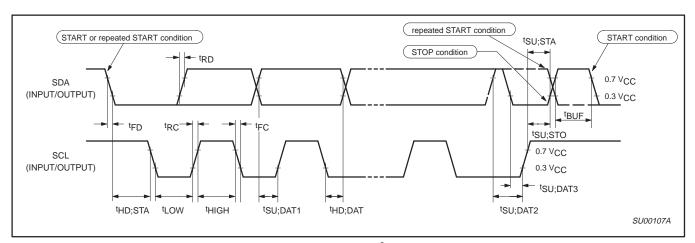


**Figure 8. AC Testing Input, Float Waveform**



**Figure 9. Timing SIO1 (I²C) Interface**

## 80C51 8-bit microcontroller

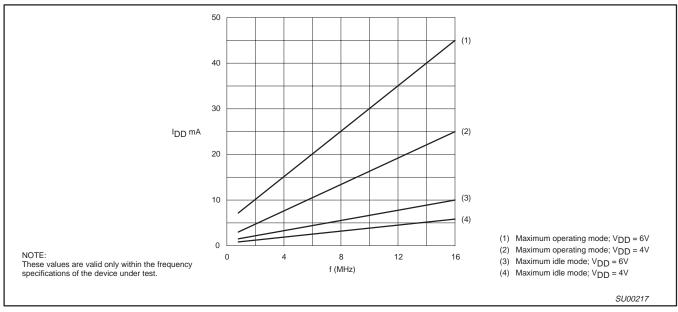8K/256 OTP, 8 channel 10 bit A/D, I²C, PWM, capture/compare, high I/O

**87C552**



NOTE:
These values are valid only within the frequency specifications of the device under test.

(1) Maximum operating mode; $V_{DD}$ = 6V
(2) Maximum operating mode; $V_{DD}$ = 4V
(3) Maximum idle mode; $V_{DD}$ = 6V
(4) Maximum idle mode; $V_{DD}$ = 4V

SU00217

**Figure 10.  16MHz Version Supply Current ($I_{DD}$) as a Function of Frequency at XTAL1 ($f_{OSC}$)**
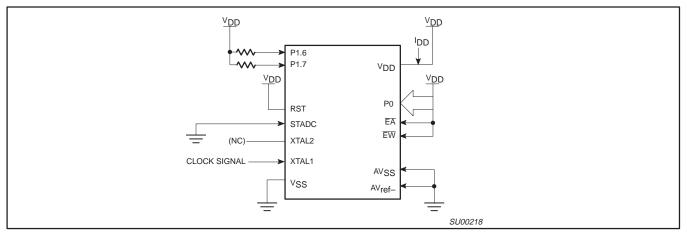


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**Figure 11.  $I_{DD}$ Test Condition, Active Mode**
**All other pins are disconnected[1]**

1. Active Mode:
   a. The following pins must be forced to $V_{DD}$: $\overline{EA}$, RST, Port 0, and $\overline{EW}$.
   b. The following pins must be forced to $V_{SS}$: STADC, $AV_{SS}$, and $AV_{ref-}$.
   c. Ports 1.6 and 1.7 should be connected to $V_{DD}$ through resistors of sufficiently high value such that the sink current into these pins cannot exceed the $I_{OL1}$ spec of these pins.
   d. The following pins must be disconnected:  XTAL2 and all pins not specified above.

## 80C51 8-bit microcontroller

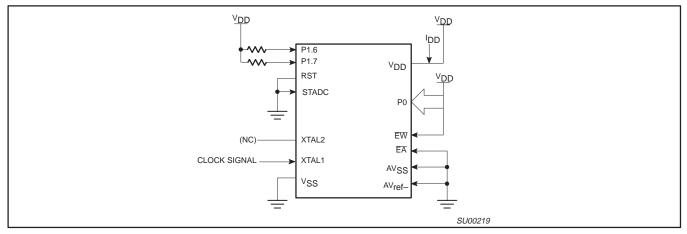8K/256 OTP, 8 channel 10 bit A/D, I²C, PWM, capture/compare, high I/O

**87C552**



**Figure 12. $I_{DD}$ Test Condition, Idle Mode**
**All other pins are disconnected[2]**

2. Idle Mode:
   a. The following pins must be forced to $V_{DD}$: Port 0 and $\overline{EW}$.
   b. The following pins must be forced to $V_{SS}$: RST, STADC, $AV_{SS}$, $AV_{ref-}$, and $\overline{EA}$.
   c. Ports 1.6 and 1.7 should be connected to $V_{DD}$ through resistors of sufficiently high value such that the sink current into these pins cannot exceed the $I_{OL1}$ spec of these pins. These pins must not have logic 0 written to them prior to this measurement.
   d. The following pins must be disconnected: XTAL2 and all pins not specified above.



**Figure 13. Clock Signal Waveform for $I_{DD}$ Tests in Active and Idle Modes**
**$t_{CLCH} = t_{CHCL} = 5ns$**



**Figure 14. $I_{DD}$ Test Condition, Power Down Mode**
**All other pins are disconnected. $V_{DD}$ = 2V to 5.5V[3]**

3. Power Down Mode:
   a. The following pins must be forced to $V_{DD}$: Port 0 and $\overline{EW}$.
   b. The following pins must be forced to $V_{SS}$: RST, STADC, XTAL1, $AV_{SS}$, $AV_{ref-}$, and $\overline{EA}$.
   c. Ports 1.6 and 1.7 should be connected to $V_{DD}$ through resistors of sufficiently high value such that the sink current into these pins cannot exceed the $I_{OL1}$ spec of these pins. These pins must not have logic 0 written to them prior to this measurement.
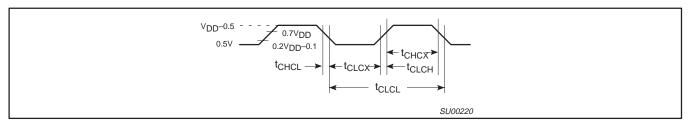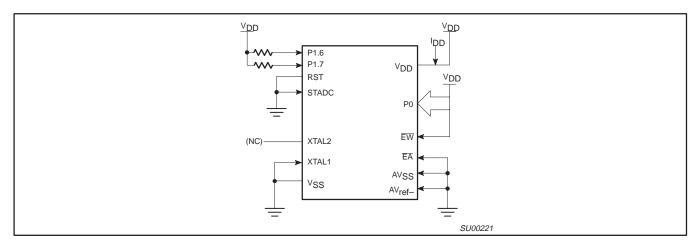   d. The following pins must be disconnected: XTAL2 and all pins not specified above.

## 80C51 8-bit microcontroller

8K/256 OTP, 8 channel 10 bit A/D, I2C, PWM, capture/compare, high I/O

**87C552**

## EPROM CHARACTERISTICS

The 87C552 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for $V_{PP}$ (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses.

The 87C552 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C552 manufactured by Philips.

Table 3 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 15 and 16. Figure 17 shows the circuit configuration for normal program memory verification.

## Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 15. Note that the 87C552 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 15. The code byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$, and pins of ports 2 and 3 specified in Table 3 are held at the "Program Code Data" levels indicated in Table 3. The ALE/$\overline{PROG}$ is pulsed low 25 times as shown in Figure 16.

To program the encryption table, repeat the 25-pulse programming sequence for addresses 0 through 1FH, using the "Pgm Encryption Table" levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 25-pulse programming sequence using the "Pgm Lock Bit" levels. After one lock bit is

programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the $\overline{EA}$/$V_{PP}$ pin must not be allowed to go above the maximum specified $V_{PP}$ level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The $V_{PP}$ source should be well regulated and free of glitches and overshoot.

## Program Verification

If lock bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be red is applied to ports 1 and 2 as shown in Figure 17. The other pins are held at the "Verify Code Data" levels indicated in Table 3. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

### Reading the Signature Bytes
The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips Components
(031H) = 94H indicates 87C552

## Program/Verify Algorithms
Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

### Table 3. EPROM Programming Modes

| MODE | RST | $\overline{PSEN}$ | ALE/$\overline{PROG}$ | $\overline{EA}$/$V_{PP}$ | P2.7 | P2.6 | P3.7 | P3.6 |
|---|---|---|---|---|---|---|---|---|
| Read signature | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| Program code data | 1 | 0 | 0* | $V_{PP}$ | 1 | 0 | 1 | 1 |
| Verify code data | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| Pgm encryption table | 1 | 0 | 0* | $V_{PP}$ | 1 | 0 | 1 | 0 |
| Pgm lock bit 1 | 1 | 0 | 0* | $V_{PP}$ | 1 | 1 | 1 | 1 |
| Pgm lock bit 2 | 1 | 0 | 0* | $V_{PP}$ | 1 | 1 | 0 | 0 |

**NOTES:**
1. 0 = Valid low for that pin; 1 = valid high for that pin.
2. $V_{PP}$ = 12.75V ±0.25V.
3. $V_{DD}$ = 5V ±10% during programming and verification.
* ALE/$\overline{PROG}$ receives 25 programming pulses while $V_{PP}$ is held at 12.75V. Each programming pulse is low for 100μs (±10μs) and high for a minimum of 10μs.

™Trademark phrase of Intel Corporation.

# 80C51 8-bit microcontroller

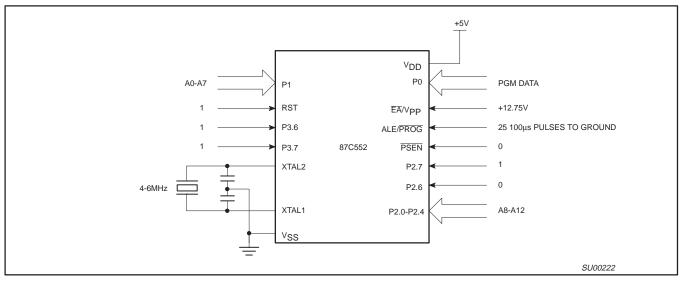8K/256 OTP, 8 channel 10 bit A/D, I²C, PWM, capture/compare, high I/O
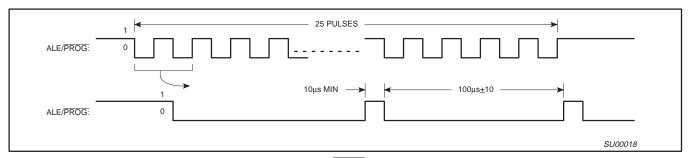
# 87C552



**Figure 15. Programming Configuration**



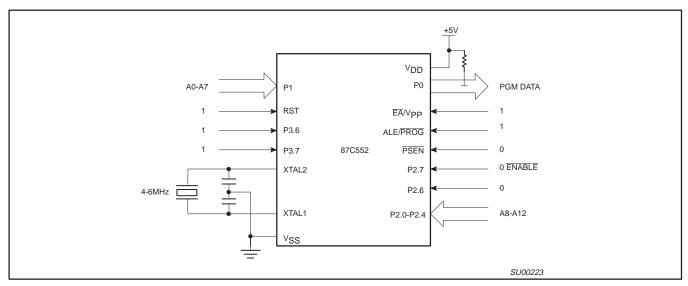**Figure 16. $\overline{\text{PROG}}$ Waveform**



**Figure 17. Program Verification**
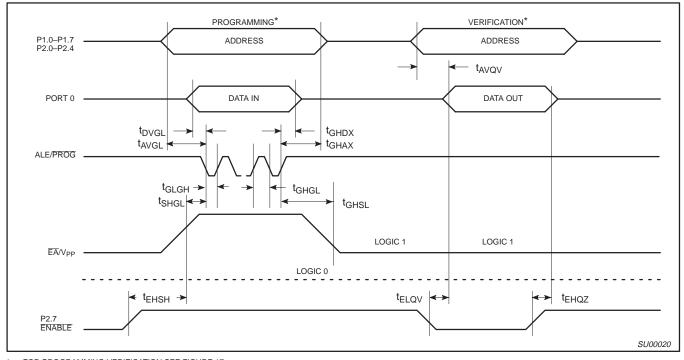
80C51 8-bit microcontroller

8K/256 OTP, 8 channel 10 bit A/D, I²C, PWM, capture/compare, high I/O

**87C552**

## EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

$T_{amb}$ = 21°C to +27°C, $V_{DD}$ = 5V±10%, $V_{SS}$ = 0V

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|--------|-----------|-----|-----|------|
| $V_{PP}$ | Programming supply voltage | 12.5 | 13.0 | V |
| $I_{PP}$ | Programming supply current | | 50 | mA |
| $1/t_{CLCL}$ | Oscillator frequency | 4 | 6 | MHz |
| $t_{AVGL}$ | Address setup to $\overline{PROG}$ low | $48t_{CLCL}$ | | |
| $t_{GHAX}$ | Address hold after $\overline{PROG}$ | $48t_{CLCL}$ | | |
| $t_{DVGL}$ | Data setup to $\overline{PROG}$ low | $48t_{CLCL}$ | | |
| $t_{GHDX}$ | Data hold after $\overline{PROG}$ | $48t_{CLCL}$ | | |
| $t_{EHSH}$ | P2.7 ($\overline{ENABLE}$) high to $V_{PP}$ | $48t_{CLCL}$ | | |
| $t_{SHGL}$ | $V_{PP}$ setup to $\overline{PROG}$ low | 10 | | µs |
| $t_{GHSL}$ | $V_{PP}$ hold after $\overline{PROG}$ | 10 | | µs |
| $t_{GLGH}$ | $\overline{PROG}$ width | 90 | 110 | µs |
| $t_{AVQV}$ | Address to data valid | | $48t_{CLCL}$ | |
| $t_{ELQZ}$ | $\overline{ENABLE}$ low to data valid | | $48t_{CLCL}$ | |
| $t_{EHQZ}$ | Data float after $\overline{ENABLE}$ | 0 | $48t_{CLCL}$ | |
| $t_{GHGL}$ | $\overline{PROG}$ high to $\overline{PROG}$ low | 10 | | µs |



* FOR PROGRAMMING VERIFICATION SEE FIGURE 17.
  FOR VERIFICATION CONDITIONS SEE TABLE 3.

**Figure 18. EPROM Programming and Verification**

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.
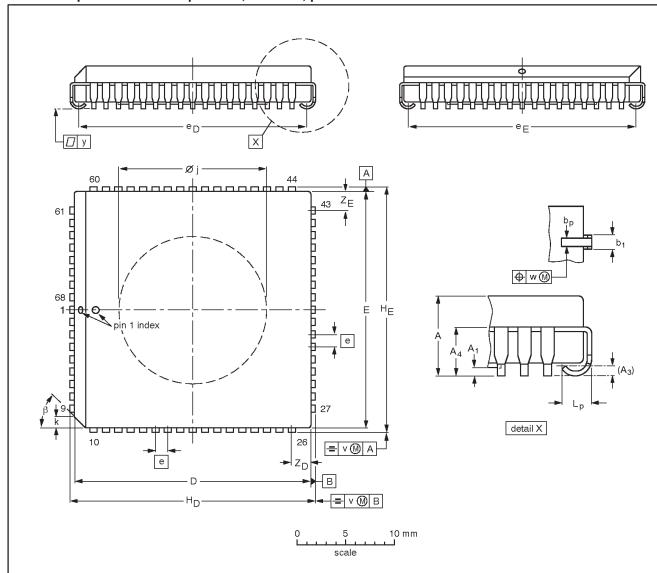
# 80C51 8-bit microcontroller

## 8K/256 OTP, 8 channel 10 bit A/D, I²C, PWM, capture/compare, high I/O

**87C552**

**PLCC68:**   plastic leaded chip carrier; 68 leads; pedestal                                                   **SOT188-3**



**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

| UNIT | A | A₁ min. | A₃ | A₄ max. | b_p | b₁ | D⁽¹⁾ | E⁽¹⁾ | e | e_D | e_E | H_D | H_E | k | Øⱼ | L_p | v | w | y | Z_D⁽¹⁾ max. | Z_E⁽¹⁾ max. | β |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.57 4.19 | 0.13 | 0.25 | 3.05 | 0.53 0.33 | 0.81 0.66 | 24.33 24.13 | 24.33 24.13 | 1.27 | 23.62 22.61 | 23.62 22.61 | 25.27 25.02 | 25.27 25.02 | 1.22 1.07 | 15.34 15.19 | 1.44 1.02 | 0.18 | 0.18 | 0.10 | 2.06 | 2.06 | 45° |
| inches | 0.180 0.165 | 0.005 | 0.01 | 0.12 | 0.021 0.013 | 0.032 0.026 | 0.958 0.950 | 0.958 0.950 | 0.05 | 0.930 0.890 | 0.930 0.890 | 0.995 0.985 | 0.995 0.985 | 0.048 0.042 | 0.604 0.598 | 0.057 0.040 | 0.007 | 0.007 | 0.004 | 0.081 | 0.081 | |

**Note**

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

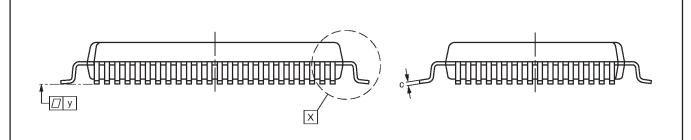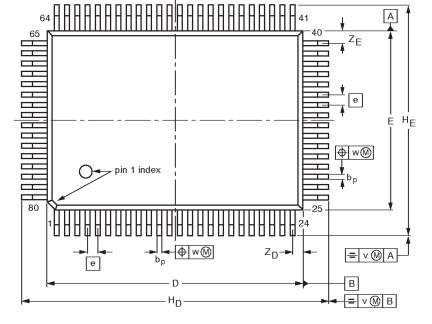| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT188-3 | 112E10 | MO-047AE | | | | ~~92-11-17~~ 95-02-25 |

## 80C51 8-bit microcontroller

**87C552**

8K/256 OTP, 8 channel 10 bit A/D, I2C, PWM, capture/compare, high I/O

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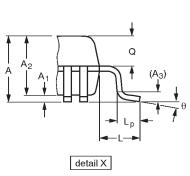**QFP80:** plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm     **SOT318-2**



**DIMENSIONS** (mm are the original dimensions)

| UNIT | A max. | A₁ | A₂ | A₃ | b_p | c | D(1) | E(1) | e | H_D | H_E | L | L_p | Q | v | w | y | Z_D(1) | Z_E(1) | θ |
|------|--------|-----|------|------|------|------|------|------|-----|------|------|------|------|------|-----|-----|-----|--------|--------|------|
| mm | 3.2 | 0.25 0.05 | 2.90 2.65 | 0.25 | 0.45 0.30 | 0.25 0.14 | 20.1 19.9 | 14.1 13.9 | 0.8 | 24.2 23.6 | 18.2 17.6 | 1.95 | 1.0 0.6 | 1.4 1.2 | 0.2 | 0.2 | 0.1 | 1.0 0.6 | 1.2 0.8 | 7° 0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|------|------|---|---------------------|------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT318-2 | | | | | | ~~92-12-15~~ 95-02-04 |

**NOTES**

## Data sheet status

| Data sheet status | Product status | Definition [1] |
|---|---|---|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product. |
| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

[1]   Please consult the most recently issued datasheet before initiating or completing a design.

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