DESCRIPTION

The 82S114 and 82S115 are Schottky-clamped Read Only Memories, incorporating on-chip data output registers. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S114 and 82S115 are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S114 and 82S115 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature Tri-State outputs for optimization of word expansion in bussed organizations. A D-type latch is used to enable the Tri-State output drivers. In the TRANSPARENT READ mode, stored data is addressed by applying a binary code to the address inputs while holding STROBE high. In this mode the bit drivers will be controlled solely by $\overline{CE1}$ and CE2 lines. In the LATCHED READ mode, after the desired address is applied and both $\overline{CE1}$ and CE2 are enabled, data will enter the output latches following the positive transition of STROBE, and the data out lines will be locked into their last valid state following the negative transition of STROBE. The latches will remain set and the outputs enabled until the chip is disabled and STROBE is brought high.

Both 82S114 and 82S115 devices are available in the commercial temperature range. For the commercial temperature range, (0°C to +75°C) specify N82S114/115, I.

FEATURES

- ORGANIZATION:
  - 82S114 – 256 X 8
  - 82S115 – 512 X 8
- ADDRESS ACCESS TIME – 60ns, MAXIMUM
- POWER DISSIPATION – 165μW/BIT, TYPICAL
- INPUT LOADING – (–100μA), MAXIMUM
- ON-CHIP ADDRESS DECODING
- ON-CHIP STORAGE LATCHES
- TRI-STATE OUTPUTS
- FAST PROGRAMMING – 5 SEC., MAXIMUM
- PIN COMPATIBLE TO N8204/N8205 ROMs

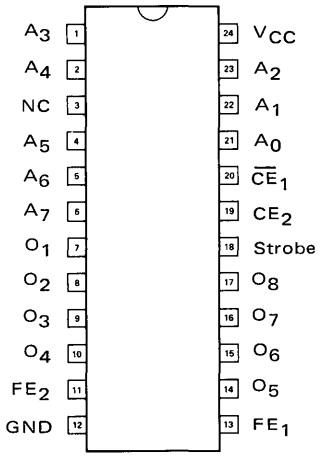
APPLICATIONS

MICROPROGRAMMING
HARDWIRE ALGORITHMS
CHARACTER GENERATION
CONTROL STORE
SEQUENTIAL CONTROLLERS

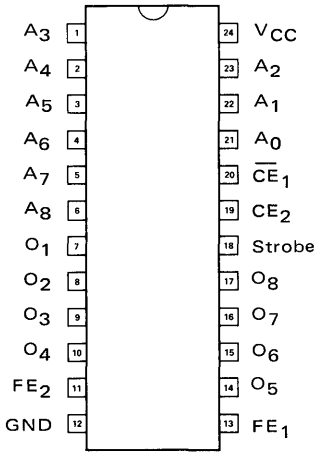
PIN CONFIGURATION

I PACKAGE*

82S114

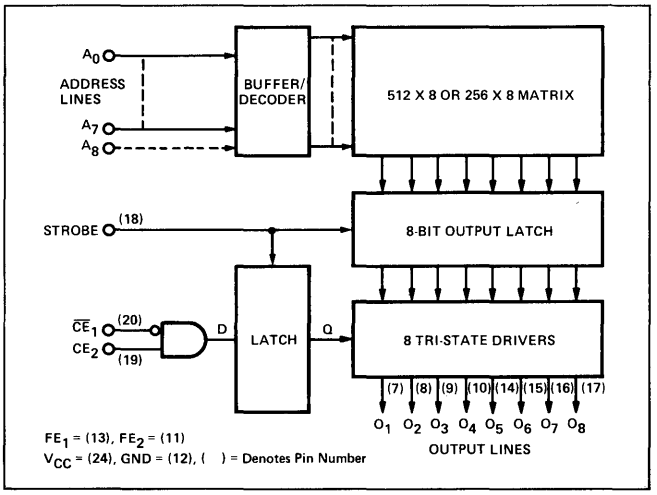


82S115



*I – Ceramic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage	+5.5	Vdc
V_O	Off-State Output Voltage	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25$

PARAMETER		TEST CONDITIONS	LIMITS[1]			UNIT
			MIN	TYP[2]	MAX	
I_{IL}	"0" Input Current	V_{IN} = 0.45V			−100	μA
I_{IH}	"1" Input Current	V_{IN} = 5.5V			25	μA
V_{IL}	"0" Level Input Voltage				.85	V
V_{IH}	"1" Level Input Voltage		2.0			V
V_{IC}	Input Clamp Voltage	I_{IN} = −18 mA		−0.8	−1.2	V
V_{OL}	"0" Output Voltage	I_{OUT} = 9.6 mA			0.5	V
V_{OH}	"1" Output Voltage	$\overline{CE_1}$ = "0", CE_2 = "1", I_{OUT} = −2 mA, "1" STORED	2.7	3.3		V
$I_{O(OFF)}$	HI-Z State Output Current	$\overline{CE_1}$ = "1" or CE_2 = 0, V_{OUT} = 5.5V			40	μA
		$\overline{CE_1}$ = "1" or CE_2 = 0, V_{OUT} = 0.5V			−40	μA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		5		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V, $\overline{CE_1}$ = "1" or CE_2 = 0		8		pF
I_{CC}	V_{CC} Supply Current			135	185	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 3)	−20		−70	mA

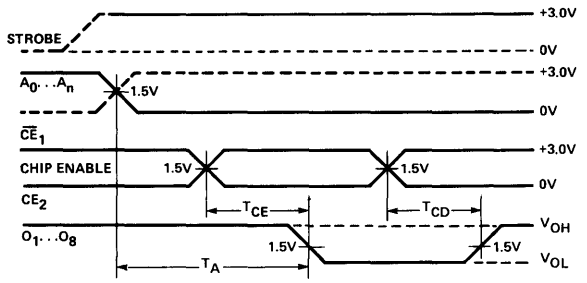
SWITCHING CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[2]	MAX	
T_{AA}	Address Access Time	LATCHED or TRANSPARENT READ		35	60	ns
T_{CE}	Chip Enable Access Time	R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF (Note 4)		20	40	ns
T_{CD}	Chip Disable Time			20	40	ns
T_{ADH}	Address Hold Time	LATCHED READ ONLY R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF (Note 5)	0	−10		ns
T_{CDH}	Chip Enable Hold Time		10	0		ns
T_{SW}	Strobe Pulse Width		30	20		ns
T_{SL}	Strobe Latch Time		60	35		ns
T_{DL}	Strobe Delatch Time				30	ns
T_{CDS}	Chip Enable Set-up Time		40			ns

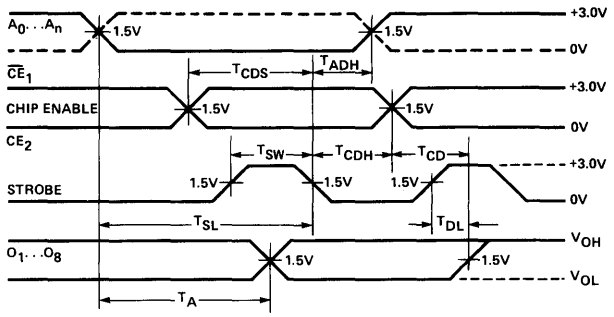
NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = +5.0V and T_A = +25° C.
3. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in "1" state.
4. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an "off" or high impedance state after it has been enabled.
5. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.

MEMORY TIMING

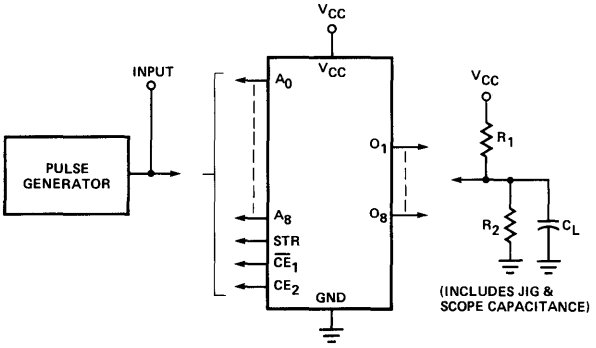
TRANSPARENT READ[5]
(Output Latches Not Used)



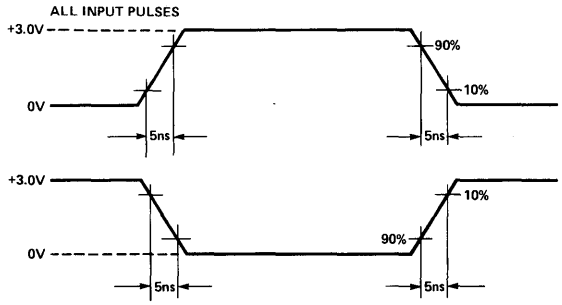
LATCHED READ[6]
(Output Latches Used)



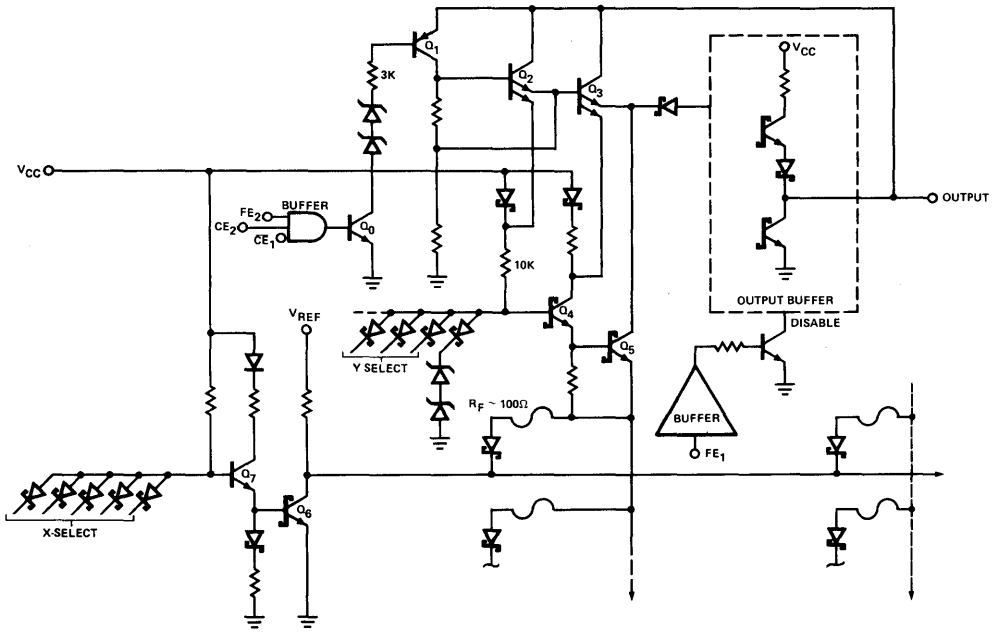
AC TEST LOAD AND WAVEFORMS



INPUT PULSES



TYPICAL FUSING PATH



RECOMMENDED PROGRAMMING PROCEDURE

The 82S114/115 are shipped with all bits at logical "0" (low). To write logical "1", proceed as follows:

SET-UP

a. Apply GND to pin 12.

b. Terminate all device outputs with a 10KΩ resistor to V_{CC}.

c. Set $\overline{CE}$ 1 to logic "0", and CE2 to logic "1" (TTL levels).

d. Set Strobe to logic "1" level.

PROGRAM-VERIFY SEQUENCE

Step 1 Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL "1" and "0" logic levels to the device address inputs.

Step 2 After 10μs delay, apply to FE1 (pin 13) a voltage source of +5.0 ± 0.5V, with 10 mA sourcing current capability.

Step 3 After 10μs delay, apply a voltage source of +17.0 ± 1.0V to the output to be programmed. The source must have a current limit of 200 mA. Program one output at the time.

Step 4 After 10μs delay, raise FE2 (pin 11) from 0V to +5.0 ± 0.5V for a period of 1ms, and then return to 0V. Pulse source must have a 10 mA sourcing current capability.

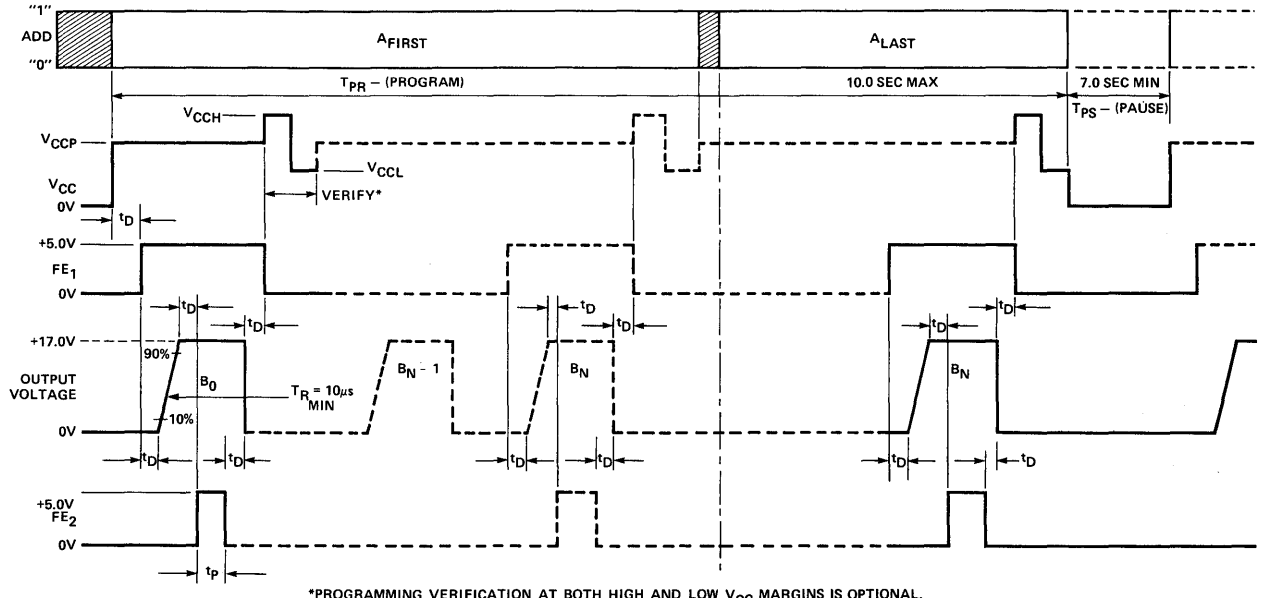
Step 5 After 10μs delay, remove +17.0V supply from programmed output.

Step 6 To verify programming, after 10μs delay, return FE1 to 0V. Raise V_{CC} to V_{CCH} = +5.5 ± .2V. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the "1" state.

Step 7 Raise V_{CC} to V_{CCP}, and repeat steps 2 through 6 to program other bits at the same address.

Step 8 Repeat steps 1 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



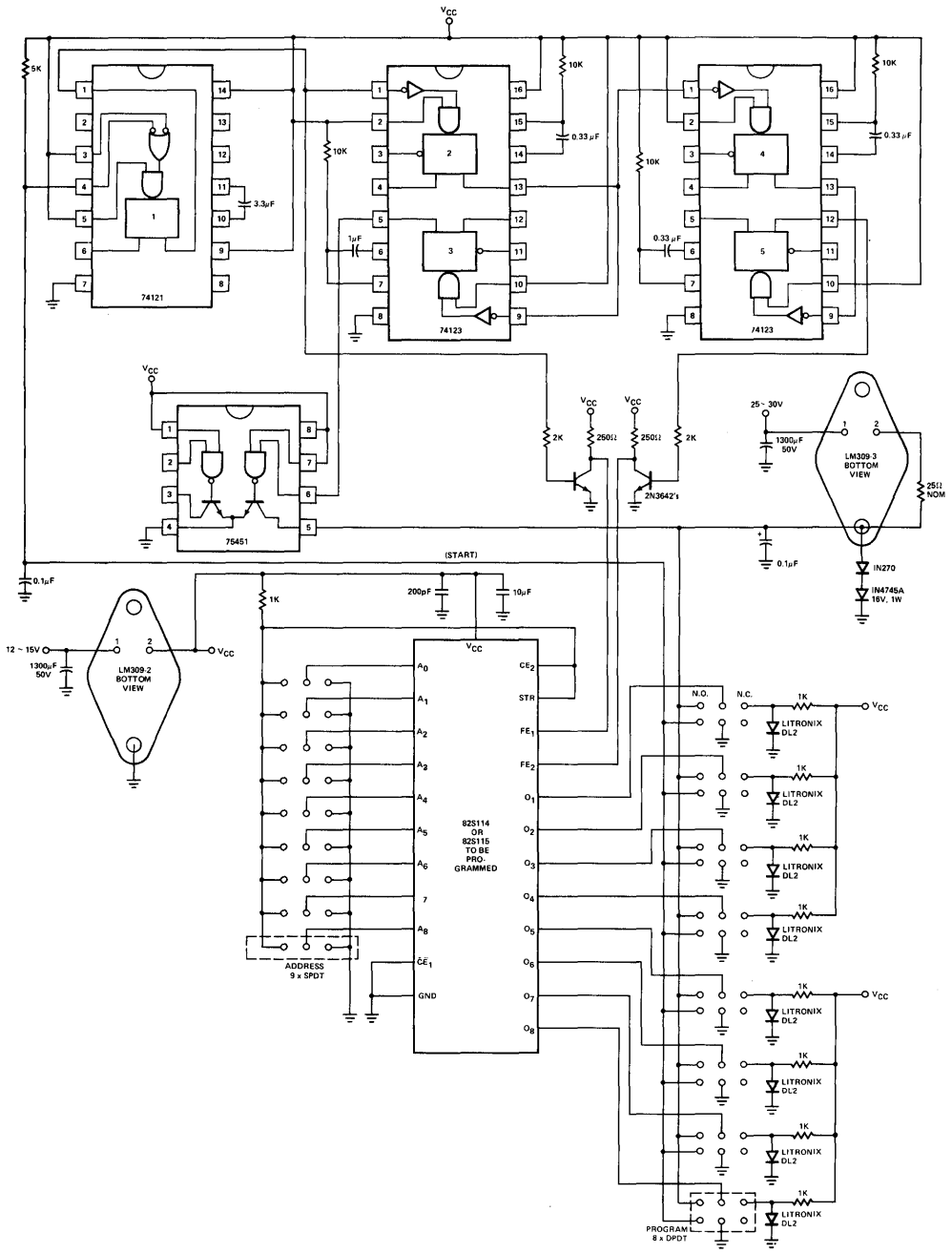
*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	$I_{CCP} = 200 \pm 25$ mA (Transient or steady state)	4.75	5.0	5.25	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +5.0 \pm .25$V	175	200	225	mA
Input Voltage						
V_{IL}	Low Level Input Voltage		0	0.4	0.8	V
V_{IH}	High Level Input Voltage		2.4		5.5	V
Input Current (FE_1 & FE_2 Only)						
I_{IL}	Low Level Input Current	$V_{IL} = +0.45$V			−100	μA
I_{IH}	High Level Input Current	$V_{IH} = +5.5$V			10	mA
Input Current (Except FE_1 & FE_2)						
I_{IL}	Low Level Input Current	$V_{IL} = +0.45$V			−100	μA
I_{IH}	High Level Input Current	$V_{IH} = +5.5$V			25	μA
V_{OUT}[2]	Output Programming Voltage	$I_{OUT} = 200 \pm 20$ mA (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17 \pm 1$V	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
t_P	FE_2 Programming Pulse Width		1		1.5	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			10	sec
T_{PS}	Programming Pause	$V_{CC} = 0$V	7			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				60	%

NOTES:
1. Bypass V_{CC} to GND with a 0.01 μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 60% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period ($V_{CC} = 0$V) of 3 mS.

82S114/115 MANUAL PROGRAMMER



TIMING SEQUENCE