DESCRIPTION

The 82S10/11 is a high speed 1024-bit random access memory organized as 1024 words X 1 bit. With a typical access time of 30ns, it is ideal for cache buffer applications and for systems requiring very high speed main memory.

Both the 82S10 and 82S11 require a single +5 volts power supply and feature very low current PNP input structures. They are fully TTL compatible, and include on-chip decoding and a chip enable input for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S10 and 82S11 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S10/11, I. For the military temperature range (−55°C to +125°C) specify S82S10/11, I.

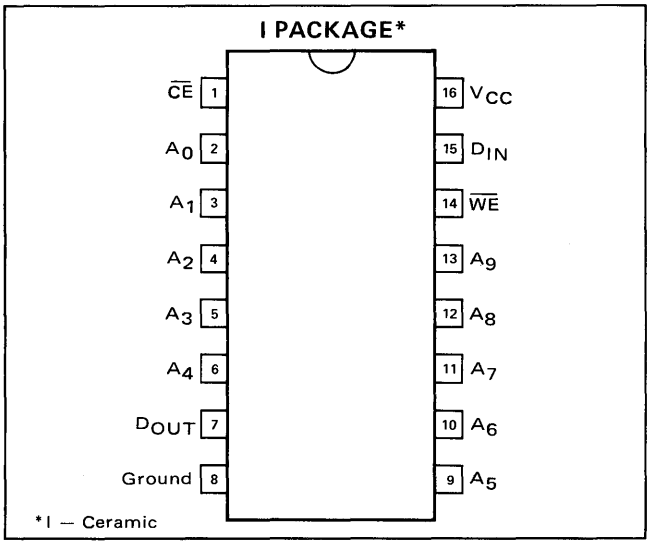
FEATURES

- ORGANIZATION – 1024 X 1
- ADDRESS ACCESS TIME:
  S82S10/11 – 70ns, MAXIMUM
  N82S10/11 – 45ns, MAXIMUM
- WRITE CYCLE TIME:
  S82S10/11 – 75ns, MAXIMUM
  N82S10/11 – 45ns, MAXIMUM
- POWER DISSIPATION – 0.5mW/BIT, TYPICAL
- INPUT LOADING:
  S82S10/11 – (−150μA) MAXIMUM
  N82S10/11 – (−100μA) MAXIMUM
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTIONS:
  82S10 – OPEN COLLECTOR
  82S11 – TRI-STATE
- NON-INVERTING OUTPUT
- BLANKED OUTPUT DURING WRITE
- 16 PIN CERAMIC PACKAGE

APPLICATIONS

HIGH SPEED MAIN FRAME
CACHE MEMORY
BUFFER STORAGE
WRITABLE CONTROL STORE

PIN CONFIGURATION

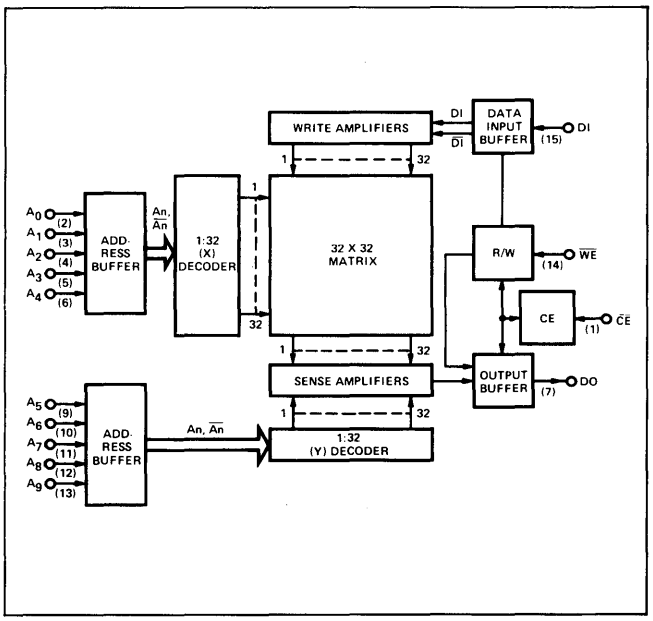


TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	D_{OUT}	
				82S10	82S11
READ	0	1	X	STORED DATA	STORED DATA
WRITE "0"	0	0	0	1	High-Z
WRITE "1"	0	0	1	1	High-Z
DISABLED	1	X	X	1	High-Z

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S10)	+5.5	Vdc
V_O	Off-State Output Voltage (82S11)	+5.5	Vdc
T_A	Operating Temperature Range (N82S10/11) (S82S10/11)	 0° to +75° −55° to +125°	 °C °C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS[9]

S82S10/11 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$
N82S10/11 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

PARAMETER		TEST CONDITIONS	S82S10/11			N82S10/11			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IL}	Low Level Input Voltage	V_{CC} = MIN (Note 1)			.80			.85	V
V_{IH}	High Level Input Voltage	V_{CC} = MAX (Note 1)	2.1			2.1			V
V_{IC}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −12mA (Note 1, 7)		−1.0	−1.5		−1.0	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = MIN, I_{OL} = 16mA (Note 1, 8)		0.35	0.50		0.35	0.45	V
V_{OH}	High Level Output Voltage (82S11)	V_{CC} = MIN, I_{OH} = −2mA (Note 1, 5)	2.4			2.4			V
I_{OLK}	Output Leakage Current (82S10)	V_{CC} = MAX, V_{OUT} = 5.5V (Note 6)		1	60		1	40	μA
$I_{O(OFF)}$	Hi-Z State Output Current (82S11)	V_{CC} = MAX, V_{OUT} = 5.5V V_{CC} = MAX, V_{OUT} = 0.45V (Note 6)		1 −1	100 −100		1 −1	60 −60	μA μA
I_{IL}	Low Level Input Current	V_{IN} = 0.45V		−10	−150		−10	−100	μA
I_{IH}	High Level Input Current	V_{IN} = 5.5V		1	40		1	25	μA
I_{OS}	Short Circuit Output Current (82S11)	V_{CC} = MAX, V_{OUT} = 0V (Note 3)	−20		−100	−20		−100	mA
I_{CC}	V_{CC} Supply Current	V_{CC} = MAX (Note 4) $0 < T_A < 25°C$ $T_A \geq 25°C$ $T_A \leq 0°C$		 120 95	 155 130 170		 120 95	 155 130 170	 mA mA mA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		4			4		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V		7			7		pF

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Duration of the short-circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic "1" stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Test each input one at the time.
8. Measured with a logic "0" stored. Output sink current is supplied through a resistor to V_{CC}.
9. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   ϕ_{JA} Junction to Ambient at 400 fpm air flow — 50°C/Watt
   ϕ_{JA} Junction to Ambient — still air — 90°C/Watt
   ϕ_{JA} Junction to Case — 20°C/Watt

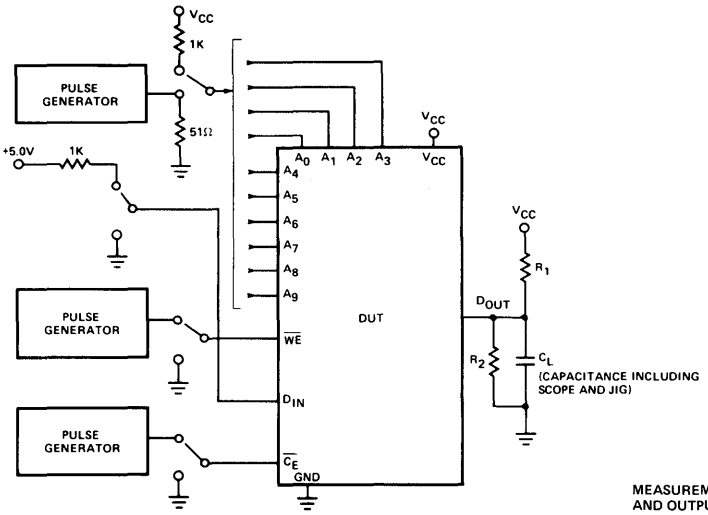
SWITCHING CHARACTERISTICS[3]

S82S10/11 $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, $4.5V \leq V_{CC} \leq 5.5$
N82S10/11 $0^{\circ}C \leq T_A \leq +75^{\circ}C$, $4.75V \leq V_{CC} \leq 5.25$

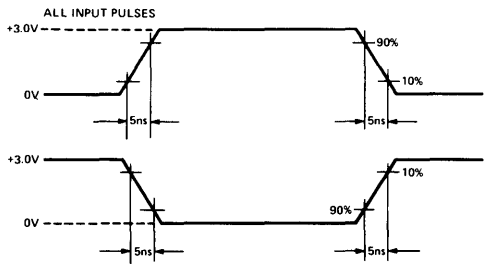
PARAMETER		TEST CONDITIONS	S82S10/11			N82S10/11			UNIT
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Propagation Delays									
T_{AA}	Address Access Time	C_L = 30pF R_1 = 270Ω R_2 = 600Ω		30	70		30	45	ns
T_{CE}	Chip Enable Access Time			15	45		15	30	ns
T_{CD}	Chip Enable Output Disable Time			15	45		15	30	ns
T_{WD}	Write Enable to Output Disable Time			20	45		20	30	ns
T_{WR}	Write Recovery Time			20	45		20	30	ns
Write Set-up Times									
T_{WSA}	Address to Write Enable		15	0		5	0		ns
T_{WSD}	Data In to Write Enable		55	35		40	35		ns
T_{WSC}	$\overline{CE}$ to Write Enable		5	0		5	0		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		10	0		5	0		ns
T_{WHD}	Data In to Write Enable		5	0		5	0		ns
T_{WHC}	$\overline{CE}$ to Write Enable		5	0		5	0		ns
T_{WP}	Write Enable Pulse Width (Note 2)		50	25		35	25		ns

AC TEST LOAD

LOADING CONDITION



INPUT PULSES



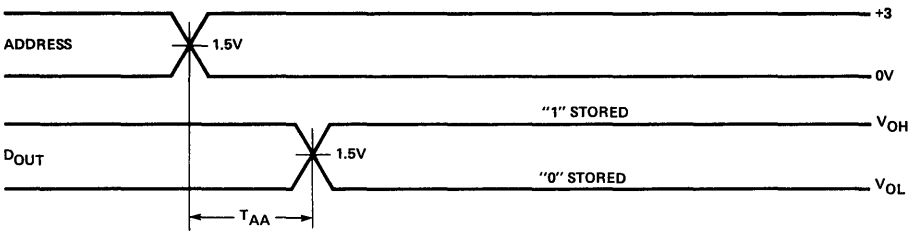
MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5V LEVEL OF INPUTS AND OUTPUT.

NOTES:
1. Typical values are at V_{CC} = +5.0V, and T_A = +25°C.
2. Minimum required to guarantee a WRITE into the slowest bit.
3. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} Junction to Ambient at 400 fpm air flow – 50° C/Watt
   θ_{JA} Junction to Ambient – still air – 90° C/Watt
   θ_{JA} Junction to Case – 20° C/Watt

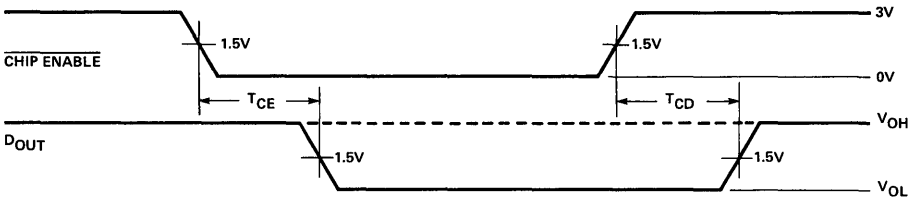
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

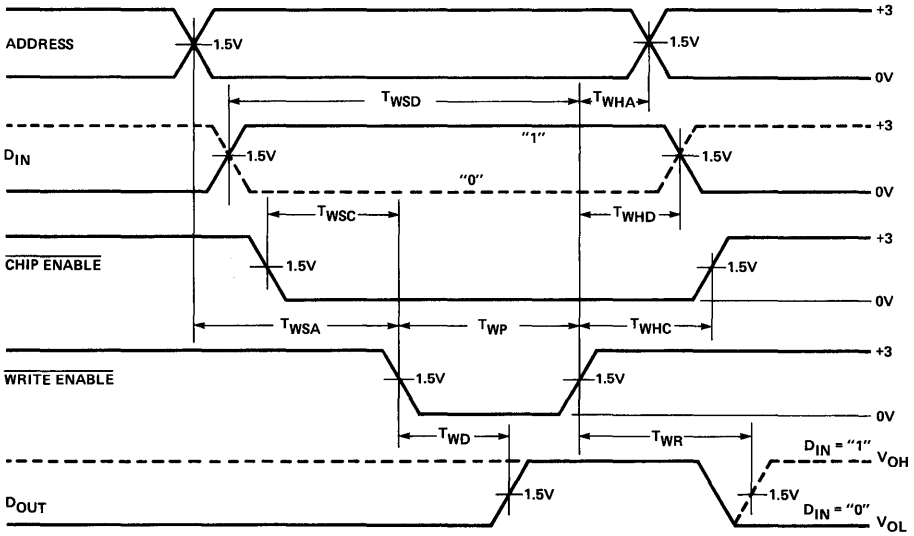
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{WR} Delay between end of WRITE ENABLE pulse and when DATA OUTPUT becomes valid. (Assuming ADDRESS still valid—not as shown.)

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT is in off state.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.