DESCRIPTION

The 82S09 is a 576-Bit, Schottky clamped TTL, random access memory, organized as 64X9. This organization allows byte manipulation of data, including parity. Where parity is not monitored, the ninth bit can be used as a flag or status indicator for each word stored. With a typical access time of 30ns, it is ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09 is fully TTL compatible, and features open collector outputs, chip enable input, and a very low current PNP input structure to enhance memory expansion.

During WRITE operation, the logic state of the device output follows the complement of the data input being written. This feature allows faster execution of WRITE-READ cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a WRITE cycle.

The 82S09 is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S09, I. For the military temperature range (−55°C to +125°C) specify S82S09, I.

FEATURES

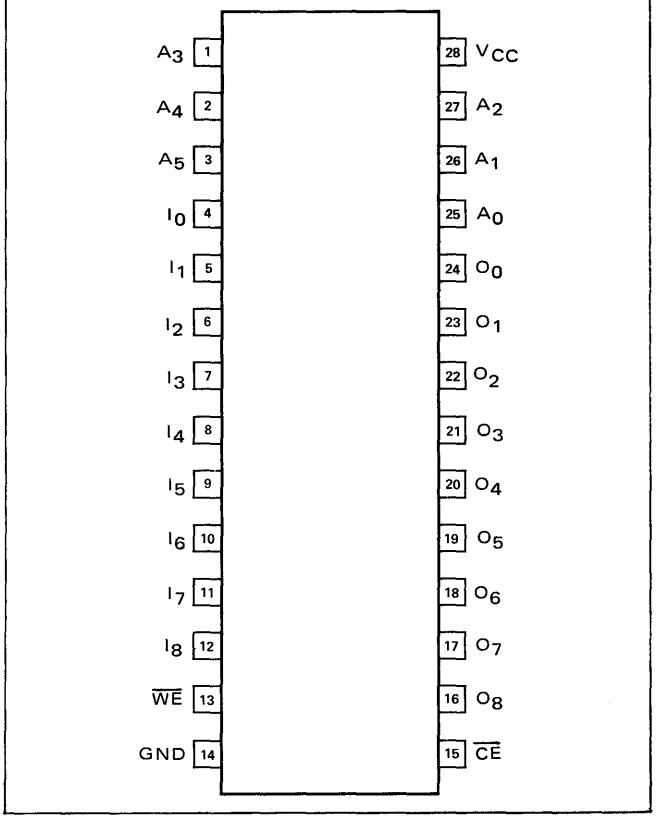
- ORGANIZATION – 64 X 9
- ADDRESS ACCESS TIME:
  - S82S09 – 80ns, MAXIMUM
  - N82S09 – 45ns, MAXIMUM
- WRITE CYCLE TIME:
  - S82S09 – 70ns, MAXIMUM
  - N82S09 – 45ns, MAXIMUM
- POWER DISSIPATION – 1.3mW/BIT TYPICAL
- INPUT LOADING:
  - S82S09 – (−150μA) MAXIMUM
  - N82S09 – (−100μA) MAXIMUM
- OUTPUT FOLLOWS COMPLEMENT OF DATA INPUT DURING WRITE
- ON-CHIP ADDRESS DECODING
- OPEN COLLECTOR OUTPUTS
- CHIP ENABLE FOR WORD EXPANSION
- BYTE I/O MANIPULATION, INCLUDING PARITY

APPLICATIONS

BUFFER MEMORY
CONTROL REGISTER
FIFO MEMORY
PUSH DOWN STACK
SCRATCH PAD

PIN CONFIGURATION

I PACKAGE

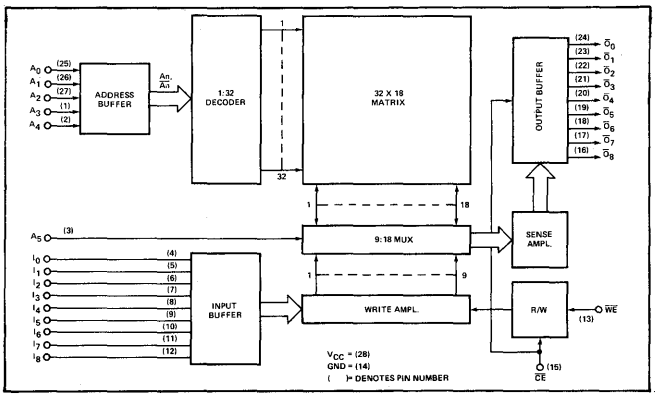


TRUTH TABLE

MODE	CE	WE	I_N	O_N
READ	0	1	X	Complement of Data Stored
WRITE "0"	0	0	0	1
WRITE "1"	0	0	1	0
DISABLED	1	X	X	1

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S10)	+5.5	Vdc
T_A	Operating Temperature Range		
	(N82S09)	0° to +75°	°C
	(S82S09)	−55° to +125°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS[7]

S82S09 $-55°C \leqslant T_A \leqslant +125°C$, $4.5V \leqslant V_{CC} \leqslant 5.5$
N82S09 $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25$

PARAMETER[1]		TEST CONDITIONS	S82S09			N82S09			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IL}	Low Level Input Voltage	V_{CC} = MIN			.80			.85	V
V_{IH}	High Level Input Voltage	V_{CC} = MAX	2.2			2.0			V
V_{IC}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −12mA (Note 5)		−1.0	−1.5		−1.0	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = MIN, I_{OL} = 6.4mA (Note 6)		0.35	0.50		0.35	0.5	V
I_{OLK}	Output Leakage Current	V_{CC} = MAX, V_{OUT} = 5.5V (Note 4)		1	60		1	40	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.45V		−10	−150		−10	−100	μA
I_{IH}	High Level Input Current	V_{IN} = 5.5V		1	40		1	25	μA
I_{CC}	V_{CC} Supply Current	V_{CC} = MAX (Note 3)		150	200		150	190	mA
C_{IN}	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V		5			5		pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V, V_{OUT} = 2.0V (Note 4)		8			8		pF

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{CC} is measured with the write enable and memory enable input grounded, all other inputs at 4.5V, and the outputs open.
4. Measured with V_{IH} applied to $\overline{CE}$.
5. Test each input one at the time.
6. Measured with the logic "0" stored. Output sink current is supplied through a resistor to V_{CC}.
7. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up.

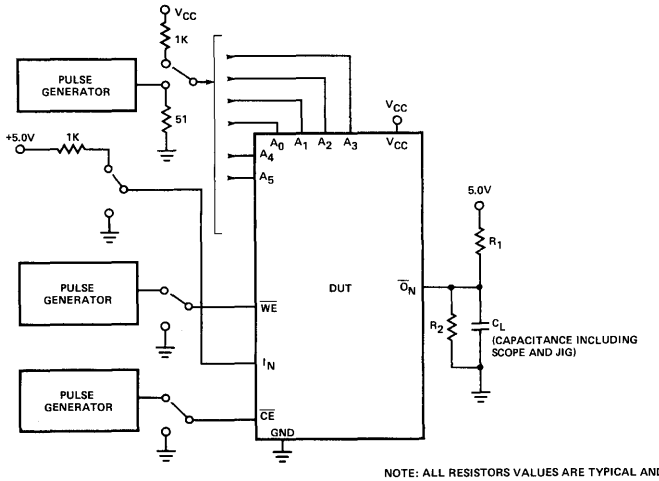
SWITCHING CHARACTERISTICS[3]

S82S09 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$
N82S09 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

PARAMETER		TEST CONDITIONS	S82S09			N82S09			UNIT
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
Propagation Delays									
T_{AA}	Address Access Time	C_L = 30pF R_1 = 600Ω R_2 = 900Ω		30	80		30	45	ns
T_{CE}	Chip Enable Access Time			15	50		15	30	ns
T_{CD}	Chip Enable Output Disable Time			15	50		15	30	ns
Write Set-up Times									
T_{WSA}	Address to Write Enable		10	0		5	0		ns
T_{WSD}	Data In to Write Enable		50	25		35	25		ns
T_{WSC}	$\overline{CE}$ to Write Enable		10	0		5	0		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		10	0		5	0		ns
T_{WHD}	Data In to Write Enable		5	0		5	0		ns
T_{WHC}	$\overline{CE}$ to Write Enable		10	0		5	0		ns
T_{WP}	Write Enable Pulse Width (Note 2)		50	25		35	25		ns

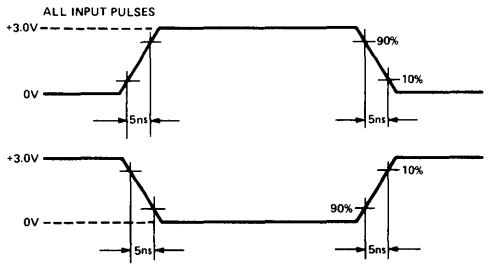
AC TEST LOAD

LOADING CONDITION



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

INPUT PULSES

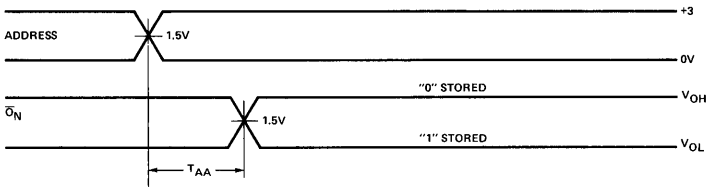


NOTES:
1. Typical values are at V_{CC} = +5.0V, and T_A = +25°C.
2. Minimum required to guarantee a WRITE into the slowest bit.
3. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up.

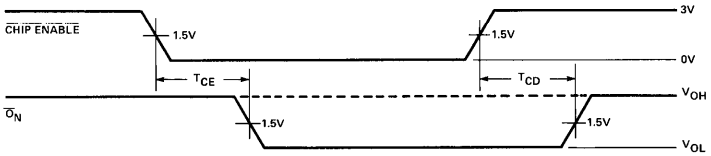
SWITCHING PARAMETERS MEASUREMENT INFORMATION

READ CYCLE

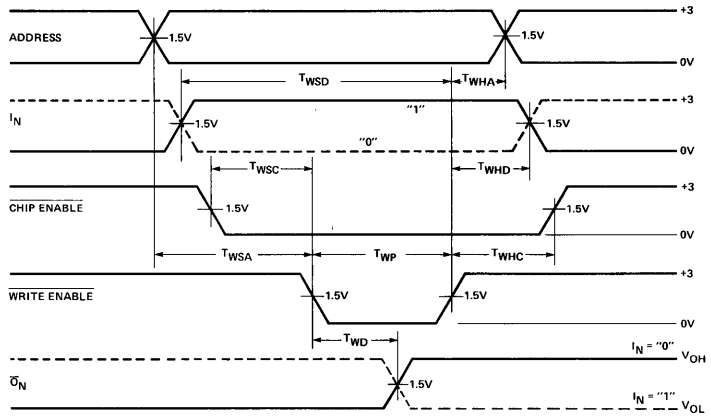
ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.

T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.

T_{WP} Width of WRITE ENABLE pulse.

T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT reflects complement of DATA INPUT.

T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.

T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.