# CMOS 8-BIT SINGLE-CHIP MICROCOMPUTER (TLCS-48C)

## TMP80C49AP/TMP80C49AP-6
## TMP80C39AP/TMP80C39AP-6
## TMP80C49AU/TMP80C49AU-6

## 1. GENERAL DESCRIPTION AND FEATURES

The TMP80C49A is a single chip microcomputer fabricated in Silicon Gate CMOS technology which provides internal 8-bit parallel architecture.
The following basic architectural functions of a computer have been included in a single chip; an 8-bit CPU, 128×8 RAM data memory, 2K×8 ROM program memory, 27 I/O lines and an 8-bit timer/event counter.
The TMP80C49A is particularly efficient as a controller. It has extensive bit handling capability as well as facilities for both binary and BCD arithmetic.

The TMP80C39A/-6 is the equivalent of a TMP80C49A/-6 without ROM program memory on chip. By using this device with external EPROM or RAM, software debugging becomes easy.

The TMP80C49AP/-6 and TMP80C39AP/-6 are in a standard Dual Inline Package.

The TMP80C49AU/-6 is in a 44-pin Micro Flat Package.

FEATURES

- TMP80C49AP/TMP80C39AP/TMP80C49AU

  1.36μs Instruction Cycle Time −40°C to 85°C, 5V±10%

- TMP80C49AP-6/TMP80C39AP-6/TMP80C49AU-6

  2.5μs Instruction Cycle Time −40°C to 85°C, 5V±20%

- Software Upward Compatible with TMP8049AP/INTEL's 8049
- 2K×8 masked ROM / 128×8 RAM
- Low Power

  10mA MAX. in Normal Operation ($V_{CC}$=5V, $f_{XTAL}$=6MHz)
  10μA MAX. in Power Down Mode ($V_{CC}$=5V, $f_{XTAL}$ : DC)

- Power Down Mode (Stand-by Mode)
- Halt Mode (Idle Mode)

# 2. PIN CONNECTIONS AND PIN FUNCTIONS

## 2.1 Pin Connections (Top View)

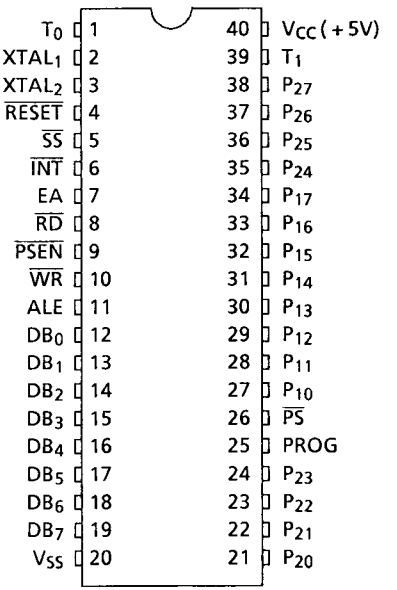



Figure 2.1 (1) DIP Pin Connections

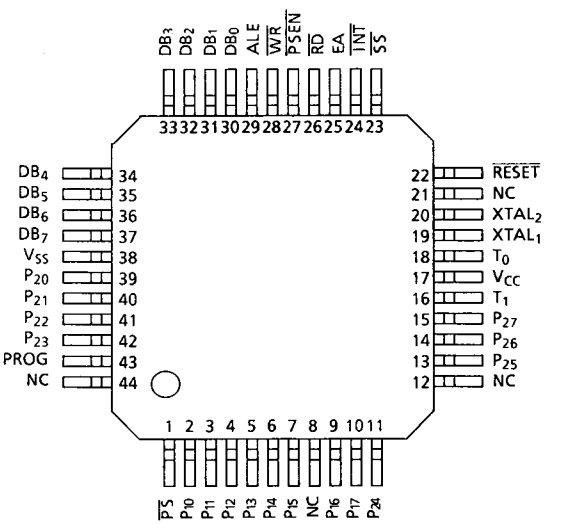



Figure 2.1 (2) Micro Flat Package Pin Connections

## 2.2 Pin Names And Pin Description

- $V_{SS}$ (Power Supply)

  Circuit GND potential

- $V_{CC}$ (Power Supply)

  +5V during operation

- $\overline{PS}$ (Input)

  The control signal for the power saving at the power down mode (Active Low)

- PROG (Output)

  Output strobe for the TMP82C43P I/O expander.

- $P_{10}$-$P_{17}$ (Input/Output) Port 1

  8-bit quasi-bidirectional port (Internal Pullup≃50KΩ).

- $P_{20}$-$P_{27}$ (Input/Output) Port 2

  8-bit quasi-bidirectional port (Internal Pullup≃50KΩ).
  $P_{20}$-$P_{23}$ contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for the TMP82C43P.

- $DB_0$-$DB_7$ (Input/Output, Tri-State)

  True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$.
  Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.

- $T_0$ (Input/Output)

  Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.

- $T_1$ (Input)

  Input pin testable using the JT1 and JNT1 instruction. Can be designated the event counter input using the timer/STRT CNT instruction.

- $\overline{INT}$ (Input)

  External interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

- $\overline{RD}$ (Output)

  Output strobe activated during a Bus read. Can be used to enable data onto the Bus from an external device. Used as a Read Strobe to External Data Memory (Active Low).

- $\overline{WR}$ (Output)

  Output strobe during a Bus write (Active Low). Used as a Write Strobe to External Data Memory.

- $\overline{RESET}$ (Input)

  Active Low signal which is used to initialize the Processor. Also used during the power down mode.

- ALE (Output)

  Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.

- $\overline{PSEN}$ (Output)

  Program Store Enable. This output occurs only during a fetch to external program memory (Active Low).

- $\overline{SS}$ (Input)

  Single step input can be used in conjunction with ALE to "single step" processor through each instruction when $\overline{SS}$ is low the CPU is placed into a wait state after it has completed the instruction being executed. Also used during the power down mode.

- EA (Input)

  External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug and essential for testing and program verification. (Active High)

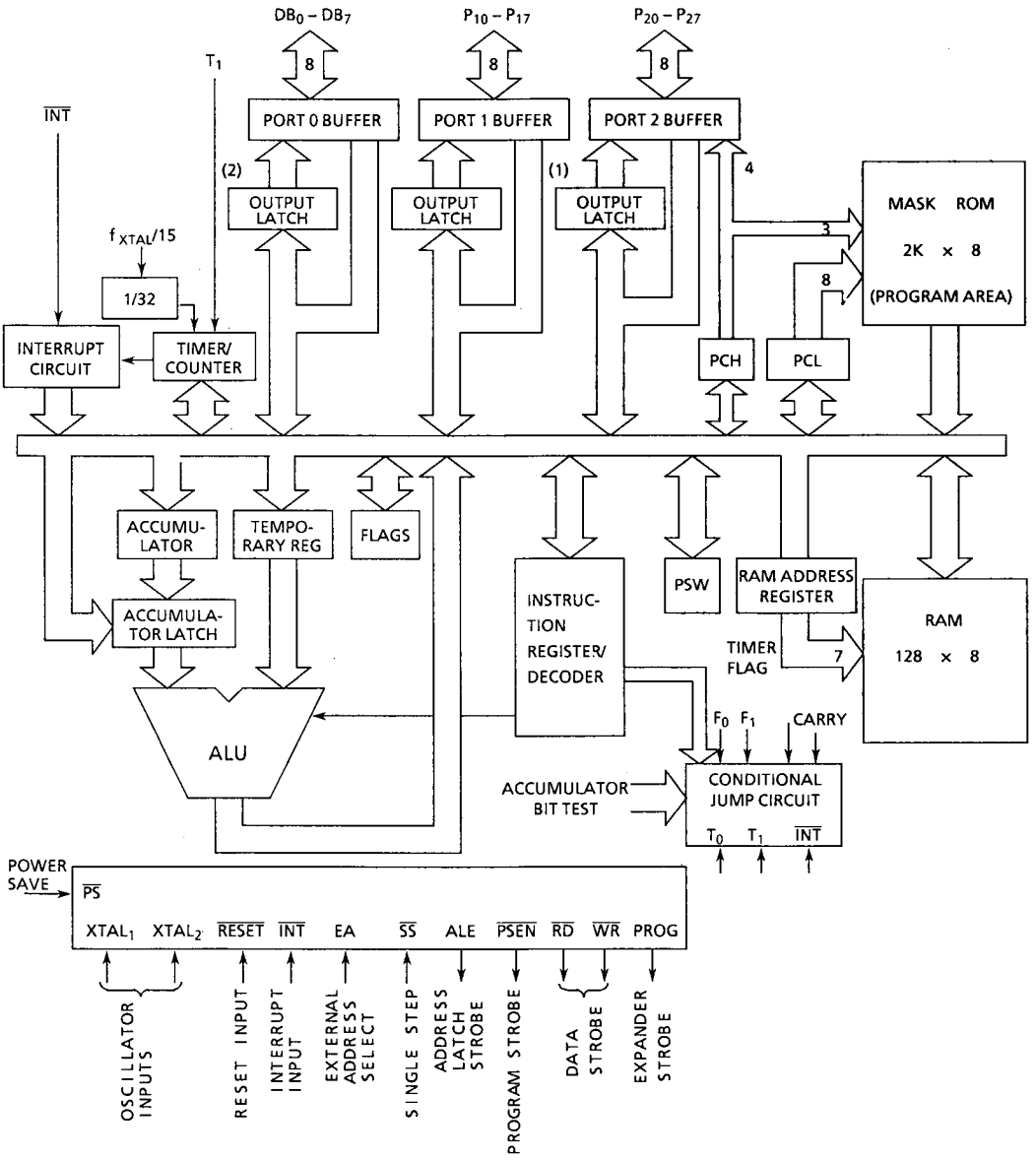
- $XTAL_1$ (Input)

  One side of crystal input for internal oscillator. Also input for external source.

- $XTAL_2$ (Input)

  Other side of crystal input.

## 2.3 Block Diagram




Note 1 : The lower order 4 bit of port 2 output latch are used also for input/output operations with the I/O expander.

Note 2 : The output latch of port 0 is also used for address output.

Figure 2.3 Block Diagram

# 3. MACHINE INSTRUCTION

The following symbols and codes are used in the list of machine instruction.

| Symbol | Meaning |
|---|---|
| Rr | Working register (0<r<7) |
| Pp | I/O port address P; (0<p<7) |
| JBb | Branch instruction in accordance with bit content (b) of operand |
| aH | Higher order 3 bits of a |
| aM | Medium order 4 bits of a |
| aL | Lower order 4 bits of a |
| aML | Medium order or lower order 8 bits of a |
| (a) | Content of a |
| [ (a) ] | Content of RAM addressed by a |
| EXT[ (a) ] | Content of external RAM addressed by a |
| PRO[ (a) ] | Content of ROM addressed by a |
| a<m> | Value at bit position m of a |
| a<m:n> | Value at bit position m to n of a |
| a←b | Store a into b |
| a↔b | Exchange a for b |
| · | Connection |
| ā | 1 complement of a |
| a+b | a plus b (Addition) |
| a−b | a minus b (Subtraction) |
| a∧b | Logical AND for a and b |
| a∨b | Logical OR for a and b |
| a∀b | Exclusive OR for a and b |
| a=b | a is equal to b |
| a<>b | a is not equal to b |
| (a) BCD | Converted value of accumulator |

List of TLCS-48 Machine Instruction (1/4)

| ITEM | Assembler Mnemonic | Object Code (1st) (2nd) Bin | Hex | Function | | Flag C, AC | Cycle |
|---|---|---|---|---|---|---|---|
| Accumulator Instruction | ADD A , Rr | 01101rrr | 68+r | (A)←(A)+(Rr) | r=0~7 | ↕ ↕ | 1 |
| | ADD A ,@Rr | 0110000r | 60+r | (A)←(A)+[(Rr)] | r=0,1 | ↕ ↕ | 1 |
| | ADD A ,#i | 00000011<br>iiiiiiii | 03<br>ii | (A)←(A)+i | | ↕ ↕ | 2 |
| | ADDC A , Rr | 01111rrr | 78+r | (A)←(A)+(Rr)+(c) | r=0~7 | ↕ ↕ | 1 |
| | ADDC A ,@Rr | 0111000r | 70+r | (A)←(A)+[(Rr)]+(c) | r=0,1 | ↕ ↕ | 1 |
| | ADDC A ,#i | 00010011<br>iiiiiiii | 13<br>ii | (A)←(A)+i+(c) | | ↕ ↕ | 2 |
| | ANL A , Rr | 01011rrr | 58+r | (A)←(A) ∧(Rr) | r=0~7 | | 1 |
| | ANL A ,@Rr | 0101000r | 50+r | (A)←(A) ∧[(Rr)] | r=0,1 | | 1 |
| | ANL A ,#i | 01010011<br>iiiiiiii | 53<br>ii | (A)←(A) ∧i | | | 2 |
| | ORL A , Rr | 01001rrr | 48+r | (A)←(A) ∨(Rr) | r=0~7 | | 1 |
| | ORL A ,@Rr | 0100000r | 40+r | (A)←(A) ∨[(Rr)] | r=0,1 | | 1 |
| | ORL A ,#i | 01000011<br>iiiiiiii | 43<br>ii | (A)←(A) ∨i | | | 2 |
| | XRL A , Rr | 11011rrr | D8+r | (A)←(A) ∀(Rr) | r=0~7 | | 1 |
| | XRL A ,@Rr | 1101000r | D0+r | (A)←(A) ∀[(Rr)] | r=0,1 | | 1 |
| | XRL A ,#i | 11010011<br>iiiiiiii | D3<br>ii | (A)←(A) ∀i | | | 2 |
| | INC A | 00010111 | 17 | (A)←(A)+1 | | | 1 |
| | DEC A | 00000111 | 07 | (A)←(A)-1 | | | 1 |
| | CLR A | 00100111 | 27 | (A)←0 | | | 1 |
| | CPL A | 00110111 | 37 | (A)←NOT(A) | | | 1 |
| | DA A | 01010111 | 57 | (A)←(A)BCD | | ↕ | 1 |
| | SWAP A | 01000111 | 47 | (A)<7:4> ↔(A)<3:0> | | | 1 |
| | RL A | 11100111 | E7 | (A)<n+1> ←(A)<n><br>(A)<0> ←(A)<7> | n=0~6 | | 1 |
| | RLC A | 11110111 | F7 | (A)<n+1> ←(A)<n><br>(C)←(A)<7><br>(A)<0> ←(C) | n=0~6 | ↕ | 1 |
| | RR A | 01110111 | 77 | (A)<n> ←(A)<n+1><br>(A)<7> ←(A)<0> | n=0~6 | | 1 |
| | RRC A | 01100111 | 67 | (A)<n> ←(A)<n+1><br>(C)←(A)<0><br>(A)<7> ←(C) | n=0~6 | ↕ | 1 |
| I/O | IN A , Pp | 000010pp | 08+p | (A)←(Pp) | P=1,2 | | 2 |
| | OUTL Pp, A | 001110pp | 38+p | (Pp) ←(A) | P=1,2 | | 2 |
| | ANL Pp,#i | 100110pp<br>iiiiiiii | 98+p<br>ii | (Pp) ←(Pp)∧i | P=1,2 | | 2 |
| | ORL Pp,#i | 100010pp<br>iiiiiiii | 88+p<br>ii | (Pp) ←(Pp)∨i | P=1,2 | | 2 |

List of TLCS-48 Machine Instruction (2/4)

| ITEM | Assembler Mnemonic | Object Code (1st) (2nd) Bin | Hex | Function | Flag C, AC | Cycle |
|---|---|---|---|---|---|---|
| I/O | INS A , BUS | 00001000 | 08 | (A)←(BUS) | | 2 |
| | OUTL BUS, A | 00000010 | 02 | (BUS)←(AC) | | 2 |
| | ANL BUS,#i | 10011000<br>iiiiiiii | 98<br>ii | (BUS)←(BUS) ∧i | | 2 |
| | ORL BUS,#i | 10001000<br>iiiiiiii | 88<br>ii | (BUS)←(BUS) ∨i | | 2 |
| | MOVD A , Pp | 000011pp | 0C+p | (A)<3:0> ←(Pp) p=4~7<br>(A)<7:4> ←0 | | 2 |
| | MOVD Pp, A | 001111pp | 3C+p | (Pp) ←(A)<3:0> p=4~7 | | 2 |
| | ANLD Pp, A | 100111pp | 9C+p | (Pp) ←(Pp)∧(A)<3:0> p=4~7 | | 2 |
| | ORLD Pp, A | 100011pp | 8C+p | (Pp) ←(Pp)∨(A)<3:0> p=4~7 | | 2 |
| (1) | INC Rr | 00011rrr | 18+r | (Rr) ←(Rr)+1 r=0~7 | | 1 |
| | INC @Rr | 0001000r | 10+r | [(Rr)] ←[(Rr)]+1 r=0,1 | | 1 |
| | DEC Rr | 11001rrr | C8+r | (Rr) ←(Rr)−1 r=0~7 | | 1 |
| Branch Instruction | JMP a | aH00100<br>aML | aH+4 | (PC)<10:0> ←a<br>(PC)<11> ←(DBF) | | 2 |
| | JMPP @A | 10110011 | B3 | (PC)<7:0>←PRO[(PC)<11:8>·(A)] | | 2 |
| | DJNZ Rr, a | 11101rrr<br>aML | E8+r | (Rr) ←(Rr)−1 r=0~7<br>if(Rr) ≠0then(PC)<7:0>←aML<br>else no operation | | 2 |
| | JC a | 11110110<br>aML | F6 | if(C)=1 then(PC)<7:0>←aML<br>else no operation | | 2 |
| | JNC a | 11100110<br>aML | E6 | if(C)=0 then(PC)<7:0>←aML<br>else no operation | | 2 |
| | JZ a | 11000110<br>aML | C6 | if(A)=0 then(PC)<7:0>←aML<br>else no operation | | 2 |
| | JNZ a | 10010110<br>aML | 96 | if(A)≠0 then(PC)<7:0>←aML<br>else no operation | | 2 |
| | JTO a | 00110110<br>aML | 36 | if T0=1 then(PC)<7:0>←aML<br>else no operation | | 2 |
| | JNTO a | 00100110<br>aML | 26 | if T0=0 then(PC)<7:0>←aML<br>else no operation | | 2 |
| | JT1 a | 01010110<br>aML | 56 | if T1=1 then(PC)<7:0>←aML<br>else no operation | | 2 |
| | JNT1 a | 01000110<br>aML | 46 | if T1=0 then(PC)<7:0>←aML<br>else no operation | | 2 |
| | JF0 a | 10110110<br>aML | B6 | if F0=1 then(PC)<7:0>←aML<br>else no operation | | 2 |
| | JF1 a | 01110110<br>aML | 76 | if F1=1 then(PC)<7:0>←aML<br>else no operation | | 2 |
| | JTF a | 00010110<br>aML | 16 | if TF=1 then(PC)<7:0>←aML<br>else no operation | | 2 |

(1) ····· Register Instruction

List of TLCS-48 Machine Instruction (3/4)

| ITEM | Assembler Mnemonic | Object Code (1st) (2nd) Bin | Hex | Function | Flag C, AC | Cycle |
|---|---|---|---|---|---|---|
| (2) | JNI a | 10000110 aML | 86 | if INT =0 then(PC)<7:0>←aML else no operation | | 2 |
| | JBb a | bbb10010 aML | b+12 | if (A)<b>=1 then (PC)<7:0>←aML else no operation b=0~7 | | 2 |
| (3) | CALL a | aH10100 aML | aH+14 | [(SP)] ←(PSW)<7:4>·(PC) (SP) ←(SP)+1 (PC)<10:0> ←a (PC)<11> ←(DBF) | | 2 |
| | RET | 10000011 | 83 | (SP)←(SP)−1 (PC) ←[(SP)]<11:0> | | 2 |
| | RETR | 10010011 | 93 | (SP)←(SP)−1 (PC) ←[(SP)]<11:0> (PSW)<7:4> ←[(SP)]<15:12> | ↕ ↕ | 2 |
| (4) | CLR C | 10010111 | 97 | (C)←0 | | 1 |
| | CPL C | 10100111 | A7 | (C)←NOT(C) | | 1 |
| | CLR F0 | 10000101 | 85 | (F0) ←0 | | 1 |
| | CPL F0 | 10010101 | 95 | (F0) ←NOT(F0) | | 1 |
| | CLR F1 | 10100101 | A5 | (F1) ←0 | | 1 |
| | CPL F1 | 10110101 | B5 | (F1) ←NOT(F1) | | 1 |
| Move Instruction | MOV A , Rr | 11111rrr | F8+r | (A)←(Rr) r=0~7 | | 1 |
| | MOV A ,@Rr | 1111000r | F0+r | (A)←[(Rr)] r=0,1 | | 1 |
| | MOV A ,#i | 00100011 iiiiiiii | 23 ii | (A) ←i | | 2 |
| | MOV Rr, A | 10101rrr | A8+r | (Rr)←(A) r=0~7 | | 1 |
| | MOV @Rr, A | 1010000r | A0+r | [(Rr)]←(A) r=0,1 | | 1 |
| | MOV Rr,#i | 10111rrr iiiiiiii | B8+r ii | (Rr)←i r=0~7 | | 2 |
| | MOV @Rr,#i | 1011000r iiiiiiii | B0+r ii | [(Rr)]←i r=0,1 | | 2 |
| | MOV A,PSW | 11000111 | C7 | (A) ←(PSW) | | 1 |
| | MOV PSW,A | 11010111 | D7 | (PSW) ←(A) | | 1 |
| | XCH A,Rr | 00101rrr | 28+r | (A) ↔(Rr) r=0~7 | | 1 |
| | XCH A,@Rr | 0010000r | 20+r | (A) ↔[(Rr)] r=0,1 | | 1 |
| | XCHD A,@Rr | 0011000r | 30+r | (A)<3:0>↔[(Rr)<3:0>] r=0,1 | | 1 |
| | MOVX @Rr,A | 1001000r | 90+r | EXT[(Rr)] ←(A) r=0,1 | | 1 |
| | MOVX A,@Rr | 1000000r | 80+r | (A) ←EXT[(Rr)] r=0,1 | | 1 |
| | MOVP A,@A | 10100011 | A3 | (A) ←PRO[(PC)<11:8>·(A)] | | 1 |
| | MOVP3 A,@A | 11100011 | E3 | (A) ←PRO[(PC)<11>·011·(A)] | | 1 |

(2) ····· Branch Instruction (3) ····· Subroutine Instruction
(4) ····· Flag Instruction

List of TLCS-48 Machine Instruction (4/4)

| ITEM | Assembler Mnemonic | Object Code (1st) (2nd) Bin | Hex | Function | Flag C, AC | Cycle |
|---|---|---|---|---|---|---|
| Timer Counter | MOV A,T | 01000010 | 42 | (A) ←(TR) | | 1 |
| | MOV T,A | 01100010 | 62 | (TR)←(A) | | 1 |
| | STRT T | 01010101 | 55 | Start Timer | | 1 |
| | STRT CNT | 01000101 | 45 | Start Counter | | 1 |
| | STOP TCNT | 01100101 | 65 | Stop Timer/Counter | | 1 |
| | EN TCNTI | 00100101 | 25 | Enable Timer/Counter Interrupt | | 1 |
| | DIS TCNTI | 00110101 | 35 | Disable Timer/Counter Interrupt | | 1 |
| Control | EN I | 00000101 | 05 | Enable External Interrupt | | 1 |
| | DIS I | 00010101 | 15 | Disable External Interrupt | | 1 |
| | SEL RB0 | 11000101 | C5 | (BS)← 0 | | 1 |
| | SEL RB1 | 11010101 | D5 | (BS)← 1 | | 1 |
| | SEL MB0 | 11100101 | E5 | (DBF) ← 0 | | 1 |
| | SEL MB1 | 11110101 | F5 | (DBF) ← 1 | | 1 |
| | ENT0 CLK | 01110101 | 75 | Enable Clock Output on To | | 1 |
| | HALT | 00000001 | 01 | Halt | | 1 |
| (5) | NOP | 00000000 | 00 | no operation | | 1 |

(5) ····· Other

# 4. ELECTRICAL CHARACTERISTICS

## 4.1 Absolute Maximum Ratings

TMP80C49AP/C39AP/C49AU

| SYMBOL | ITEM | RATTING |
|---|---|---|
| $V_{CC}$ | $V_{CC}$ Supply Voltage (with respect to GND (VSS)) | − 0.5V to + 7V |
| $V_{INA}$ | Input Voltage (Except EA) | − 0.5V to VCC + 0.5V |
| $V_{INB}$ | Input Voltage (Only EA) | − 0.5V to + 13V |
| $P_D$ | Power Dissipation (Ta = 85°C) | 250mW |
| $T_{SOLDER}$ | Soldering Temperature (Soldering Time 10 sec) | 260°C |
| $T_{STG}$ | Storage Temperature | − 65°C to 150°C |
| $T_{OPR}$ | Operating Temperature | − 40°C to 85°C |

## 4.2 DC Characteristics

TMP80C49AP/C39AP/C49AU
$T_{OPR}$ = − 40°C to 85°C, VCC = + 5V ± 10%, $V_{SS}$ = 0V, unless otherwise noted.

| SYMBOL | PARAMETER | | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| VIL | Input Low Voltage (Except $XTAL_1$, $XTAL_2$, $\overline{RESET}$) | | | − 0.5 | — | 0.8 | V |
| VIL1 | Input Low Voltage ($XTAL_1$, $XTAL_2$, $\overline{RESET}$) | | | − 0.5 | — | 0.6 | V |
| VIH | Input High Voltage (Except $XTAL_1$, $XTAL_2$, $\overline{RESET}$, $\overline{PS}$) | | | 2.2 | — | $V_{CC}$ | V |
| VIH1 | Input High Voltage ($XTAL_1$, $XTAL_2$, $\overline{RESET}$, $\overline{PS}$) | | | 0.7x $V_{CC}$ | — | $V_{CC}$ | V |
| VOL | Output Low Voltage (Except $P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOL = 1.6mA | — | — | 0.45 | V |
| VOL1 | Output Low Voltage ($P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOL = 1.2mA | — | — | 0.45 | V |
| VOH11 | Output High Voltage (Except $P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOH = − 1.6mA | 2.4 | — | — | V |
| VOH12 | Output High Voltage (Except $P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOH = − 400μA | $V_{CC}$ − 0.8 | — | — | V |
| VOH21 | Output High Voltage ($P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOH = − 50μA | 2.4 | — | — | V |
| VOH22 | Output High Voltage ($P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOH = − 25μA | $V_{CC}$ − 0.8 | — | — | V |
| ILI | Input Leak Current ($T_1$, $\overline{INT}$, EA, $\overline{PS}$) | | $V_{SS} \leqq V_{IN} \leqq V_{CC}$ | — | — | ± 10 | μA |
| ILI1 | Input Leak Current ($\overline{SS}$, $\overline{RESET}$) | | $V_{SS} \leqq V_{IN} \leqq V_C$ | — | — | − 50 | μA |
| ILI2 | Output Leak Current ($P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | $V_{SS}$ + 0.45V $\leqq V_{IN} \leqq V_{CC}$ | — | — | − 500 | μA |
| ILO | Output Leak Current (BUS, $T_O$) (High impedace condition) | | $V_{SS}$ + 0.45V $\leqq V_{IN} \leqq V_{CC}$ | — | — | ± 10 | μA |
| ICC1 | $V_{CC}$ Supply Current | Normal operation | $V_{CC}$ = 5V, $f_{XTAL}$ = 6MHz VIH = $V_{CC}$ − 0.2V VIL = 0.2V | — | — | 10 | mA |
| ICCH1 | | HALT Mode | | — | — | 2.5 | |
| ICC2 | $V_{CC}$ Supply Current | Normal operation | $V_{CC}$ = 5V, $f_{XTAL}$ = 11MHz VIH = $V_{CC}$ − 0.2V VIL = 0.2V | — | — | 15 | mA |
| ICCH2 | | HALT Mode | | — | — | 4.0 | |

## 4.3 AC Charactristics

TMP80C49AP/C39AP/C49AU
$T_{OPR}$ = −40°C to 85°C, $V_{CC}$ = +5V ± 10%, $V_{SS}$ = 0V, unless otherwise noted.

| SYMBOL | PARAMETER | TEST CONDITION | f (t) | 11MHz | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| t | Clock Period | Note 2 | 1/xtal f | 90.9 | 1000 | ns |
| $t_{LL}$ | ALE Pulse Width | | 3.5t − 170 | 150 | − | ns |
| $t_{AL}$ | Address Setup Time (ALE) | | 2t − 110 | 70 | − | ns |
| $t_{LA}$ | Address Hold Time (ALE) | CL = 20pF | t − 40 | 50 | − | ns |
| $t_{CC1}$ | Control Pulse Width ($\overline{RD}$, $\overline{WR}$) | | 7.5t − 200 | 480 | − | ns |
| $t_{CC2}$ | Control Pulse Width ($\overline{PSEN}$) | | 6t − 200 | 350 | − | ns |
| $t_{DW}$ | Data Setup Time ($\overline{WR}$) | | 6.5t − 200 | 390 | − | ns |
| $t_{WD}$ | Data Hold Time ($\overline{WR}$) | CL = 20pF | t − 50 | 40 | − | ns |
| $t_{DR}$ | Data Hold Time ($\overline{RD}$, $\overline{PSEN}$) | CL = 20pF | 1.5t − 30 | 0 | 110 | ns |
| $t_{RD1}$ | Data Input Read Time ($\overline{RD}$) | | 5.5t − 120 | − | 375 | ns |
| $t_{RD2}$ | Data Input Read Time ($\overline{PSEN}$) | | 4t − 120 | − | 240 | ns |
| $t_{AW}$ | Address Setup Time ($\overline{WR}$) | | 5t − 150 | 300 | − | ns |
| $t_{AD1}$ | Address Setup Time ($\overline{RD}$) | | 10t − 170 | − | 730 | ns |
| $t_{AD2}$ | Address Setup Time ($\overline{PSEN}$) | | 7t − 170 | − | 460 | ns |
| $t_{AFC1}$ | Address Float Time ($\overline{RD}$, $\overline{WR}$) | CL = 20pF | 2t − 40 | 140 | − | ns |
| $t_{AFC2}$ | Address Float Time ($\overline{PSEN}$) | CL = 20pF | 0.5t − 40 | 10 | − | ns |
| $t_{LAFC1}$ | ALE to Control Time ($\overline{RD}$, $\overline{WR}$) | | 3t − 75 | 200 | − | ns |
| $t_{LAFC2}$ | ALE to Control Time ($\overline{PSEN}$) | | 1.5t − 75 | 60 | − | ns |
| $t_{CA1}$ | Control to ALE Time ($\overline{RD}$, $\overline{WR}$, PROG) | | t − 65 | 25 | − | ns |
| $t_{CA2}$ | Control to ALE Time ($\overline{PSEN}$) | | 4t − 70 | 290 | − | ns |

AC Charactristics (Continue)
$T_{OPR}$ = −40°C to 85°C, $V_{CC}$ = +5V ± 10%, $V_{SS}$ = 0V, unless otherwise noted.

| SYMBOL | PARAMETER | TEST CONDITION | f(t) | 11MHz | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| $t_{CP}$ | Port Control Setup Time (PROG) | | 1.5t − 80 | 50 | − | ns |
| $t_{PC}$ | Port Control Hold Time (PROG) | | 4t − 260 | 100 | − | ns |
| $t_{PR}$ | Port 2 Input Data Setup Time (PROG) | | 8.5t − 120 | − | 650 | ns |
| $t_{PF}$ | Port 2 Input Data Hold Time (PROG) | | 1.5t | 0 | 140 | ns |
| $t_{DP}$ | Port 2 Output Data Setup Time (PROG) | | 6t − 290 | 250 | − | ns |
| $t_{PD}$ | Port 2 Output Data Hold Time (PROG) | | 1.5t − 90 | 40 | − | ns |
| $t_{PP}$ | PROG Pulse Width | | 10.5t − 250 | 700 | − | ns |
| $t_{PL}$ | Port 2 I/O Data Setup Time (ALE) | | 4t − 200 | 160 | − | ns |
| $t_{LP}$ | Port 2 I/O Data Hold Time (ALE) | | 0.5t − 30 | 15 | − | ns |
| $t_{PV}$ | Port Output Delay Time (ALE) | | 4.5t + 100 | − | 510 | ns |
| $t_{OPRR}$ | $T_0$ Clock Period | | 3t | 270 | − | ns |
| $t_{CY}$ | Cycle Time | | 15t | 1.36 | 15.0 | μs |

Note : 1. Control Output CL = 80pF. BUS Output CL = 150pF.
2. The f(t) assumes 50% duty cycle on $XTAL_1$ and $XTAL_2$.
The Max. Clock frequency is 11MHz. and the Min. Clock frequency is 1MHz.

## 4.4 Absolute Maximum Ratings

TMP80C49AP-6/TMP80C39AP-6/TMP80C49AU-6

| SYMBOL | ITEM | RATTING |
|---|---|---|
| $V_{CC}$ | $V_{CC}$ Supply Voltage (with respect to GND ($V_{SS}$)) | − 0.5V to + 7V |
| $V_{INA}$ | Input Voltage (Except EA) | − 0.5V to VCC + 0.5V |
| $V_{INB}$ | Input Voltage (Only EA) | − 0.5V to + 13V |
| $P_D$ | Power Dissipation (Ta = 85°C) | 250mW |
| $T_{SOLDER}$ | Soldering Temperature (Soldering Time 10 sec) | 260°C |
| $T_{STG}$ | Storage Temperature | − 65°C to 150°C |
| $T_{OPR}$ | Operating Temperature | − 40°C to 85°C |

## 4.5 DC Characteristics (I)

TMP80C49AP-6/TMP80C39AP-6/TMP80C49AU-6
$T_{OPR}$ = − 40°C to 85°C, $V_{CC}$ = + 5V ± 10%, $V_{SS}$ = 0V, unless otherwise noted

| SYMBOL | PARAMETER | | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| VIL | Input Low Voltage | | | − 0.5 | — | 0.8 | V |
| VIH | Input High Voltage (Except $XTAL_1$, $XTAL_2$, $\overline{RESET}$, $\overline{PS}$) | | | 2.2 | — | $V_{CC}$ | V |
| VIH1 | Input High Voltage ($XTAL_1$, $XTAL_2$, $\overline{RESET}$, $\overline{PS}$) | | | 0.7 x $V_{CC}$ | — | $V_{CC}$ | V |
| VOL | Output Low Voltage (Except $P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOL = 1.6mA | — | — | 0.45 | V |
| VOL1 | Output Low Voltage ($P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOL = 1.2mA | — | — | 0.45 | V |
| VOH11 | Output High Voltage (Except $P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOH = − 1.6mA | 2.4 | — | — | V |
| VOH12 | Output High Voltage ($P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOH = − 400μA | $V_{CC}$ − 0.8 | — | — | V |
| VOH21 | Output High Voltage ($P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOH = − 50μA | 2.4 | — | — | V |
| VOH22 | Output High Voltage ($P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOH = − 25μA | $V_{CC}$ − 0.8 | — | — | V |
| ILI | Input Leak Current ($T_1$, $\overline{INT}$, EA, $\overline{PS}$) | | $V_{SS} \leqq V_{IN} \leqq V_{CC}$ | — | — | ± 10 | μA |
| ILI1 | Input Leak Current ($\overline{SS}$, $\overline{RESET}$) | | $V_{SS} \leqq V_{IN} \leqq V_{CC}$ | — | — | − 50 | μA |
| ILI2 | Input Leak Current ($P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | $V_{SS}$ + 0.45V $\leqq V_{IN} \leqq V_{CC}$ | — | — | − 500 | μA |
| ILO | Output Leak Current (BUS, $T_0$) (High impedance condition) | | $V_{SS}$ + 0.45V $\leqq V_{IN} \leqq V_{CC}$ | — | — | ± 10 | μA |
| ICC1 | $V_{CC}$ Supply Current | Normal operation | $V_{CC}$ = 5V, $f_{XTAL}$ = 6MHz VIH = $V_{CC}$ − 0.2V VIL = 0.2V | — | — | 10 | mA |
| ICCH1 | | HALT Mode | | — | — | 2.5 | |

## 4.6 DC Characteristics (II)

TMP80C49AP-6/TMP80C39AP-6/TMP80C49AU-6
$T_{OPR}$ = −40°C to 85°C, $V_{CC}$ = +5V ± 20%, $V_{SS}$ = 0V, unless otherwise noted

| SYMBOL | PARAMETER | | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| VIL | Input Low Voltage | | | −0.5 | — | 0.15 × $V_{CC}$ | V |
| VIH | Input High Voltage (Except $XTAL_1$, $XTAL_2$, $\overline{RESET}$, $\overline{PS}$) | | | 0.5 × $V_{CC}$ | — | $V_{CC}$ | V |
| VIH1 | Input High Voltage ($XTAL_1$, $XTAL_2$, $\overline{RESET}$, $\overline{PS}$) | | | 0.7 × $V_{CC}$ | — | $V_{CC}$ | V |
| VOL | Output Low Voltage (Except $P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOL = 1.6mA | — | — | 0.45 | V |
| VOL1 | Output Low Voltage ($P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOL = 1.2mA | — | — | 0.45 | V |
| VOH12 | Output High Voltage (Except $P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOH = −400μA | $V_{CC}$ − 0.8 | — | — | V |
| VOH22 | Output High Voltage ($P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | IOH = −25μA | $V_{CC}$ − 0.8 | — | — | V |
| ILI | Input Leak Current ($T_1$, $\overline{INT}$, EA, $\overline{PS}$) | | $V_{SS} \leqq VIN \leqq V_{CC}$ | — | — | ±10 | μA |
| ILI1 | Input Leak Current ($\overline{SS}$, $\overline{RESET}$) | | $V_{SS} \leqq VIN \leqq V_{CC}$ | — | — | $\frac{-V_{CC}}{0.1}$ | μA |
| ILI2 | Input Leak Current ($P_{10}$-$P_{17}$, $P_{20}$-$P_{27}$) | | $V_{SS}$ + 0.45V ≦ VIN ≦ $V_{CC}$ | — | — | $\frac{-V_{CC}}{0.01}$ | μA |
| ILO | Output Leak Current (BUS, $T_0$) (High impedance condition) | | $V_{SS}$ + 0.45V ≦ VIN ≦ $V_{CC}$ | — | — | ±10 | μA |
| ICC1 | $V_{CC}$ Supply Current | Normal operation | $V_{CC}$ = 5V, $f_{XTAL}$ = 6MHz VIH = $V_{CC}$ − 0.2V VIL = 0.2V | — | — | 10 | mA |
| ICCH1 | | HALT Mode | | — | — | 2.5 | |

## 4.7 AC Charactristics

TMP80C49AP-6/TMP80C39AP-6/TMP80C49AU-6
$T_{OPR}$ = −40°C to 85°C, $V_{CC}$ = +5V ± 20%, $V_{SS}$ = 0V, unless otherwise noted.

| SEMBOL | PARAMETER | TEST CONDITION | f (t) | 6 MHz | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| t | Clock Period | Note 2 | 1 / xtal f | 166.6 | 1000 | ns |
| $t_{LL}$ | ALE Pulse Width | | 3.5t − 170 | 410 | — | ns |
| $t_{AL}$ | Address Setup Time (ALE) | | 2t − 110 | 220 | — | ns |
| $t_{LA}$ | Address Hold Time (ALE) | CL = 20pF | t − 40 | 120 | — | ns |
| $t_{CC1}$ | Control Pulse Width ($\overline{RD}$,$\overline{WR}$) | | 7.5t − 200 | 1050 | — | ns |
| $t_{CC2}$ | Control Pulse Width ($\overline{PSEN}$) | | 6t − 200 | 800 | — | ns |
| $t_{DW}$ | Data Setup Time ($\overline{WR}$) | | 6.5t − 200 | 880 | — | ns |
| $t_{WD}$ | Data Hold Time ($\overline{WR}$) | CL = 20pF | t − 50 | 120 | — | ns |
| $t_{DR}$ | Data Hold Time ($\overline{RD}$,$\overline{PSEN}$) | CL = 20pF | 1.5t − 30 | 0 | 220 | ns |
| $t_{RD1}$ | Data Input Read Time ($\overline{RD}$) | | 5.5t − 120 | — | 880 | ns |
| $t_{RD2}$ | Data Input Read Time ($\overline{PSEN}$) | | 4t − 120 | — | 550 | ns |
| $t_{AW}$ | Address Setup Time ($\overline{WR}$) | | 5t − 150 | 680 | — | ns |
| $t_{AD1}$ | Address Setup Time ($\overline{RD}$) | | 10t − 170 | — | 1500 | ns |
| $t_{AD2}$ | Address Setup Time ($\overline{PSEN}$) | | 7t − 170 | — | 1000 | ns |
| $t_{AFC1}$ | Address Float Time ($\overline{RD}$, $\overline{WR}$)) | CL = 20pF | 2t − 40 | 290 | — | ns |
| $t_{AFC2}$ | Address Float Time ($\overline{PSEN}$) | CL = 20pF | 0.5t − 40 | 40 | — | ns |
| $t_{LAFC1}$ | ALE to Control Time ($\overline{RD}$,$\overline{WR}$) | | 3t − 75 | 420 | — | ns |
| $t_{LAFC2}$ | ALE to Control Time ($\overline{PSEN}$) | | 1.5t − 75 | 175 | — | ns |
| $t_{CA1}$ | Control to ALE Time ($\overline{RD}$,$\overline{WR}$,PROG) | | t − 65 | 100 | — | ns |
| $t_{CA2}$ | Control to ALE Time ($\overline{PSEN}$) | | 4t − 70 | 590 | — | ns |

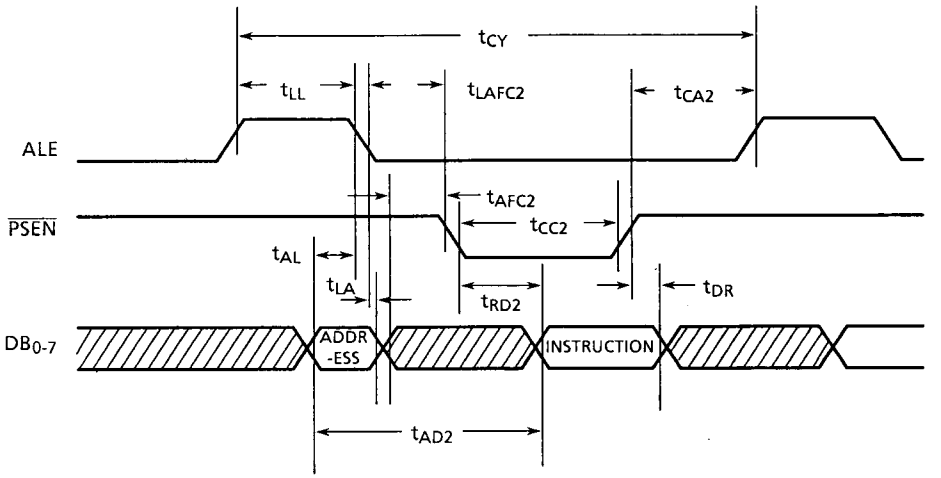
AC Charactristics (Continue)
$T_{OPR}$ = −40°C to 85°C, $V_{CC}$ = +5V ± 10%, $V_{SS}$ = 0V, unless otherwise noted.

| SYMBOL | PARAMETER | TEST CONDITION | f (t) | 11MHz | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| $t_{CP}$ | Port Control Setup Time (PROG) | | 1.5t − 80 | 170 | − | ns |
| $t_{PC}$ | Port Control Hold Time (PROG) | | 4t − 260 | 400 | − | ns |
| $t_{PR}$ | Port 2 Input Data Setup Time (PROG) | | 8.5t − 120 | − | 1290 | ns |
| $t_{PF}$ | Port 2 Input Data Hold Time (PROG) | | 1.5t | 0 | 250 | ns |
| $t_{DP}$ | Port 2 Output Data Setup Time (PROG) | | 6t − 290 | 710 | − | ns |
| $tP_D$ | Port 2 Output Data Hold Time (PROG) | | 1.5t − 90 | 160 | − | ns |
| $t_{PP}$ | PROG Pulse Width | | 10.5t − 250 | 1500 | − | ns |
| $t_{PL}$ | Port 2 I/O Data Setup Time (ALE) | | 4t − 200 | 460 | − | ns |
| $t_{LP}$ | Port 2 I/O Data Hold Time (ALE) | | 0.5t − 30 | 130 | − | ns |
| $t_{PV}$ | Port Output Delay Time (ALE) | | 4.5t + 100 | − | 850 | ns |
| $t_{0PRR}$ | $T_0$ Clock Period | | 3t | 500 | − | ns |
| $t_{CY}$ | Cycle Time | | 15t | 2.5 | 15.0 | μs |

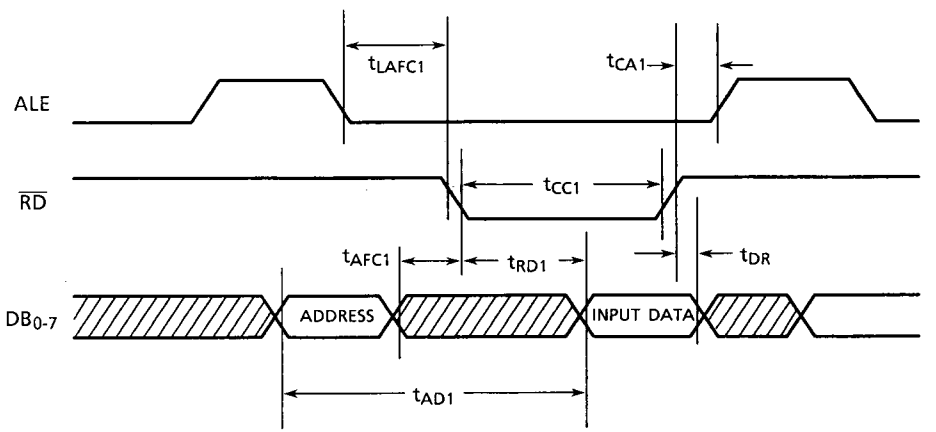
Note : 1. Control Output CL = 80pF. BUS Output CL = 150pF.
2. The f (t) assumes 50% duty cycle on $XTAL_1$ and $XTAL_2$.
The Max. Clock frequency is 6MHz. and the Min. Clock frequency is 1MHz.

4.8 Timing Waveform

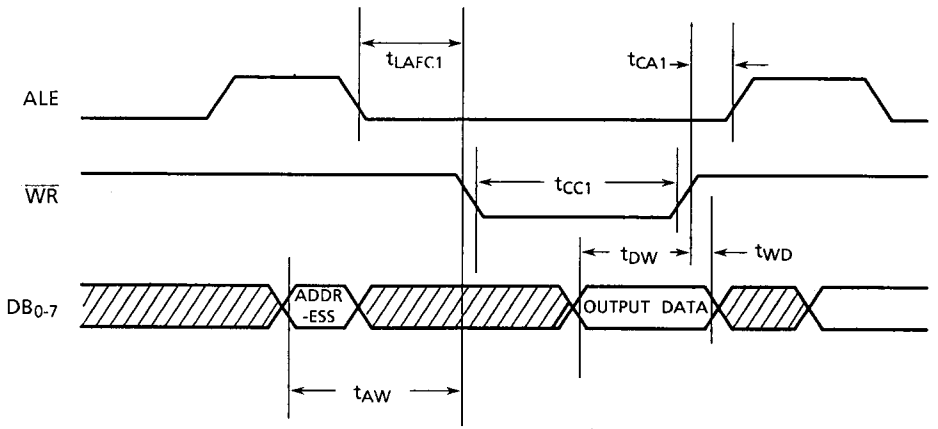
A. Instruction Fetch from External Program Memory



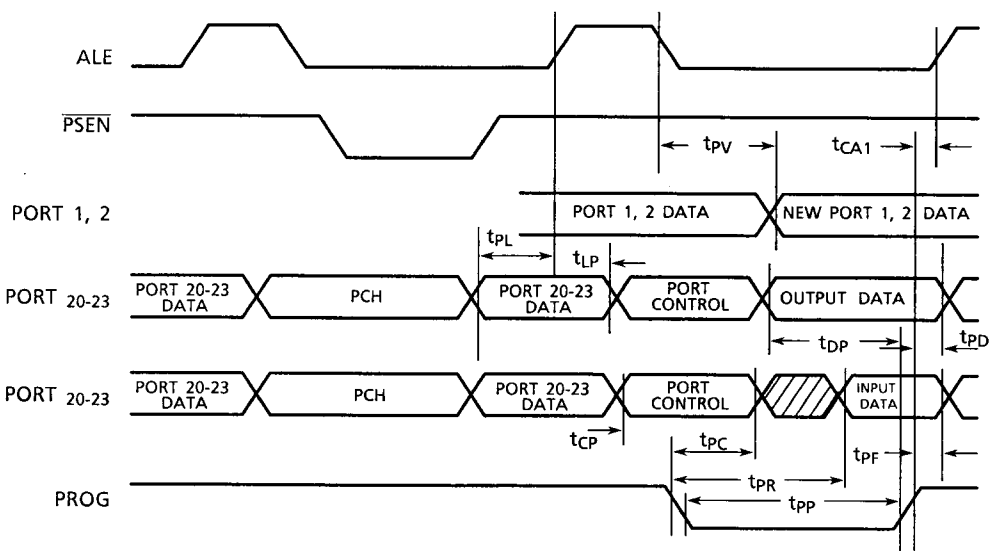

B. Read from External Data Memory



C. Write into External Data Memotry




D. Timing of Port 2 during Expandar Instruction Execution



## 4.9 Stand-By Function

### 4.9.1 PoweR Down Mode (I) ····· Data Hold Mode in RAM

The operation of oscillation circuit is suspended by setting $\overline{PS}$ terminal to low level after $\overline{RESET}$ terminal has been set to low level. Consequently, all the data in RAM area can be held in low power consumption.

The minimum hold voltage of $V_{CC}$ in this mode is 2V.

$\overline{PS}$ terminal is set to high level to resume oscillation after $V_{CC}$ has been reset to 5V, and then $\overline{RESET}$ terminal is set to high level, thus, the normal mode is restarted from the initialize operation (address 0).

(1) DC Characteristics

TMP80C49AP/C39AP/C49AU
TMP80C49AP-6/C39AP-6/C49AU-6 : $T_{OPR}$ = −40°C to 85°C, $V_{SS}$ = 0V

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| VSB1 | Standby Voltage (1) | | 2.0 | — | 6.0 | V |
| ISB1 | Standby Current (1) | $V_{CC}$ = 5V, VIH = $V_{CC}$ − 0.2V, VIL = 0.2V | — | 0.5 | 10 | μA |

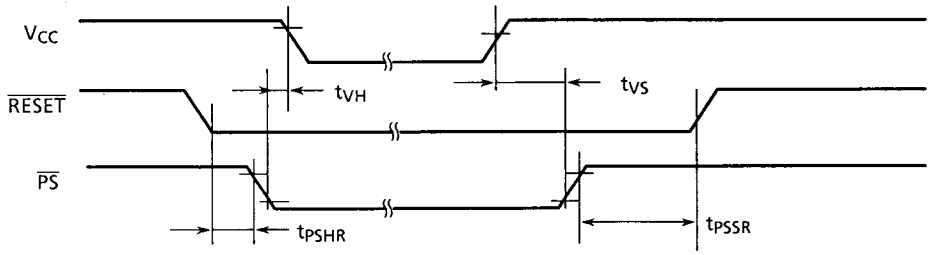
(2) AC Characteristics

TMP80C49AP/C39AP/C49AU : $V_{CC}$ = + 5V ± 10%, $V_{SS}$ = 0V
TMP80C49AP-6/C39AP-6/C50AU-6 : $V_{CC}$ = + 5V ± 20%, $V_{SS}$ = 0V

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $t_{PSHR}$ | Power Save Hold Time ($\overline{RESET}$) | | 10 | — | — | μs |
| $t_{PSSR}$ | Power Save Setup Time ($\overline{RESET}$) | | 10 | — | — | ms |
| $t_{VH}$ | $V_{CC}$ Hold Time ($\overline{PS}$) | | 5 | — | — | μs |
| $t_{VS}$ | $V_{CC}$ Setup Time ($\overline{PS}$) | | 5 | — | — | μs |

Note : $t_{CY}$ = 2.5μs ($f_{XTAL}$ = 6MHz)

(3) Timing Waveform



4.9.2 Power Down Mode (II) ····· ALL Data Hold Mode

The operation of oscillation circuit is suspended by setting $\overline{PS}$ terminal to low level after $\overline{SS}$ terminal has been set to low level. Consequently, all data can be held in low power consumption.

The minimum hold voltage of $V_{CC}$ in this mode is 3V.

$\overline{PS}$ terminal is set to high level to resume oscillation after $V_{CC}$ has been reset to 5V, and then $\overline{SS}$ terminal is set to high level, thus, the normal mode is restarted continuously from the state just before the power down mode (II).

(1) AC Characteristics

TMP80C49AP/C39AP/C49AU
TMP80C49AP-6/C39AP-6/C49AU-6 : $T_{OPR}$ = −40°C to 85°C, $V_{SS}$ = 0V

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $VSB_2$ | Standby Voltage (2) | | 3.0 | — | 6.0 | V |
| $ISB_2$ | Standby Current (2) | $V_{CC}$ = 5V, VIH = $V_{CC}$ − 0.2V, VIL = 0.2V | — | 0.5 | 10 | μA |

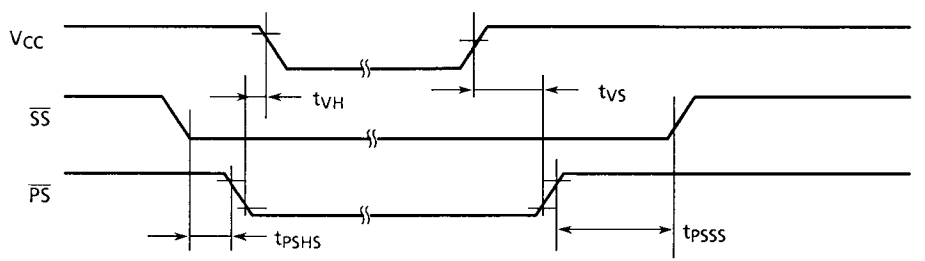
(2) AC Characteristics

TMP80C49AP/C39AP/C49AU : $V_{CC}$ = +5V ± 10%, $V_{SS}$ = 0V
TMP80C49AP-6/C39AP-6/C49AU-6 : $V_{CC}$ = +5V ± 20%, $V_{SS}$ = 0V

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $t_{PSHR}$ | Power Save Hold Time ($\overline{SS}$) | | 10 | — | — | μs |
| $t_{PSSR}$ | Power Save Setup Time ($\overline{SS}$) | | 10 | — | — | ms |
| $t_{VH}$ | $V_{CC}$ Hold Time ($\overline{PS}$) | | 5 | — | — | μs |
| $t_{VS}$ | $V_{CC}$ Setup Time ($\overline{PS}$) | | 5 | — | — | μs |

Note : $t_{CY}$ = 2.5μs ($f_{XTAL}$ = 6MHz)

(3) Timing Waveform



### 4.9.3 HALT MODE

(1) HALT INSTRUCTION

OP code is "01H". HALT INSTRUCTION is an additional instruction to the standard 8048/8049 instruction set.

(2) Entry to HALT MODE

On the execution of HALT INSTRUCTION, TMP80C49A/TMP80C39A enter HALT MODE.

(3) Status in HALT MODE

The oscillator continues its operation, however, the internal clocks and internal logic values just prior to the execution of HALT INSTRUCTION are maintained. Power consumption in HALT MODE is less than 50% of normal operation. The status of each pins are described in the following table.

(4) Release from HALT MODE

HALT MODE is released by either of two signals ($\overline{\text{RESET}}$, $\overline{\text{INT}}$).

(4.1) $\overline{\text{RESET}}$ Release Mode : An active $\overline{\text{RESET}}$ input signal causes the normal reset function. TMP80C49A/TMP80C39A start the program at address "000H".

(4.2) $\overline{\text{INT}}$ Release Mode : An active $\overline{\text{INT}}$ input signal causes the normal operation.

- In case of interrupt enable mode (EI MODE), TMP80C49A/TMP80C39A execute the interrupt service routine, after the execution of one instruction which is located at the next address after HALT INSTRUCTION.
- In case of interrupt disable mode (DI MODE), TMP80C49A/TMP80C39A execute normal operation from the next address after HALT INSTRUCTION.

(5) Supply Voltage Range in HALT MODE

The operating supply voltage range and the operating temperature range are same as in normal operation.

TMP80C49AP/C39AP/C49AU : $V_{CC}=5V\pm10\%$
TMP80C49AP-6/C39AP-6/C49AU-6 : $V_{CC}=5V\pm20\%$

4.9.4 Pin Status In Power Down Mode (I) (II)

| PIN NAME | STATUS |
|---|---|
| $DB_0$~$DB_7$ | High impedance<br>Input disabled |
| $P_{10}$~$P_{17}$ | |
| $P_{20}$~$P_{27}$ | |
| $T_0$ | High impedance, input disabled |
| $T_1$ | Input disabled |
| $XTAL_1$ | High impedance |
| $XTAL_2$ | Output "High" Level |
| $\overline{RESET}$, $\overline{SS}$ | Input disabled when oscillator is stopped. Pull-up transistors turn off. |
| $\overline{INT}$, EA | Input disabled when oscilltor is stopped. |
| $\overline{RD}$, $\overline{WR}$, ALE<br>PROG, $\overline{PSEN}$ | High impedance |

4.9.5 Pin Status In HALT MODE

| PIN NAME | STATUS |
|---|---|
| $DB_0$~$DB_7$ | Values prior to the execution of HALT INSTRUCTION are maintained. |
| $P_{10}$~$P_{17}$ | |
| $P_{20}$~$P_{27}$ | |
| $T_0$ | Status prior to the execution of HALT INSTRUCTION is maintained. |
| $T_1$ | Input disabled |
| $XTAL_1$, $XTAL_2$ | Continue oscillation |
| $\overline{RESET}$, $\overline{INT}$ | Input enabled |
| $\overline{SS}$, EA | Input disabled |
| $\overline{RD}$, $\overline{WR}$<br>PROG, $\overline{PSEN}$ | Output "High" level |
| ALE | Output "Low" level |

## 5. OSCILLATOR

QUARTZ CRYSTAL

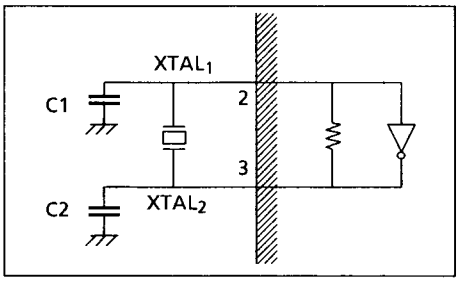
f = 1MHz to 4MHz : C1 = C2 = 30pF

f = 4MHz to 11MHz : C1 = C2 = 20pF

CERAMIC RESONATOR

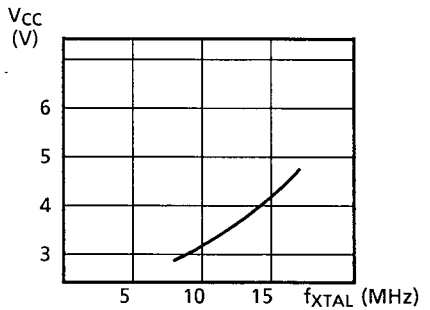
f = 1MHz to 3MHz : C1 = C2 = 100pF

f = 3MHz to 11MHz : C1 = C2 = 30PF

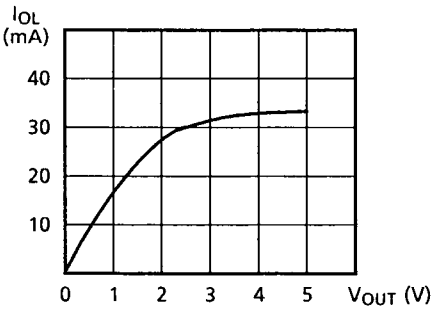



## 6. TYPICAL CHARACTERISTICS

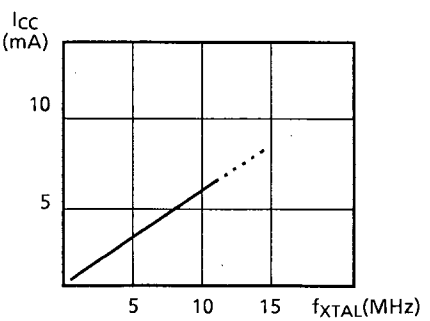
: Vcc = 5V, Ta = 25°C, unless Otherwise noted.



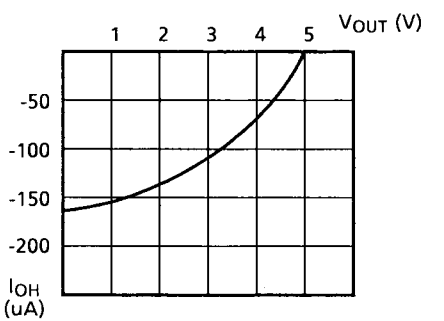

$V_{CC}$ – $f_{MAX.}$ TYPICAL CURVE



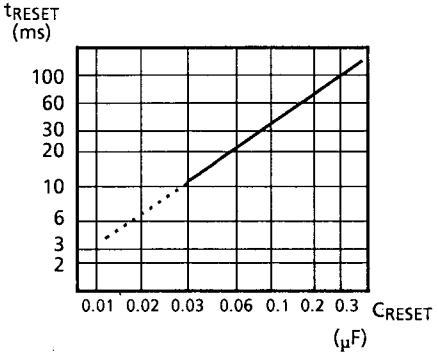

$V_{OUT}$ – $I_{OL}$ TYPICAL CURVE



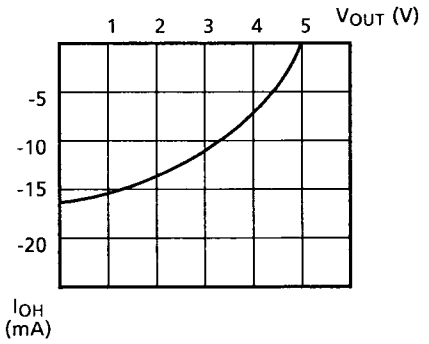

$f_{XTAL}$ – $I_{CC}$ TYPICAL CURVE




$V_{OUT}$ – $I_{OH}$ TYPICAL CURVE
(PORT 1, 2)




CRESET – tRESET TYPICAL CURVE



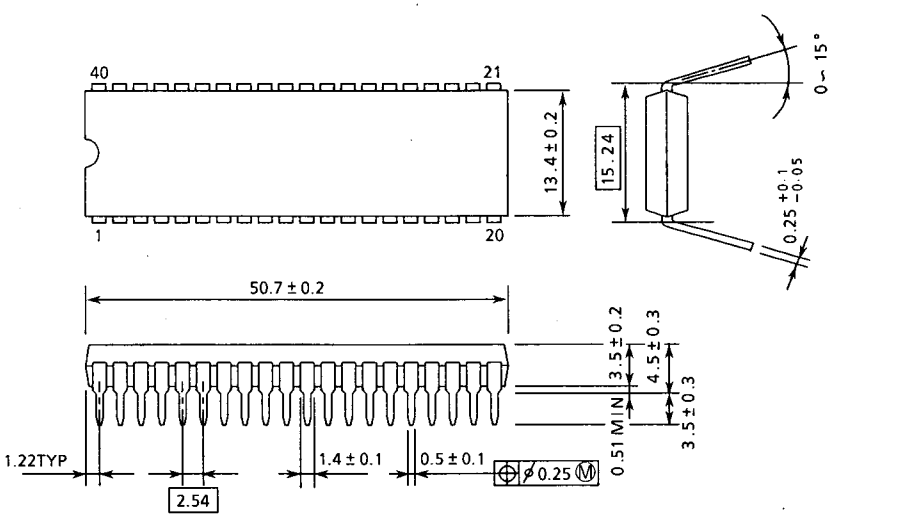

VOUT – IOH TYPICAL CURVE
(DB, CONTROL)

## 7. OUTLINE DRAWING

### 7.1 Outline Drawing For TMP80C49AP/-6,TMP80C39AP/-6 (DIP:Dual Inline Package)

DIP40-P-600

Unit : mm

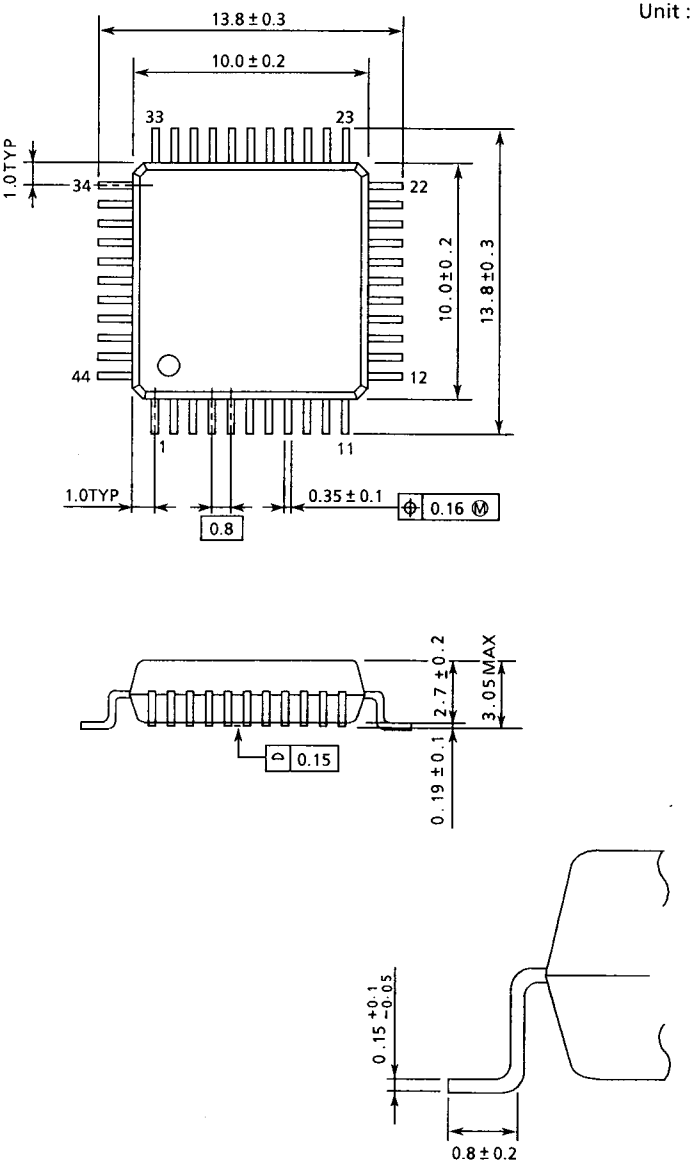



Note: 1. This dimension is measured at the center of bending point of leads.
2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

7.2 Outline Drawing For TMP80C49AU/-6
(Micro Flat Package)

QFP44-P-1010A

Unit : mm




Note: 1. The above dimensions don't include the burr of package and the residue of tie-bar cut. The burr of package and the residure of tie-bar cut should be 0.15 mm (Max.).
2. Applied ti the lead flat porttion.